Ceramic Column Grid Array

Table of Contents

Introduction

Ceramic Column Grid Array (CCGA) packages are becoming increasingly popular as an alternative to Ceramic Ball Grid Array (CBGA) packages for applications requiring very high-density interconnections with higher board-level reliability. The CCGA packages use high-temperature solder columns instead of high-temperature balls. This creates a greater standoff, providing a flexible interconnection with improved thermal characteristic, significantly increasing the thermal fatigue life of the package solder joint.

Microsemi has selected the CCGA technology as part of its high-density, high I/O count hermetic package offering. A 624-pin CCGA (CG624), 1152 pin-CCGA (CG1152), and 1272-pin CCGA (CG1272) are offered for the RTAX-S, RTAX-SL, RTSX-SU, Axcelerator® and ProASIC PLUS® FPGA product families. Figure 1 through Figure 3 on page 2 show the top and bottom views of the CG624, CG1152, and CG1272 packages.

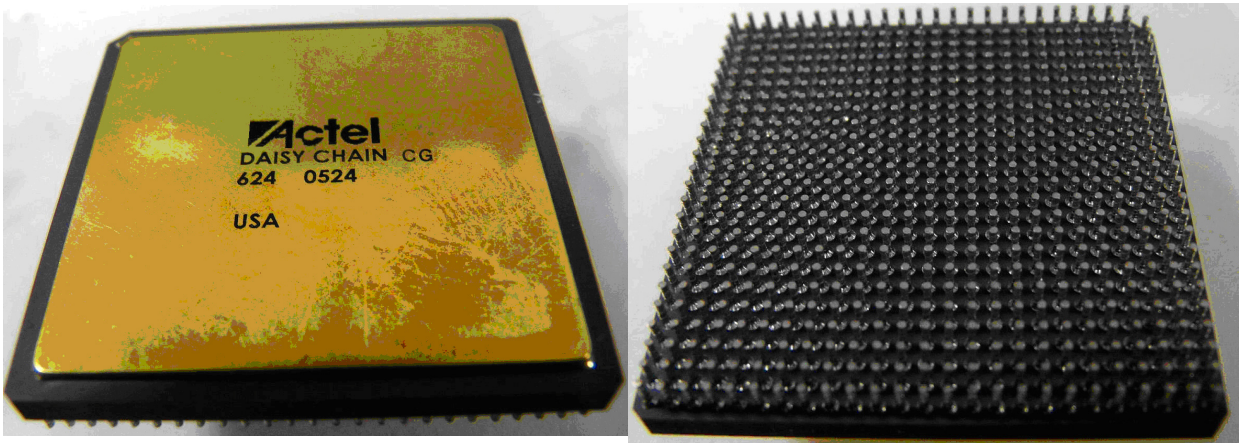


***Figure 1* • CG624 Package Top and Bottom View**

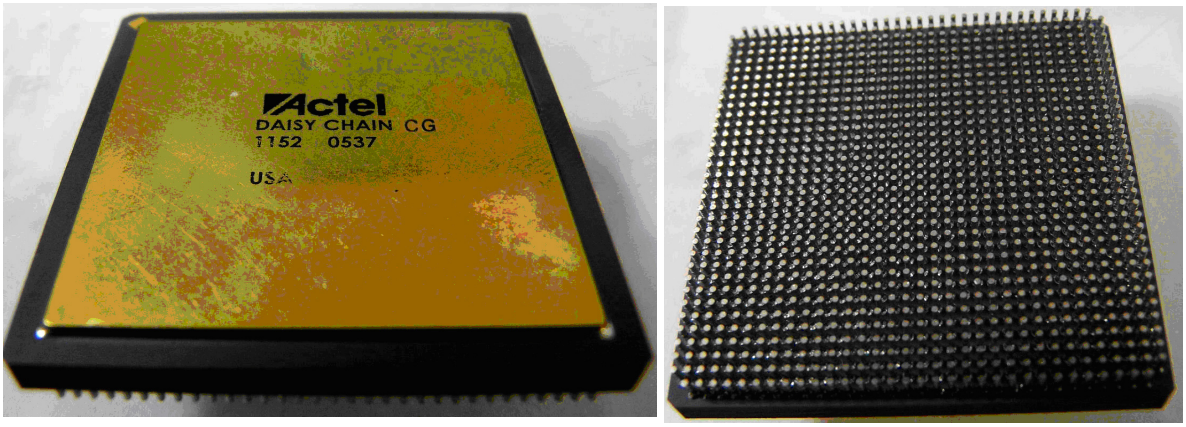


***Figure 2* • CG1152 Package Top and Bottom View**

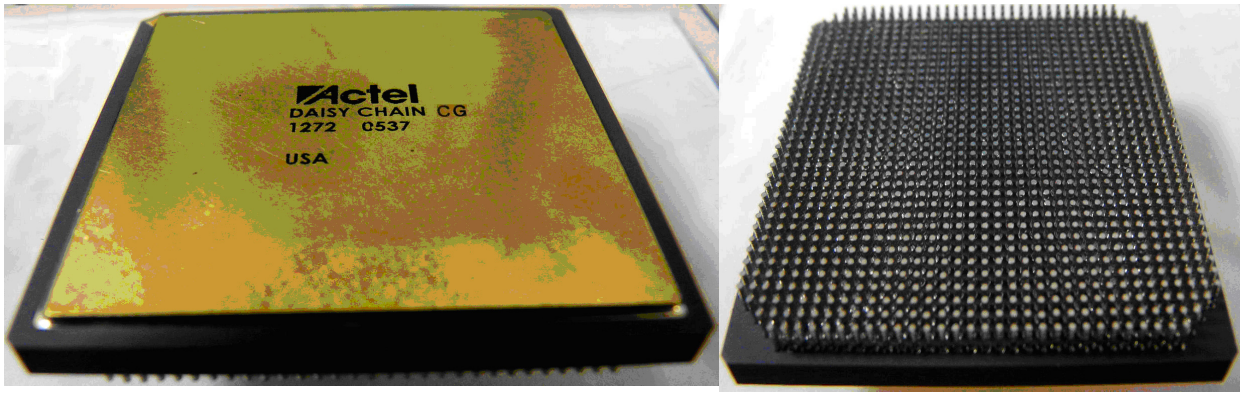


***Figure 3* • CG1272 Package Top and Bottom View**

CCGA Package Description

The CCGA is a multi-layer ceramic package with attributes including:

1. Dark ceramic, same material as Microsemi's CQ208, CQ256, and CQ352 packages
2. The solder column is either 90 Pb/10 Sn or 80 Pb/20 Sn, with a copper ribbon (refer to Figure 4 and Figure 5 on page 3) attached to the ceramic substrate I/O pads via eutectic 37/63 Pb/Sn, forming a eutectic solder joint. Please see Figure 6 on page 3 for more details.
3. Wire bond interconnect used to connect silicon to package.
4. The die cavity is on the top side of the package and hermetically sealed with AuSn eutectic material.
5. The lid is connected to GND.

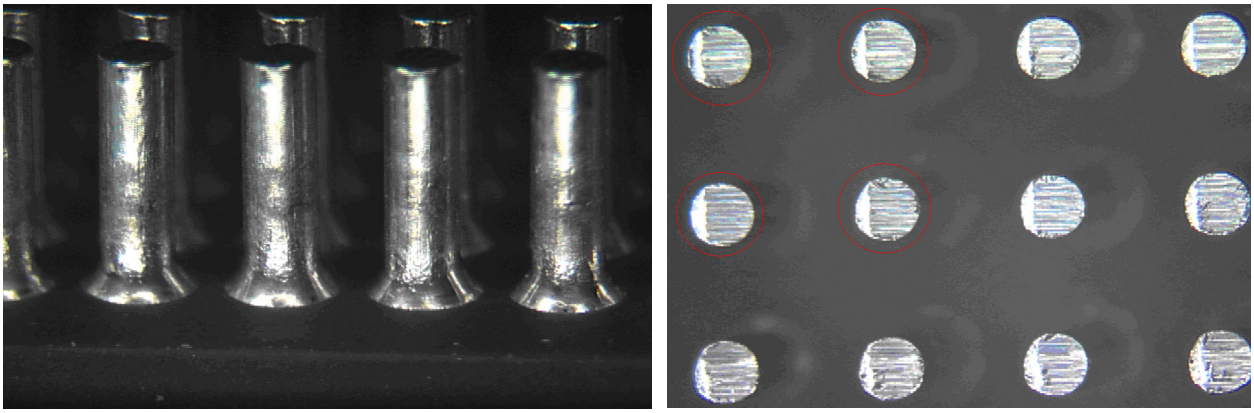


***Figure 4* • 90Pb/10Sn Column Side View and Tip View, with 20 mils Diameter**

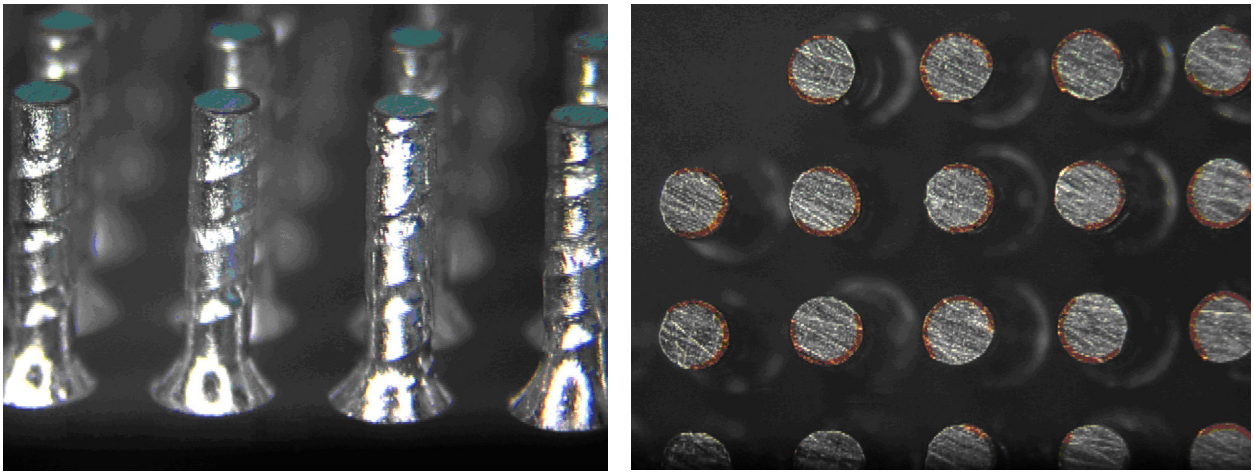


***Figure 5* • Change to 80Pb/20Sn Column Side View and Tip View, with 20 mils Diameter**

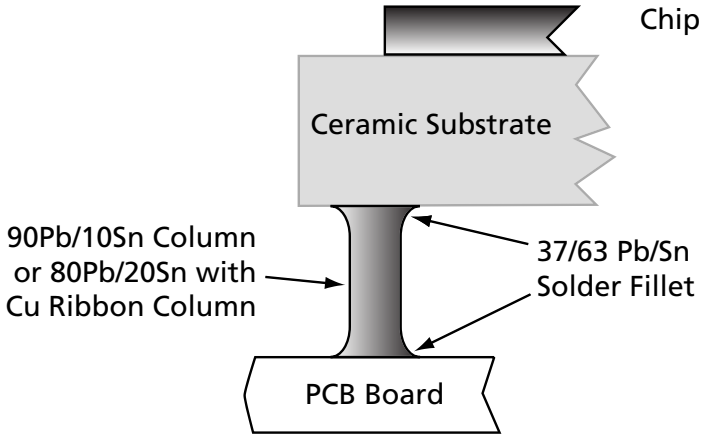


***Figure 6* • CCGA on PCB**

Table 1 contains package dimensions, descriptions, and details on the packaging and solder columns used in the assembly process for each of the Microsemi CCGA packages:

Table 1 • **Microsemi CCGA Package Matrix**

	CGS624	CG1152	CG1272
Column Information			
Column Attach Site	Six Sigma	Six Sigma	Six Sigma
Column Composition	80Pb/20Sn	80Pb/20Sn	80Pb/20Sn
Copper Ribbon	Yes	Yes	Yes
Column Height	2.21 mm (0.087")	2.21 mm (0.087")	2.21 mm (0.087")
Column Diameter	0.51mm (0.020")	0.51mm (0.020")	0.51mm (0.020")
Column Coplanarity	0.15mm (0.006")	0.15mm (0.006")	0.15mm (0.006")
Package Information			
Body Size	32.5 mm square	35.0 mm square	37.5mm square
Column Pins	624	1152	1272
Column Pin Notes	Orientation pin A1 – no column	Corner stress relief – 1 pin each corner	Corner stress relief – 6 pins each corner
Lead Pitch	1.27 mm	1.00 mm	1.00 mm
Ceramic Thickness	2.25 mm	2.77 mm	2.77 mm
Total Weight of Columns	2.36 g	4.35 g	4.80 g
JEDEC Registration	JEDEC MO-158 VAR BE-1	JEDEC MO-158 VAR CG-1	JEDEC MO-158 VAR CH-2

Column Attach and CCGA Board-Level Reliability

The 90Pb/10Sn solder column attachment process for Microsemi CCGA devices is provided by BAE Systems in Manassas, Virginia. BAE licensed their CCGA technology directly from IBM and has completed extensive board-level reliability testing, including Thermal Cycle, Pro Shock, and Vibration tests for its CCGA packaging process, qualifying it for space-flight-level applications. Microsemi 90Pb/10Sn CCGA packages follow the CCGA design and manufacturing rules of BAE Systems. Therefore, we are incorporating the BAE Systems board-level reliability qualification data results into our overall qualification plan. A copy of the BAE Systems CCGA qualification summary may be obtained by contacting Microsemi.

The 80Pb/20Sn solder column with copper ribbon attachment process for Microsemi CCGA devices is provided by Six Sigma in Milpitas, California. Microsemi 80Pb/20Sn CCGA packages follow the CCGA design and manufacturing rules of Six Sigma. Six Sigma's CCGA qualification summary may be obtained by contacting either Microsemi or Six Sigma directly.

In addition to the qualification data provided by BAE Systems and Six Sigma, Microsemi completed its own CCGA board-level thermal cycling test on both the 90Pb/10Sn column and 80Pb/20Sn column devices. This test report can be downloaded at www.microsemi.com/soc/documents/CCGA_board_level_testing_report.pdf.

Board-level reliability is affected by many factors, including PCB design, layout, fabrication rules, PCB construction method and material, assembly process variations (such as solder paste screening, component placement, solder reflow, thermal profile, cleaning, inspection, and rework process, etc.), and various application environments. Microsemi recommends that the end user of CCGA devices evaluate specific application conditions and define a customized qualification plan.

Manufacturing Handling and Assembly

Handling CCGA Packages During Manufacturing and Programming

Due to the difficulty in handling the solder columns, Microsemi initially processes the CCGA packages in the Land Grid Array (LGA) format (column pins are not attached at this stage; see Figure 7, Figure 8 on page 5 and Figure 9 on page 5). CCGA devices are assembled as LGA packages with complete test, burn-in, and QCI testing (group A/B/C/D). Column pins are attached to the LGA at the last step after all processes have been completed. The only processing conducted after solder column attachments is 100% continuity testing and 100% mechanical visual inspection.

It is very important for end users to handle CCGA packages in the proper manner in order to prevent damage to the column pins. Extreme care must taken when handling CCGA devices during programming, testing, and PCB assembly.

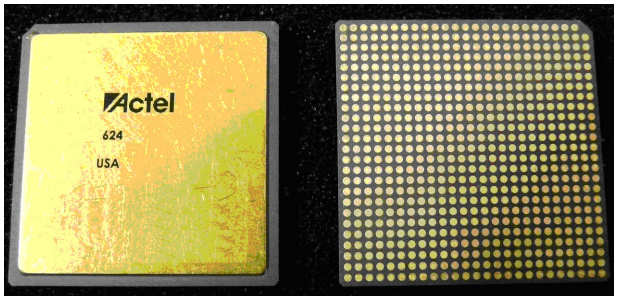


***Figure 7* • LG624 Top and Bottom View**

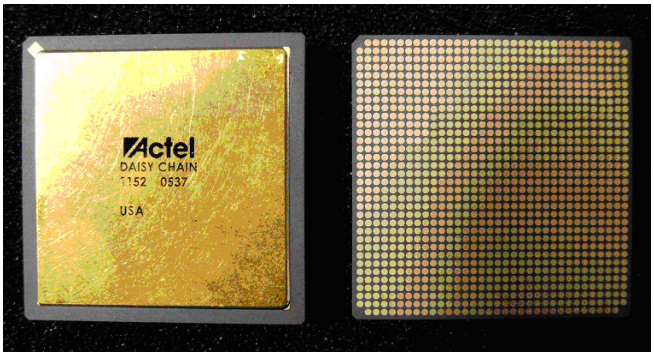


***Figure 8* • LG1152 Top and Bottom View**

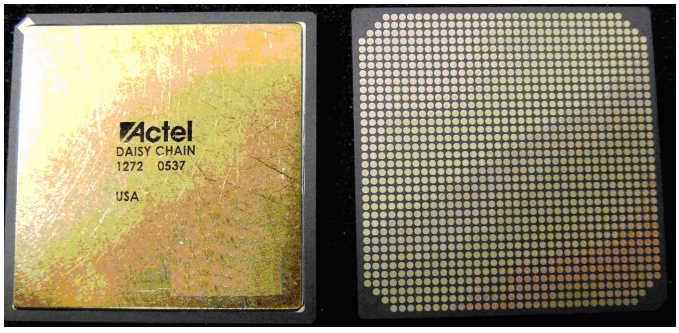


***Figure 9* • LG1272 Top and Bottom View**

Handling of CCGA Packaged Parts

1. Microsemi ships each CCGA packaged part in a tray carrier with a column protection feature. The tray carrier is then stored in a black ESD-protective jewel box and sealed in a dry pack. See Figure 10 on page 6. The user must be aware that solder columns are very soft and easily bent.
2. CCGA packaged devices must remain in dry pack until ready for use. Removal of the dry pack material will initiate the solder column oxidation that occurs over time.

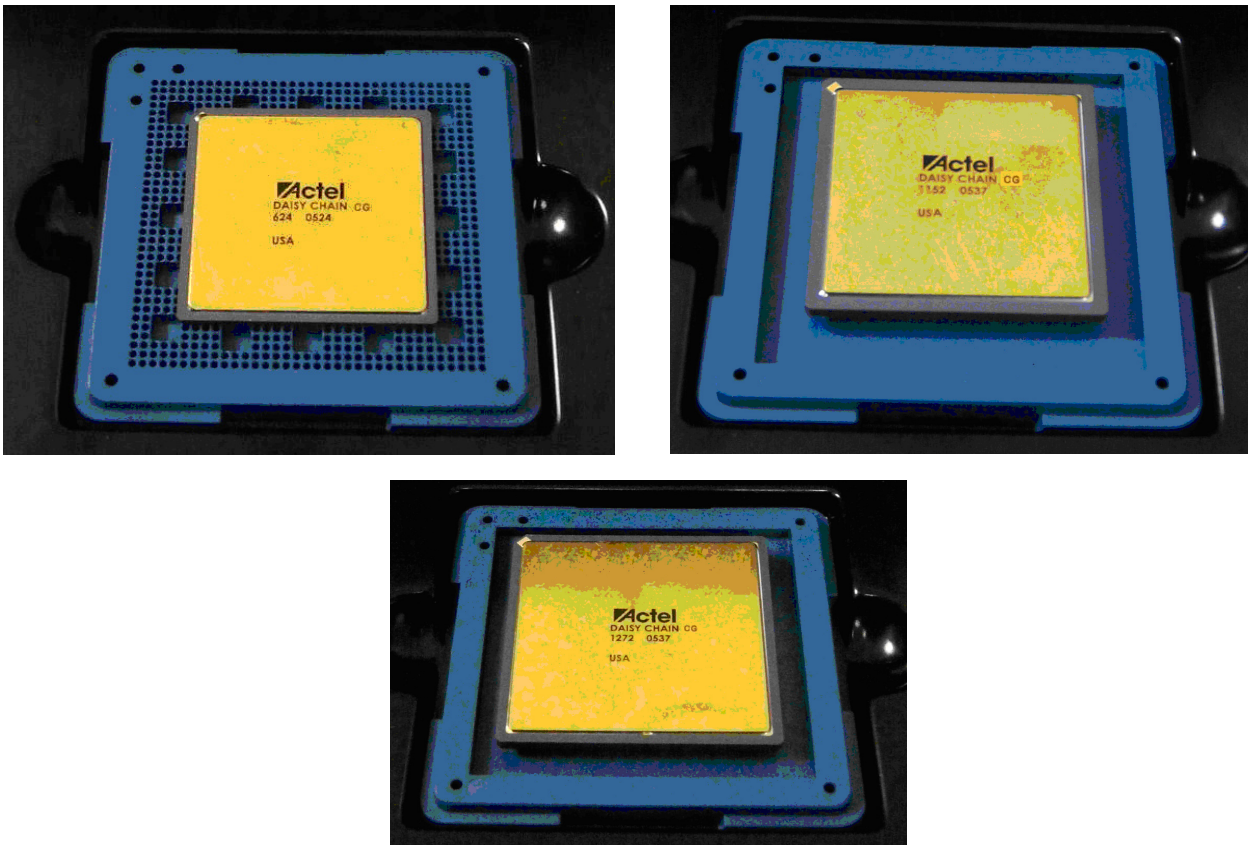


***Figure 10* • From Left to Right: CG624, CG1152, and CG1272 in their Respective Tray Carriers**

Programming with CCGA Packaged Part

In preparation for device programming, open the dry-pack bag and use a vacuum pick-up pen to lift the unit from the tray carrier. Do not handle manually; column pins can be easily bent if carelessly handled when attempting to pick up the unit from the carrier.

1. Carefully place the unit into the programming socket. Align the packaged unit with the socket frame using extra care, since any misalignment will bend the column pins. There are no easy repair methods for damaged column pins.
2. Make sure the unit is fully seated into the socket alignment frame with no misalignment or binding. Carefully close the socket lid and begin programming.
3. When programming is complete, use the vacuum pick-up pen to gently remove the unit from the socket, placing it back in the tray carrier.
4. Conduct board-level assembly as soon as possible or return the part to dry pack until it is ready for board-level assembly. This step is to prevent solder oxidation. (Note: Excess vacuum pressure during re-dry-pack may damage the black ESD jewel box, which in turn may damage the CG package.)

Damaged or Bent Columns

1. If the column is bent in such a way that the center of the column is offset more than 35º and cannot fit into the shipping carrier, then rework must be done to straighten the damaged column.
2. Microsemi does not offer solder column rework. Damaged columns are expensive and time consuming to repair. Therefore, it is important for end users to closely follow the CCGA package handling instructions in order to prevent costly column pin damage.
3. Microsemi's Silicon Sculptor programming module is designed specifically for solder columns manufactured and attached by both BAE Systems and Six Sigma. Microsemi does not guarantee Silicon Sculptor will operate correctly with solder columns reworked by third parties or columns other than those supplied by Microsemi and its column attach partners.

Incoming Visual Inspection for CCGA Devices

1. End users may require incoming visual inspection of CCGA devices after they are received from Microsemi. Precaution must be exercised to not only ensure the CCGA devices are not damaged during inspection but also make sure devices are seated properly on the tray carrier, which is stored in the black jewel box and secured there with extra ESD tape. After the inspection, all devices must be resealed with dry pack as soon as possible. For long-term storage, Microsemi strongly recommends using a nitrogen-filled environment.
2. The following are inspection acceptance criteria for CCGA product from Microsemi. Inspection of these items must be performed at 10X with confirmation at 30X.
   - No missing columns other than those columns indicated on the CCGA assembly drawing
   - No two columns may be touching or joined by reflowed solder.
   - No flux residue, stains, metal smear, or solder bridging is allowed to reduce the space between two adjacent bottom-surface-metallization (BSM) I/O pads by more than 50% of the clearance distance.
   - Eutectic solder fillets shall have no evidence of incomplete reflow and must show a positive wetting angle and filleting of at least 75% (95% target) around column circumference.
   - Solder joints covering less than 75% of the wetted area of the I/O pad area are unacceptable.
   - For solder fillets, foreign material, residue, and stains that are proven to be non-ionic and not larger than 3 mils in length are permitted.
   - No discoloration within 20 mils from the tip of the column is allowed.
   - No twisted or crushed columns are permitted.
   - Voids, holes, and pits less than 3 mils deep are permitted on the column attach bottom surface.
   - Voids, holes and pits greater than or equal to 3 mils deep but less than or equal to 6 mils deep are permitted on the column attach bottom surface provided they cumulatively do not exceed 10 mils diameter area. Damage to one column beyond the cumulative 10 mils diameter area is not acceptable.
   - Voids, holes, and pits greater than 6 mils deep on the column attach bottom surface are not acceptable.
   - Voids, holes, pits, and indentations along the column are acceptable provided they are less than or equal to 3 mils deep and they cumulatively do not exceed 10 mils diameter area. However, rough edges from the cutting process, pogo pin marks from testing and the programming socket (pogo pin base) are not considered voids or holes, and are acceptable.
   - No cracks are permitted within the solder column body greater than 3 mils in length.
   - No loose non-conductive fibers are acceptable, regardless of size, during final inspection. Operators can remove loose fibers with a 20 psi air gun as needed. Microsemi recommends, however, that end customers inspect and air blow parts prior to attaching CCGA packages to their boards. This will eliminate any loose non-conductive fibers resulting from shipping, handling, and programming.
   - Cracks, chip-outs, or scratches that disturb metallization on the ceramic substrate are not acceptable.

- Cracks or chip-outs that exceed 0.060 inch in any direction on the surface and have a depth that exceeds 25% of the thickness of the affected package element (e.g., base or wall) are not acceptable.
- Part marking must remain legible after the column attachment process.
- Solder wetting to component lid shall be voided per the following:
  a. Inside the marking area – Reject if solder splatter is greater than 0.005".
  b. Outside the marking area – Reject if solder splatter is greater than 0.015" for a single spot or 4 spots greater than 0.005".
- Eutectic solder on the outer substrate I/O pads must form an angle with the solder column such that there is no reflection of light when viewed straight on from the top of the column at 1X (unaided eye).

Daisy Chain and Mechanical Samples

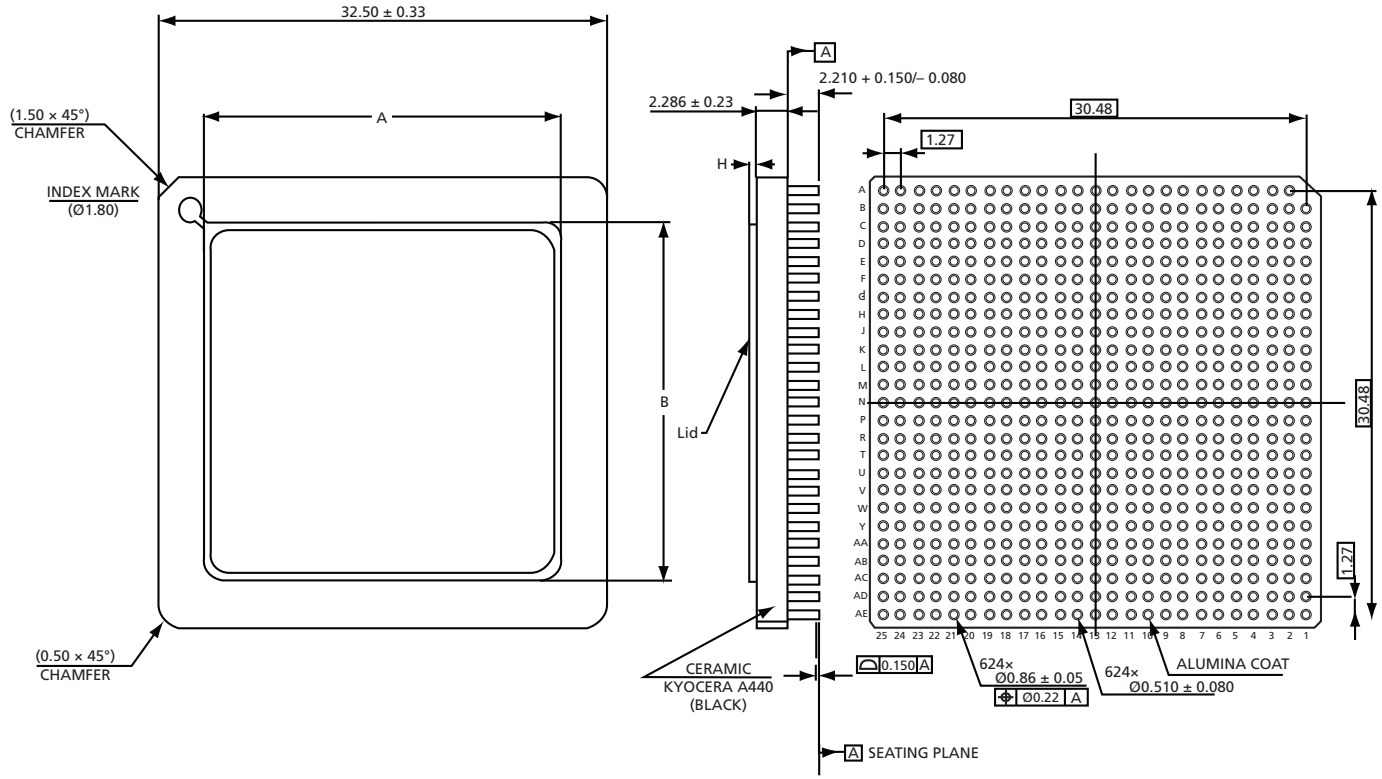
1. Daisy-chain devices used to conduct assembly process development and board-level qualifications are available from Microsemi. End users should contact Microsemi to purchase daisy-chain samples of the CG624, CG1152, or CG1272 packages.
2. Frequently, end users of Microsemi FPGAs request mechanical samples for production setup. These will not be available for the CG624, CG1152, and CG1272 packages due to the high cost of solder column attachment.

Conclusion

CCGA packages will continue to be the high-reliability, high-density package solution of choice for space applications. Similar to CBGA in methodology and board-level manufacturing techniques, care must be exercised in handling solder column devices to reduce both damage and oxidation. CCGA packages, with their enhanced reliability due to heat dissipation and reduced thermal expansion, enable a more reliable interconnection to the PCB and provide the best solution for achieving high I/O counts on a reduced footprint. This application note provides general guidelines to assist end users in implementing CCGA packages in high-reliability applications. For further assistance please contact either your local Microsemi sales representative, email Technical Support at soc_tech@microsemi.com or call the Microsemi hotline at (800) 262-1060.

Appendix – CCGA Package Dimensioning and Assembly Parameters (reference only)

CGGA Package Outline Drawings

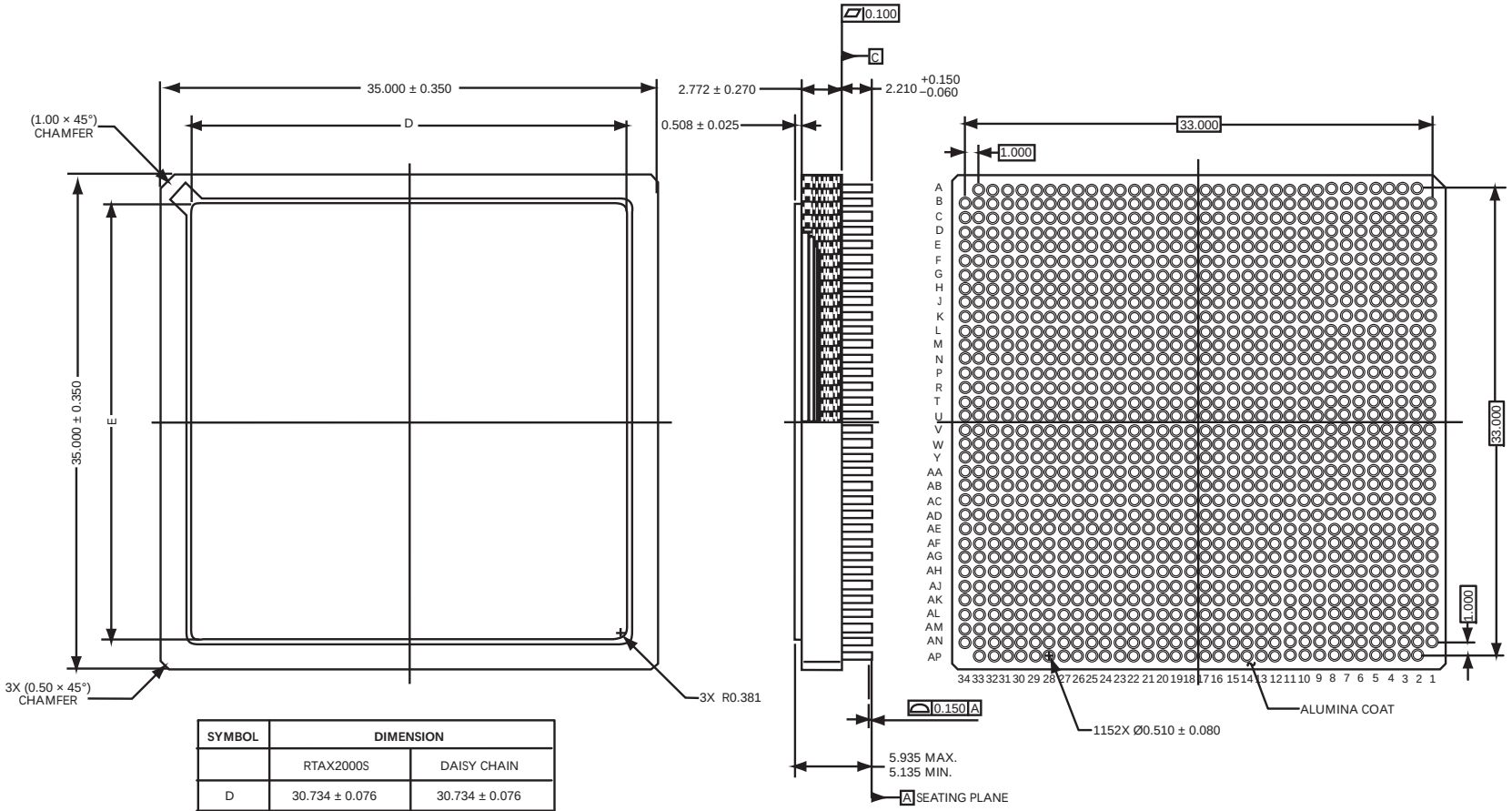


Device	LID Size A × B × H (inches)
A54SX72A	0.72 × 0.72 × 0.015
RT54SX72S	0.90 × 0.90 × 0.015
AX1000	0.86 × 0.86 × 0.015
RTAX1000S	1.00 × 1.00 × 0.020
AX2000	1.00 × 1.00 × 0.020
RTAX2000S	1.06 × 1.06 × 0.015
APA600	0.77 × 0.77 × 0.015
APA1000	1.00 × 1.00 × 0.020
Daisy Chain	1.06 × 1.06 × 0.015

Notes:

1. *Solder Column Material: 90Pb/10Sn or 80Pb/20Sn with Cu Ribbon*
2. *Units: mm*

***Figure 11* • Outline Drawing for CG624**

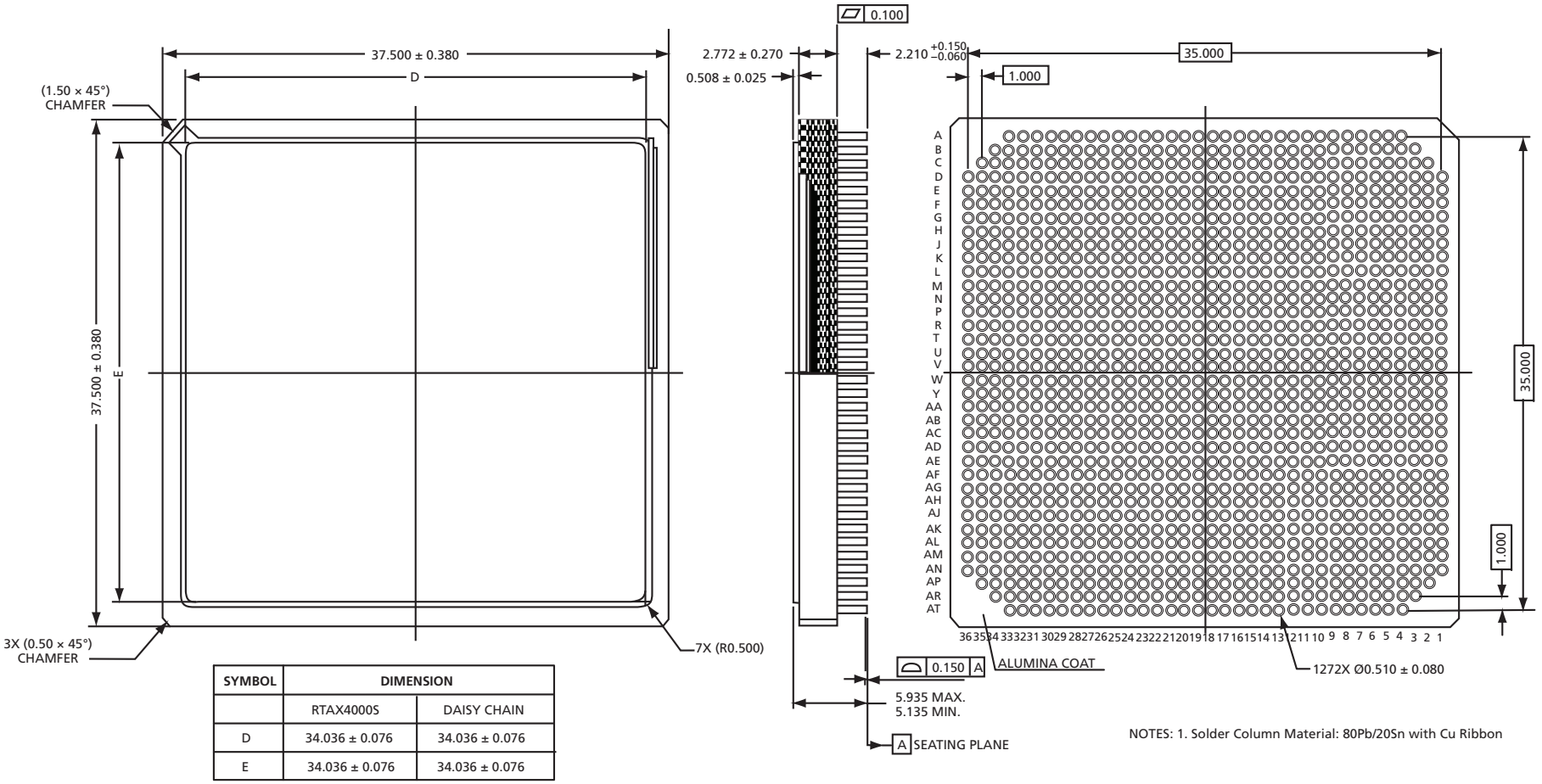


SYMBOL	DIMENSION	
	RTAX2000S	DAISY CHAIN
D	30.734 ± 0.076	30.734 ± 0.076
E	30.734 ± 0.076	30.734 ± 0.076

Notes:

1. *Solder Column Material: 80Pb/20Sn with Cu Ribbon*
2. *Units: mm*

Figure 12 • **Outline Drawing for CG1152**



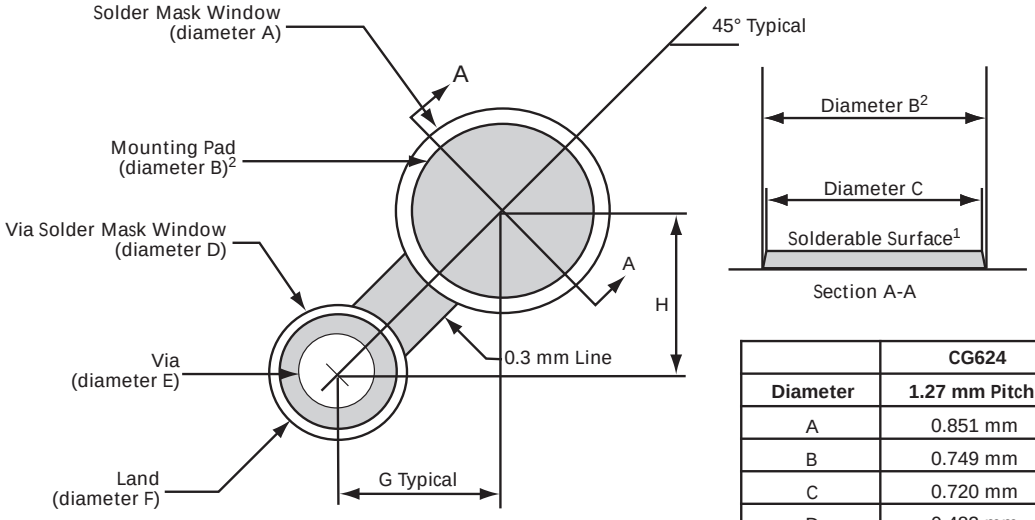
SYMBOL	DIMENSION	
	RTAX4000S	DAISY CHAIN
D	34.036 ± 0.076	34.036 ± 0.076
E	34.036 ± 0.076	34.036 ± 0.076

Notes:

1. *Solder Column Material: 80Pb/20Sn with Cu Ribbon*
2. *Units: mm*

***Figure 13* • Outline Drawing for CG1272**

PCB Pad Layout Reference



All dimensions are in mm unless otherwise specified.

Notes:
1. Functional surface
2. Normal diameter at Copper/Polyimate interface with typical edge angle

	CG624	CG1152/1272
Diameter	**1.27 mm Pitch**	**1.00 mm Pitch**
A	0.851 mm	0.80 mm
B	0.749 mm	0.70 mm
C	0.720 mm	0.67 mm
D	0.483 mm	0.38 mm
E	0.305 mm	0.20 mm
F	0.560 mm	0.46 mm
G	0.635 mm	0.50 mm
H	0.635 mm	0.50 mm

Figure 14 • **CCGA PCB Layout Reference**

PCB Solder Stencil and Paste

Stencil screen opening

CG624: 30 x 30 x 7 mils

CG1152 and CG1272: Ø28 x 6 mils

Solder Paste: Qualitek, Type 798 Water Soluble, Alloy Sn63/Pb37

Note: Use circle screen opening (instead of square screen opening) for CG1152 and CG1272 to avoid solder paste bridging for 1.0 mm pitch.

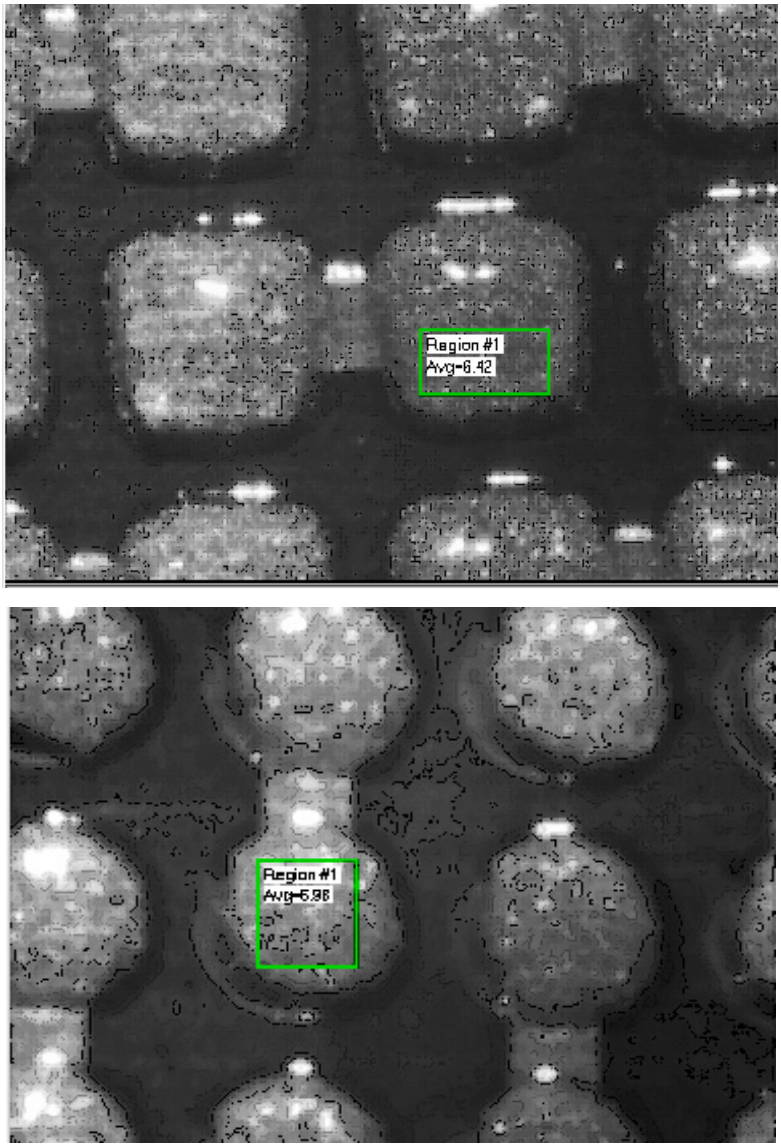
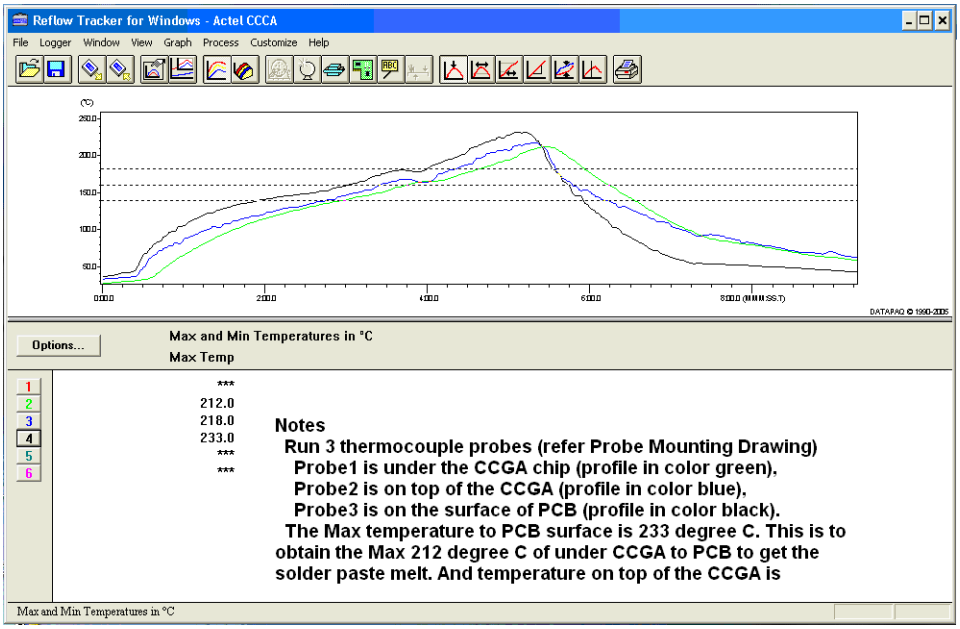
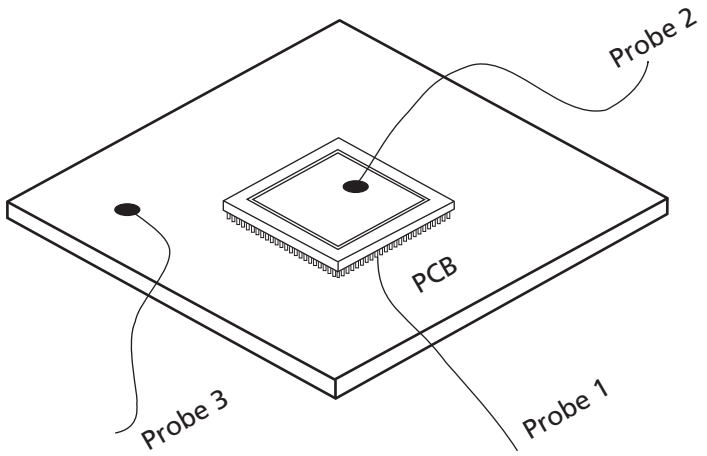


Figure 15 **• Solder Paste on CCGA624 PCB (upper) and on CCGA1152/1272 (lower)**

PCB Reflow Reference





Probe Mounting Drawing

Figure 16 • **CCGA Assembly Reflow Profile (upper) and Temperature Probe Locations (lower)**

Note: 1. Probe 1 is mounted on PCB top surface and in center of package.

2. Probe 2 is mounted on top LID of package.

3. Probe 3 is mounted on PCB top surface.

4. Adjust reflow oven parameter to achieve the 3 probes with similar profile (without large variation).

Related Documents

Thermal Cycling Test Report for Ceramic Column Grid Array Packages--CCGA

Ceramic Column Grid Array Assembly and Rework

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 2 (January 2013)	Modified Table 1 (SAR 41355).	4
	Modified "Column Attach and CCGA Board-Level Reliability" section (SAR 42037)	4

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

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