TEXAS INSTRUMENTS

AN-1457 LP3884X-ADJ Evaluation Board

1 Introduction

The LP38841-ADJ and LP38842-ADJ are ultra low dropout linear regulators that provide adjustable output voltages and load currents up to 800 mA (LP38841) and 1.5A (LP38842). This document describes the evaluation board provided to demonstrate the performance of these parts.

2 Basic Application Circuit

The basic application circuit shown in Figure 1 reflects the electrical connections and component identifiers used on the evaluation board.
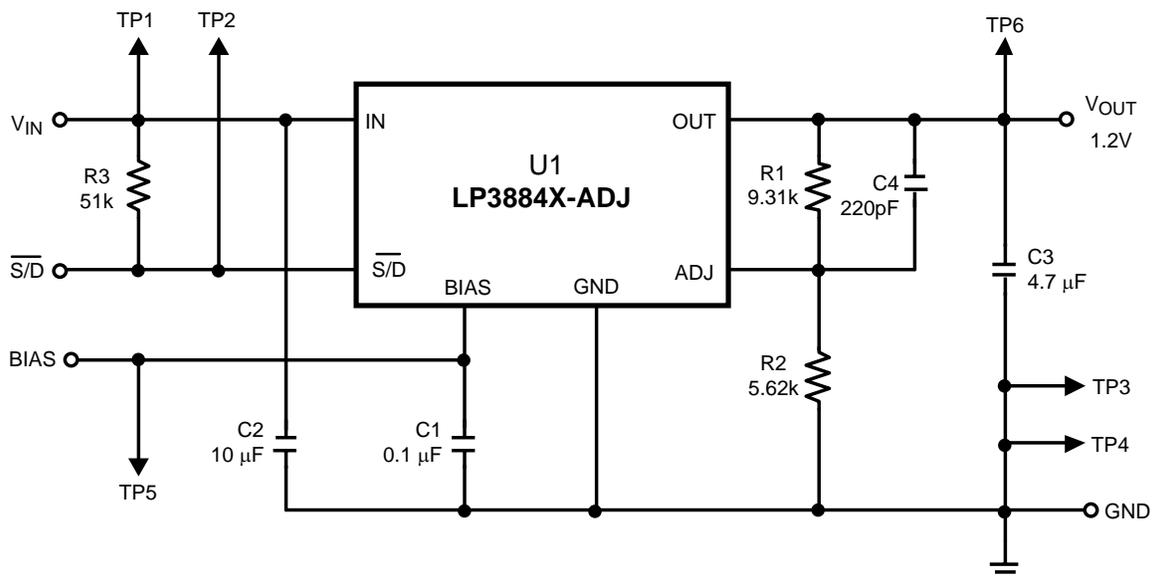

Figure 1. Basic Application Circuit Schematic

3 Capacitor C4 (Feedforward Compensation)

The feedforward capacitor C4 is used to provide increased phase margin. Any good quality X5R/X7R dielectric ceramic capacitor can be used. The value of capacitance for C4 depends on the value of R1. C4 may be calculated using the formula in Equation 1:

$$C4 = 1 / (2 \text{ X } \pi \text{ X } 70k \text{ X } R1) \tag{1}$$

The value of C4 is calculated after R1 is selected to set the output voltage needed for the specific application.

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4 Setting the Output Voltage

The first build of evaluation boards used R1/R2 values, which set the output voltage to 1.2 V. The nominal output voltage is easily changed by replacing R1. The formula that can be used to calculate the new value of R1 for a different output voltage is shown in Equation 2:

$$V_{OUT} = V_{ADJ} \, (R1/R2) + V_{ADJ} \tag{2}$$

Solved for R1:

$$R1 = (V_{OUT} - V_{ADJ}) / V_{ADJ} \, X \, R2 \tag{3}$$

The evaluation board is shipped with a 5.62 kΩ resistor installed at R2.

5 Power Dissipation

Power dissipation must be limited so that the junction temperature does not exceed 125°C. Power dissipation can be calculated using Equation 4:

$$P_{DISS} = ((V_{IN} - V_{OUT}) \, X \, I_{LOAD} \,) + (V_{IN} \, X \, I_{Q(VIN)}) + (V_{BIAS} \, X \, I_{Q(VBIAS)}) \tag{4}$$

In calculating junction temperature, a value of θJ-A (junction-to-ambient thermal resistance) of approximately 50°C/W should be assumed for this board. Junction temperature (T_J) is calculated using Equation 5:

$$T_J = P_{DISS} \, X \, \theta_{(J-A)} + T_{AMBIENT} = P_{DISS} X \, 50 + T_{AMBIENT} \tag{5}$$

Table 1. Component List

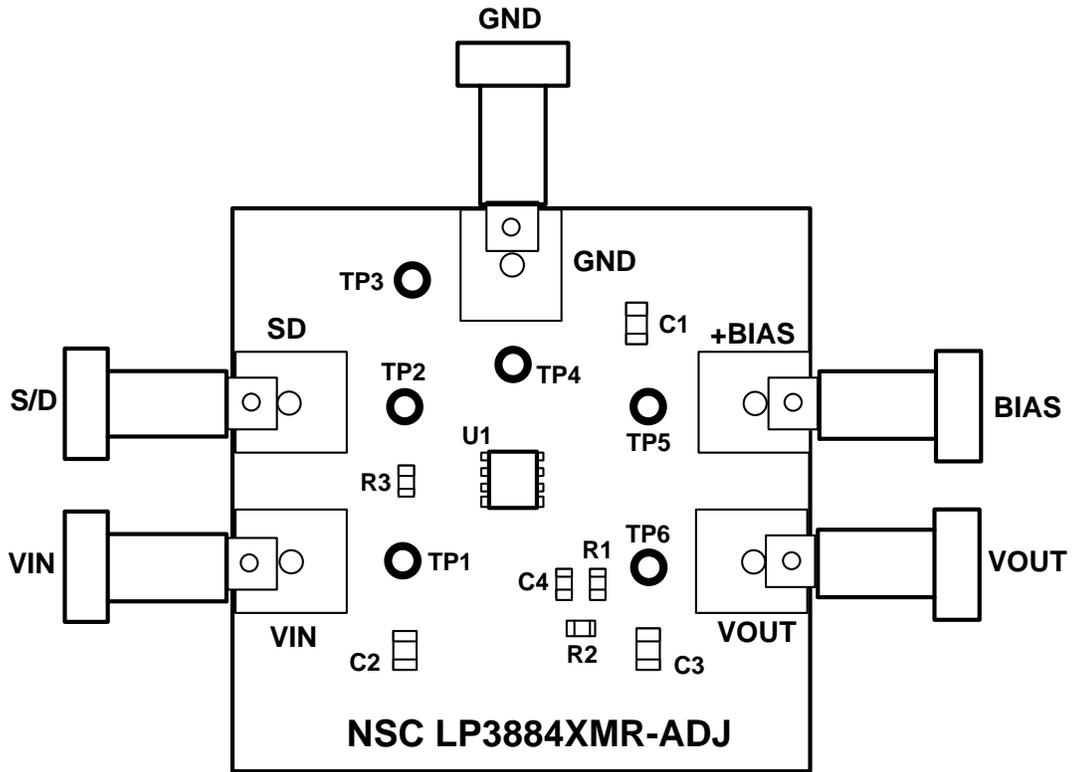|	
PCB	551012613-001 Rev A
U1	LP38842
TP1, TP2, TP3, TP4, TP5, TP6	Test point terminal, NEWARK 97H6311
VIN CONNECTOR	Banana jack (RED): DIGI-KEY 108-0902-001
VOUT CONNECTOR	Banana jack (BLUE): DIGI-KEY 108-0910-001
GROUND CONNECTOR	Banana jack (BLACK): DIGI-KEY 108-0903-001
S/D CONNECTOR	Banana jack (YELLOW): DIGI-KEY 108-0907-001
BIAS CONNECTOR	Banana jack (GREEN): DIGI-KEY 108-0904-001
R1	Banana, 0805 case, 9.31 kΩ, 1% DIGI-KEY 311-(9.31K)CCT-ND
R2	Resistor, 0805 case, 5.62 kΩ, 1% DIGI-KEY 311-(5.62K)CCT-ND
R3	R3: resistor, 0805 case, 51 kΩ, 5% DIGI-KEY 311-(51K)ACT-ND
C1	Ceramic capacitor, 0805 case, 0.1 µF, X5R/X7R dielectric: DIGI-KEY 478-3351-1-ND
C2	Ceramic capacitor, 10 µF, Taiyo-Yuden #LMK325BJ106MN
C3	Ceramic capacitor, 4.7 µF, Taiyo-Yuden # JMK316BJ475MD
C4	Ceramic capacitor, 0805 case, 220 pF, X5R/X7R dielectric: DIGI-KEY 311-1123-1-ND

6 PCB Layout Diagram

Figure 2. Top View

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