

**400mA LOAD SWITCH FEATURING PNP TRANSISTOR AND N-MOSFET WITH GATE PULL-DOWN RESISTOR**
**Product Summary**

Reference	Device Type	R1 (NOM)	R2 (NOM)	R3 (NOM)	Figure
Q1	PNP Transistor	10K	220	—	2
Q2	N-MOSFET	—	—	37K	2

**Description**

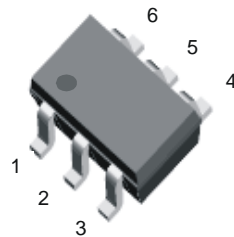
LMN400B01 is best suited for applications where the load needs to be turned on and off using control circuits like micro-controllers, comparators etc. particularly at a point of load. It features a discrete pass transistor with stable  $V_{CE(SAT)}$  which does not depend on input voltage and can support continuous maximum current of 400 mA. It also contains a discrete N-MOSFET with gate pull-down resistor that can be used as control. The component devices can be used as a part of a circuit or as a stand alone discrete device.

**Features**

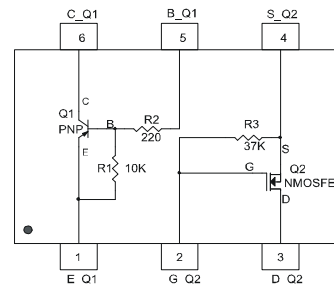
- Voltage Controlled Small Signal Switch
- N-MOSFET with Gate Pull-Down Resistor
- Ideally Suited for Automated Assembly Processes
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

**Mechanical Data**

- Case: SOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture sensitivity: Level 1 per J-STD-020C
- Terminal Connections: See Diagram
- Terminals: Finish - Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 **(e3)**
- Weight: 0.016 grams (approximate)



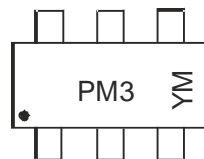
Top View


 Top View  
Internal Schematic

**Ordering Information (Note 4)**

Part Number	Case	Packaging
LMN400B01-7	SOT26	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com>.

**Marking Information**


PM3 = Product Type Marking Code,  
 YM = Date Code Marking  
 Y = Year, e.g., Z = 2012  
 M = Month, e.g., 9 = September

## Date Code Key

Year	2006	2007	.....	2012	2013	2014	2015	2016	2017
Code	T	U	.....	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P <sub>D</sub>	300	mW
Power Derating Factor above +100°C	P <sub>DER</sub>	2.4	mW/°C
Output Current	I <sub>OUT</sub>	400	mA

**Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C
Thermal Resistance, Junction to Ambient Air (Note 5)	R <sub>θJA</sub>	417	°C/W

**Maximum Ratings:**
**Pre-Biased PNP Transistor (Q1)** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V <sub>CBO</sub>	-50	V
Collector-Emitter Voltage	V <sub>CEO</sub>	-50	V
Supply Voltage	V <sub>CC</sub>	-50	V
Input Voltage	V <sub>IN</sub>	-6 to +5	V
Output Current	I <sub>C</sub>	-400	mA

**Maximum Ratings:**
**ESD Protected N-Channel MOSFET (Q2)** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DSS</sub>	60	V
Drain Gate Voltage (R <sub>GS</sub> ≤ 1MΩ)	V <sub>DGR</sub>	60	V
Gate-Source Voltage	V <sub>GSS</sub>	Continuous	+/-20
		Pulsed (tp < 50μS)	+/-40
Drain Current (Note 5)	I <sub>D</sub>	Continuous (V <sub>GS</sub> = 10V)	115
		Pulsed (tp < 10μS, Duty Cycle < 1%)	800
Continuous Source Current	I <sub>S</sub>	115	mA

Note: 5. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch; pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

**Electrical Characteristics: Pre-Biased PNP Transistor (Q1)** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 6)</b>						
Collector-Base Cut Off Current	$I_{CBO}$	—	—	-500	nA	$V_{CB} = -50\text{V}, I_E = 0$
Collector-Emitter Cut Off Current	$I_{CEO}$	—	—	-1	$\mu\text{A}$	$V_{CE} = -50\text{V}, I_B = 0$
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	-50	—	—	V	$I_C = -10\mu\text{A}, I_E = 0$
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	-50	—	—	V	$I_C = -2\text{mA}, I_B = 0$
Input Off Voltage	$V_{I(OFF)}$	-0.3	—	—	V	$V_{CE} = -5\text{V}, I_C = -100\mu\text{A}$
Output Current	$I_{O(OFF)}$	—	—	-1	$\mu\text{A}$	$V_{CC} = -50\text{V}, V_I = 0\text{V}$
<b>ON CHARACTERISTICS (Note 6)</b>						
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	—	-0.06	-0.15	V	$I_C = -10\text{mA}, I_B = -0.3\text{mA}$
		—	-0.18	-0.30	V	$I_C = -300\text{mA}, I_B = -30\text{mA}$
		—	-0.28	-0.60	V	$I_C = -500\text{mA}, I_B = -50\text{mA}$
DC Current Gain	$h_{FE}$	55	220	—	—	$V_{CE} = -5\text{V}, I_C = -50\text{mA}$
		55	260	—	—	$V_{CE} = -5\text{V}, I_C = -100\text{mA}$
		55	265	—	—	$V_{CE} = -5\text{V}, I_C = -200\text{mA}$
		55	225	—	—	$V_{CE} = -5\text{V}, I_C = -400\text{mA}$
Input On Voltage	$V_{I(ON)}$	-3.0	-1.5	—	$V_{DC}$	$V_O = -0.3\text{V}, I_C = -2\text{mA}$
Input Current	$I_i$	—	-18	-45	mA	$V_I = -5\text{V}$
Base-Emitter Turn-on Voltage	$V_{BE(ON)}$	—	-1.2	-1.6	V	$V_{CE} = -5\text{V}, I_C = -400\text{mA}$
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	—	-1.9	-2.5	V	$I_C = -50\text{mA}, I_B = -5\text{mA}$
		—	-5.25	-6.00		$I_C = -400\text{mA}, I_B = -20\text{mA}$
Input Resistor (Base), +/- 30%	R2	0.154	0.220	0.286	K $\Omega$	—
Pull-up Resistor (Base to $V_{CC}$ supply), +/- 30%	R1	7	10	13	K $\Omega$	—
Resistor Ratio (Input Resistor/Pullup resistor)	R1/R2	36	45	55	—	—
<b>SMALL SIGNAL CHARACTERISTICS</b>						
Gain Bandwidth Product	$f_T$	—	200	—	MHz	$V_{CE} = -10\text{V}, I_E = -5\text{mA}, f = 100\text{MHz}$

\* Pulse Test: Pulse width,  $t_p < 300\mu\text{s}$ , Duty Cycle,  $d \leq 0.02$   
 Note: 6. Short duration pulse test used to minimize self-heating effect.

**Electrical Characteristics:**  
**ESD Protected N-Channel MOSFET (Q2)** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 6)</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	60	—	—	V	$V_{GS} = 0V, I_D = 10\mu A$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	1	$\mu A$	$V_{GS} = 0V, V_{DS} = 60V$
Gate-Body Leakage Current, Forward	$I_{GSSF}$	—	—	0.95	mA	$V_{GS} = 20V, V_{DS} = 0V$
Gate-Body Leakage Current, Reverse	$I_{GSSR}$	—	—	-0.95	mA	$V_{GS} = -20V, V_{DS} = 0V$
<b>ON CHARACTERISTICS (Note 6)</b>						
Gate Source Threshold Voltage	$V_{GS(th)}$	1	1.6	2.5	V	$V_{DS} = V_{GS}, I_D = 0.25mA$
Static Drain-Source On-State Voltage	$V_{DS(on)}$	—	0.09	1.5	V	$V_{GS} = 5V, I_D = 50mA$
		—	0.6	3.75		$V_{GS} = 10V, I_D = 500mA$
On-State Drain Current	$I_{D(on)}$	500	—	—	mA	$V_{GS} = 10V,$ $V_{DS} \geq 2 * V_{DS(on)}$
Static Drain-Source On Resistance	$R_{DS(on)}$	—	1.6	3	$\Omega$	$V_{GS} = 5V, I_D = 50mA$
		—	1.2	2		$V_{GS} = 10V, I_D = 500mA$
Forward Transconductance	$g_{FS}$	80	260	—	mS	$V_{DS} \geq 2 * V_{DS(on)}, I_D = 200 mA$
Gate Pull-Down Resistor, +/- 35%	R3	—	37	—	k $\Omega$	—
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	$C_{iss}$	—	—	50	pF	$V_{DS} = -25V, V_{GS} = 0V, f = 1MHz$
Output Capacitance	$C_{oss}$	—	—	25	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	—	5	pF	
<b>SWITCHING CHARACTERISTICS*</b>						
Turn-On Delay Time	$t_{d(on)}$	—	—	20	ns	$V_{DD} = 30V, V_{GS} = 10V,$ $I_D = 200mA,$ $R_G = 25\Omega, R_L = 150\Omega$
Turn-Off Delay Time	$t_{d(off)}$	—	—	40	ns	
<b>SOURCE-DRAIN (BODY) DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
Drain-Source Diode Forward On-Voltage	$V_{SD}$	—	0.88	1.5	V	$V_{GS} = 0V, I_S = 300 mA^*$
Maximum Continuous Drain-Source Diode Forward Current (Reverse Drain Current)	$I_S$	—	—	300	mA	—
Maximum Pulsed Drain-Source Diode Forward Current	$I_{SM}$	—	—	800	mA	—

\* Pulse Test: Pulse width,  $t_p < 300\mu s$ , Duty Cycle,  $d \leq 0.02$

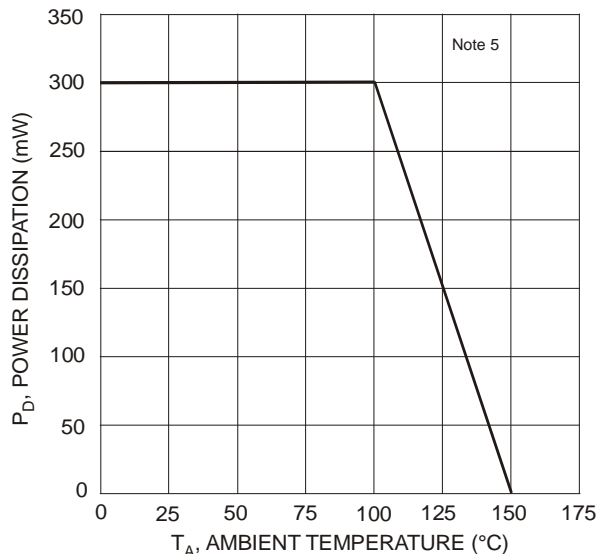


Fig. 3 Max Power Dissipation vs. Ambient Temperature

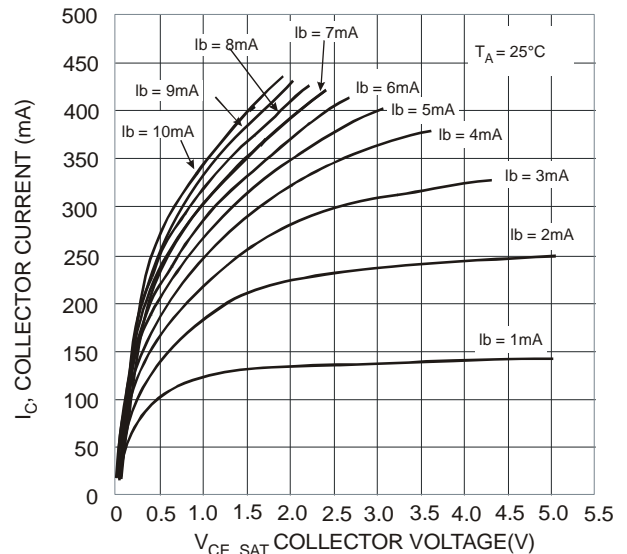


Fig. 4 Output Current vs. Voltage Drop (Pass Element PNP)

**Pre-Biased PNP Transistor Characteristics**

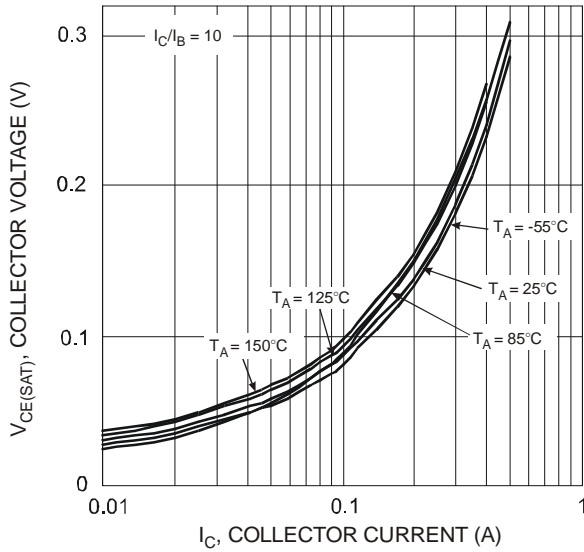


Fig. 5  $V_{CE(SAT)}$  vs.  $I_C$

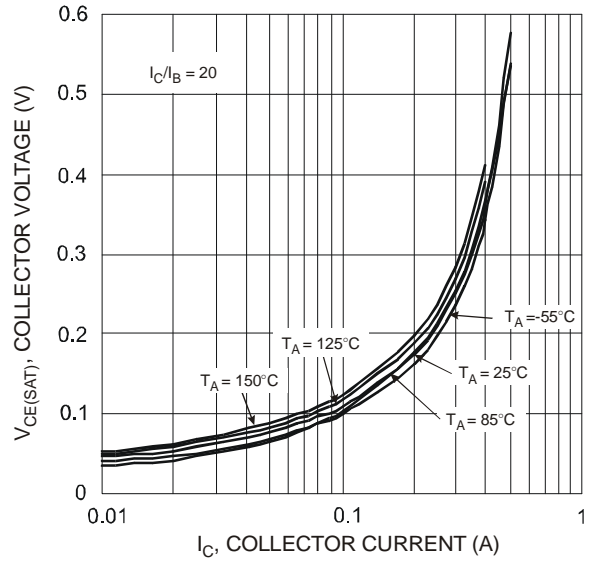


Fig. 6  $V_{CE(SAT)}$  vs.  $I_C$

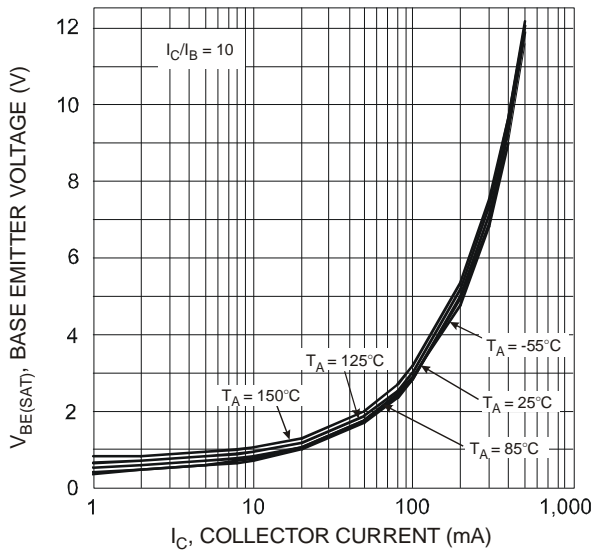


Fig. 7  $V_{BE(SAT)}$  vs.  $I_C$

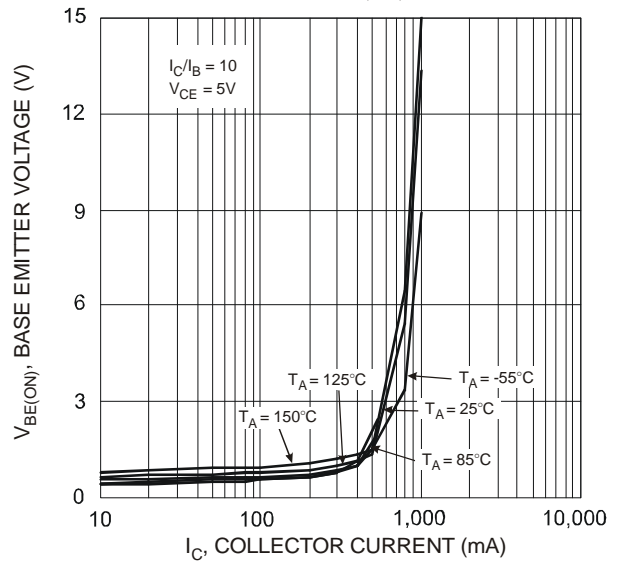


Fig. 8  $V_{BE(ON)}$  vs.  $I_C$

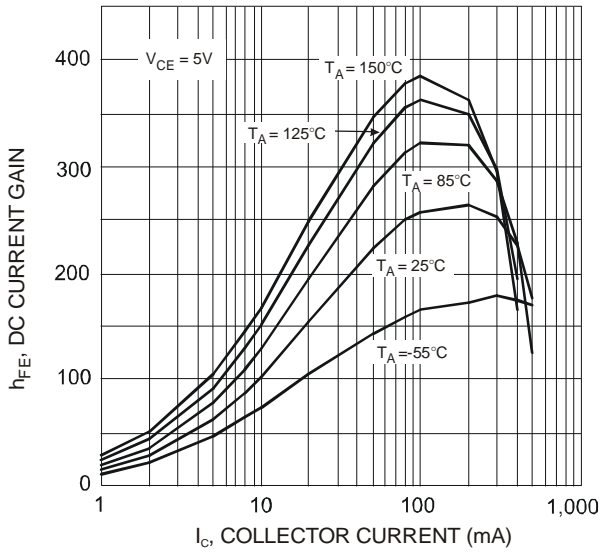
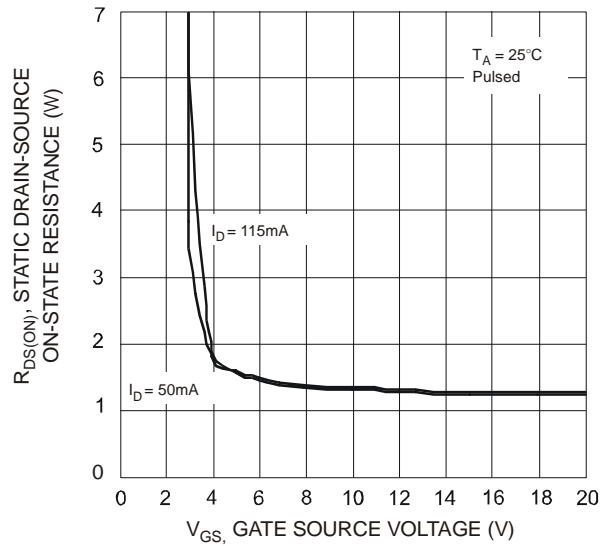
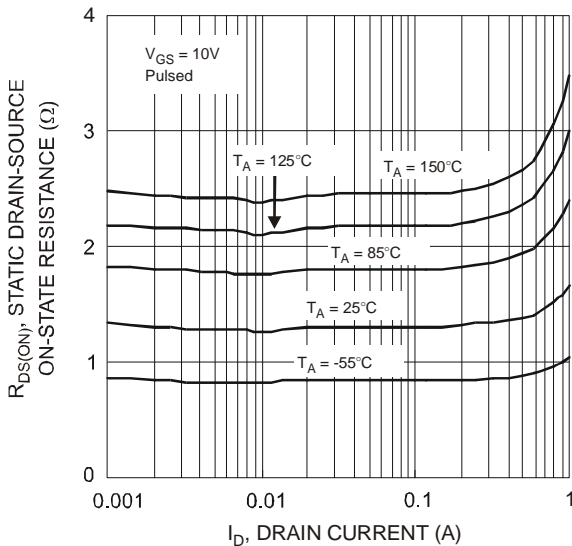
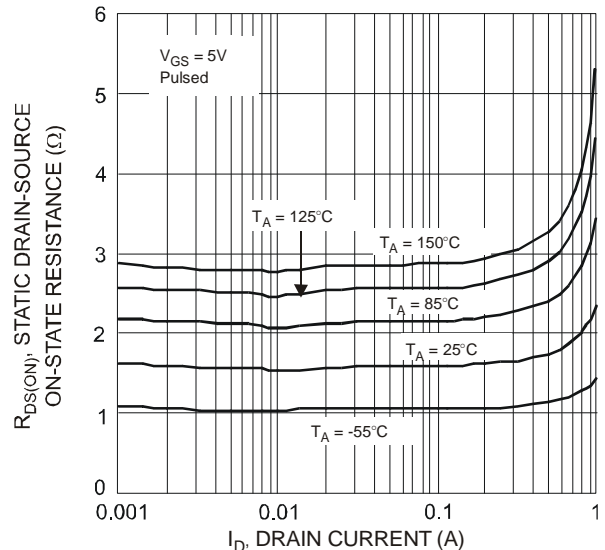
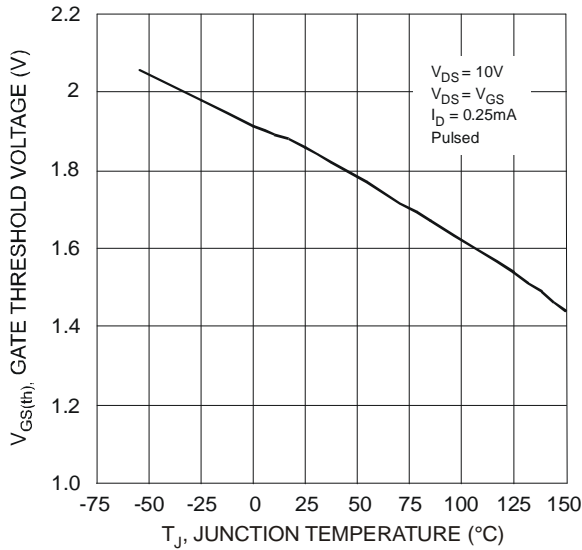
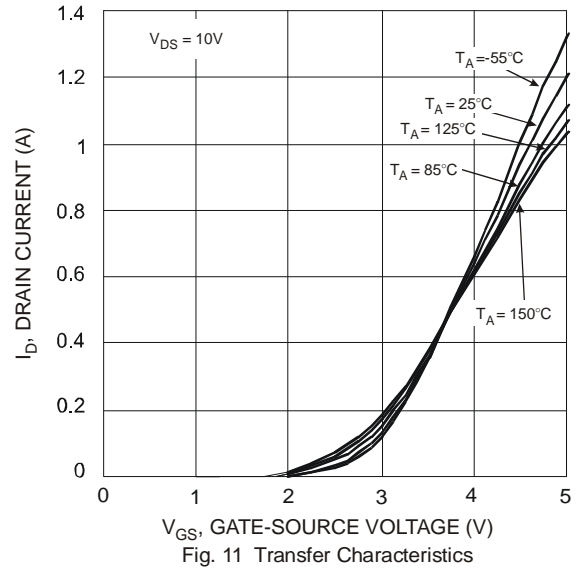
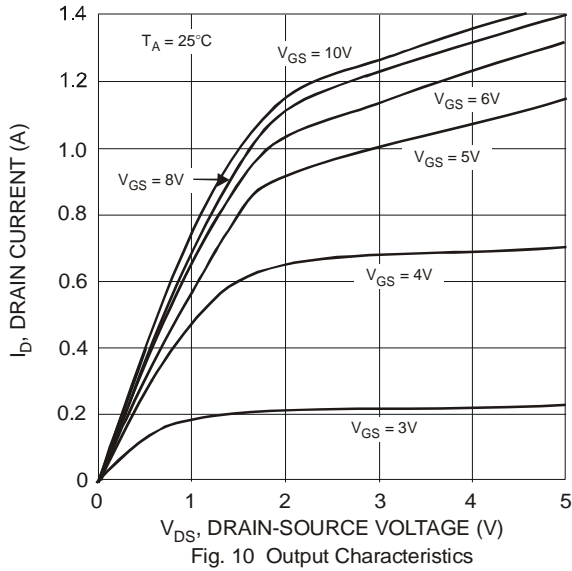


Fig. 9  $h_{FE}$  vs.  $I_C$

**Typical N-Channel MOSFET (Q2) Characteristics**



**Typical N-Channel MOSFET (Q2) Characteristics (cont.)**

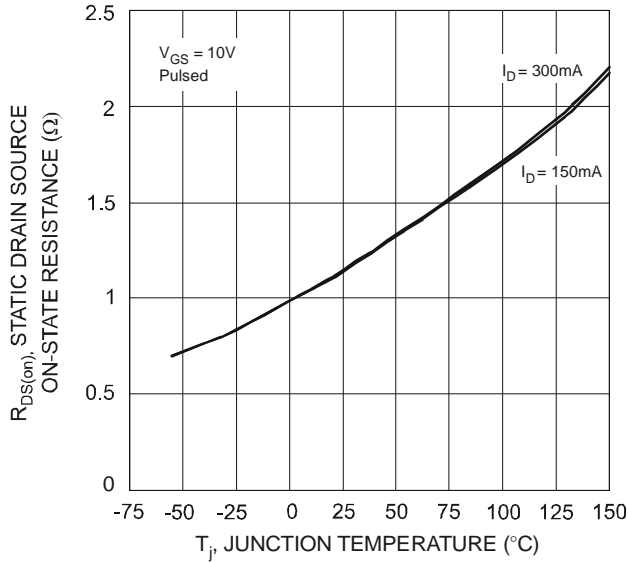


Fig. 16 Static Drain-Source On-State Resistance vs. Junction Temperature

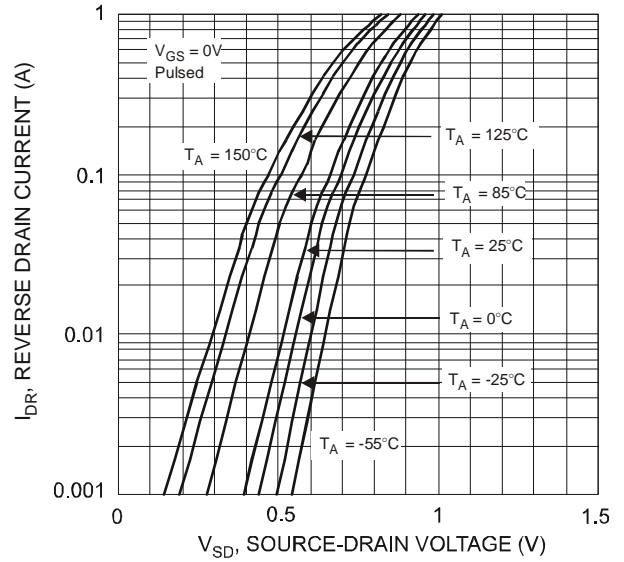


Fig. 17 Reverse Drain Current vs. Source-Drain Voltage

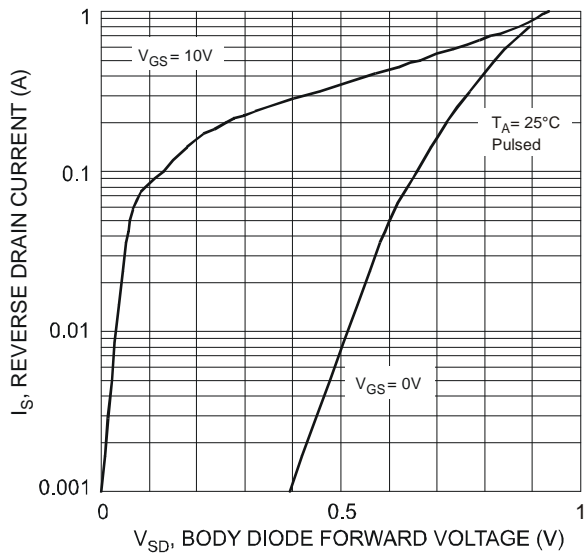


Fig. 18 Reverse Drain Current vs. Source-Drain Voltage

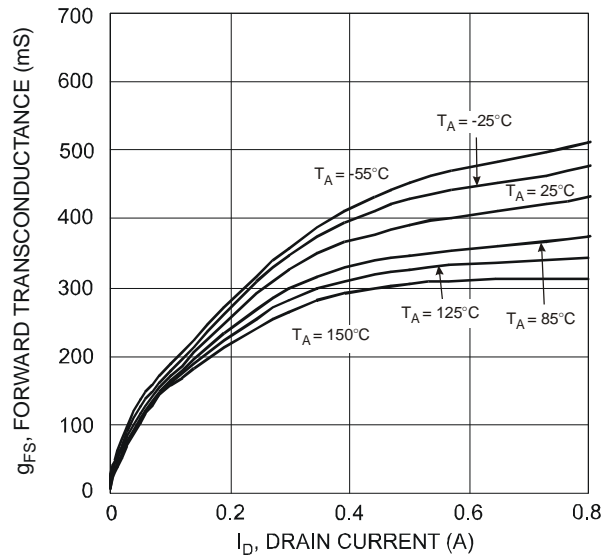


Fig. 19 Forward Transconductance vs. Drain Current ( $V_{DS} > I_D * R_{DS(ON)}$ )

## Application Details

PNP Transistor and ESD Protected N-MOSFET integrated as one in LMN400E01 can be used as a discrete entity for general applications or as an integrated circuit to function as a Load Switch. When it is used as the latter as shown in Figure 20, various input voltage sources can be used as long as it does not exceed the maximum ratings of the device. These devices are designed to deliver continuous output load current up to a maximum of 400mA. The MOSFET Switch draws no current, hence the loading of the control circuitry is prevented. Care must be taken for higher levels of dissipation while designing for higher load conditions. These devices provide high power and also consume less space. The product mainly helps in optimizing power usage, thereby conserving battery life in a controlled load system like portable battery powered applications. (Please see Figure 21 for one example of a typical application circuit used in conjunction with a voltage regulator as a part of power management system).

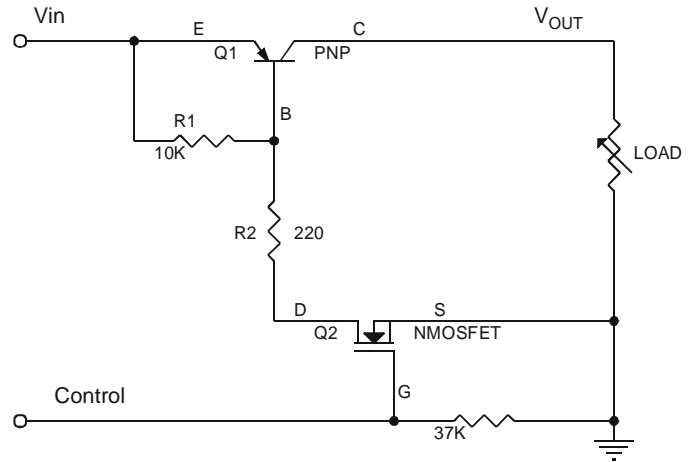


Figure 20 Circuit Diagram

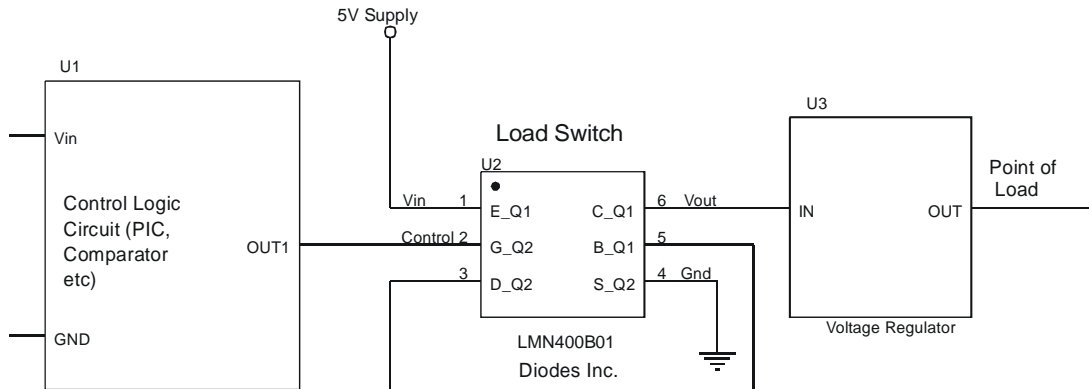
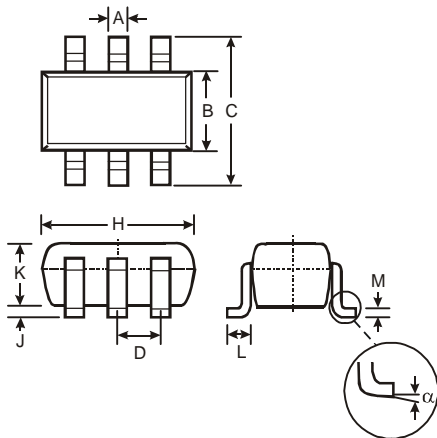


Figure 21 Typical Application Circuit

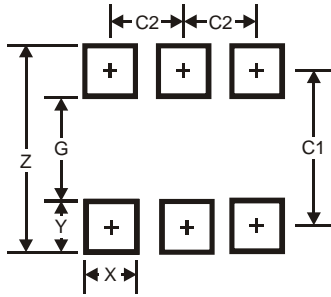
## Package Outline Dimensions



SOT26			
Dim	Min	Max	Typ
A	0.35	0.50	0.38
B	1.50	1.70	1.60
C	2.70	3.00	2.80
D	—	—	0.95
H	2.90	3.10	3.00
J	0.013	0.10	0.05
K	1.00	1.30	1.10
L	0.35	0.55	0.40
M	0.10	0.20	0.15
$\alpha$	0°	8°	—
<b>All Dimensions in mm</b>			



## Suggested Pad Layout



Dimensions	Value (in mm)
Z	3.20
G	1.60
X	0.55
Y	0.80
C1	2.40
C2	0.95

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

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