



# ByteBlaster II Download Cable

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## User Guide



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## Introduction

The ByteBlaster™ II download cable allows you to program and configure Altera® devices. This cable drives configuration data from a standard parallel printer port on your PC to the device on the PCB. Because design changes are downloaded directly to the device, prototyping is easy and you can accomplish multiple design iterations in quick succession.

## Supported Devices

You can use the ByteBlaster II download cable to download configuration data to the following Altera devices:

- Stratix® series FPGAs
- Cyclone® series FPGAs
- MAX® series CPLDs
- Arria™ GX series FPGAs
- APEX™ series FPGAs
- ACEX® 1K FPGAs
- Mercury™ FPGAs
- FLEX 10K® series FPGAs
- Excalibur™ FPGAs

You can perform in-system programming of the following devices:

- Advanced configuration devices including EPC2, EPC4, EPC8, and EPC16 devices.
- Serial configuration devices including EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128 devices.

In addition, you can perform SignalTap® II logic analysis.

The ByteBlaster II download cable supports target systems using 5.0-V TTL, 3.3-V LVTTTL/LVCMOS, and single-ended I/O standards from 1.5 V to 3.3 V.

## Power Requirements

The ByteBlaster II download cable requires between 1.5 V and 5.0 V from the target circuit board.

The ByteBlaster II cable can be used in 1.8-V, 2.5-V, 3.3-V, and 5.0-V systems.

The ByteBlaster II  $V_{CC(TRGT)}$  pin must be connected to the appropriate voltage for the device that is being programmed. The pull-up resistors on the target circuit board for the configuration/programming signals must be connected to the same power supply as the ByteBlaster II  $V_{CC(TRGT)}$ .

## Software Requirements


The ByteBlaster II download cable is available for Windows 2000, Windows NT, Windows XP, and Linux.

Use the Quartus® II software version 4.0 or later to configure your device. The ByteBlaster II download cable also supports the following tools:

- Quartus II Programmer (for programming and configuration), which you can run within the Quartus II software or as a standalone version
- Quartus II SignalTap II Embedded Logic Analyzer (for logic analysis), which you can run within the Quartus II software or as a standalone version
- Nios® II IDE (for software downloading and debugging)
- Nios II IDE Flash Programmer (for programming Flash devices)

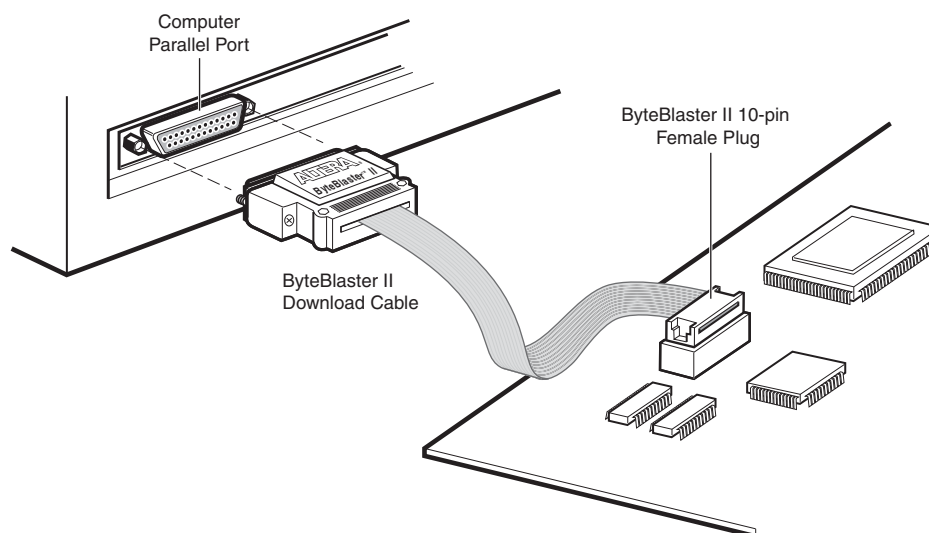
## Hardware Setup

This section describes how to install and set up the ByteBlaster II download cable for device configuration and programming.


 For plug and header dimensions, pin names, and operating conditions, refer to [Chapter 2, ByteBlaster II Specifications](#) chapter. Connect your ByteBlaster II download cable to the circuit board as instructed below:

1. Disconnect the power cable from the circuit board.
2. Connect the ByteBlaster II cable to a parallel port on your PC.
3. Connect the ByteBlaster II download cable to the 10-pin header on the device board. [Figure 1-1](#) shows the ByteBlaster II download cable and the circuit board connector.

**Figure 1-1.** The ByteBlaster II Download Cable



4. Connect the power cable to reapply power to the circuit board.

-  If the **Found New Hardware** wizard prompts you to install a new hardware driver, close the wizard and install the hardware driver using the instructions provided in “[Installing the Driver on a Windows System](#)” or “[Installing the Driver on a Linux System](#)”, depending on your system.

## Software Setup

This section describes the following topics:

- “[Installing the Driver on a Windows System](#)” on page 1-3
- “[Installing the Driver on a Linux System](#)” on page 1-4
- “[Setting Up the ByteBlaster II Hardware in the Quartus II Software](#)” on page 1-5

### Installing the Driver on a Windows System

This section describes how to install the ByteBlaster II driver on a Windows system.


Before you begin the installation, verify the ByteBlaster II driver is located in your directory:

```
\<Quartus II system directory>\drivers\win2000\win2000.inf
```

#### Installing the Driver for Windows 2000 and Windows XP

To install the driver for Windows 2000 or Windows XP, perform the following steps:

1. For Windows 2000, choose **Settings > Control Panel** (Windows Start menu). For Windows XP, choose **Control Panel** (Windows Start menu).
2. Click **Switch to Classic View** if necessary (Control Panel window).
3. Double-click the **Add Hardware** icon to start the **Add Hardware** wizard and click **Next** to continue.
4. Select **Yes, I have already connected the hardware** and click **Next**.
5. Select **Add a new hardware device** from the **Installed hardware** list, and click **Next** to continue.
6. Select **Install from a list or specified location (Advanced)** and click **Next** to continue.

 Depending on your system, the wording of this option may vary slightly.

7. Select **Sound, video and game controllers**, and click **Next** to continue.
8. Select **Have Disk** and browse to the location of the driver on your system. The default location is the `\<Quartus II system directory>\drivers\win2000` directory.
9. Select **win2000.inf** and click **Open** to continue.
10. Click **OK** to install the selected driver.
11. Click **Continue Anyway** when the Software Installation warning appears.
12. Select **Altera ByteBlaster** and click **Next** to continue.
13. Click **Next** to install the driver.

14. Click **Continue Anyway** when the Hardware Installation warning appears.
15. Click **Finish** in the Completing the Add Hardware Wizard window. Reboot your system.

### Installing the Driver for Windows NT

To install the driver for Windows NT, perform the following steps:

1. For Windows NT, choose **Settings > Control Panel** (Windows Start menu).
2. Double-click the **Multimedia** icon in the **Control Panel** window.
3. Click the **Devices** tab and click the **Add** button.
4. Click **Unlisted or Updated Driver** from the **List of Drivers** list box and click **OK**.
5. Browse to the location of the driver on your system. The default location is the `\<Quartus II system directory>\ drivers \win2000` directory. Click **OK**.
6. Select **Altera ByteBlaster** or **Altera ByteBlaster II** in the **Add Unlisted or Updated Driver** window and click **OK**. Reboot your system.

### Installing the Driver on a Linux System

The Altera ByteBlaster kernel driver is required for Linux workstations running Red Hat Linux version 7.3 or 8.0 or Red Hat Enterprise Linux version 3.0 or later that use the ByteBlaster II download cable. You must install and compile the Altera ByteBlaster kernel driver separately from the Quartus II software.

To compile the Altera ByteBlaster kernel driver, you must have the following Red Hat Package Manager (RPM) packages, which are available from the Red Hat website at [www.redhat.com](http://www.redhat.com):

- **.gcc-2.96-81**
- **.make-3.79.1-5**
- **.binutils-2.10.91.0.2-3**
- **kernel-headers** (RPM version must correspond to kernel version)

To verify that an RPM is installed, use the `rpm -q <name>` command. For example, `rpm -q gcc` verifies that the gcc RPM is installed.



You do not need to install the ByteBlaster II download cable before installing the Altera ByteBlaster kernel driver.



You must have superuser or “root” privileges to install this driver.

To install the driver for Linux, perform the following steps:

1. Decompress the **byteblaster.tar.gz** file by typing the following command at the command prompt:

```
tar -xzvf byteblaster.tar.gz ↵
```

2. Access the new directory by typing the following command at the command prompt:

```
cd byteblaster ↵
```

3. Run the **configure** install script by typing the following command at the command prompt:

```
./configure ←
```

4. Compile the Altera ByteBlaster kernel driver by typing the following command at the command prompt:

```
make ←
```

5. Become root and compile the Altera ByteBlaster kernel driver module and device nodes by typing the following command at the command prompt:

```
make install ←
```

6. To install the Altera ByteBlaster kernel driver, type the following command at the command prompt:

```
jtagconfig --add byteblaster2 /dev/byteblaster0 ←
```

7. To determine whether the ByteBlaster II download cable and the Altera ByteBlaster kernel driver are installed correctly, display a list of available devices by typing the following command at the command prompt:

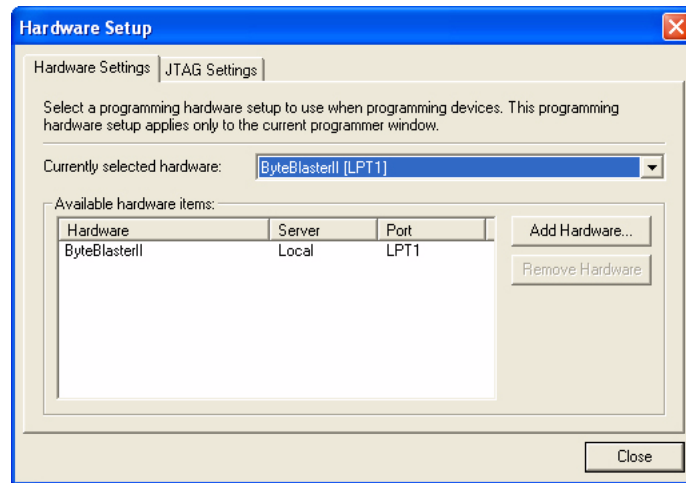
```
jtagconfig ←
```

You should see a list of devices on your JTAG chain, including the ByteBlaster II download cable.

## Setting Up the ByteBlaster II Hardware in the Quartus II Software

To set up the ByteBlaster II hardware in the Quartus II software, perform the following steps:

1. Start the Quartus II software.
2. On the Tools menu, click **Programmer**.
3. Click **Hardware Setup**. The **Hardware Settings** tab of the **Hardware Setup** dialog box appears.
4. In the **Currently selected hardware** list, select **ByteBlasterII [LPT1]**.
5. Click **Add Hardware**. The **Add Hardware** dialog box appears. Select **ByteBlaster MV** or **ByteBlaster II** and click **OK**.
6. **ByteBlasterII** is now visible in the **Available hardware items list of the Hardware Setup** dialog box, as shown in [Figure 1-2](#).

**Figure 1–2.** Hardware Setup Dialog Box

7. Click **Close** to close the **Hardware Setup** dialog box.
8. In the **Mode** list, select the desired mode (Programmer window). [Table 1–1](#) describes each mode.



The ByteBlaster II supports the Joint Test Action Group (JTAG), Passive Serial Programming, and Active Serial modes.

**Table 1–1.** Programming Modes

Mode	Mode Description
Joint Test Action Group (JTAG)	Programs or configures all Altera devices supported by the Quartus II software, excluding FLEX 6000 and EPCS serial configuration devices.
In-Socket Programming	Not supported by the ByteBlaster II cable.
Passive Serial Programming	Configures all Altera devices supported by the Quartus II software, excluding MAX 3000, MAX 7000, MAX II, and EPCS serial configuration devices.
Active Serial Programming	Programs a single EPCS1, EPCS4, EPCS16, EPCS64 or EPCS128 serial configuration device.



For details about the Quartus II Programmer, refer to the [Quartus II Programmer](#) chapter in volume 1 of the [Quartus II Handbook](#).



For details about programming devices and creating secondary programming files, refer to the [Programming & Configuration](#) chapter of the [Introduction to the Quartus II Software](#) manual.



For more information, refer to the Programming module of the Quartus II software online tutorial and the following topics in the Quartus II Help:

- Changing the Hardware Setup
- Programmer Introduction
- Overview: Working with Chain Description Files

- Overview: Converting Programming Files





### Overview

This chapter provides comprehensive information about the ByteBlaster™ II download cable, including the following:

- ByteBlaster II connections
  - Voltage requirements
  - Cable-to-board connection
  - ByteBlaster II 25-pin header connection
  - ByteBlaster II 10-pin header connection
  - Circuit board header connection
- Operating conditions

### ByteBlaster II Connections

The ByteBlaster II cable has a 25-pin male header parallel printer plug that connects to the PC, and a 10-pin female plug that connects to the circuit board. Data is downloaded from the parallel printer port on the PC through the ByteBlaster II cable to the circuit board.

### Voltage Requirements

The ByteBlaster II  $V_{CC(TrGT)}$  pin must be connected to a specific voltage for the device that is being programmed. Connect pull-up resistors to the same power supply as the ByteBlaster II  $V_{CC(TrGT)}$ . Refer to [Table 2-1](#) for voltage requirements for specific device families.

**Table 2-1.** ByteBlaster II  $V_{CC(TrGT)}$  Pin Voltage Requirements (Part 1 of 2)

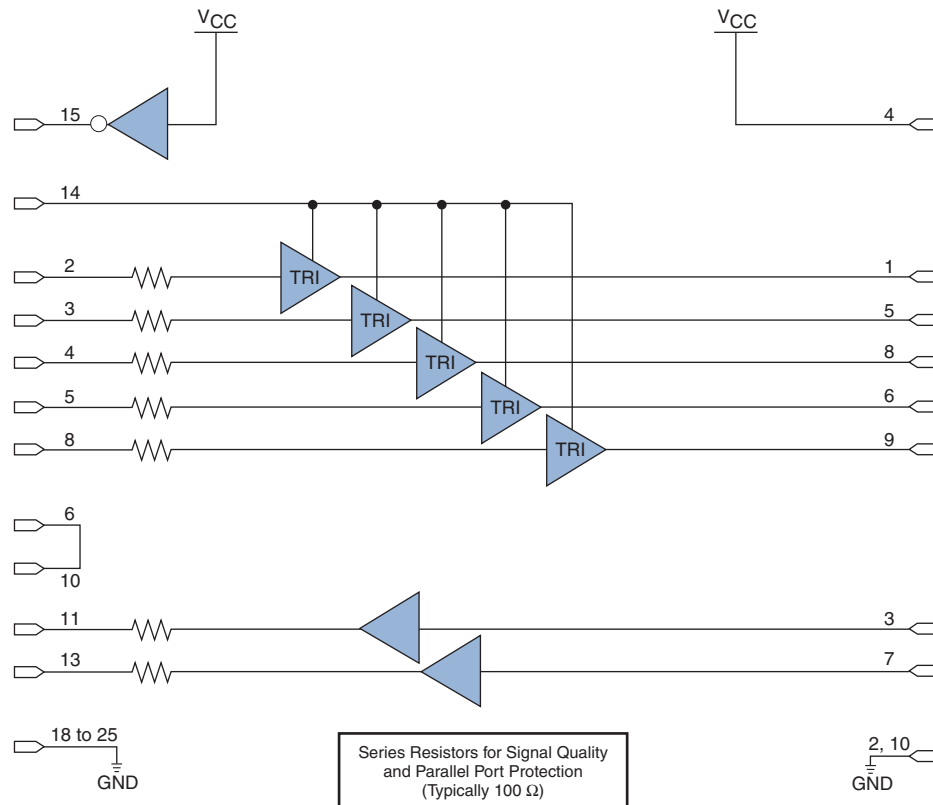
Device Family	ByteBlaster II VCC Voltage Required
MAX® II devices	As specified by VCCIO of Bank 1
MAX 7000S devices	5 V
MAX 7000AE and MAX 3000A devices	3.3 V
MAX 7000B device	2.5 V
Stratix® III and Stratix IV devices	As specified by $V_{CCPGM}$ or $V_{CCPD}$
Cyclone® III devices	As specified by $V_{CCA}$ or $V_{CCIO}$
Stratix II, Stratix, Stratix II GX, Stratix GX, and Arria™ GX devices	As specified by VCCSEL
Cyclone II, Cyclone, APEX™ II, APEX 20K, and Mercury™ devices	As specified by VCCIO
FLEX 10K®, FLEX 8000, and FLEX 6000 devices	5 V
FLEX 10KE devices	2.5 V
FLEX 10KA and FLEX 6000A devices	3.3 V
EPC2	5 V or 3.3 V

**Table 2-1.** ByteBlaster II  $V_{CC(TRGT)}$  Pin Voltage Requirements (Part 2 of 2)

EPC4, EPC8, and EPC16 devices	3.3 V
EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128 devices	3.3 V

## Cable-to-Board Connection

The ByteBlaster II cable has a standard parallel printer plug that connects to the PC. [Figure 2-1](#) shows a block diagram of the ByteBlaster II download cable.

**Figure 2-1.** ByteBlaster II Block Diagram

## ByteBlaster II 25-Pin Header Connection

The 25-pin male header connects to a parallel port with a standard parallel cable. [Table 2-2](#) identifies the plug pin names and the corresponding programming modes.

**Table 2-2.** ByteBlaster II 25-Pin Header Pin-Outs (Part 1 of 2)

Pin	AS Mode		PS Mode		JTAG Mode	
	Signal Name	Description	Signal Name	Description	Signal Name	Description
2	DCLK	Clock signal	DCLK	Clock signal	TCK	Clock signal
3	nCONFIG	Configuration control	nCONFIG	Configuration control	TMS	JTAG state machine control
4	nCS	Serial configuration device chip select	—	No connect	—	No connect

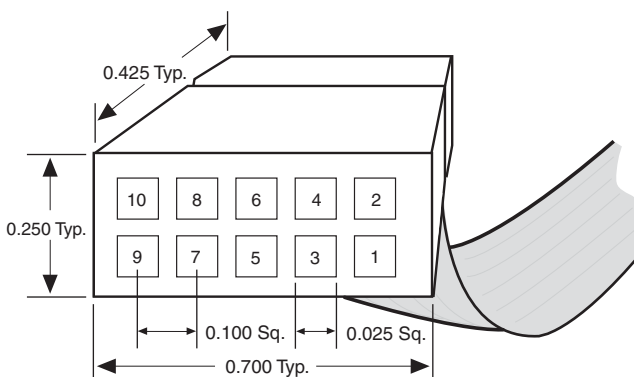
**Table 2-2.** ByteBlaster II 25-Pin Header Pin-Outs (Part 2 of 2)

5	nCE	Cyclone chip enable	—	No connect	—	No connect
8	ASDI	Active serial data in	DATA0	Data to device	TDI	Data to device
11	CONF_DONE	Configuration done	CONF_DONE	Configuration done	TDO	Data from device
13	DATAOUT	Active serial data out	nSTATUS	Signal status	—	No connect
15	nVCC Detect	—	nVCC Detect	—	nVCC Detect	—
18 to 25	GND	Signal ground	GND	Signal ground	GND	Signal ground

## ByteBlaster II 10-Pin Header Connection

The 10-pin female plug connects to a 10-pin male header on the circuit board. [Figure 2-2](#) shows the dimensions of the female plug.

**Figure 2-2.** ByteBlaster II 10-Pin Female Plug Dimensions



Dimensions are shown in inches. Spacing between pin centers is 0.1 inches.

[Table 2-3](#) identifies the 10-pin female plug signal names and the corresponding programming mode.

**Table 2-3.** ByteBlaster II Female Plug Signal Names and Programming Modes (Part 1 of 2)

Pin	AS Mode		PS Mode		JTAG Mode	
	Signal Name	Description	Signal Name	Description	Signal Name	Description
1	DCLK	Clock signal	DCLK	Clock signal	TCK	Clock signal
2	GND	Signal ground	GND	Signal ground	GND	Signal ground
3	CONF_DONE	Configuration done	CONF_DONE	Configuration done	TDO	Data from device
4	VCC (TRGT)	Target power supply	VCC (TRGT)	Target power supply	VCC (TRGT)	Target power supply
5	nCONFIG	Configuration control	nCONFIG	Configuration control	TMS	JTAG state machine control
6	nCE	Cyclone chip enable	—	No connect	—	No connect
7	DATAOUT	Active serial data out	nSTATUS	Configuration status	—	No connect
8	nCS	Serial configuration device chip select	—	No connect	—	No connect


**Table 2-3.** ByteBlaster II Female Plug Signal Names and Programming Modes (Part 2 of 2)

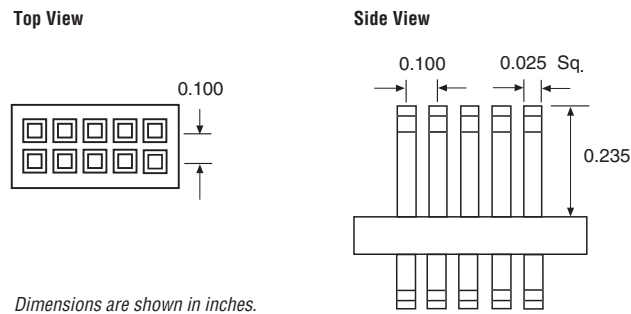
9	ASDI	Active serial data in	DATA0	Data to device	TDI	Data to device
10	GND	Signal ground	GND	Signal ground	GND	Signal ground

 The circuit board must supply VCC(TRGT) and ground to the ByteBlaster II cable for the I/O drivers.

## Circuit Board Header Connection

The circuit board's 10-pin male header has two rows of five pins connected to the device's programming or configuration pins. Figure 2-3 shows the dimensions of a typical 10-pin male header.

 Although a 10-pin surface mount header can be used for the JTAG, AS or PS download cable, Altera recommends using a through-hole connector due to the repeated insertion and removal force needed.

**Figure 2-3.** 10-Pin Male Header Dimensions

## Operating Conditions

Table 2-4 through Table 2-6 summarize the maximum ratings, recommended operating conditions, and DC operating conditions for the ByteBlaster II cable.

**Table 2-4.** ByteBlaster II Cable Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(TRGT)}$	Target supply voltage	With respect to ground	-0.3	5.5	V
$I_I$	Input current	TDO or dataout	-10.0	10.0	mA
$I_O$	Output current	TCK, TMS, TDI, nCS, nCE	-20.0	20.0	mA

**Note to Table 2-4:**

(1) The operating conditions are identical for both leaded and lead-free ByteBlaster II download cables.

**Table 2-5.** ByteBlaster II Cable Recommended Operating Conditions (Note 1)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(TRGT)}$	Target supply voltage, 5.0-V operation	—	4.75	5.25	V
	Target supply voltage, 3.3-V operation	—	3.0	3.6	V
	Target supply voltage, 2.5-V operation	—	2.375	2.625	V
	Target supply voltage, 1.8-V operation	—	1.71	1.89	V
	Target supply voltage, 1.5-V operation	—	1.43	1.57	V

**Note to Table 2-5:**

(1) The operating conditions are identical for both leaded and lead-free ByteBlaster II download cables.

**Table 2-6.** ByteBlaster II Cable DC Operating Conditions (Note 1)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{IH}$	High-level input voltage	—	$V_{CC(TRGT)} - 0.2$	—	V
$V_{IL}$	Low-level input voltage	—	—	0.15	V
$V_{OH}$	5.0-V high-level output voltage	$V_{CC(TRGT)} = 4.5\text{ V}, I_{OH} = 8\text{ mA}$	4.4	—	V
	3.3-V high-level output voltage	$V_{CC(TRGT)} = 3.0\text{ V}, I_{OH} = 4\text{ mA}$	2.9	—	V
	2.5-V high-level output voltage	$V_{CC(TRGT)} = 2.375\text{ V}, I_{OH} = 2\text{ mA}$	2.275	—	V
	1.8-V high-level output voltage	$V_{CC(TRGT)} = 1.71\text{ V}, I_{OH} = 2\text{ mA}$	1.61	—	V
	1.5-V high-level output voltage	$V_{CC(TRGT)} = 1.43\text{ V}, I_{OH} = 2\text{ mA}$	1.33	—	V
$V_{OL}$	5.0-V low-level output voltage	$V_{CC(TRGT)} = 5.5\text{ V}, I_{OL} = 8\text{ mA}$	—	0.125	V
	3.3-V low-level output voltage	$V_{CC(TRGT)} = 3.6\text{ V}, I_{OL} = 4\text{ mA}$	—	0.125	V
	2.5-V low-level output voltage	$V_{CC(TRGT)} = 2.625\text{ V}, I_{OL} = 2\text{ mA}$	—	0.125	V
	1.8-V low-level output voltage	$V_{CC(TRGT)} = 1.89\text{ V}, I_{OL} = 2\text{ mA}$	—	0.125	V
	1.5-V low-level output voltage	$V_{CC(TRGT)} = 1.57\text{ V}, I_{OL} = 2\text{ mA}$	—	0.125	V
$I_{CC(TRGT)}$	Operating current (No Load)	(Typical $I_{CC} = 80\text{ mA}$ )	—	150	mA

**Note to Table 2-6:**

(1) The DC operating conditions are identical for both leaded and lead-free ByteBlaster II download cables.



The RoHS sticker on the ByteBlaster II download cable reflects the hardware upgrade to meet the RoHS lead-free requirement.

## Statement of China-RoHS Compliance

Table 2-7 lists hazardous substances included with the lead-free ByteBlaster II download cable.

**Table 2-7.** Table of Hazardous Substances' Name and Concentration (Note 1)

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Electronic Components	0	0	0	0	0	0
Populated Circuit Board	0	0	0	0	0	0

**Table 2-7.** Table of Hazardous Substances' Name and Concentration *(Note 1)*

<b>Part Name</b>	<b>Lead (Pb)</b>	<b>Cadmium (Cd)</b>	<b>Hexavalent Chromium (Cr6+)</b>	<b>Mercury (Hg)</b>	<b>Polybrominated biphenyls (PBB)</b>	<b>Polybrominated diphenyl Ethers (PBDE)</b>
Manufacturing Process	0	0	0	0	0	0
Packing	0	0	0	0	0	0

**Notes to Table 2-7:**

- (1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

## Referenced Documents

For more information about configuration and in-system programmability (ISP), refer to the following sources:

- *AN 39: IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*
- *AN 95: In-System Programmability in MAX Devices*
- *Configuring Arria GX Devices* chapter in volume 2 of the *Arria GX Device Handbook*
- *Configuring Cyclone FPGAs* chapter in the *Cyclone Device Handbook*
- *Configuring Cyclone II Devices* chapter in the *Cyclone II Device Handbook*
- *Configuring Cyclone III Devices* chapter in volume 1 of the *Cyclone III Device Handbook*
- *Configuring Stratix and Stratix GX Devices* chapter in the *Stratix Device Handbook*
- *Configuring Stratix II and Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*
- *Configuring Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*
- *In-System Programmability Guidelines for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Configuration, Design Security, and Remote System Upgrades in Stratix IV Devices* chapter in volume 1 of the *Stratix IV Device Handbook*
- *Programming & Configuration* chapter in the *Introduction to the Quartus II Software* manual
- *Quartus II Programmer* chapter in volume 3 of the *Quartus II Handbook*
- *Serial Configuration Devices (EPCS1, EPCS4, EPCS16, EPCS64, and EPCS128) Data Sheet* chapter in the *Configuration Handbook*
- Programming module of the Quartus® II online tutorial
- Refer to the following glossary definitions in Quartus II Help:
  - ByteBlaster II Cable (general description)
  - Configuration scheme (general description)
  - Programming files (general description)
- Refer to the following procedures in Quartus II Help:
  - Programming a Single Device or Multiple Devices in JTAG or Passive Serial Mode
  - Programming a Single Device in Active Serial Programming Mode
  - Selecting the Communications Cable for the SignalTap II Logic Analyzer

- Refer to the following introduction and overview topics in Quartus II Help:
  - Programmer Introduction
  - Overview: Working with Chain Description Files
  - Overview: Converting Programming Files

## Revision History

The following table shows the revision history of this user guide.

**Table Info-1.** Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2008 v1.4	Updates included: <ul style="list-style-type: none"> <li>■ Added the “Additional Information” page</li> <li>■ General update to the format and style of the user guide</li> <li>■ Updated the “Supported Devices” section</li> <li>■ Updated the “Setting Up the ByteBlaster II Hardware in the Quartus II Software” section</li> <li>■ Updated Table 2-1</li> <li>■ Added a hand note to the “Circuit Board Header Connection” section</li> <li>■ Updated Table 2-6</li> </ul>	—
April 2008 v1.3	Added “Statement of China-RoHS Compliance” section. Added Table 2-7.	—
January 2008 v1.2	Updated “Supported Devices” section. Updated Table 1-1. Updated Table 2-1. Added new note to Table 2-4, Table 2-5, and Table 2-6. Added note about RoHS compliance. Updated “Revision History”	—
December 2004 v1.1	Re-release	—
July 2004 v1.0	Initial release	—



## How to Contact Altera

For the most up-to-date information about Altera® products, refer to the following table.

**Table Info-2.** How to Contact Altera

Contact (1)	Contact Method	Address
Technical support	Website	<a href="http://www.altera.com/support">www.altera.com/support</a>
Technical training	Website	<a href="http://www.altera.com/training">www.altera.com/training</a>
	Email	<a href="mailto:custrain@altera.com">custrain@altera.com</a>
Product literature	Website	<a href="http://www.altera.com/literature">www.altera.com/literature</a>
Altera literature services	Email	<a href="mailto:literature@altera.com">literature@altera.com</a>
Non-technical support (General) (Software Licensing)	Email	<a href="mailto:nacomp@altera.com">nacomp@altera.com</a>
	Email	<a href="mailto:authorization@altera.com">authorization@altera.com</a>

**Note to Table Info-2**

(1) You can also contact your local Altera sales office or sales representative.






## Typographic Conventions

This document uses the typographic conventions shown below.

**Table Info-3.** Typographic Conventions (Part 1 of 2)

Visual Cue	Meaning
<b>Bold Type with Initial Capital Letters</b>	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: <b>Save As</b> dialog box.
<b>bold type</b>	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: <b>f<sub>MAX</sub></b> , <b>\qdesigns</b> directory, <b>d:</b> drive, <b>chiptrip.gdf</b> file.
<i>Italic Type with Initial Capital Letters</i>	Document titles are shown in italic type with initial capital letters. Example: <i>AN 75: High-Speed Board Design</i> .
<i>Italic type</i>	Internal timing parameters and variables are shown in italic type. Examples: <i>t<sub>PIA</sub></i> , <i>n + 1</i> . Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <file name>, <project name>.pof file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
Courier type	Signal and port names are shown in lowercase Courier type. Examples: data1, tdi, input. Active-low signals are denoted by suffix n, for example, resetn. Anything that must be typed exactly as it displays is shown in Courier type. For example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword SUBDESIGN), as well as logic function names (e.g., TRI) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● ●	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.

**Table Info-3.** Typographic Conventions (Part 2 of 2)

<b>Visual Cue</b>	<b>Meaning</b>
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or the user's work.
	A warning calls attention to a condition or possible situation that can cause injury to the user.
	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information about a particular topic.

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