DS91M125 125 MHz 1:4 M-LVDS Repeater with LVDS Input

Check for Samples: DS91M125

FEATURES

- **DC - 125 MHz / 250 Mbps Low Jitter, Low Skew, Low Power Operation**
- **Independent Driver Enable Pins**
- **Outputs Conform to TIA/EIA-899 M-LVDS Standard**
- **Controlled Transition Times Minimize Reflections**
- **Inputs Conform to TIA/EIA-644-A LVDS Standard**
- **8 kV ESD on M-LVDS Output Pins Protects Adjoining Components**
- **Flow-Through Pinout Simplifies PCB Layout**
- **Industrial Operating Temperature Range (−40°C to +85°C)**
- **Available in a Space Saving SOIC-16 Package**

APPLICATIONS

- **Multidrop / Multipoint Clock and Data Distribution**
- **High-Speed, Low Power, Short-Reach Alternative to TIA/EIA-485/422**
- **Clock Distribution in AdvancedTCA (ATCA) and MicroTCA (μTCA, uTCA) Backplanes**

DESCRIPTION

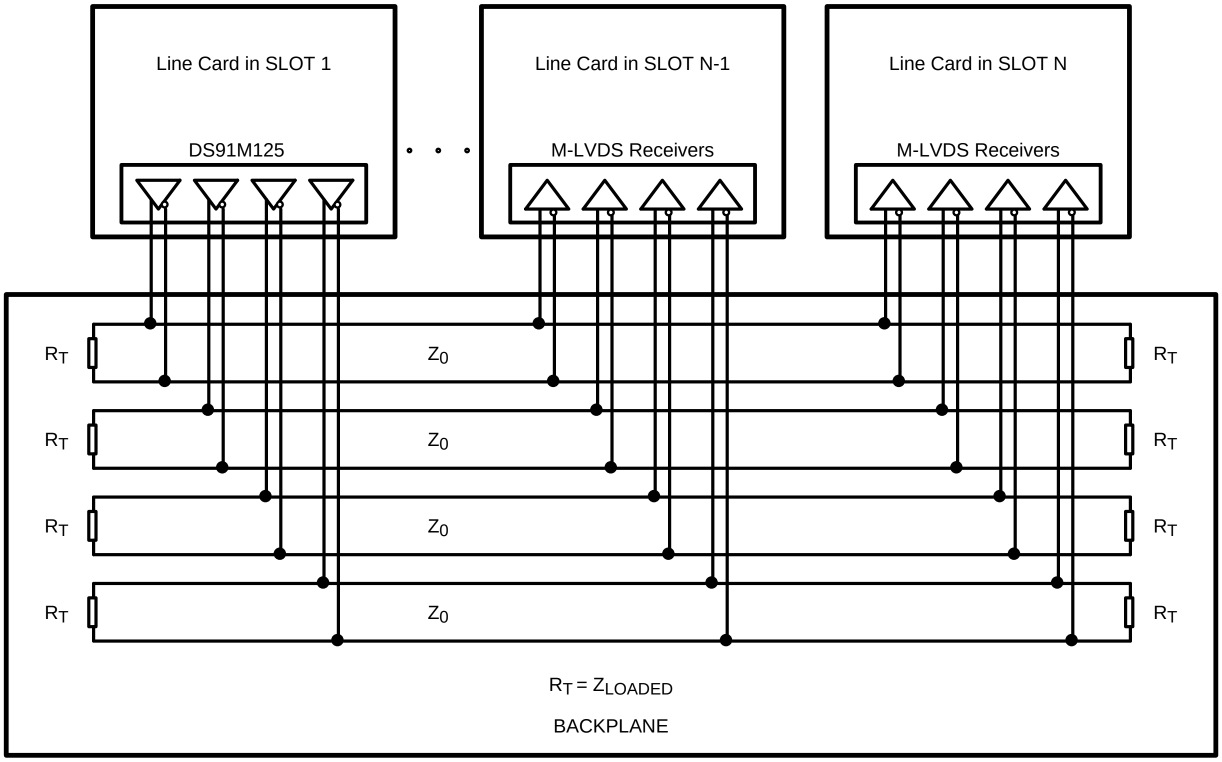
The DS91M125 is a 1:4 M-LVDS repeater designed for driving and distributing clock or data signals to up to four multipoint networks.

M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multi-point applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs.

A single DS91M125 channel is a 1:4 repeater that accepts M-LVDS/LVDS/CML/LVPECL signals and converts them to M-LVDS signal levels. Each output has an associated independent driver enable pin. The DS91M125 input conforms to the LVDS standard.

The DS91M125 has a flow-through pinout for easy PCB layout. It provides a new alternative for high speed multipoint interface applications. It is packaged in a space saving SOIC-16 package.

Typical Application



Connection Diagram

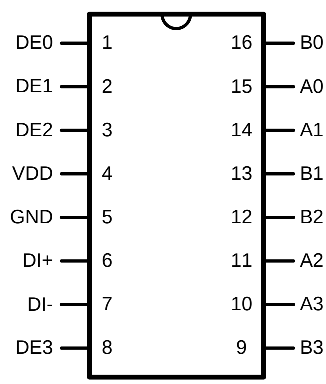
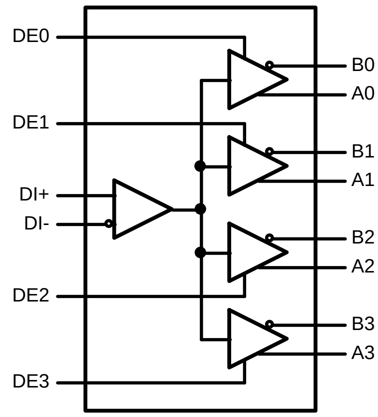


Figure 1. 16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC See Package Number D

Logic Diagram



PIN DESCRIPTIONS

Number	Name	I/O, Type	Description
1, 2, 3, 8	DE	I, LVCMOS	Driver enable pins: When DE is low, the driver is disabled. When DE is high, the driver is enabled. There is a 300 kΩ pulldown resistor on each pin.
6	DI+	I, LVDS	Non-inverting receiver input pin.
7	DI-	I, LVDS	Inverting receiver input pin.
5	GND	Power	Ground pin.
10, 11, 14, 15	A	O, M-LVDS	Non-inverting driver output pin.
9, 12, 13, 16	B	O, M-LVDS	Inverting driver output pin.
4	V_{DD}	Power	Power supply pin, +3.3V ± 0.3V

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[1][2]

Supply Voltage		−0.3V to +4V
LVCMOS Input Voltages		−0.3V to (V_{DD} + 0.3V)
M-LVDS Output Voltages		−1.9V to +5.5V
LVDS Input Voltages		−0.3V to (V_{DD} + 0.3V)
Maximum Package Power Dissipation at +25°C	SOIC Package	2.21W
	Derate SOIC Package	19.2 mW/°C above +25°C
Thermal Resistance (4-Layer, 2 oz. Cu, JEDEC)	θ_{JA}	52°C/W
	θ_{JC}	19°C/W
Maximum Junction Temperature		140°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)		260°C
ESD Susceptibility	HBM[3]	≥ 8 kV
	MM[4]	≥ 250V
	CDM[5]	≥ 1250V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

RECOMMENDED OPERATING CONDITIONS

	Min	Typ	Max	Units
Supply Voltage, V_{DD}	3.0	3.3	3.6	V
Voltage at M-LVDS Outputs	−1.4		+3.8	V
Voltage at LVDS Inputs	0		V_{DD}	V
LVCMOS Input Voltage High V_{IH}	2.0		V_{DD}	V
LVCMOS Input Voltage Low V_{IL}	0		0.8	V
Operating Free Air Temperature T_A	−40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified.[1][2][3][4]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC Specifications						
V_{IH}	High-Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low-Level Input Voltage		GND		0.8	V
I_{IH}	High-Level Input Current	V_{IH} = 3.6V	-15	±1	15	μA
I_{IL}	Low-Level Input Current	V_{IL} = 0V	-15	±1	15	μA
V_{CL}	Input Clamp Voltage	I_{IN} = -18 mA	-1.5			V
M-LVDS Driver DC Specifications						
$\|V_{AB}\|$	Differential output voltage magnitude	R_L = 50Ω, C_L = 5pF	480		650	mV
ΔV_{AB}	Change in differential output voltage magnitude between logic states	See Figure 2and Figure 4	−50	0	+50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	R_L = 50Ω, C_L = 5pF	0.3	1.6	2.1	V
$\|\Delta V_{OS(SS)}\|$	Change in steady-state common-mode output voltage between logic states	See Figure 2 and Figure 3	0		+50	mV
$V_{A(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 5	0		2.4	V
$V_{B(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	R_L = 50Ω, C_L = 5pF,C_D = 0.5pF See Figure 7 and Figure 8 [5]			$1.2V_{SS}$	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		$-0.2V_{SS}$			V
I_{OS}	Differential short-circuit output current	See Figure 6 [6]	-43		43	mA
I_A	Driver output current	V_A = 3.8V, V_B = 1.2V			32	μA
		V_A = 0V or 2.4V, V_B = 1.2V	−20		+20	μA
		V_A = −1.4V, V_B = 1.2V	−32			μA
I_B	Driver output current	V_B = 3.8V, V_A = 1.2V			32	μA
		V_B = 0V or 2.4V, V_A = 1.2V	−20		+20	μA
		V_B = −1.4V, V_A = 1.2V	−32			μA
I_{AB}	Driver output differential current ($I_A - I_B$)	$V_A = V_B$, −1.4V ≤ V ≤ 3.8V	−4		+4	μA
$I_{A(OFF)}$	Driver output power-off current	V_A = 3.8V, V_B = 1.2V, DE = 0V 0V ≤ V_{DD} ≤ 1.5V			32	μA
		V_A = 0V or 2.4V, V_B = 1.2V, DE = 0V 0V ≤ V_{DD} ≤ 1.5V	−20		+20	μA
		V_A = −1.4V, V_B = 1.2V, DE = 0V 0V ≤ V_{DD} ≤ 1.5V	−32			μA

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(3) Typical values represent most likely parametric norms for V_{DD} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(4) C_L includes fixture capacitance and C_D includes probe capacitance.
(5) Specification is ensured by characterization and is not tested in production.
(6) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)(4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{B(OFF)}$	Driver output power-off current	V_B = 3.8V, V_A = 1.2V, DE = 0V 0V ≤ V_{DD} ≤ 1.5V			32	µA
		V_B = 0V or 2.4V, V_A = 1.2V, DE = 0V 0V ≤ V_{DD} ≤ 1.5V	−20		+20	µA
		V_B = −1.4V, V_A = 1.2V, DE = 0V 0V ≤ V_{DD} ≤ 1.5V	−32			µA
$I_{AB(OFF)}$	Driver output power-off differential current ($I_{A(OFF)}$ − $I_{B(OFF)}$)	V_A = V_B, −1.4V ≤ V ≤ 3.8V, DE = 0V 0V ≤ V_{DD} ≤ 1.5V	−4		+4	µA
C_A	Driver output capacitance	V_{DD} = OPEN		7.8		pF
C_B	Driver output capacitance			7.8		pF
C_{AB}	Driver output differential capacitance			3		pF
$C_{A/B}$	Driver output capacitance balance (C_A/C_B)			1		
LVDS Receiver DC Specifications						
V_{IT+}	Positive-going differential input voltage threshold			-5	100	mV
V_{IT-}	Negative-going differential input voltage threshold		−100	-5		mV
V_{CMR}	Common mode voltage range	VID = 100 mV	0.05		V_{DD}-0.05	V
I_{IN}	Input current	VIN = 3.6V, V_{DD} = 3.6V		±1	±10	µA
		VIN = 0V, V_{DD} = 3.6V		±1	±10	µA
C_{IN}	Input capacitance	V_{DD} = OPEN		5		pF
POWER SUPPLY CURRENT						
I_{CCD}	Driver Supply Current	R_L = 50Ω, DE = V_{DD}		67	78	mA
I_{CCZ}	TRI-STATE Supply Current	DE = GND		21	26	mA

SWITCHING CHARACTERISTICS

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AC SPECIFICATION						
t_{PLH}	Differential Propagation Delay Low to High	R_L = 50Ω, C_L = 5 pF,	3.0	5.5	8.5	ns
t_{PHL}	Differential Propagation Delay High to Low	C_D = 0.5 pF	3.0	5.5	8.5	ns
t_{SKD1} ($t_{sk(p)}$)	Pulse Skew $\|t_{PLHD} - t_{PHLD}\|$ (4) (5)	See Figure 7 and Figure 8		65	350	ps
t_{SKD2}	Channel-to-Channel Skew (6) (5)			65	400	ps
t_{SKD3}	Part-to-Part Skew (7) (5)			2.2	2.5	ns
t_{SKD4}	Part-to-Part Skew (8)				5.5	ns
t_{TLH} (t_r)	Rise Time (5)		1.1	2.0	3.0	ns
t_{THL} (t_f)	Fall Time (5)		1.1	2.0	3.0	ns
t_{PZH}	Enable Time (Z to Active High)	R_L = 50Ω, C_L = 5 pF,		6	11	ns
t_{PZL}	Enable Time (Z to Active Low)	C_D = 0.5 pF		6	11	ns
t_{PLZ}	Disable Time (Active Low to Z)	See Figure 9 and Figure 10		6	11	ns
t_{PHZ}	Disable Time (Active High to Z)			6	11	ns
f_{MAX}	Maximum Operating Frequency (5)		125			MHz

(1) The ELECTRICAL CHARACTERISTICS tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes.
(2) Typical values represent most likely parametric norms for V_{DD} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(3) C_L includes fixture capacitance and C_D includes probe capacitance.
(4) t_{SKD1}, $|t_{PLHD} - t_{PHLD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) Specification is ensured by characterization and is not tested in production.
(6) t_{SKD2}, Channel-to-Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.
(7) t_{SKD3}, Part-to-Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
(8) t_{SKD4}, Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.

TEST CIRCUITS AND WAVEFORMS

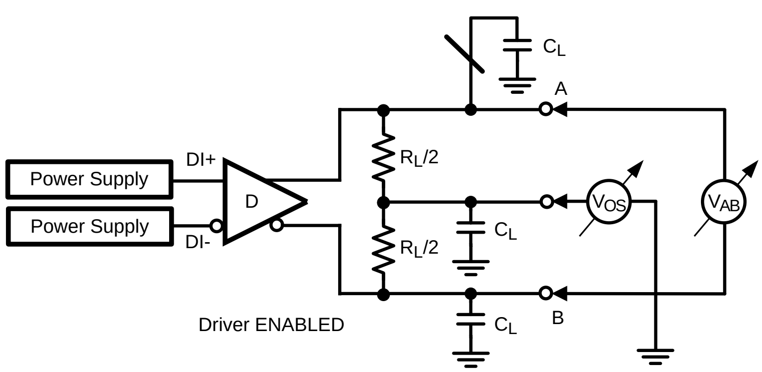


Figure 2. Differential Driver Test Circuit

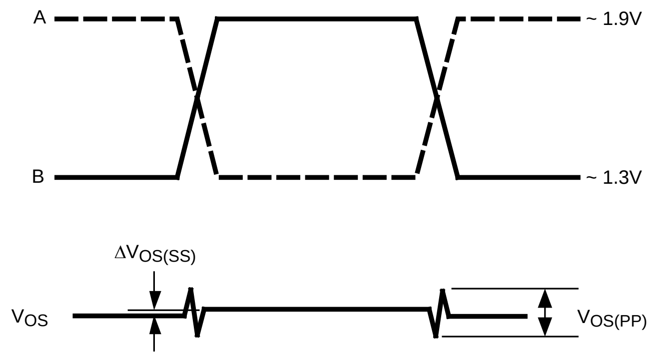


Figure 3. Differential Driver Waveforms

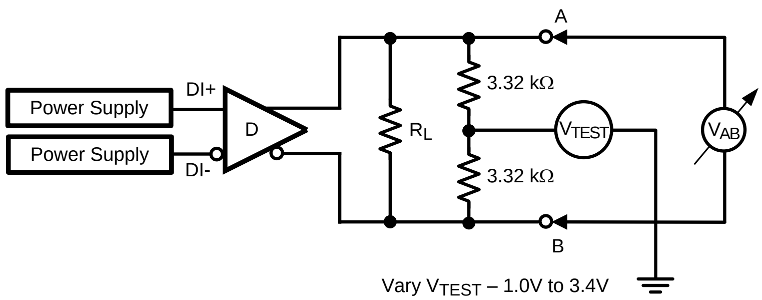


Figure 4. Differential Driver Full Load Test Circuit

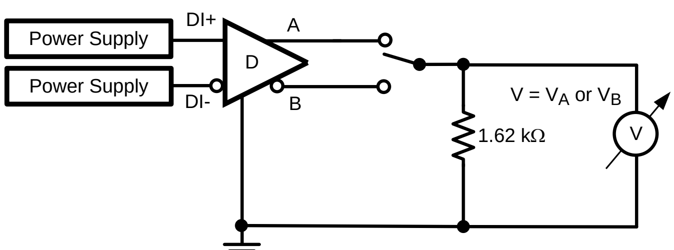


Figure 5. Differential Driver DC Open Test Circuit

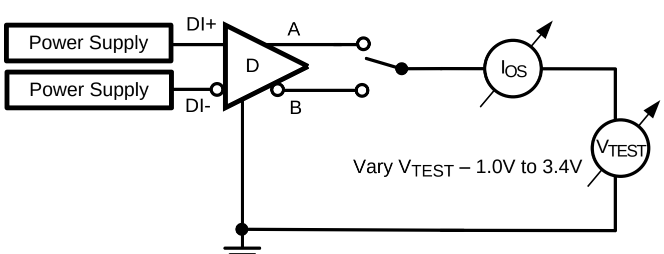


Figure 6. Differential Driver Short-Circuit Test Circuit

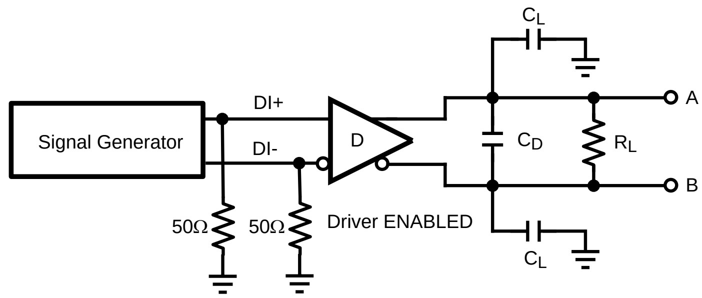


Figure 7. Driver Propagation Delay and Transition Time Test Circuit

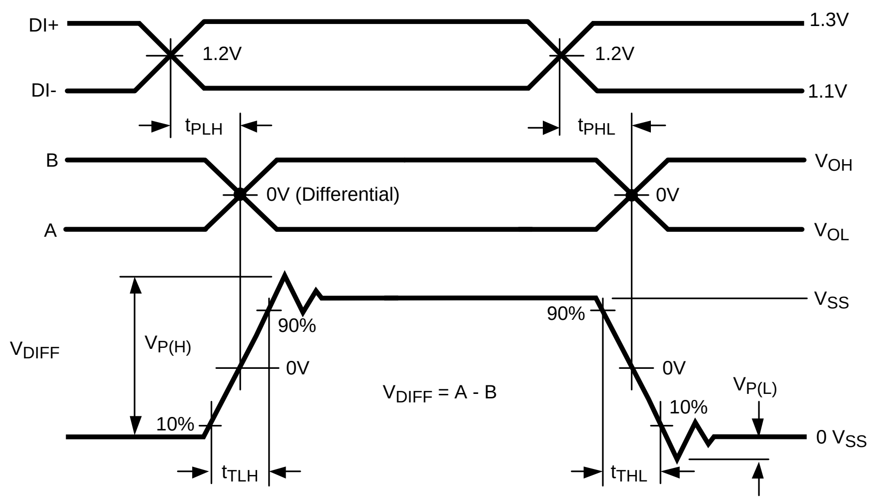


Figure 8. Driver Propagation Delays and Transition Time Waveforms

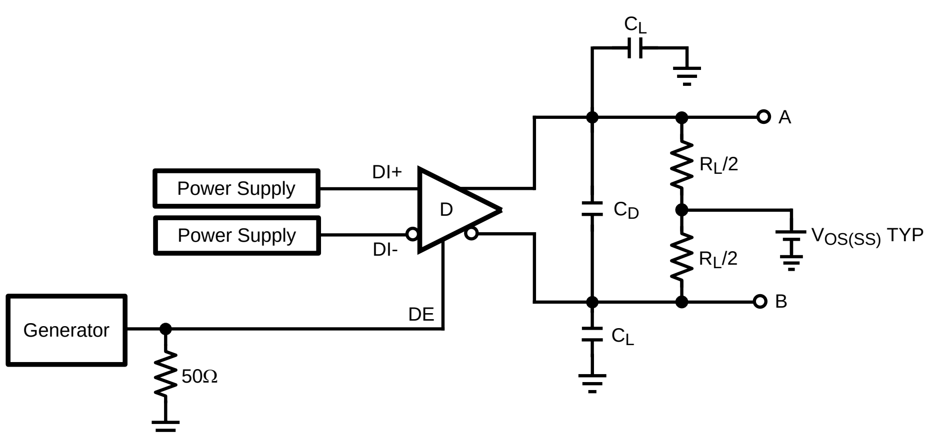


Figure 9. Driver TRI-STATE Delay Test Circuit

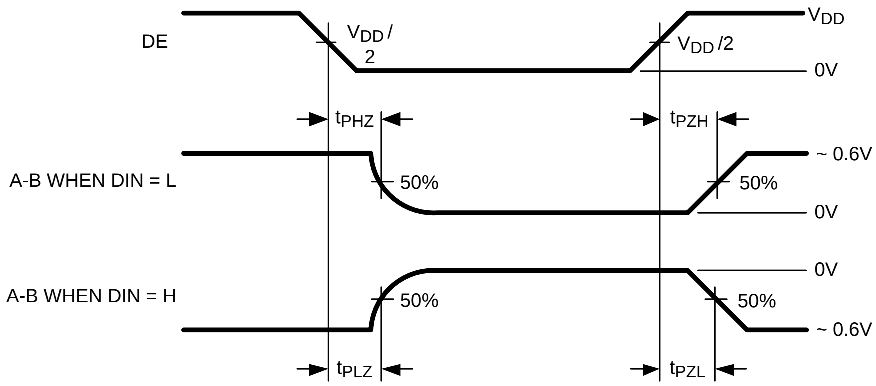


Figure 10. Driver TRI-STATE Delay Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

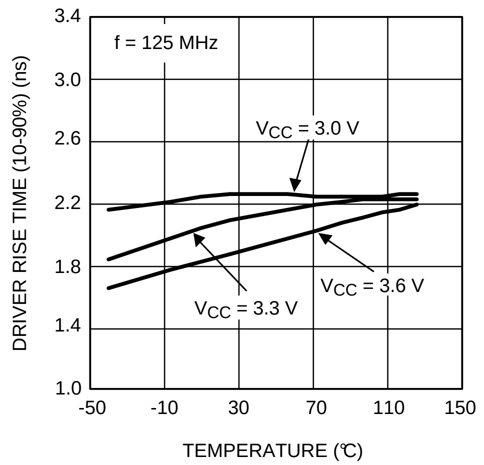


Figure 11. Driver Rise Time as a Function of Temperature

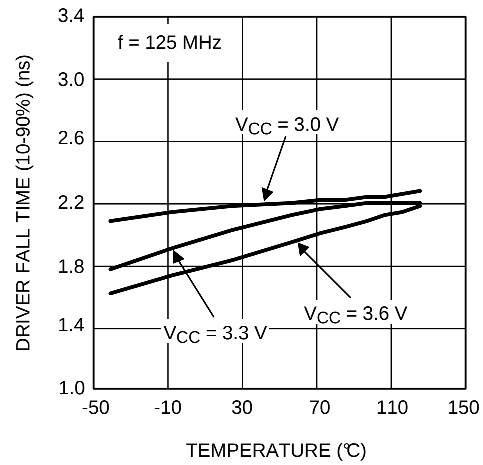


Figure 12. Driver Fall Time as a Function of Temperature

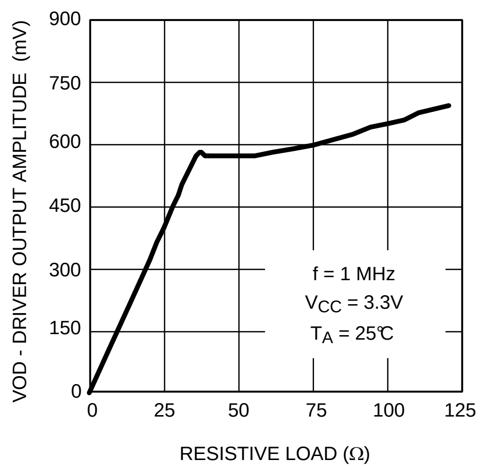


Figure 13. Driver Output Signal Amplitude as a Function of Resistive Load

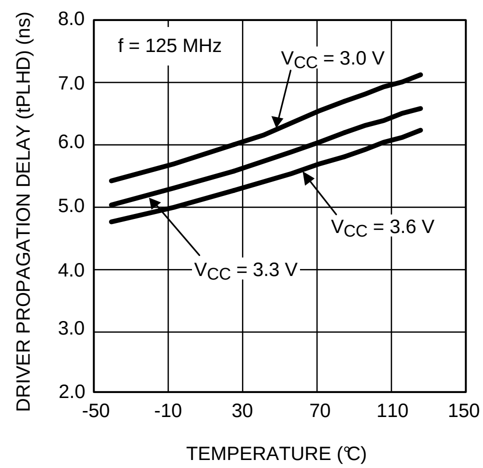


Figure 14. Driver Propagation Delay (tPLHD) as a Function of Temperature

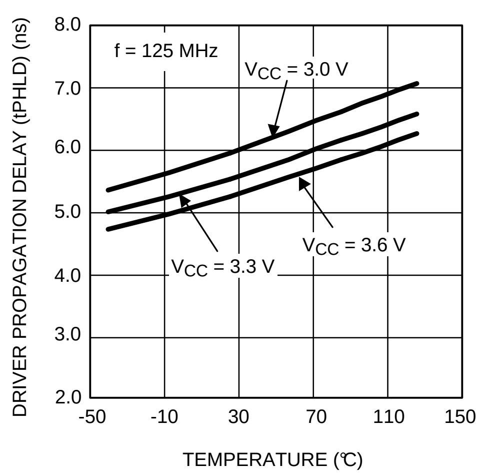


Figure 15. Driver Propagation Delay (tPHLD) as a Function of Temperature

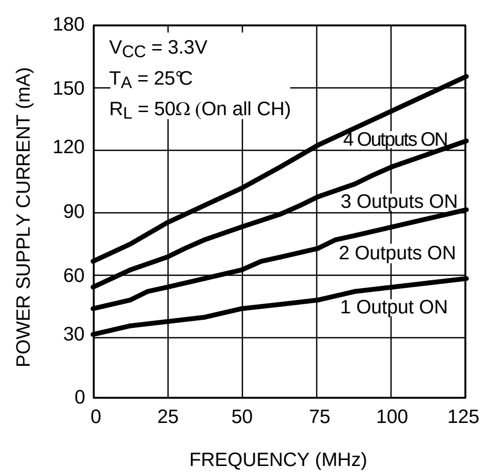


Figure 16. Driver Power Supply Current as a Function of Frequency

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS91M125TMA/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS91M125 TMA	Samples
DS91M125TMAX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS91M125 TMA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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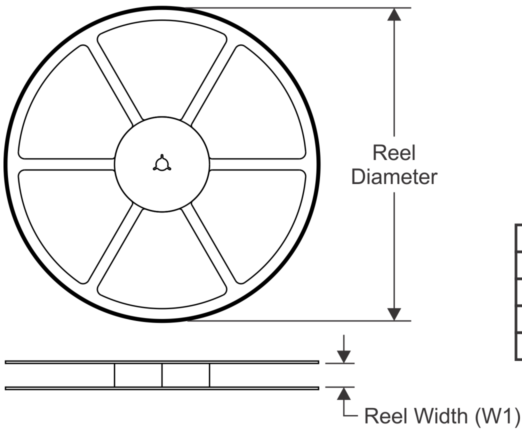
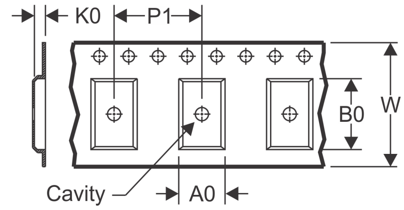
TAPE AND REEL INFORMATION

REEL DIMENSIONS

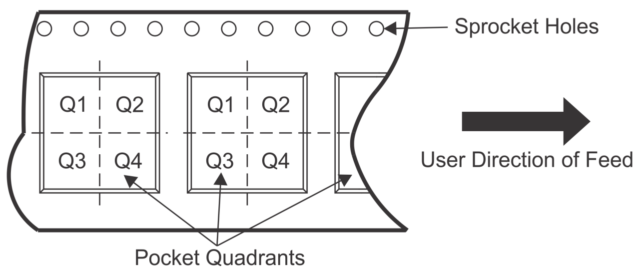


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

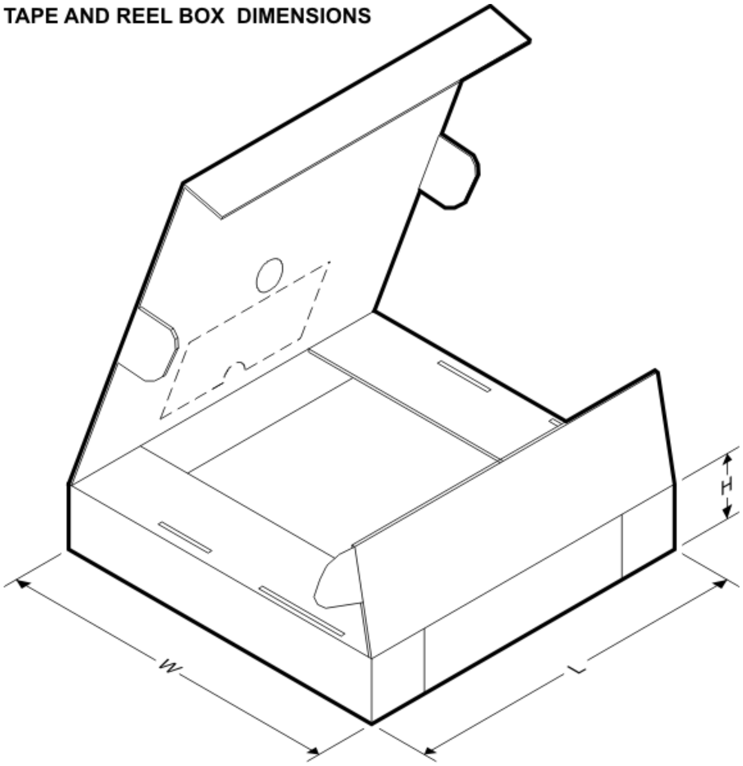
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS91M125TMAX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

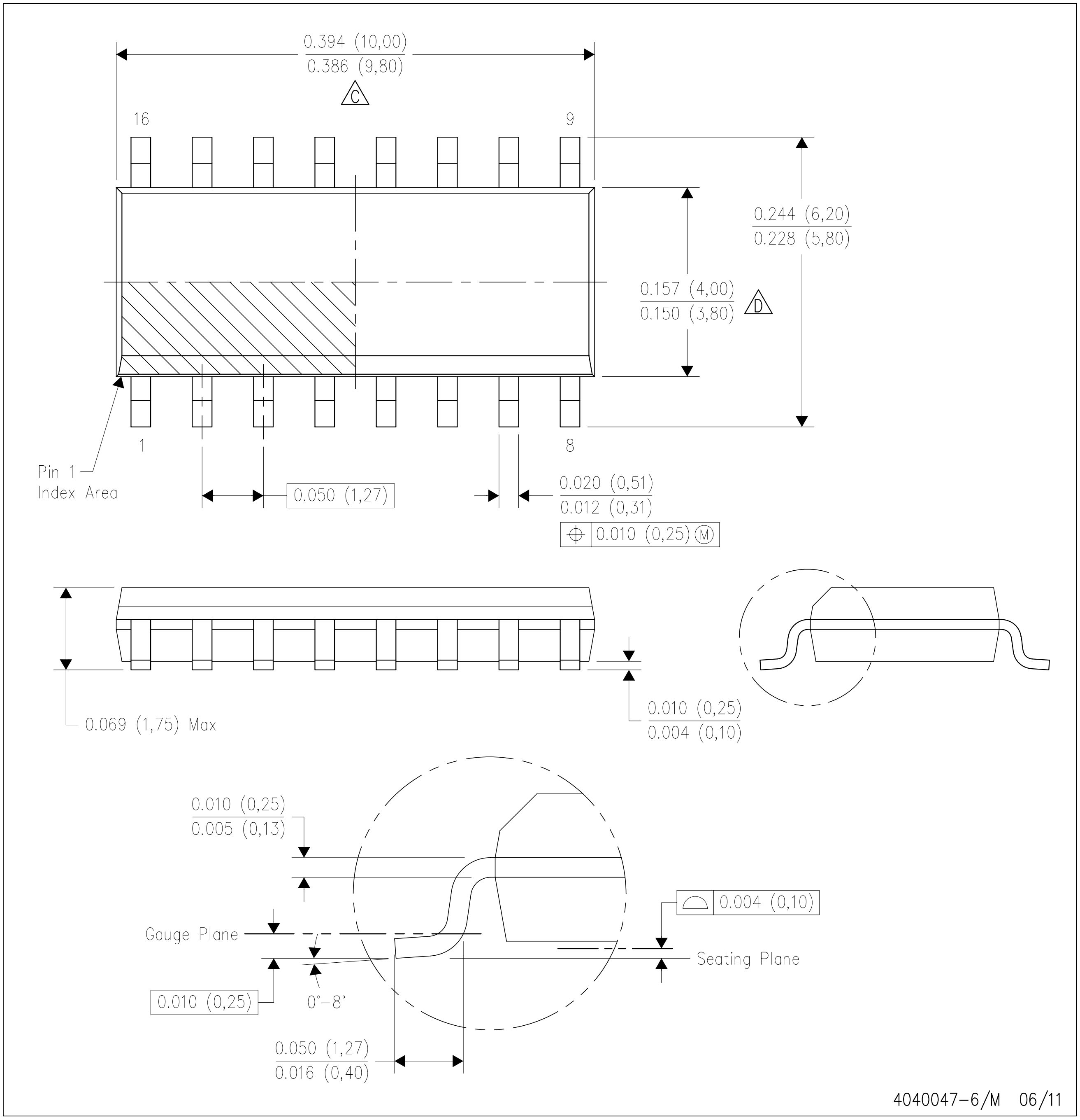
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS91M125TMAX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE

Products		**Applications**	
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