

DirectFET® N-Channel Power MOSFET

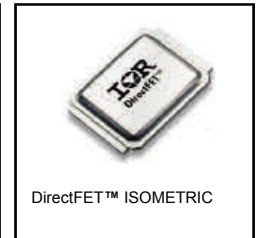
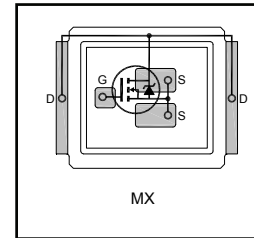
Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dv/dt and di/dt Capability
- RoHS Compliant Containing no Lead, no Bromide and no Halogen

V_{DSS}	40V
R_{DS(on)} typ.	1.1mΩ
	max
I_D	198A



Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF7946TRPbF	DirectFET MX	Tape and Reel	4800	IRF7946TRPbF

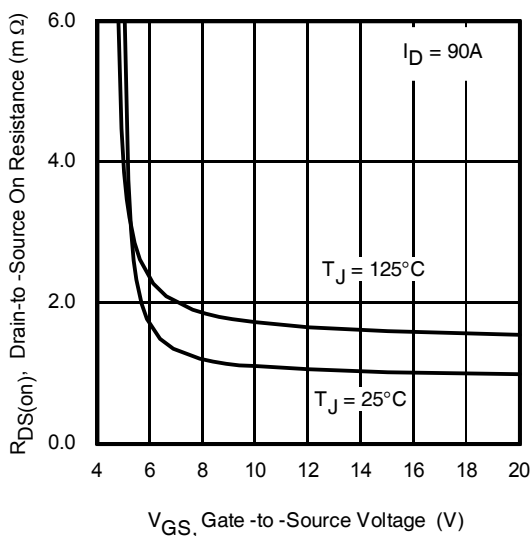


Fig 1. Typical On-Resistance vs. Gate Voltage

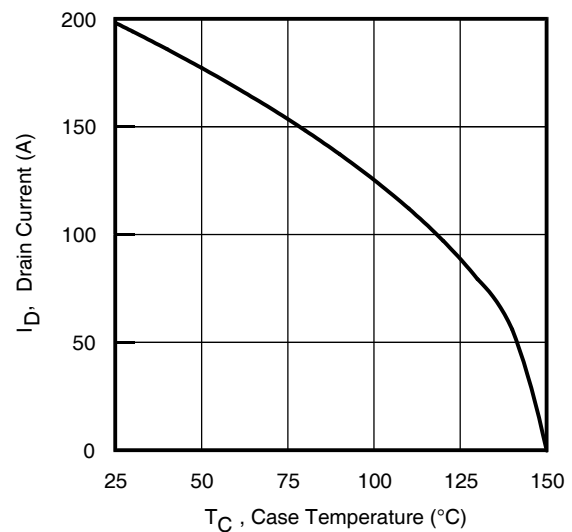


Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	198	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	125	
I_{DM}	Pulsed Drain Current ①	793	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	96	W
	Linear Derating Factor	0.77	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Avalanche Characteristics

E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	85	mJ
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	200	
I_{AR}	Avalanche Current ①	See Fig.15,16, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ①		mJ

Thermal Resistance

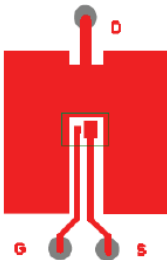
Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ①	—	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ③	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ②	20	—	
$R_{\theta JC}$	Junction-to-Case ④⑤	—	1.3	
$R_{\theta JA-PCB}$	Junction-to-PCB Mounted	1.0	—	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

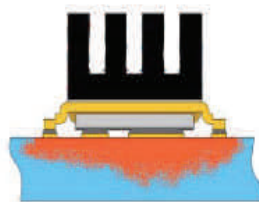
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.03	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1.0\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.1	1.4	mΩ	$V_{GS} = 10\text{V}, I_D = 90\text{A}$ ④
		—	1.7	—		$V_{GS} = 6.0\text{V}, I_D = 72\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}, I_D = 150\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
R_G	Internal Gate Resistance	—	0.67	—	Ω	

Notes:

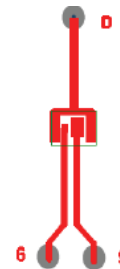
- ① Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ② Used double sided cooling , mounting pad with large heatsink.
- ③ TC measured with thermocouple mounted to top (Drain) of part.



① Surface mounted on 1 in. square Cu board (still air).



② Mounted to a PCB with small clip heatsink (still air)

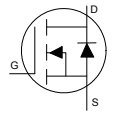


③ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	91	—	—	S	V _{DS} = 10V, I _D = 90A
Q _g	Total Gate Charge	—	141	212	nC	I _D = 90A V _{DS} = 20V V _{GS} = 10V ④
Q _{gs}	Gate-to-Source Charge	—	36	—		
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	44	—		
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	97	—		
t _{d(on)}	Turn-On Delay Time	—	20	—	ns	V _{DD} = 20V I _D = 30A R _G = 2.7Ω V _{GS} = 10V ④
t _r	Rise Time	—	49	—		
t _{d(off)}	Turn-Off Delay Time	—	54	—		
t _f	Fall Time	—	41	—		
C _{iss}	Input Capacitance	—	6852	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz V _{GS} = 0V, V _{DS} = 0V to 32V ⑥ V _{GS} = 0V, V _{DS} = 0V to 32V ⑤
C _{oss}	Output Capacitance	—	1046	—		
C _{rss}	Reverse Transfer Capacitance	—	735	—		
C _{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	1307	—		
C _{oss} eff. (TR)	Effective Output Capacitance (Time Related)	—	1465	—		

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	96	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	793		
V _{SD}	Diode Forward Voltage	—	0.75	1.2	V	T _J = 25°C, I _S = 90A, V _{GS} = 0V ④
dv/dt	Peak Diode Recovery ③	—	1.6	—	V/ns	T _J = 150°C, I _S = 90A, V _{DS} = 40V
t _{rr}	Reverse Recovery Time	—	49	—	ns	T _J = 25°C V _R = 34V, T _J = 125°C I _F = 90A
Q _{rr}	Reverse Recovery Charge	—	74	—		
I _{RRM}	Reverse Recovery Current	—	73	—	nC	T _J = 25°C T _J = 125°C
		—	2.6	—		

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.021mH, R_G = 50Ω, I_{AS} = 90A, V_{GS} = 10V.
- ③ I_{SD} ≤ 90A, di/dt ≤ 1135A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note # AN-994. <http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑧ R_θ is measured at T_J approximately 90°C.
- ⑨ Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 20A, V_{GS} = 10V.

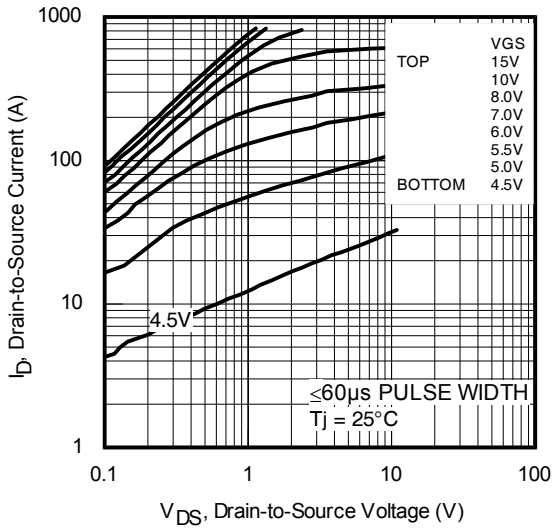


Fig 3. Typical Output Characteristics

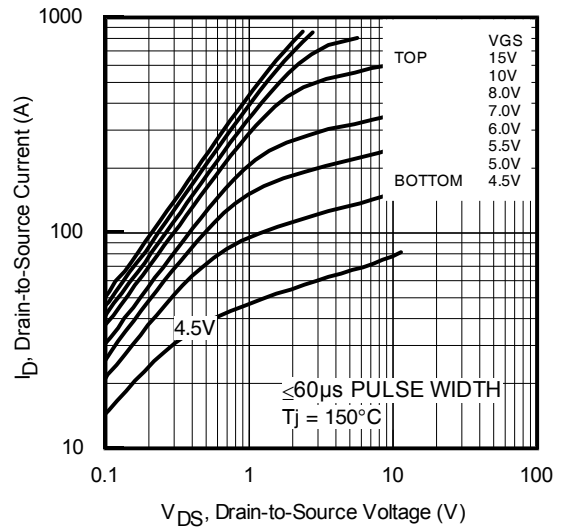


Fig 4. Typical Output Characteristics

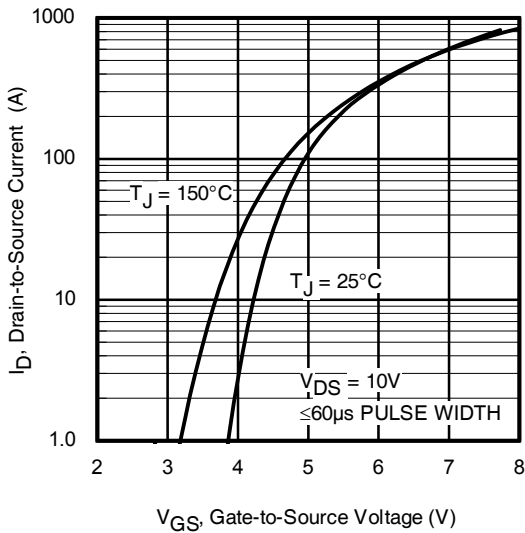


Fig 5. Typical Transfer Characteristics

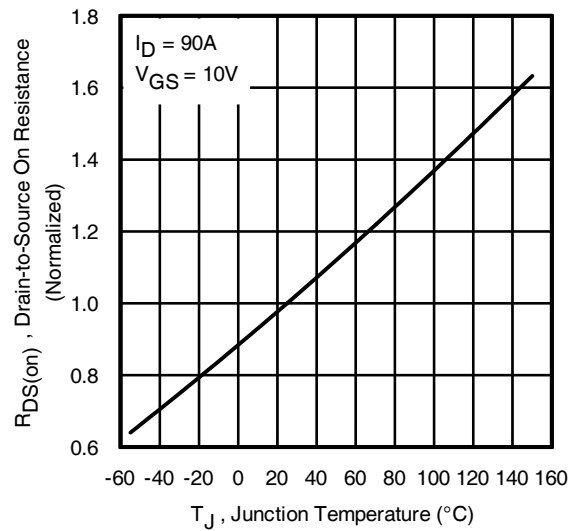


Fig 6. Normalized On-Resistance vs. Temperature

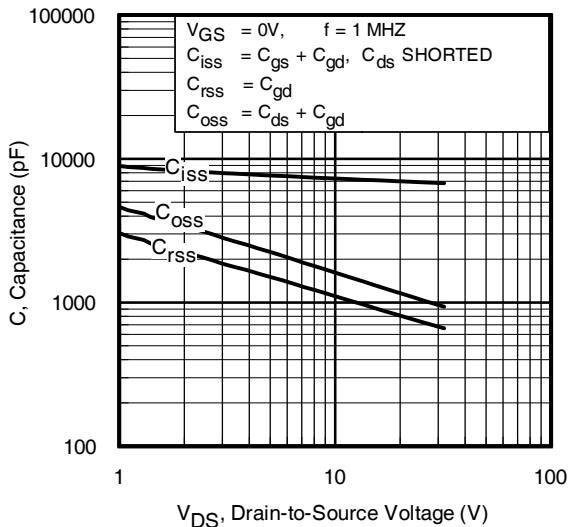


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

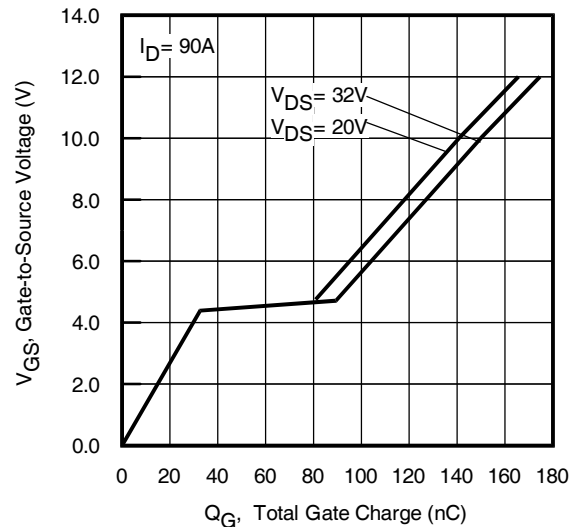


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

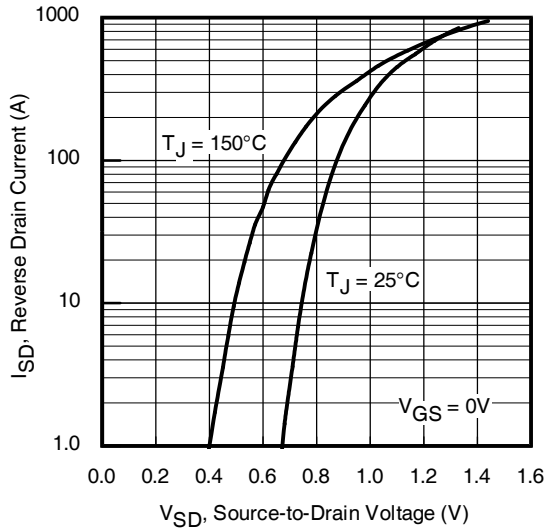


Fig 9. Typical Source-Drain Diode Forward Voltage

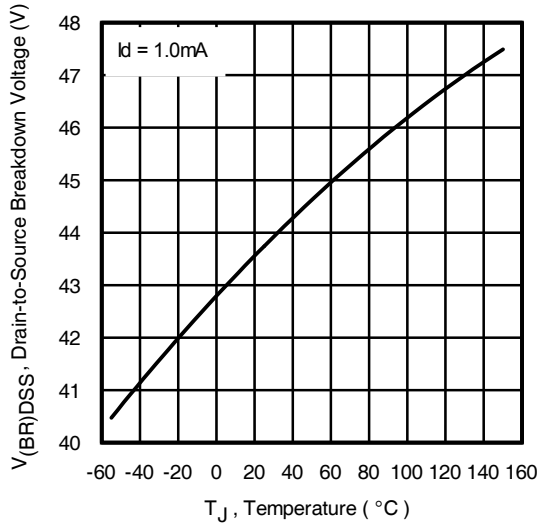


Fig 11. Drain-to-Source Breakdown Voltage

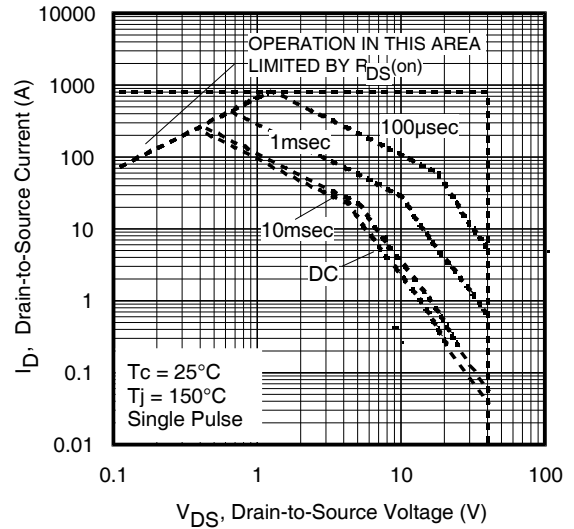


Fig 10. Maximum Safe Operating Area

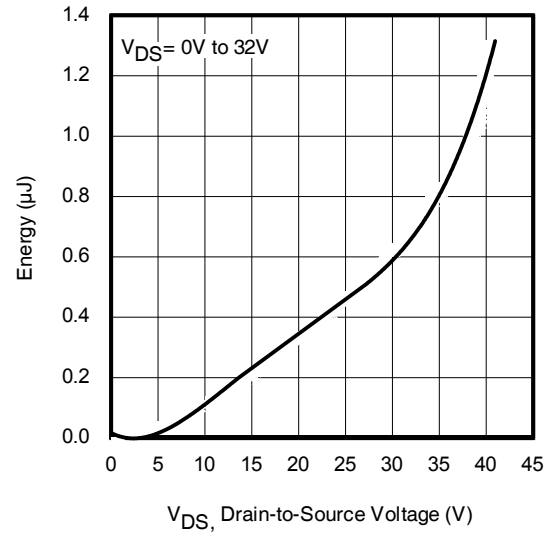


Fig 12. Typical C_{oss} Stored Energy

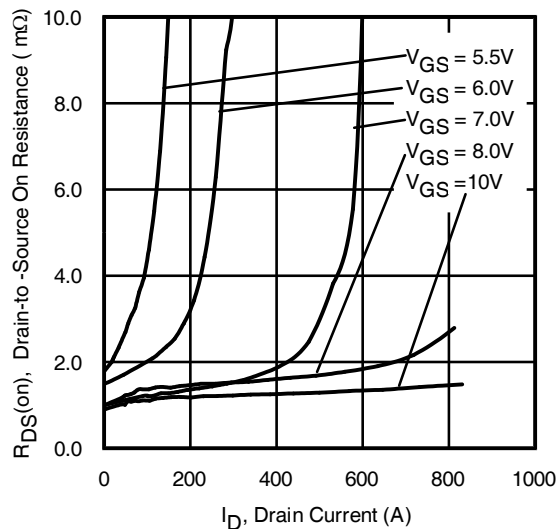


Fig 13. Typical On-Resistance vs. Drain Current

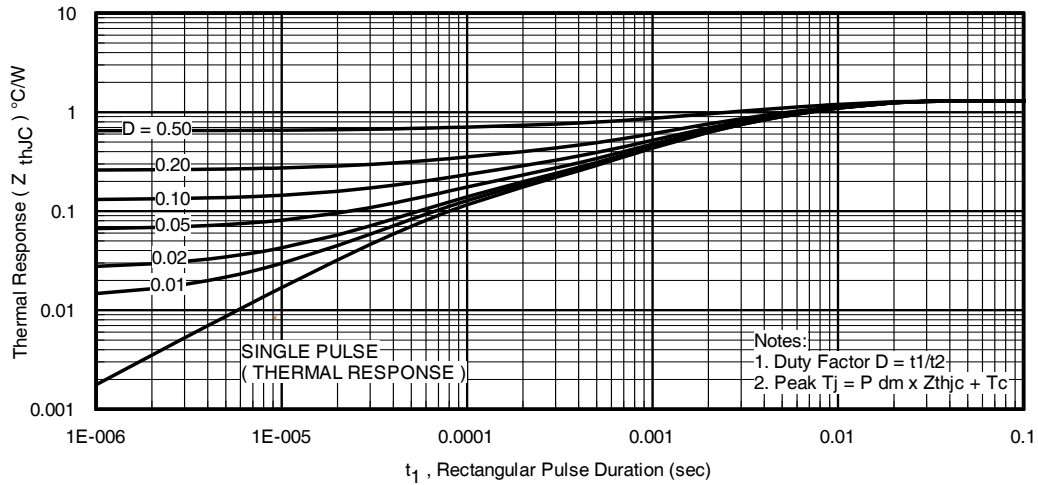


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

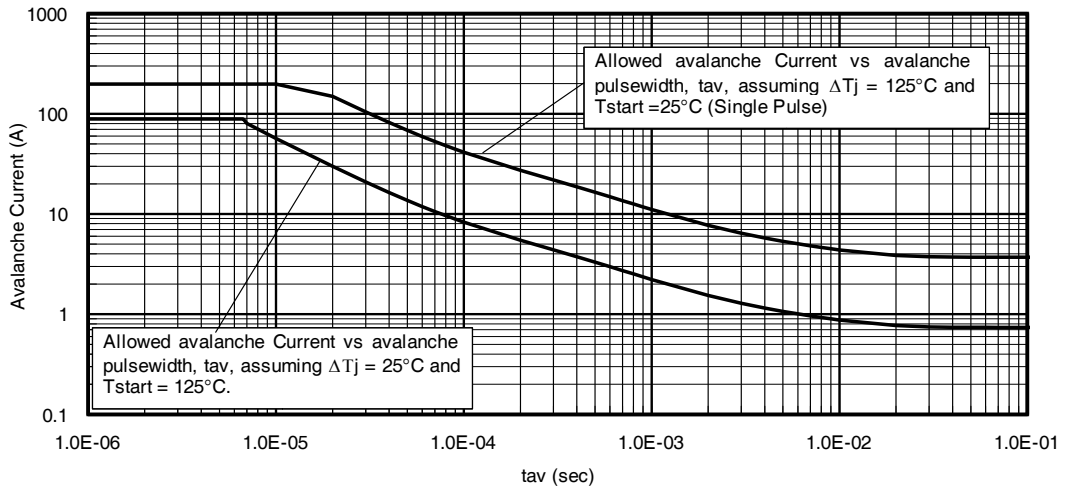


Fig 15. Avalanche Current vs. Pulse Width

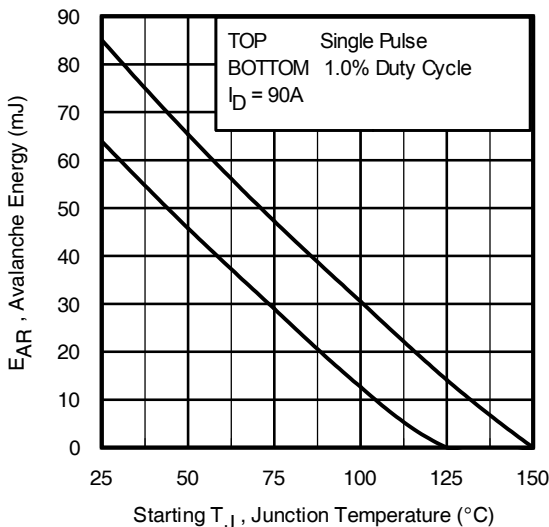


Fig 16. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as $25^{\circ}C$ in Figure 14, 15).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = $t_{av} \cdot f$

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

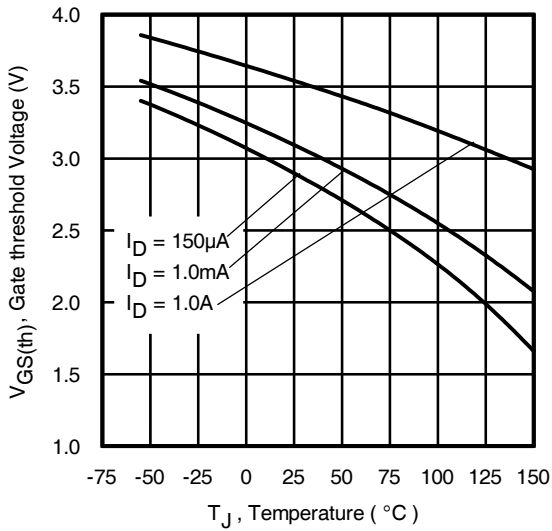


Fig 17. Threshold Voltage vs. Temperature

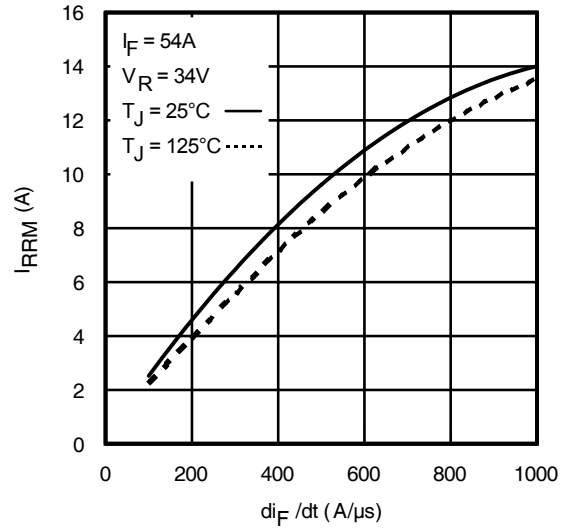


Fig 18. Typical Recovery Current vs. dif/dt

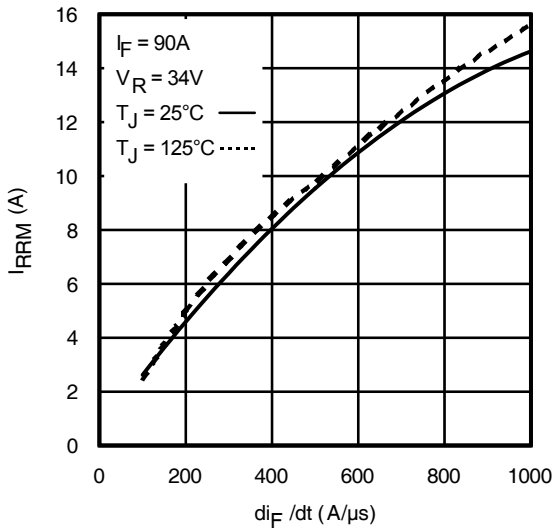


Fig 19. Typical Recovery Current vs. dif/dt

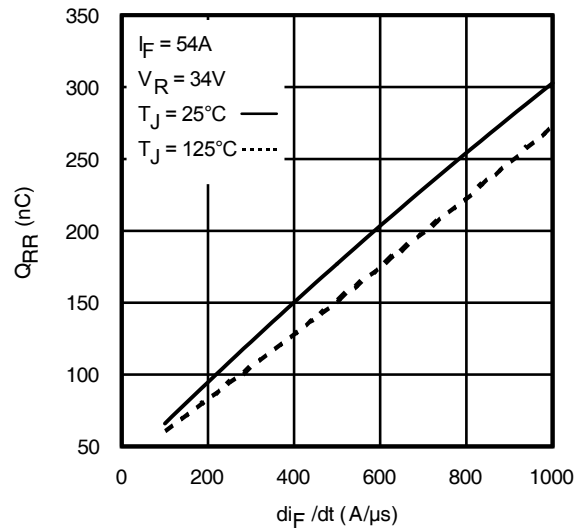


Fig 20. Typical Stored Charge vs. dif/dt

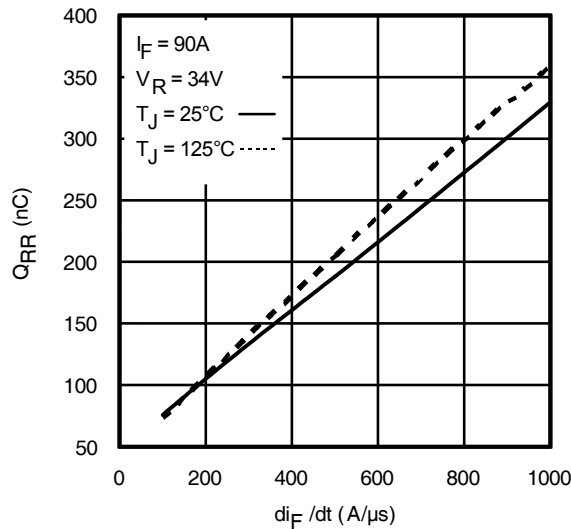


Fig 21. Typical Stored Charge vs. dif/dt

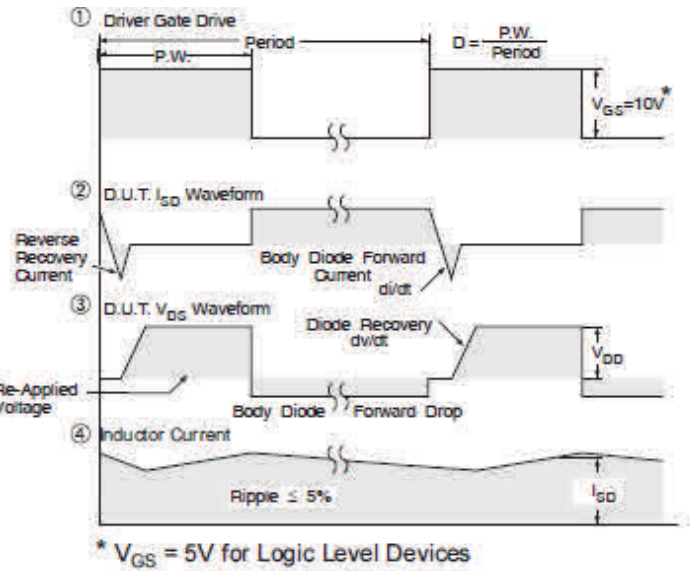
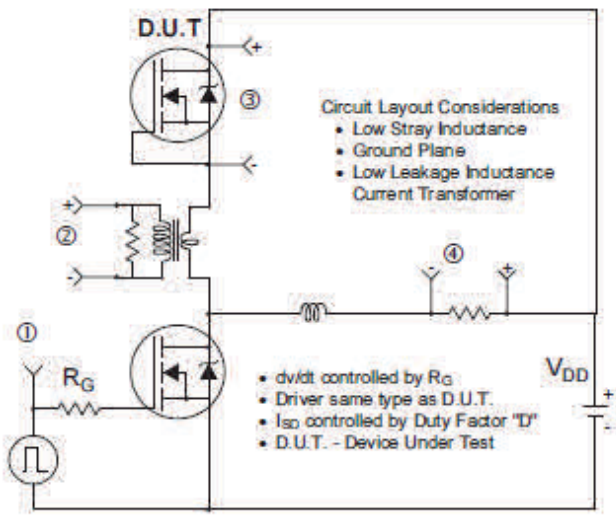


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

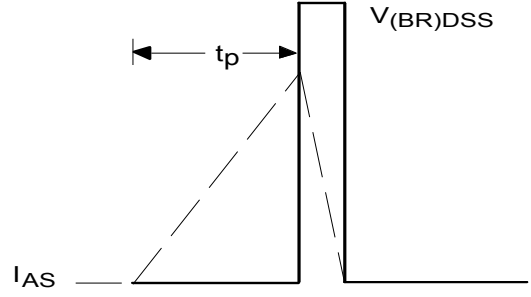
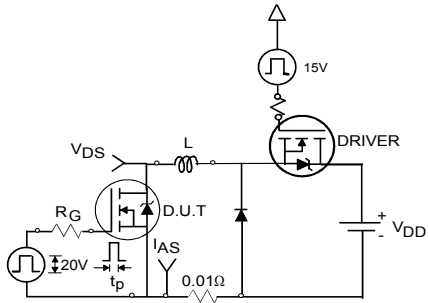


Fig 23a. Unclamped Inductive Test Circuit

Fig 23b. Unclamped Inductive Waveforms

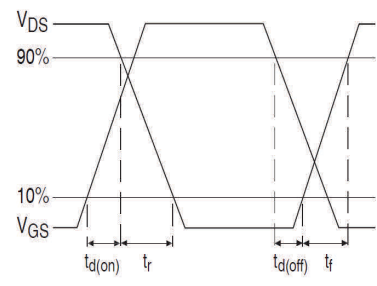
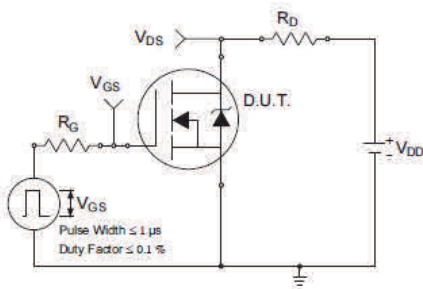


Fig 24a. Switching Time Test Circuit

Fig 24b. Switching Time Waveforms

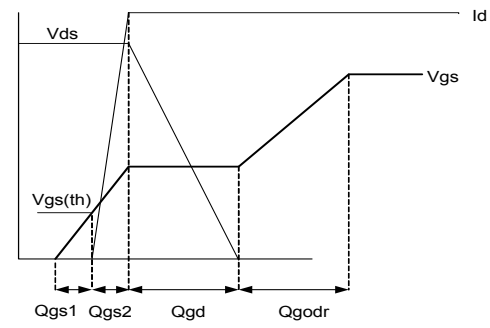
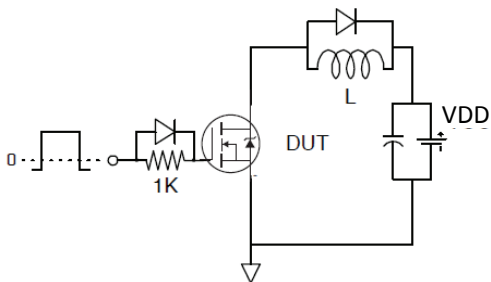
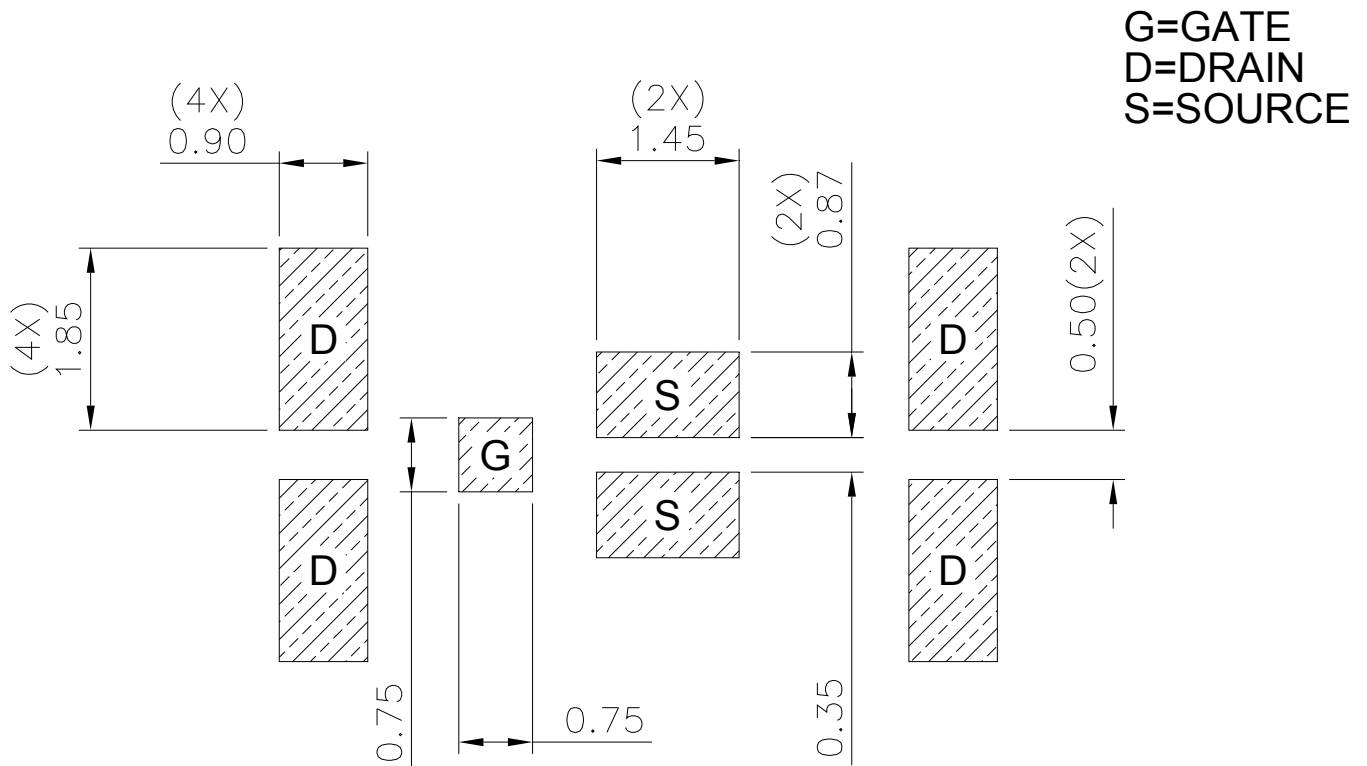
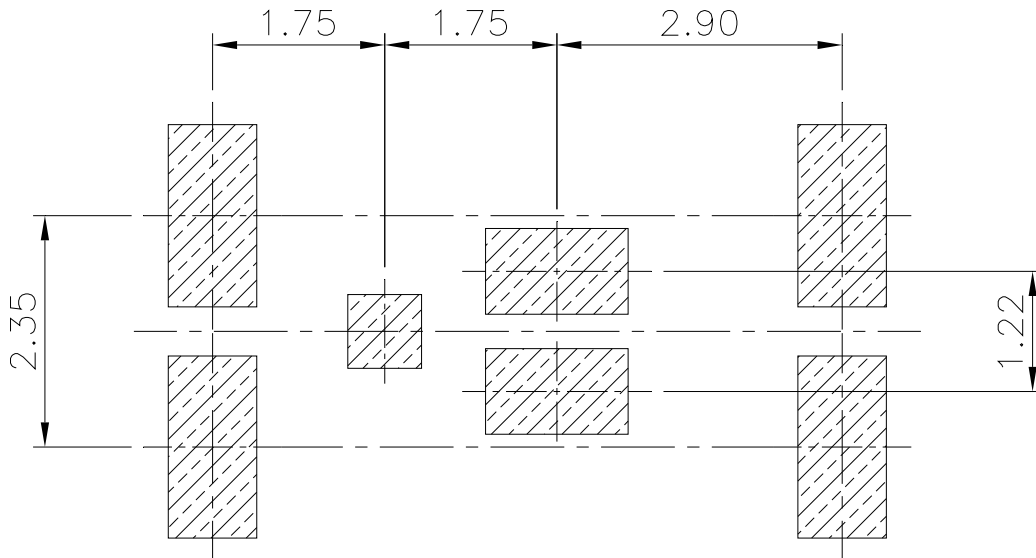


Fig 25a. Gate Charge Test Circuit

Fig 25b. Gate Charge Waveform

**DirectFET® Board Footprint, MX Outline
 (Medium Size Can, X-Designation).**

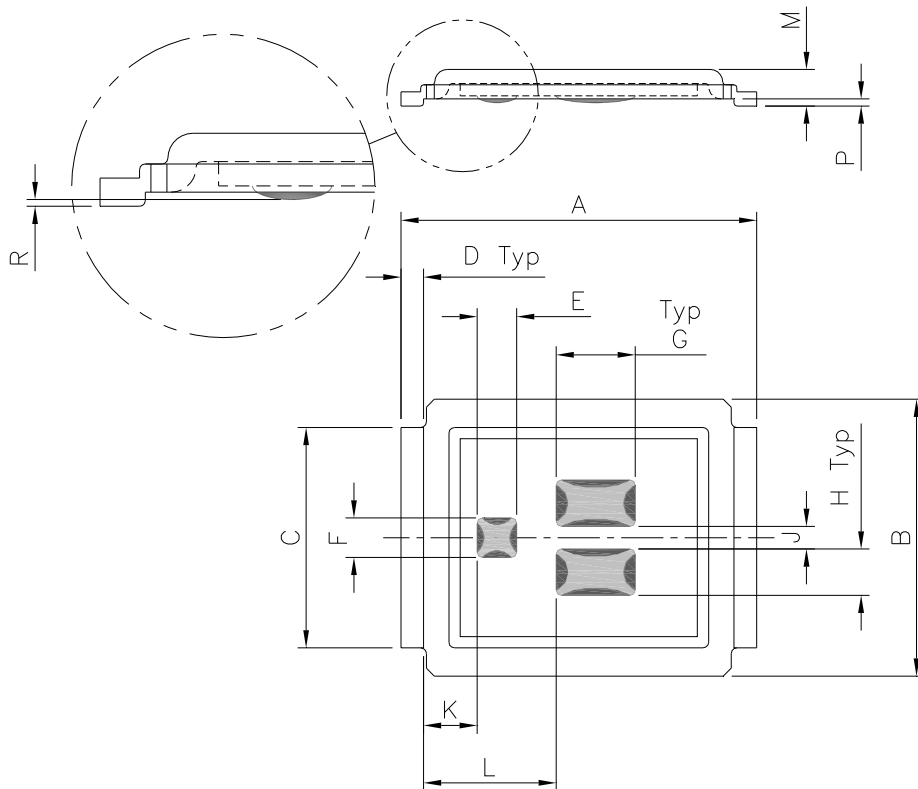
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

DirectFET® Outline Dimension, MX Outline (Medium Size Can, X-Designation).

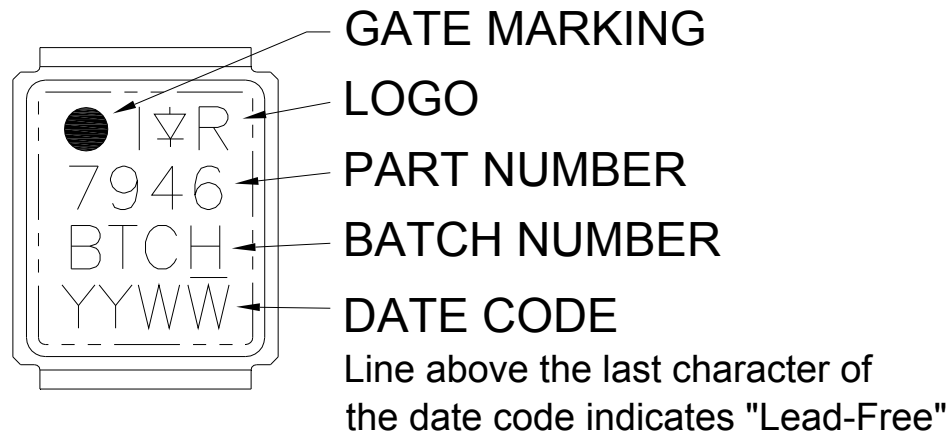
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.



CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.68	0.72	0.027	0.028
F	0.68	0.72	0.027	0.028
G	1.38	1.42	0.054	0.056
H	0.80	0.84	0.031	0.033
J	0.38	0.42	0.015	0.017
K	0.88	1.02	0.035	0.040
L	2.28	2.42	0.090	0.095
M	0.59	0.70	0.023	0.028
R	0.03	0.08	0.001	0.003
P	0.08	0.17	0.003	0.007

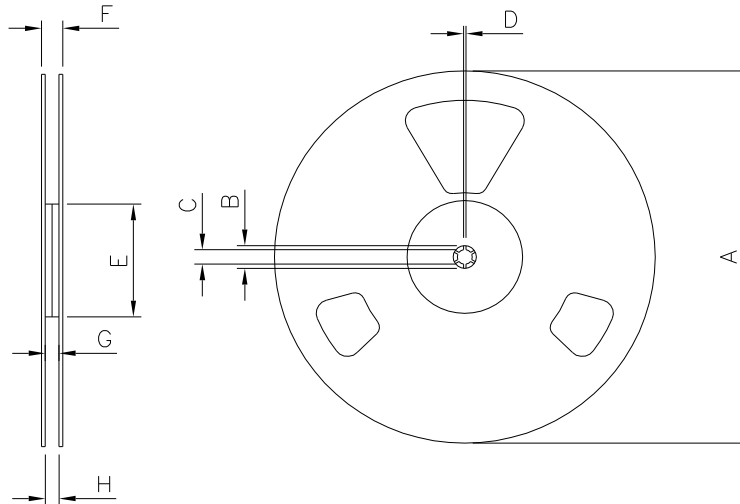
Dimensions are shown in millimeters (inches)

DirectFET® Part Marking



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

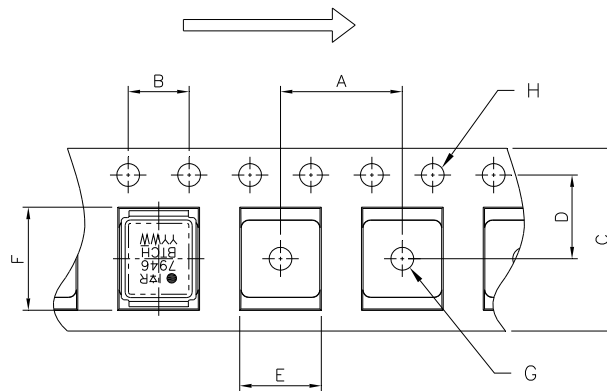
DirectFET® Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm Std reel.
 quantity is 4800 parts. (ordered as IRF7946PBF).

REEL DIMENSIONS				
STANDARD OPTION(QTY 4800)				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C
B	20.2	N.C	0.795	N.C
C	12.8	13.2	0.504	0.520
D	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C
F	N.C	18.4	N.C	0.724
G	12.4	14.4	0.488	0.567
H	11.9	15.4	0.469	0.606

LOADED TAPE FEED DIRECTION



NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Consumer ^{††} (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	DFET 1.5	MSL1 (per JEDEC J-STD-020D ^{††})
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site
<http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
05/07/2014	<ul style="list-style-type: none"> Updated data sheet based on corporate template. Updated Qual level from "MSL3" to "MSL1" on page12. Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #264).
05/30/2014	<ul style="list-style-type: none"> Remove IRF7946TR1PBF quantity= 1000 from ordering table on page1. Remove continuous drain current package limit=90A from Absolute Maximum table-on page2.
11/25/2014	<ul style="list-style-type: none"> Updated $E_{AS(L=1mH)} = 200mJ$ on page 2 Updated note 10 "Limited by T_{Jmax}, starting $T_J = 25^{\circ}C$, $L = 1mH$, $R_G = 50\Omega$, $I_{AS} = 20A$, $V_{GS} = 10V$". on page 3 Updated $R\theta JA$ from "60°C/W" to "45°C/W" on page 2
09/09/2015	<ul style="list-style-type: none"> Removed package limit "90A" and updated Fig.2 & Fig.10 on page1 and page 5 . Removed note1 and rename all notes on page 3. Corrected typo dv/dt test condition from "$T_J = 175^{\circ}C$" to "$T_J = 150^{\circ}C$" on page 3.