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March 2015

FDD6635

35V N-Channel PowerTrench® MOSFET

General Description

This N-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench technology to deliver low Rdson and optimized Bvdss capability to offer superior performance benefit in the applications.

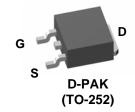
Applications

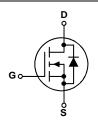
- Inverter
- Power Supplies

Features

- 59 A, 35 V $R_{DS(ON)} = 10 \ m\Omega \ @ \ V_{GS} = 10 \ V$ $R_{DS(ON)} = 13 \ m\Omega \ @ \ V_{GS} = 4.5 \ V$
- · Fast Switching
- · RoHS compliant







Absolute Maximum Ratings TA=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units		
V _{DSS}	Drain-Source Voltage	ce Voltage		35	V	
V _{DS(Avalanche)}	Drain-Source Avalanche	Voltage (maximu	ım) (Note 4)	40	V	
V _{GSS}	Gate-Source Voltage			±20	V	
I _D	Continuous Drain Current	@T _C =25°C	(Note 3)	59	А	
		@T _A =25°C	(Note 1a)	15		
		Pulsed	(Note 1a)	100		
E _{AS}	Single Pulse Avalanche Energy (N		(Note 5)	113	mJ	
P _D	Power Dissipation	@T _c =25°C	(Note 3)	55	W	
		@T _A =25°C	(Note 1a)	3.8		
		@T _A =25°C	(Note 1b)	1.6		
T _J , T _{STG}	Operating and Storage Ju	inction Tempera	ture Range	-55 to +150	°C	

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	2.7	°C/W		
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	°C/W		
R _{e.IA}	Thermal Resistance, Junction-to-Ambient	(Note 1b)	96	°C/W		

Package Marking and Ordering Information

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Device Marking		Device	Package	Reel Size	Tape width	Quantity		
	FDD6635	FDD6635	D-PAK (TO-252)	13"	16mm	2500 units		

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics(Note 2)			<u> </u>		l .
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = 250 \mu\text{A}$	35			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$, Referenced to 25°C		32		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 28 \text{ V}, V_{GS} = 0 \text{ V}$			1	μА
I _{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA
On Chara	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C		- 5		mV/°(
$R_{\text{DS(on)}}$	Static Drain–Source On–Resistance	$ \begin{vmatrix} V_{GS} = 10 \text{ V}, & I_D = 15 \text{ A} \\ V_{GS} = 4.5 \text{ V}, & I_D = 13 \text{ A} \\ V_{GS} = 10 \text{ V}, & I_D = 15 \text{ A}, T_J = 125 ^{\circ}\text{C} \\ \end{vmatrix} $		8.2 10.2 12.4	10 13 16	mΩ
g _{FS}	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 15 \text{ A}$		53		S
Dynamic	Characteristics					
C _{iss}	Input Capacitance			1400		pF
Coss	Output Capacitance	$V_{DS} = 20 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		317		pF
C _{rss}	Reverse Transfer Capacitance	f = 1.0 MHz		137		pF
R_{G}	Gate Resistance	V _{GS} = 15 mV, f = 1.0 MHz		1.4		Ω
Switchin	q Characteristics (Note 2)					
t _{d(on)}	Turn-On Delay Time			11	20	ns
t _r	Turn-On Rise Time	$V_{DD} = 20 \text{ V}, \qquad I_D = 1 \text{ A},$		6	12	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		28	45	ns
t _f	Turn-Off Fall Time]		14	25	ns
Q _{g (TOT)}	Total Gate Charge, V _{GS} = 10V			26	36	nC
Qg	Total Gate Charge, V _{GS} = 5V	$V_{DS} = 20 \text{ V}, I_{D} = 15 \text{ A}$		13	18	nC
Q_{gs}	Gate-Source Charge			3.9		nC
Q_{gd}	Gate-Drain Charge]		5.3		nC

Electric	ai Characteristics	T _A = 25°C unless otherwise noted						
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units		
Drain-Sc	ource Diode Characteristics							
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 15 \text{ A}$ (Note 2)		0.8	1.2	V		
trr	Diode Reverse Recovery Time	IF = 15 A, diF/dt = 100 A/μs		26		ns		
Qrr	Diode Reverse Recovery Charge			16		nC		

Notes

 R_{8,JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{8,JC} is guaranteed by design while R_{8,CA} is determined by the user's board design.



 a) R_{0JA} = 40°C/W when mounted on a 1in² pad of 2 oz copper



b) R_{θJA} = 96°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300μ s, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at $T_C = 25^{\circ}C$ and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS} = 10V$. Package current limitation is 21A

4. BV(avalanche) Single-Pulse rating is guaranteed if device is operated within the UIS SOA boundary of the device.

5. Starting $T_J=25\,^{\circ}C,\,L=1mH,\,I_{AS}=15A,\,V_{DD}=35V,\,V_{GS}=10V$

Typical Characteristics

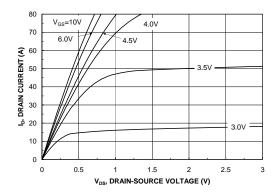


Figure 1. On-Region Characteristics

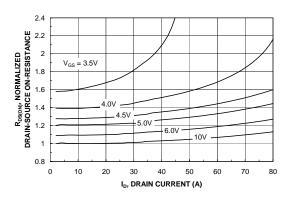


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

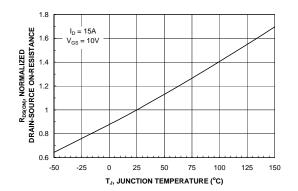


Figure 3. On-Resistance Variation with Temperature

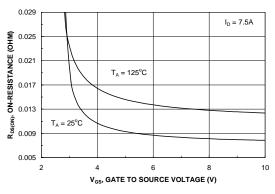


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

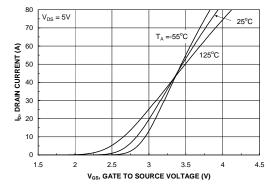


Figure 5. Transfer Characteristics

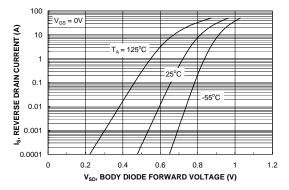


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

f = 1MHz $V_{GS} = 0 V$

Typical Characteristics

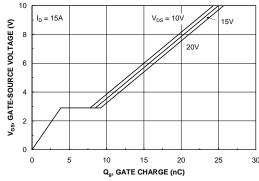
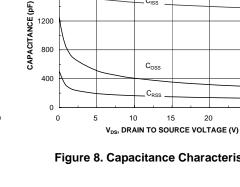


Figure 7. Gate Charge Characteristics



2000

1600

Figure 8. Capacitance Characteristics

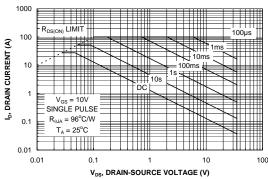


Figure 9. Maximum Safe Operating Area

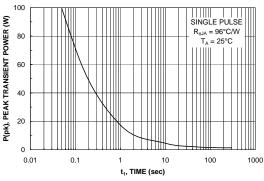


Figure 10. Single Pulse Maximum **Power Dissipation**

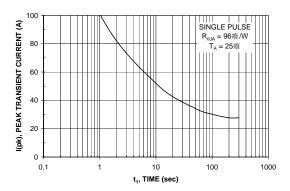


Figure 11. Single Pulse Maximum Peak Current

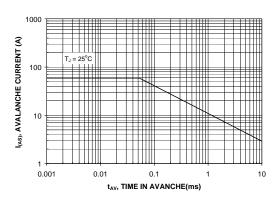


Figure 12. Unclamped Inductive Switching Capability

Typical Characteristics

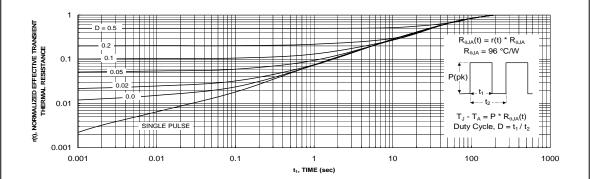
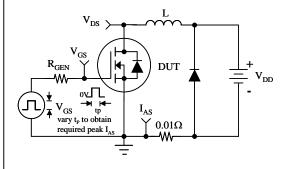


Figure 13. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

Test Circuits and Waveforms



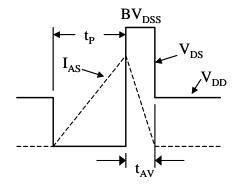
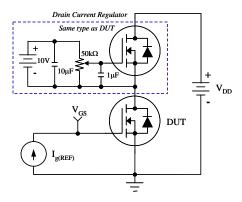


Figure 14. Unclamped Inductive Load Test Circuit

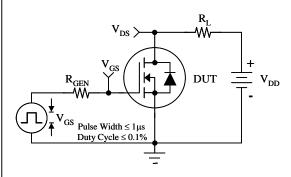
Figure 15. Unclamped Inductive Waveforms



 Q_{G} V_{GS} Q_{GS} Q_{GD} Charge, (nC)

Figure 16. Gate Charge Test Circuit

Figure 17. Gate Charge Waveform



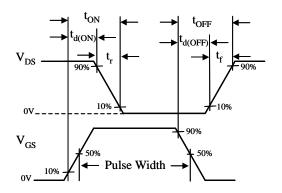


Figure 18. Switching Time Test Circuit

Figure 19. Switching Time Waveforms



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