TEXAS INSTRUMENTS

DS8921, DS8921A, DS8921AT

SNLS374D – MAY 1998 – REVISED JANUARY 2015

DS8921x Differential Line Driver and Receiver Pair

1 Features

- 12-ns Typical Propagation Delay
- Output Skew: 0.5 ns Typical
- Meets the Requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High Differential or Common-Mode Input Voltage Ranges of ±7 V
- ±0.2 V Receiver Sensitivity Over the Input Voltage Range
- Receiver Input Hysteresis: 70 mV Typical
- DS8921AT Industrial Temperature Operation: (−40°C to +85°C)

2 Applications

- Differential Line Driver and Receiver for:
  - ST506 Disk Drive Standard
  - ST412 Disk Drive Standard
  - ESDI Disk Drive Standard
  - RS-422 Interface

3 Description

The DS8921, DS8921A, and DS8921AT devices are differential line driver and receiver pairs designed specifically for applications meeting the ST506, ST412, and ESDI disk drive standards. In addition, these devices meet the requirements of the EIA standard RS-422.

The DS8921x receivers offer an input sensitivity of 200 mV over a ±7 V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms.

The DS8921x drivers are designed to provide unipolar differential drive to twisted-pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typical) with propagation delays of 12 ns.

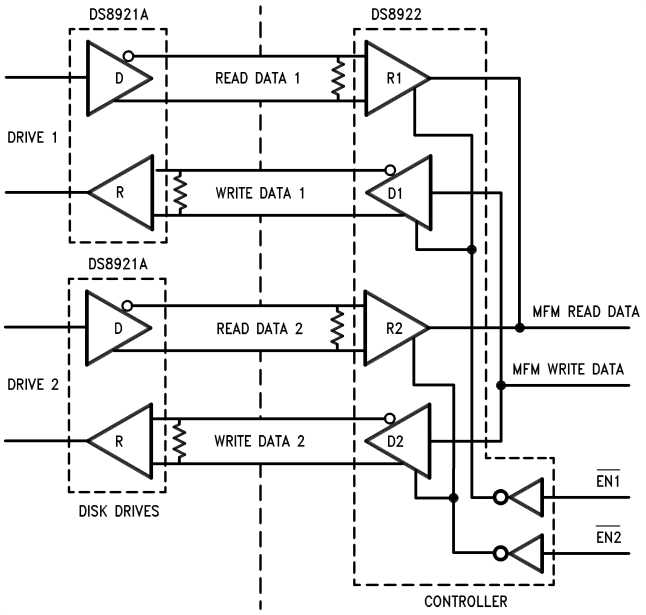
The DS8921x devices are designed to be compatible with TTL and CMOS.

Device Information(1)

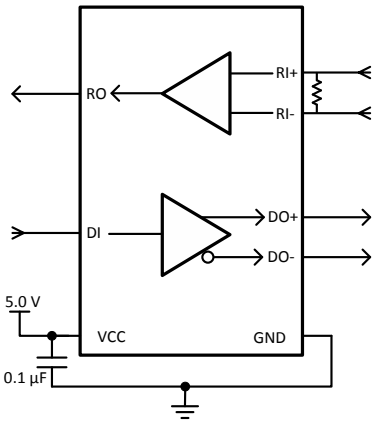
PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS8921 DS8921A DS8921AT	SOIC (8)	4.90 mm x 3.91 mm
	PDIP (8)	9.81 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Block Diagram



Simplified Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D — **Page**

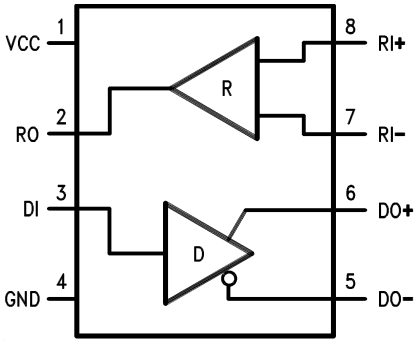
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (November 2004) to Revision C — **Page**

- Changed layout of National Data Sheet to TI format. ... 1

5 Pin Configuration and Functions

D, P Package
8 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DIFFERENTIAL SIGNALING I/O			
DI	3	I	TTL/CMOS Compatible Driver Input
DO+, DO–	6, 5	O	Inverting and non-inverting differential driver outputs
RI+, RI–	8, 7	I	Inverting and non-inverting differential receiver inputs
RO	2	O	Receiver Output Pin
POWER			
GND	4	Power	Ground Pin
VCC	1	Power	Supply pin, provide 5-V supply

6 Specifications

6.1 Absolute Maximum Ratings (1) (2)

	MIN	MAX	UNIT
Supply Voltage		7	V
Driver Input Voltage	−0.5	7	V
Output Voltage		5.5	V
Receiver Output Sink Current		50	mA
Receiver Input Voltage	–10	10	V
Differential Input Voltage	–12	12	V
Maximum Package Power Dissipation at 25°C: D Package		730	mW
Maximum Package Power Dissipation at 25°C: P Package		1160	mW
Derate D Package, above 25°C		9.3	mW/°C
Derate P Package, above 25°C		5.8	mW/°C
Lead Temperature		260	°C
(Soldering, 4 sec.)		260	°C
Maximum Junction Temperature		150	°C
Storage Temperature, T_{stg}	−65	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instrument Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage	4.5	5.5	V
Temperature (T_A): DS8921/DS8921A	0	70	°C
Temperature (T_A): DS8921AT	−40	85	°C

6.4 Electrical Characteristics

Over operating free-air temperature range unless otherwise noted. (1)(2)(3)

TEST CONDITIONS		MIN	TYP	MAX	UNIT
RECEIVER					
V_{TH}	−7 V ≤ V_{CM} ≤ +7 V	−200	±35	+200	mV
V_{HYST}	−7 V ≤ V_{CM} ≤ +7 V	15	70		mV
R_{IN}	V_{IN} = −7 V, +7 V, (Other Input = GND)	4.0	6.0		kΩ
I_{IN}	V_{IN} = 10 V			3.25	mA
	V_{IN} = −10 V			−3.25	mA
V_{OH}	I_{OH} = −400 µA	2.5			V
V_{OL}	I_{OL} = 8 mA			0.5	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0 V	−15		−100	mA
DRIVER					
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	V_{CC} = MAX, V_{IN} = 0.4 V		−40	−200	µA
I_{IH}	V_{CC} = MAX, V_{IN} = 2.7 V			20	µA
I_I	V_{CC} = MAX, V_{IN} = 7.0 V			100	µA
V_{CL}	V_{CC} = MIN, I_{IN} = −18 mA			−1.5	V
V_{OH}	V_{CC} = MIN, I_{OH} = −20 mA	2.5			V
V_{OL}	V_{CC} = MIN, I_{OL} = +20 mA			0.5	V
I_{OFF}	V_{CC} = 0V, V_{OUT} = 5.5 V			100	µA
$\lvert V_T\rvert - \lvert\overline{VT}\rvert$				0.4	V
V_T		2.0			V
$\lvert V_{OS} - \overline{V}_{OS}\rvert$				0.4	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0 V	−30		−150	mA
DRIVER AND RECEIVER					
I_{CC}	V_{CC} = MAX, V_{OUT} = Logic 0			35	mA

(1) All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.
(2) All typical values are V_{CC} = 5 V, T_A = 25°C.
(3) Only one output at a time should be shorted.

6.5 Receiver Switching Characteristics

TEST CONDITIONS		MIN	TYP	MAX 8921	MAX 8921A	MAX 8921AT	UNIT
t_{pLH}	C_L = 30 pF (Figure 3 and Figure 4)		14	22.5	20	20	ns
t_{pHL}	C_L = 30 pF (Figure 3 and Figure 4)		14	22.5	20	20	ns
$\lvert t_{pLH} - t_{pHL} \rvert$	C_L = 30 pF (Figure 3 and Figure 4)		0.5	5	3.5	5	ns

6.6 Driver Switching Characteristics: Single-Ended Characteristics

TEST CONDITIONS		MIN	TYP	MAX 8921	MAX 8921A	MAX 8921AT	UNIT
t_{pLH}	C_L = 30 pF (Figure 5 and Figure 6)		10	15	15	15	ns
t_{pHL}	C_L = 30 pF (Figure 5 and Figure 6)		10	15	15	15	ns
t_{TLH}	C_L = 30 pF (Figure 9 and Figure 10)		5	8	8	9.5	ns
t_{THL}	C_L = 30 pF (Figure 9 and Figure 10)		5	8	8	9.5	ns
Skew	CL = 30 pF(1) (Figure 5 and Figure 6)		1	5	3.5	3.5	ns

(1) Difference between complementary outputs at the 50% point.

6.7 Driver Switching Characteristics: Differential Characteristics(1)

TEST CONDITIONS		MIN	TYP	MAX 8921	MAX 8921A	MAX 8921AT	UNIT
t_{pLH}	C_L = 30 pF (Figure 5, Figure 7, and Figure 8)		10	15	15	15	ns
t_{pHL}	C_L = 30 pF (Figure 5, Figure 7, and Figure 8)		10	15	15	15	ns
$\lvert t_{pLH} - t_{pHL} \rvert$	C_L = 30 pF (Figure 5, Figure 7, and Figure 8)		0.5	6	2.75	2.75	ns

(1) Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE). The calculated ATE results assume a linear transition between measurement points and are a result of the following equations: $T_{cr} = \frac{(T_{fb} \times T_{rb}) - (T_{ra} \times T_{fa})}{T_{rb} - T_{ra} - T_{fa} + T_{fb}}$ Where: T_{cr} = Crossing Point T_{ra}, T_{rb}, T_{fa} and T_{fb} are time measurements with respect to the input. See Figure 8.

6.8 Typical Characteristics

Test Setup: Figure 5. Data Rate, Test Pattern: 2 Mbps, 1010 Pattern. T: 25°C

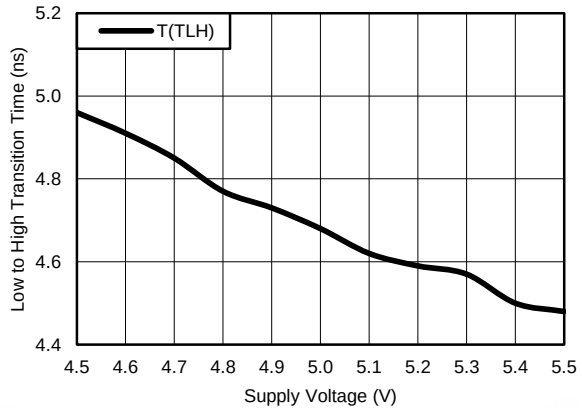


Figure 1. Typical Driver Output Low to High Transition Time vs Supply Voltage

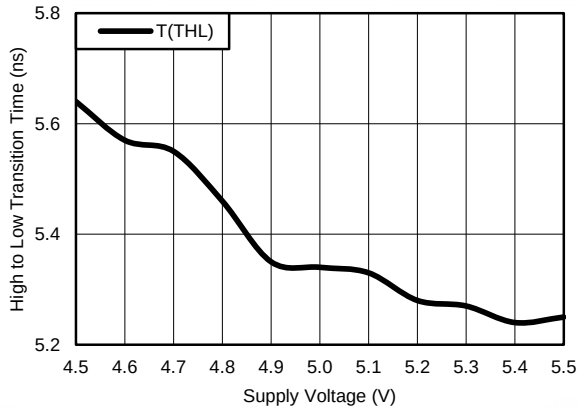


Figure 2. Typical Driver Output High to Low Transition Time vs Supply Voltage

7 Parameter Measurement Information

7.1 AC Test Circuits and Switching Diagrams

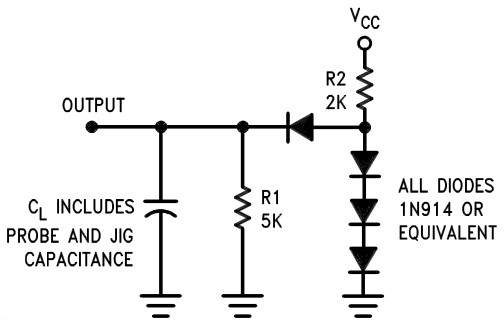


Figure 3. Test Circuit for Receiver Output

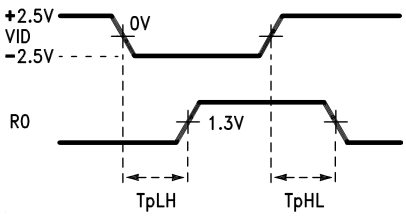
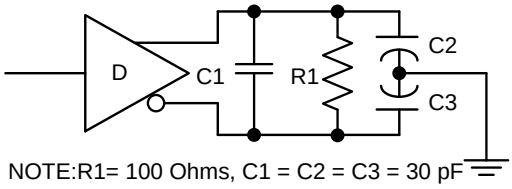


Figure 4. Receiver Propagation Delay



NOTE:R1= 100 Ohms, C1 = C2 = C3 = 30 pF

Figure 5. Driver Test Circuit

AC Test Circuits and Switching Diagrams (continued)

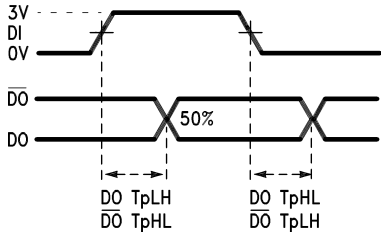


Figure 6. Driver Single-Ended Propagation Delay

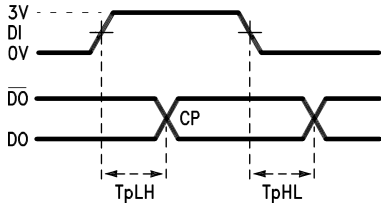


Figure 7. Driver Differential Propagation Delay

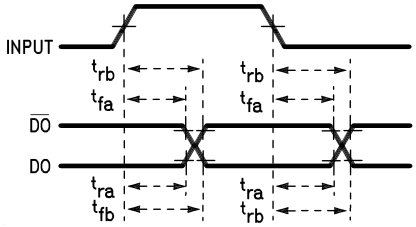


Figure 8. Driver Delay ATE Testing

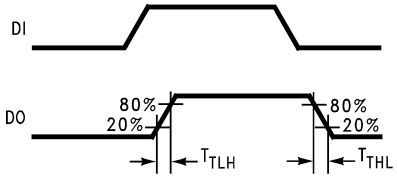


Figure 9. Driver Output Transition Time

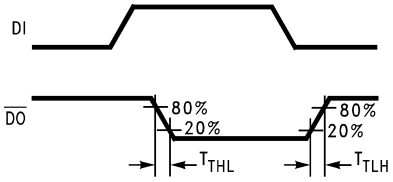


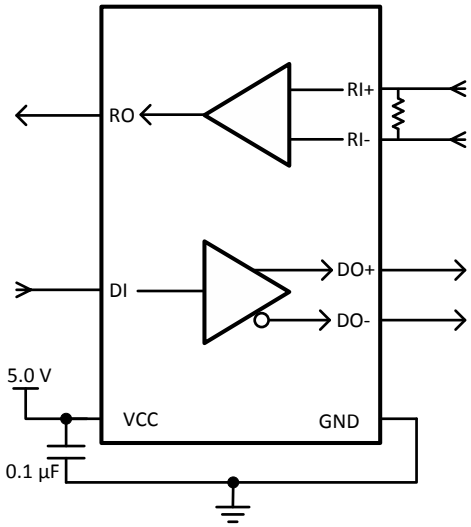
Figure 10. Driver Output Transition Time

8 Detailed Description

8.1 Overview

The DS8921x devices are each a differential line driver and receiver pair in a single package. The devices are designed specifically for ST506, ST412, and ESDI disk drive standards, as well as RS-422 interface applications. The DS8921 and DS8921A are rated at a commercial temperature range of 0°C to 70°C, whereas the DS8921AT is rated at an extended temperature range of -40°C to +85°C.

8.2 Functional Block Diagram



8.3 Feature Description

The DS8921x devices each contain a differential driver and receiver.

The driver converts a TTL or CMOS input to complementary outputs that provide differential drive to a twisted-pair or parallel wire transmission line. The receiver converts the differential signals at its input pins to a TTL output. The receiver offers an input sensitivity of ±200 mV and supports a common-mode input voltage of ±7 V.

8.4 Device Functional Modes

Table 1. Function Table

RECEIVER		DRIVER		
INPUT	OUTPUT	INPUT	OUTPUT	
RI+, RI-	RO	DI	DO+	DO-
V_{ID} (1) ≥ V_{TH} (MAX)	1	1	1	0
V_{ID} (1) ≤ V_{TH} (MIN)	0	0	0	1
Open	1			

(1) V_{ID} is the input differential voltage between RI+ and RI–.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS8921 is a differential line driver and receiver pair in a single package, designed for applications for the ST506, ST412, and ESDI Disk Drive Standards. The DS8921 is compatible to EIA RS-422 signaling standards, supporting 200-mV input sensitivity across a ±7-V common mode operating range. This transceiver is intended for driving differential signal across long transmission lines and translating received differential signals into their CMOS/TTL single-ended equivalence. The DS8921 transmits and reproduces received data in communications links where ground reference difference, or noisy environment are common.

9.2 Typical Application

Figure 11 shows a typical implementation of the DS8921x device in a ST506 and ST412 disk drive application. The differential outputs of the driver are connected to a twisted-pair transmission line, carrying data from the driver to the differential receiver at the other end of the cable. A differential termination resistor should be connected across the input pins of the receiver.

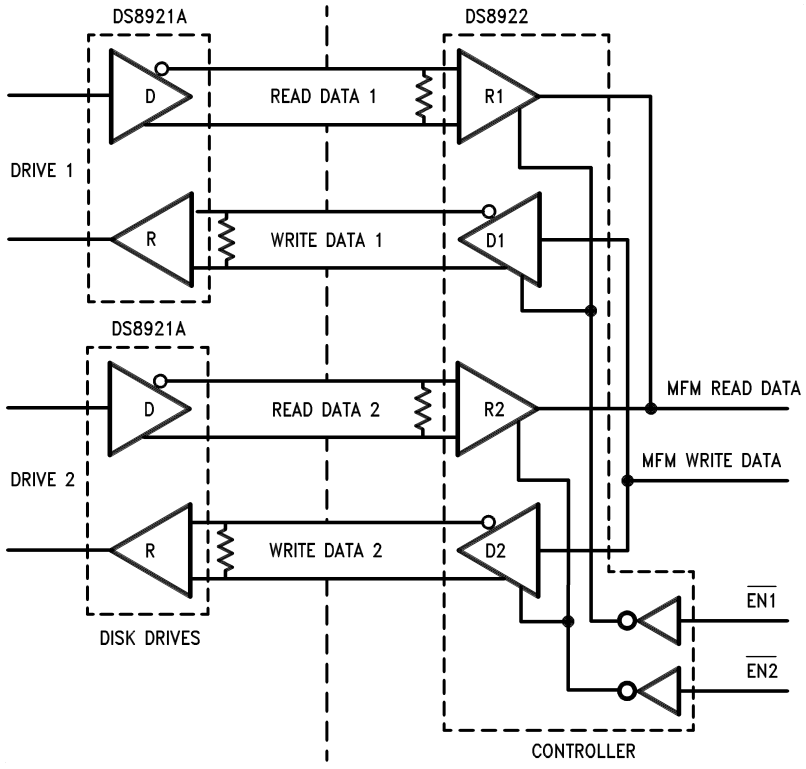


Figure 11. ST506 and ST412 Application

Typical Application (continued)

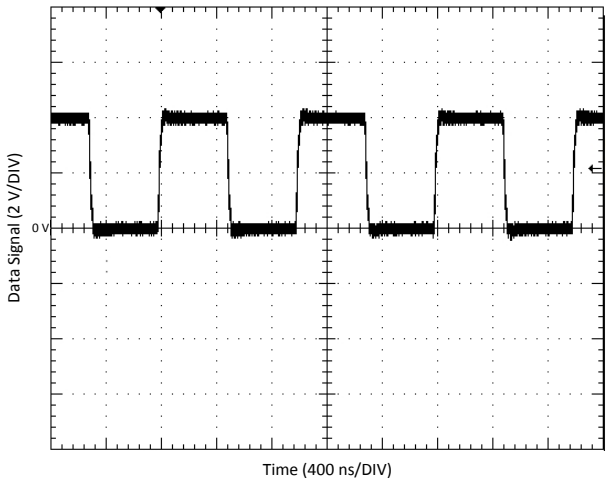
9.2.1 Design Requirements

- Apply TTL or LVCMOS signal to driver input at DI
- Transmit complementary outputs at DO+ and DO-
- Receive complimentary input signals at RI+ and RI-
- Receive TTL output signal at RO
- Use controlled-impedance transmission lines such as printed circuit board traces, twisted-pair wires or parallel wire cable
- Place terminating resistor at the far end of the differential pair

9.2.2 Detailed Design Procedure

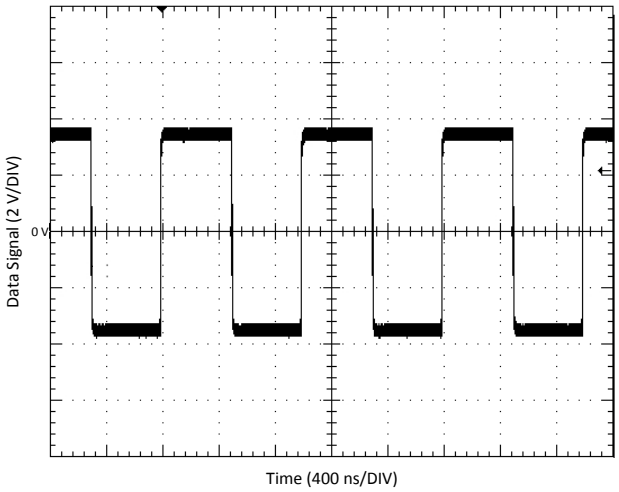
- Connect VCC and GND pins to the power and ground planes of the printed circuit board, with 0.1-uF bypass capacitor
- Use TTL/LVCMOS logic levels at DI and RO
- Use controlled-impedance transmission media for the differential signals DI+- and RO+-
- Place a terminating resistor at the far-end of the differential pair to avoid reflection
- Ensure the received complimentary signals at RO+ and RO- are within the signal threshold of ±200 mV

9.2.3 Application Curves



2.0 Mbps Single-Ended 1010 Data Pattern

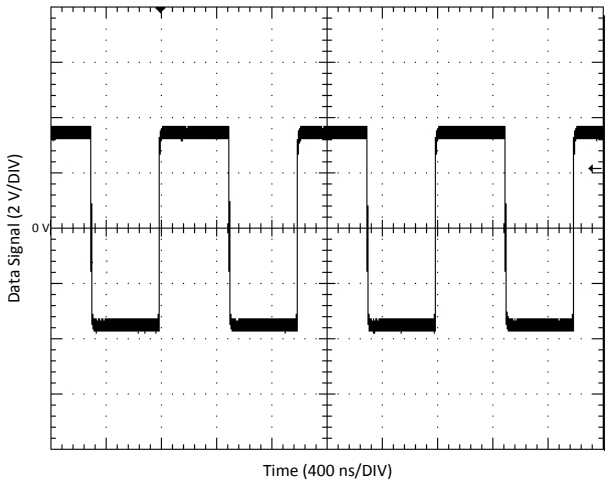
Figure 12. Driver Single-Ended Input Signal



2.0 Mbps Differential Data Pattern
Note: The input for the driver is Figure 12

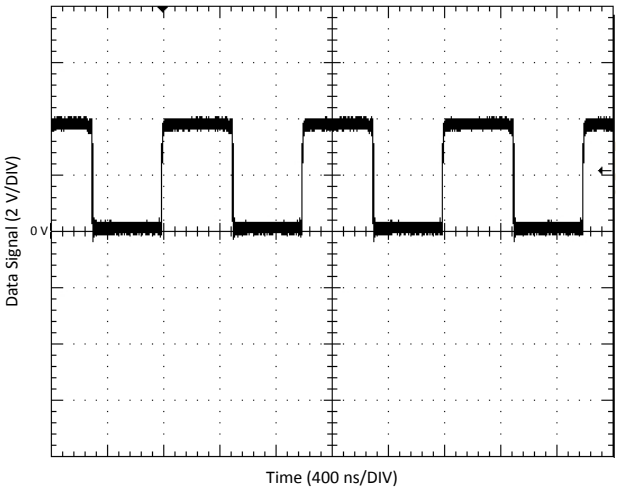
Figure 13. Driver Differential Output Signal

Typical Application (continued)



2.0 Mbps Differential Data Pattern

Figure 14. Receiver Differential Input Signal



2.0 Mbps Single-Ended 1010 Data Pattern
Note: The input for the receiver is Figure 14

Figure 15. Receiver Single-Ended Output Signal

10 Power Supply Recommendations

TI recommends connecting the supply (VCC) and ground (GND) pins to power planes that are routed on adjacent layers of the PCB. Additionally, careful attention should be paid to bypassing the supply using a capacitor. A 0.1-µF bypass capacitor should be connected to the VCC pin such that the capacitor is as close as possible to the device.

11 Layout

11.1 Layout Guidelines

High-speed interconnects should be treated as transmission lines with a controlled impedance. The differential interconnect can be a pair of printed-circuit board (PCB) traces, twisted-pair wires, or a parallel wire cable. A termination resistor should be placed at the differential input, and the resistor value should be approximately the same as the differential impedance of the transmission line to minimize reflections.

It is preferable to connect the VCC and GND pins to the power and ground planes using plated-through-holes. Additionally, a 0.1-µF bypass capacitor should be placed close to the VCC pin across VCC and GND.

Place a terminating resistor at the receiving end of the interconnect transmission line, as close as possible to the input pins of the receiver. The terminating resistor value should be approximately the same as the differential pair impedance to minimize reflection, and the transmission line should have a controlled impedance with minimum impedance discontinuities.

The input and output differential signals of the device should have traces that are routed exclusively on one layer of the board, and the differential pairs should also be routed away from other differential pairs in order to minimize crosstalk between transmission lines. Additionally, the differential pairs should have a controlled impedance with minimum impedance discontinuities and be terminated with a resistor that is closely matched to the differential pair impedance in order to minimize transmission line reflections. The differential pairs should be routed with uniform trace width and spacing to minimize impedance mismatch.

11.2 Layout Example

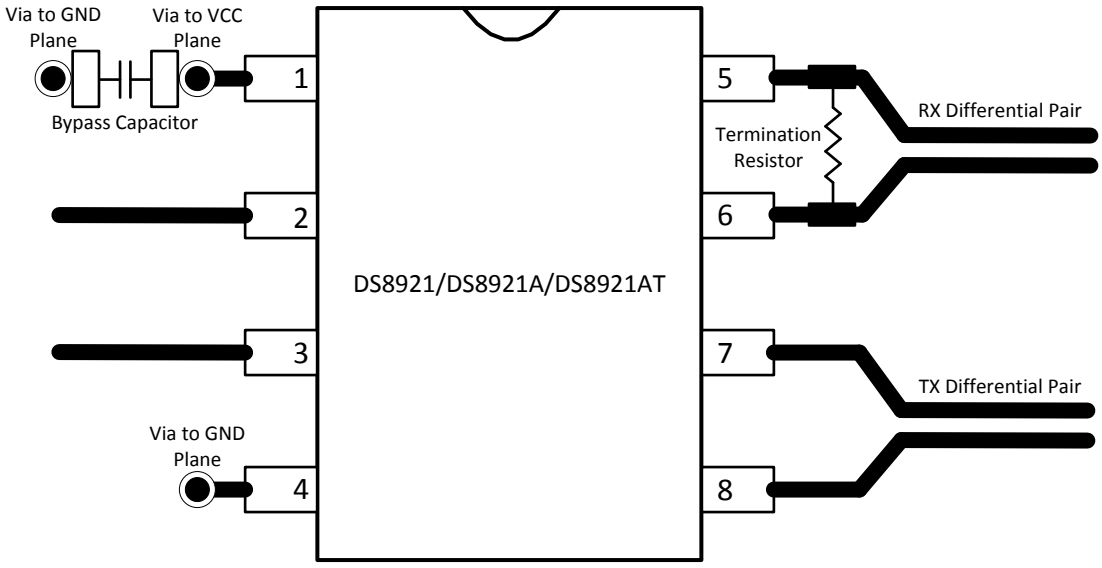


Figure 16. DS8921 Example Layout

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DS8921	Click here	Click here	Click here	Click here	Click here
DS8921A	Click here	Click here	Click here	Click here	Click here
DS8921AT	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS8921AM	LIFEBUY	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	DS89 21AM	
DS8921AM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS89 21AM	Samples
DS8921AMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS89 21AM	Samples
DS8921ATM	LIFEBUY	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	DS892 1ATM	
DS8921ATM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS892 1ATM	Samples
DS8921M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS892 1M	Samples
DS8921MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS892 1M	Samples
DS8921N/NOPB	LIFEBUY	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	DS8921N	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

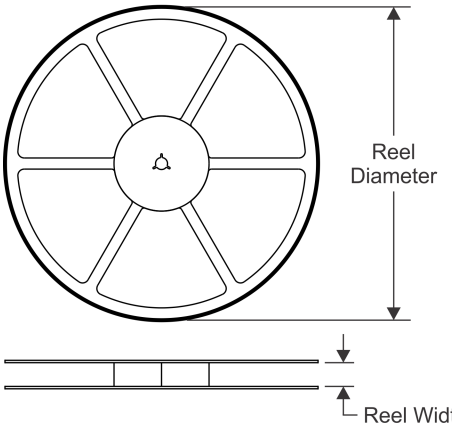
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

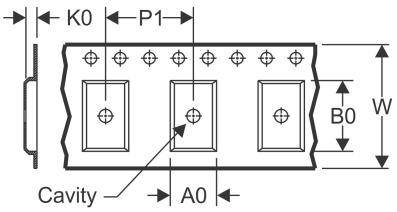
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

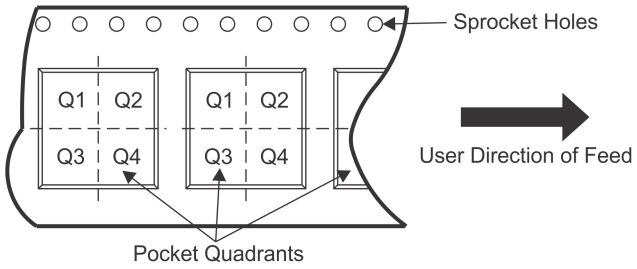


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

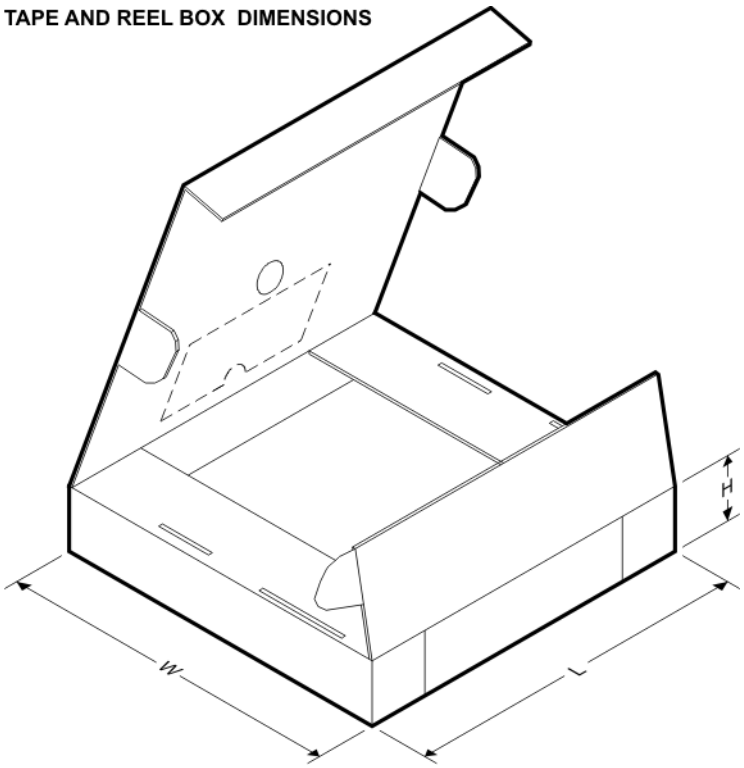
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS8921AMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
DS8921MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

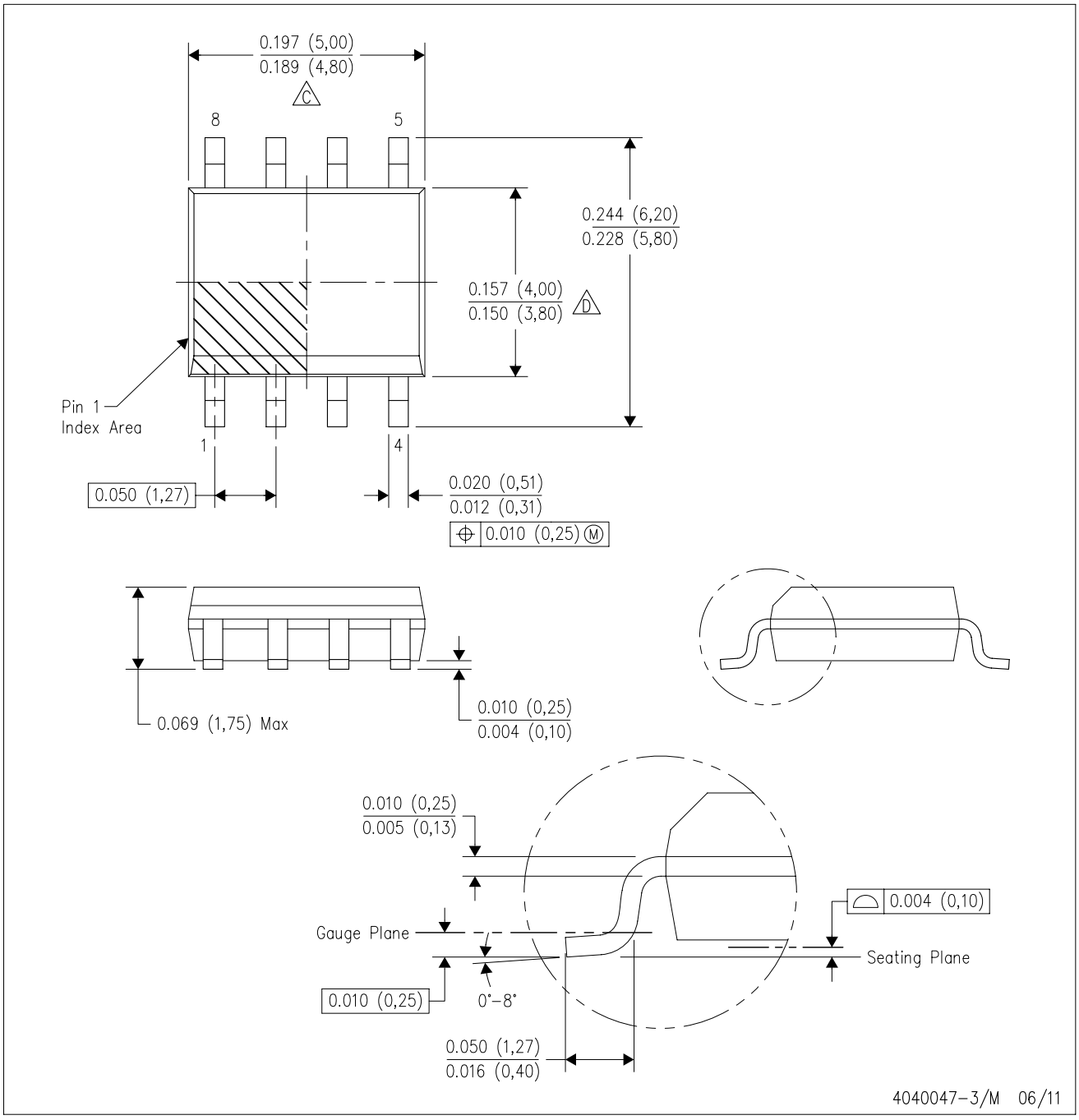
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

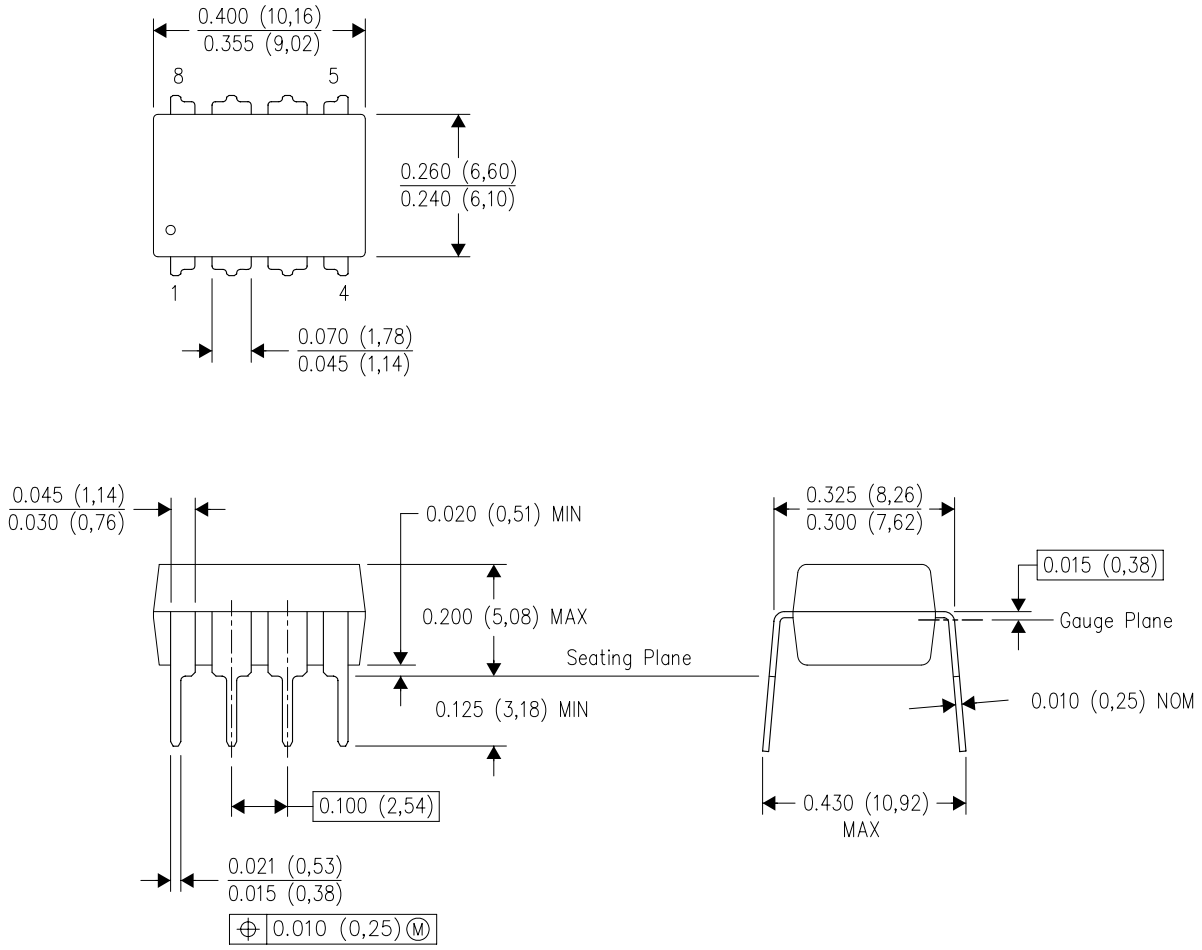
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS8921AMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
DS8921MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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