LMH2191 Dual Channel 52 MHz Clock Tree Driver

Check for Samples: LMH2191

FEATURES

- **One Input Clock, Two Output Clocks**
- **1.8V Square Wave Clock Outputs**
- **Inverted Clock Outputs**
- **Independent Clock Requests**
- **High Isolation of Supply Noise to Clock Input**
- **High Output-to-Output Isolation**
- **Integrated 1.8V Low-Dropout Regulator**
  - **Low Output-Noise Voltage**
  - **10 mA Load Current**
- **EMI Filtering**
- **Ultra Low Standby Current**
- **V_{BAT} Range = 2.5V to 5.5V**
- **8-Bump DSBGA Package**

APPLICATIONS

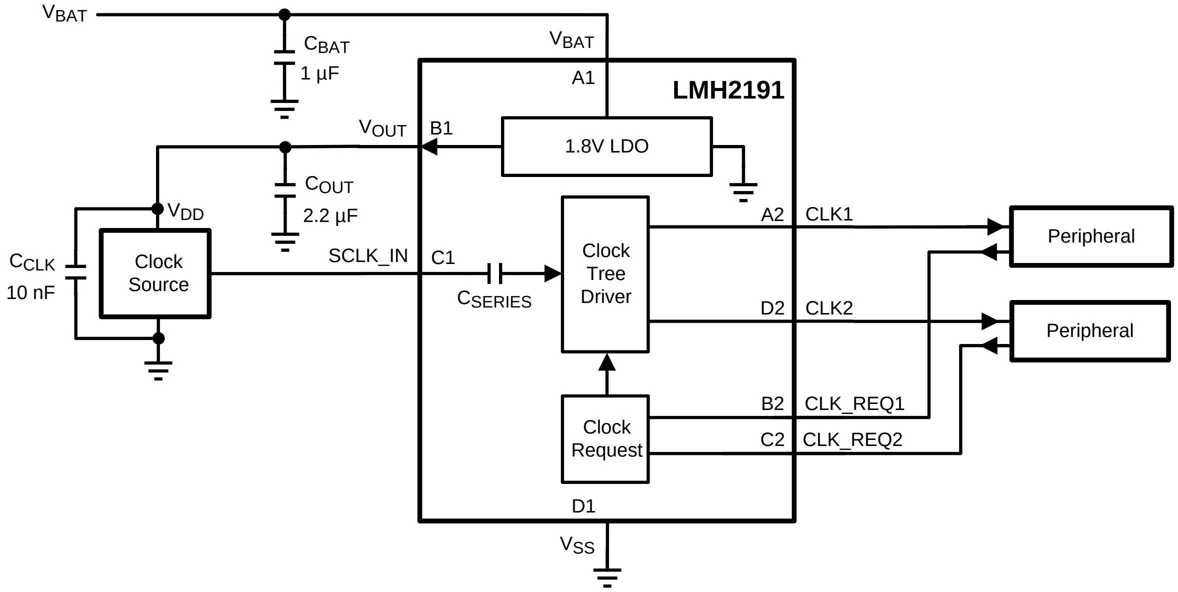
- **Mobile Handsets**
- **Portable Equipment**

DESCRIPTION

The LMH2191 is a dual-channel clock tree driver that supplies a digital system clock to peripherals in mobile handsets or other applications. It provides a solution to clocking issues such as limited drive capability for fanout or longer traces. It also provides protection of the master clock from varying loads and frequency pulling effects, isolation from noisy modules, and crosstalk isolation. It has very low phase noise which enables it to drive sensitive modules such as Wireless LAN and Bluetooth.

The LMH2191 can be clocked up to 52 MHz and has an independent clock request pin for each clock output which allows the peripheral to control the clock. It features an integrated LDO which provides an ultra low-noise voltage supply with 10 mA external load current which can be used to supply the TCXO or other clock source. The LMH2191 dual clock distributor is offered in a tiny 1.61 mm x 1.063 mm 8-bump DSBGA package. Its small size and low supply current make it ideal for portable applications.

Typical Application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2010–2013, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage	V_{BAT} - V_{SS}	-0.3V to 6V
	LVCMOS port IO voltage	-0.3V to (V_{OUT} + 0.3V)
ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
	Charge Device Model	1000V
Output Short Circuit Duration(4)	LDO	infinite
	Clock Output	infinite
For Soldering Information see http://www.ti.com/lit/SNOA549		
Storage Temperature Range		−65°C to 150°C
Junction Temperature(5)		150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For specifications and the test conditions, see the Electrical Characteristics Tables.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) Human body model, applicable std. MIL-STD-883, Method 3015.7. Machine model, applicable std. JESD22–A115–A (ESD MM std of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22–C101–C. (ESD FICDM std. of JEDEC)

(4) Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150^0C.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

OPERATING RATINGS(1)

Supply Voltage (V_{BAT} - V_{SS})		2.5V to 5.5V
Input Clock, SCLK_IN	Frequency	10 MHz to 52 MHz
	Duty Cycle	45% to 55%
Temperature Range		-40°C to +85°C
Package Thermal Resistance θ_{JA}(2)		Board specification: 4LCELLPHONE
Package YFX		153 °C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not specified. For specifications and the test conditions, see the Electrical Characteristics Tables.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

3.5 V ELECTRICAL CHARACTERISTICS(1)

Unless otherwise specified, all limits are specified at T_J = 25°C, V_{BAT} = 3.5V, C_{BAT} = 1μF, C_{OUT} = 2.2 μF(2), f_{SCLK_IN} = 26 MHz, I_{OUT} = 1mA, **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min(3)	Typ(4)	Max(3)	Units
Supply Current(5)(6)						
I_{DD}	Supply Current	Active Mode SCLK_IN = 19.2 MHz; both clock outputs toggling; C_{LOAD} CLK1/2 = 0pF; I_{OUT} = 0mA		1.4	1.65 **1.7**	mA
		Active Mode SCLK_IN = 19.2 MHz; both clock outputs toggling; C_{LOAD} for CLK1/2 = 33.5pF; I_{OUT} = 0mA		3.7	4.45 **4.50**	mA
		Active Mode SCLK_IN = 26 MHz, both clock outputs toggling, C_{LOAD} for CLK1/2 = 0pF, I_{OUT}=0mA		1.9	2.15 **2.25**	mA
		Active Mode SCLK_IN = 26 MHz, both clock outputs toggling, C_{LOAD} for CLK1/2 = 33.5 pF, I_{OUT}=0mA		5	5.80 **5.95**	mA
		In shutdown. Input clock not active. CLK_REQ1/2=Low		0.1	**1**	µA
		In shutdown. Input clock toggling. CLK_REQ1/2=Low		0.1	**1**	uA
C_{PD}	Power Dissipation Capacitance per CLK output	C_{LOAD} for CLK1,2 = 0pF, Defined with respect to V_{OUT} = 1.8V		20	23.0 **24.0**	pF
Clock Outputs (CLK1/2) Figure 1, Figure 2						
t_{PD_LH}	Propagation Delay - Low to High	50% to 50%; C_{LOAD} = 33 pF; measured on CLK1		6.1	**10.5**	ns
t_{PD_HL}	Propagation Delay - High to Low	50% to 50%; C_{LOAD} = 33 pF; measured on CLK1		6.1	**10.5**	
t_{SKEW}	Skew Between Outputs (Either Edge)	CLK1 to CLK2. 50% to 50%		1.5	**3.1**	
t_{RISE}	Rise Time(7)	For C_L between 33.5 pF - 50 pF, 20% to 80%; typical value based on 40 pF load	**2.1**	3.7	**5.9**	ns
t_{FALL}	Fall Time(7)	For C_L between 33.5 pF - 50 pF, 20% to 80%; typical value based on 40pF load	**2**	3.5	**5**	
CLK_DC	Output Clock Duty Cycle	For C_L between 33.5 pF - 50 pF	**42**	50	**58**	%
$Jitter_{RMS}$	Additive RMS period Jitter	$f_{SCLK-IN}$= 26 MHz, BW = 100 Hz to 1MHz; CLK1		95		fs
		$f_{SCLK-IN}$= 26 MHz, BW = 100 Hz to 1MHz; CLK2		110		

---

(1) Electrical Table values apply only for factory testing (ATE) conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

(2) C_{BAT}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

(3) Limits are 100% production tested at 25°C. Limits over temperature range are specified through correlations using statistical quality control (SQC) method.

(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

(5) Supply current depends on switching frequency and load.

(6) Positive current is current flowing into the device.

(7) This parameter is specified by design and/or characterization and is not tested in production.

3.5 V ELECTRICAL CHARACTERISTICS(1) (continued)

Unless otherwise specified, all limits are specified at T_J = 25°C, V_{BAT} = 3.5V, C_{BAT} = 1µF, C_{OUT} = 2.2 µF(2), f_{SCLK_IN} = 26 MHz, I_{OUT} = 1mA, **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition		Min(3)	Typ(4)	Max(3)	Units
CLK1 Phase Noise	Additive Phase Noise	All outputs enabled at 26 MHz	f = 100 Hz		-128		dBc/Hz
			f = 1 kHz		-144		
			f = 10 kHz		-150		
			f = 100 kHz		-160		
			f = 1 MHz		-163		
		All outputs enabled at 19.2 MHz	f = 100 Hz		-127		
			f = 1 kHz		-146		
			f = 10 kHz		-153		
			f = 100 kHz		-161		
			f = 1 MHz		-163		
CLK2 Phase Noise	Additive Phase Noise	All outputs enabled at 26 MHz	f = 100 Hz		-127		
			f = 1 kHz		-142		
			f = 10 kHz		-148		
			f = 100 kHz		-160		
			f = 1 MHz		-162		
		All outputs enabled at 19.2 MHz	f = 100 Hz		-129		
			f = 1 kHz		-144		
			f = 10 kHz		-151		
			f = 100 kHz		-163		
			f = 1 MHz		-164		
V_{OH}	CLK1/2 Output Voltage High Level	I_{OH} = -2mA (equivalent output load 800Ω)		**1.6**			V
V_{OL}	CLK1/2 Output Voltage Low Level	I_{OL} = 2mA				**0.2**	
R_{OFF}	Ouput Impedance when disabled	with other output enabled (LDO enabled)			grounded		
		Both outputs disabled (LDO disabled)			diode to ground		
System Clock Input (SCLK_IN)							
$V_{I\text{-}pp}$	SCLK_IN peak- to- peak input level(7)	For duty cycle variation < 1%		**0.6**	1	**1.8**	V
I_{IH}	Current into SCLK_IN pin (Input HIGH)	SCLK_IN = 1.8V, CLK_REQ1/2=Low			0	**0.1**	µA
I_{IL}	Current into SCLK_IN pin (Input LOW)	SCLK_IN = 0V, CLK_REQ1/2=Low		**–0.1**	0		
C_{IN}	Input Capacitance(8)	CLK_REQ1/2=High			7.5	**13**	pF
R_{IN}	Input Resistance(8)	CLK_REQ1/2=High see Application Note: Input Impedance			14	**20**	kΩ
Switching Characteristics: System Clock Input							
f_{SCLK_IN}	System Clock			**10**	26	**52**	MHz
CLK_DC	Input Clock Duty Cycle			45	50	55	%

(8) This parameter is specified by design and/or characterization and is not tested in production.

3.5 V ELECTRICAL CHARACTERISTICS(1) (continued)

Unless otherwise specified, all limits are specified at T_J = 25°C, V_{BAT} = 3.5V, C_{BAT} = 1µF, C_{OUT} = 2.2 µF(2), f_{SCLK_IN} = 26 MHz, I_{OUT} = 1mA, **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition		Min(3)	Typ(4)	Max(3)	Units
Clock Request Inputs (CLK_REQ1/2)							
t_{SET}	Setup Time from CLK_REQx to SCLK_IN, to enable CLKx (Figure 3)			**12**	6.2		ns
V_{IH}	CLK_REQ1/2 logic HIGH input level. (clock output = ON)(9)	V_{BAT} = 2.5V		**1.4**			V
		V_{BAT} = 3.5V		**1.4**			
		V_{BAT} = 5.5V		**1.4**			
V_{IL}	CLK_REQ1/2 logic LOW input level. (clock output = OFF)	V_{BAT} = 2.5V				**0.4**	V
		V_{BAT} = 3.5V				**0.4**	
		V_{BAT} = 5.5V				**0.4**	
I_{IH}	Current into CLK_REQ pin	V_{IH} = 1.8V, 200 kΩ pull down resistor (Input HIGH)			8.5	**14**	µA
I_{IL}	Current into CLK_REQ pin	V_{IL} = V_{SS}, (Input LOW)		**-0.2**	0		µA
LDO							
V_{OUT}	Output Voltage	I_{OUT} = 1mA		**1.73**	1.8	**1.88**	V
I_{LOAD}	Load Current(10)	V_{OUT} > 1.7V		0		10	mA
V_{DO}	Dropout Voltage(11)	I_{OUT} = 10 mA Vout=1.7V			125		mV
I_{SC}	Short Circuit Current Limit				300		mA
PSRR	Power Supply Rejection Ratio	V_{BAT} ripple = 200 mV_{PP}, I_{OUT} = 10 mA	f = 100 Hz		92		dB
			f = 217.5 Hz		90		
			f = 1 kHz		78		
			f = 10 kHz		60		
			f = 100 kHz		50		
			f = 1 MHz		50		
			f = 3.25 MHz		42		
E_N	Output Noise Voltage(12)	BW = 10 Hz to 100 kHz, CLK_REQ1/2=High, Input clock not active			18		$µV_{RMS}$
T_{SHTDWN}	Thermal Shutdown	Temperature			160		°C
		Hysteresis			20		
$ΔV_{OUT}$	Line Transient	V_{BAT} = 2.8V to 3.4V in 30 µs, I_{OUT} = 1mA		**-1**			mV
		V_{BAT} = 3.4V to 2.8V in 30 µs, I_{OUT} = 1mA				**1**	
	Load Transient	I_{OUT} = 0mA to 10 mA in 10 µs		**-15**			mV
		I_{OUT} = 10 mA to 0mA in 10 µs				**10**	
	Overshoot on Startup					**20**	mV
R_{OUT}	DC Output Resistance				5		Ω
T_{ON}	Turn on Time	From rising edge of CLK_REQ1 to 95% of V_{OUT}(NOM)			200	260 **350**	µs

(9) Clock Request Inputs can tolerate logic high input levels up to V_{BAT}.
(10) The device maintains stable, regulated output voltage without a load.
(11) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
(12) The noise figure is the noise of the LDO only; harmonics of the output clocks are excluded.

TIMING DIAGRAMS

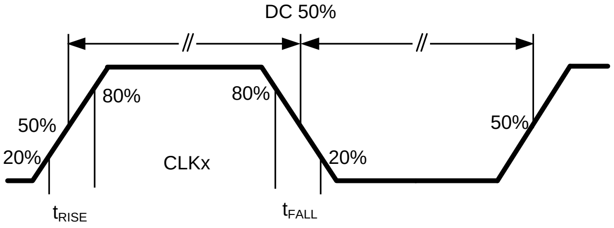

DC 50%
50%
20%
80%
CLKx
80%
20%
50%
tRISE
tFALL

Figure 1. Rise / Fall time and Duty Cycle Waveform for Clock Outputs

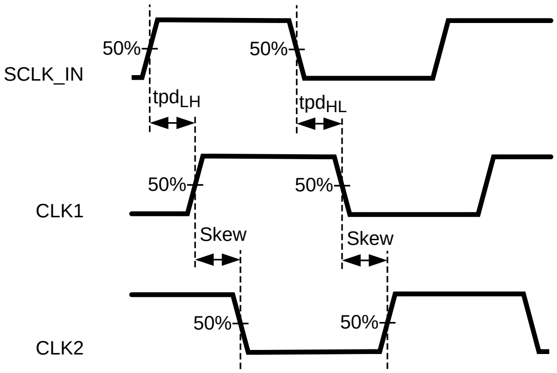

SCLK_IN
50%
50%
tpdLH
tpdHL
CLK1
50%
50%
Skew
Skew
CLK2
50%
50%

Figure 2. Clock Output Timing Waveforms

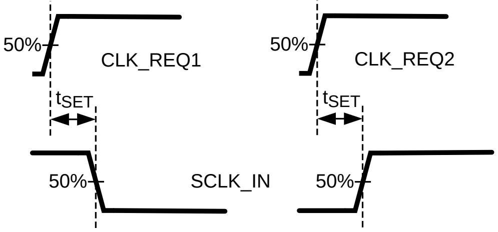

50%
CLK_REQ1
50%
CLK_REQ2
tSET
tSET
50%
SCLK_IN
50%

Figure 3. Clock Request Timing Waveforms

Connection Diagram

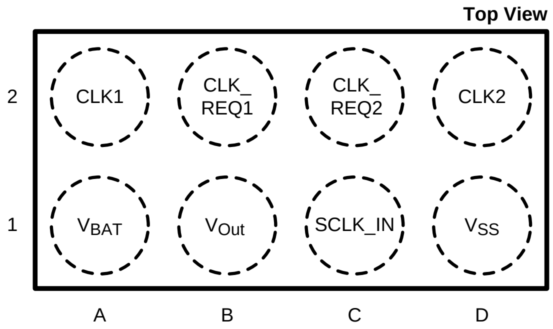


Figure 4. 8-Bump DSBGA
See YFX0008 Package

PIN DESCRIPTIONS

Pin	Pin Name	Port / Direction	Type[1]	Description
C1	SCLK_IN	Host	Input	Source Clock Input
A2	CLK1	Peripheral	Output	Clock Output 1
B2	CLK_REQ1	Peripheral	Input	Clock Request Input 1 Clock1 = ON at high level
D2	CLK2	Peripheral	Output	Clock Output 2
C2	CLK_REQ2	Peripheral	Input	Clock Request Input 2 Clock2 = ON at high level
A1	V_{BAT}	Battery / Input	Power	Power Supply
B1	Vout	LDO / Output	Power	Power Supply to Clock Source and clock outputs
D1	V_{SS}	Ground	Ground	Ground Pin

(1) I = Input, O = Output, I/O = Input / Output

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, C_{OUT} = 2.2 µF

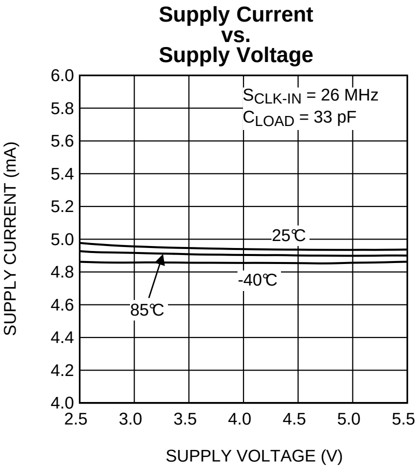

Supply Current vs. Supply Voltage

Figure 5.

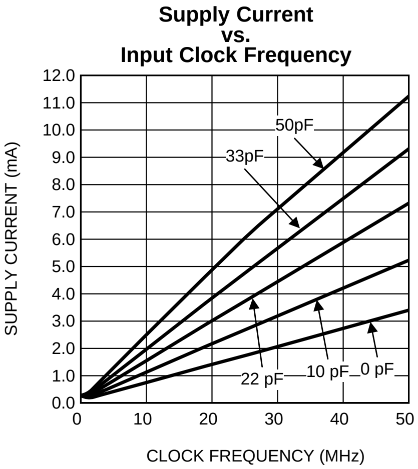

Supply Current vs. Input Clock Frequency

Figure 6.

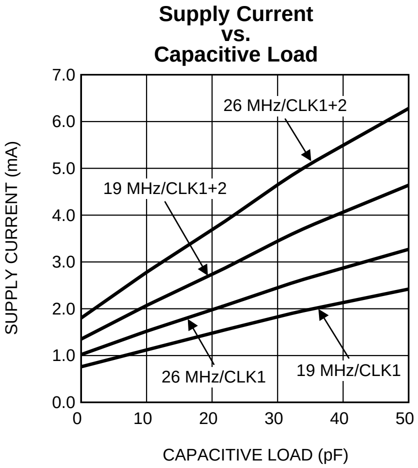

Supply Current vs. Capacitive Load

Figure 7.

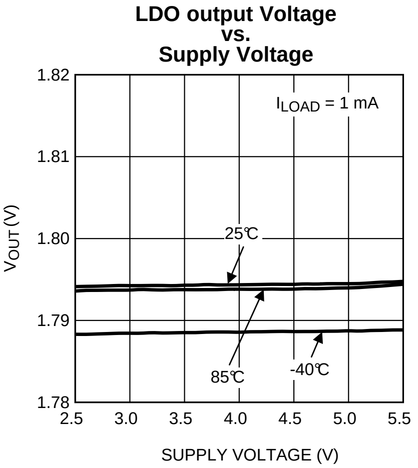

LDO output Voltage vs. Supply Voltage

Figure 8.

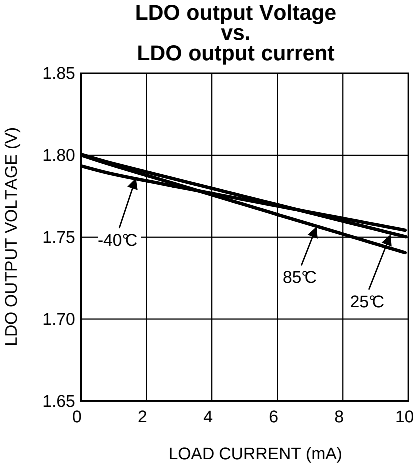

LDO output Voltage vs. LDO output current

Figure 9.

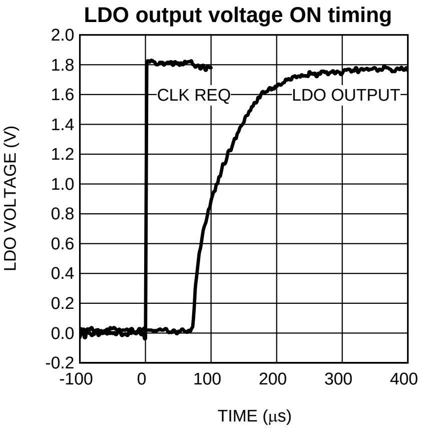

LDO output voltage ON timing

Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, C_{OUT} = 2.2 µF

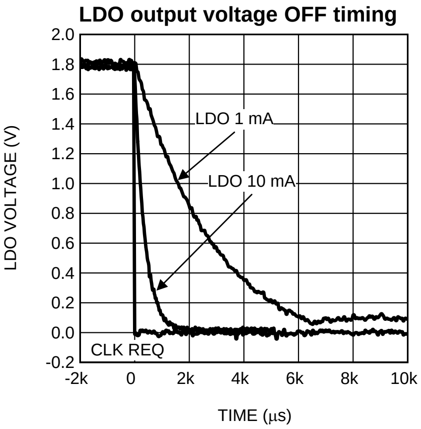

LDO output voltage OFF timing

Figure 11.

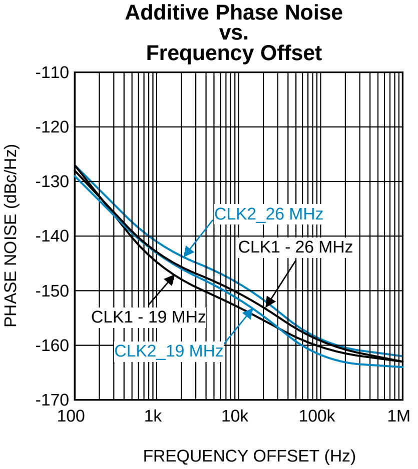

Additive Phase Noise vs. Frequency Offset

Figure 12.

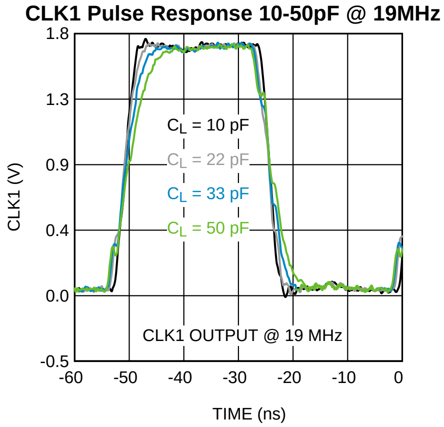

CLK1 Pulse Response 10-50pF @ 19MHz

Figure 13.

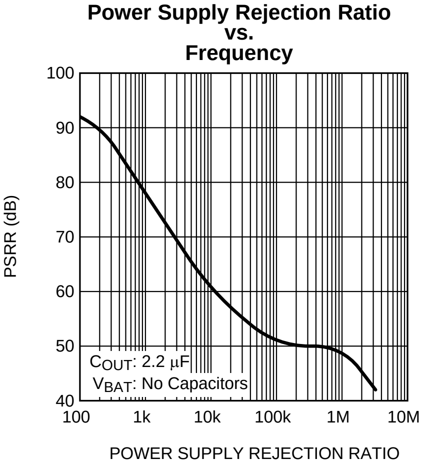

Power Supply Rejection Ratio vs. Frequency

Figure 14.

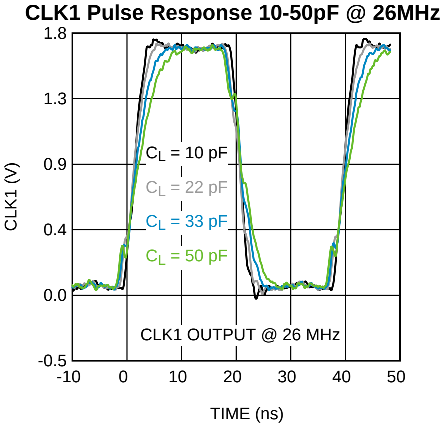

CLK1 Pulse Response 10-50pF @ 26MHz

Figure 15.

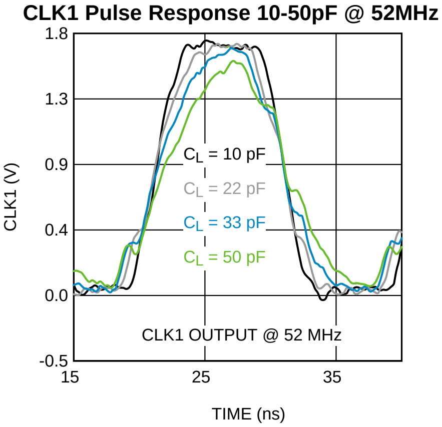

CLK1 Pulse Response 10-50pF @ 52MHz

Figure 16.

APPLICATION INFORMATION

The LMH2191 is a complete 52 MHz clocking conditioner and clock tree driver. The LMH2191 is used to supply a common clock to mobile phone peripherals such as Bluetooth, Wireless LAN, and/or Digital Video Broadcast-H (DVB-H). The high isolation between the clock outputs ensures that the peripherals don't disrupt each other. Its excellent phase noise characteristics prevent the clock quality from deteriorating. A typical LMH2191 setup is depicted in Figure 17.

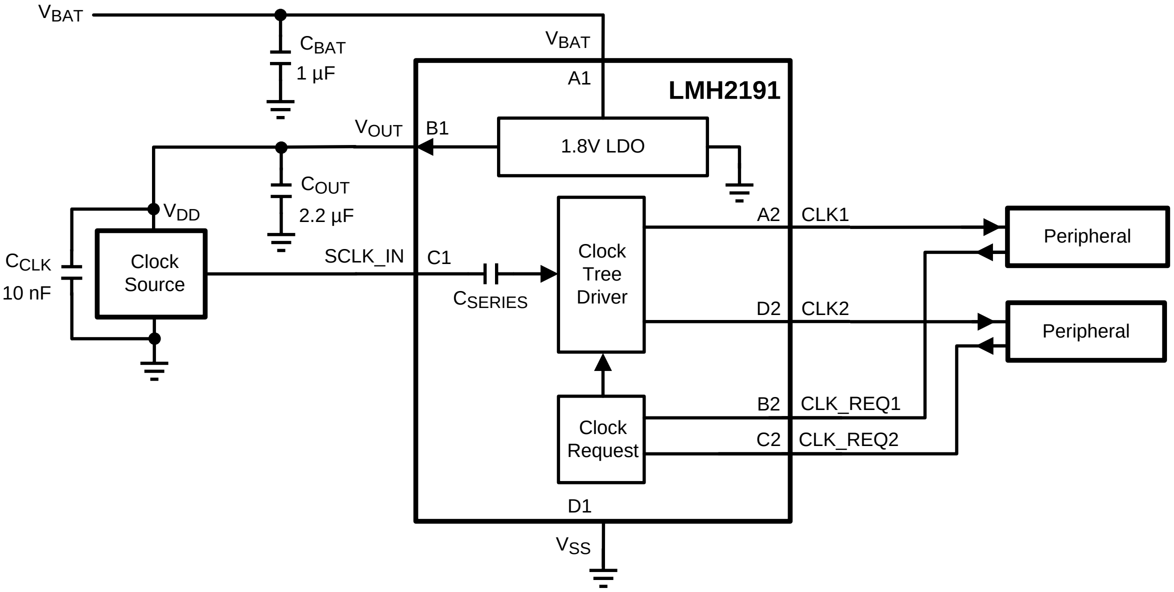

V_{BAT}
C_{BAT}
1 µF
V_{BAT}
A1
LMH2191
V_{OUT}
B1
1.8V LDO
C_{OUT}
2.2 µF
V_{DD}
C_{CLK}
10 nF
Clock Source
SCLK_IN
C1
C_{SERIES}
Clock Tree Driver
A2
CLK1
Peripheral
D2
CLK2
Peripheral
B2
CLK_REQ1
C2
CLK_REQ2
Clock Request
D1
V_{SS}

Figure 17. LMH2191 Typical Application Schematic

The internal structure of the LMH2191 is depicted in the block diagram of Figure 18.

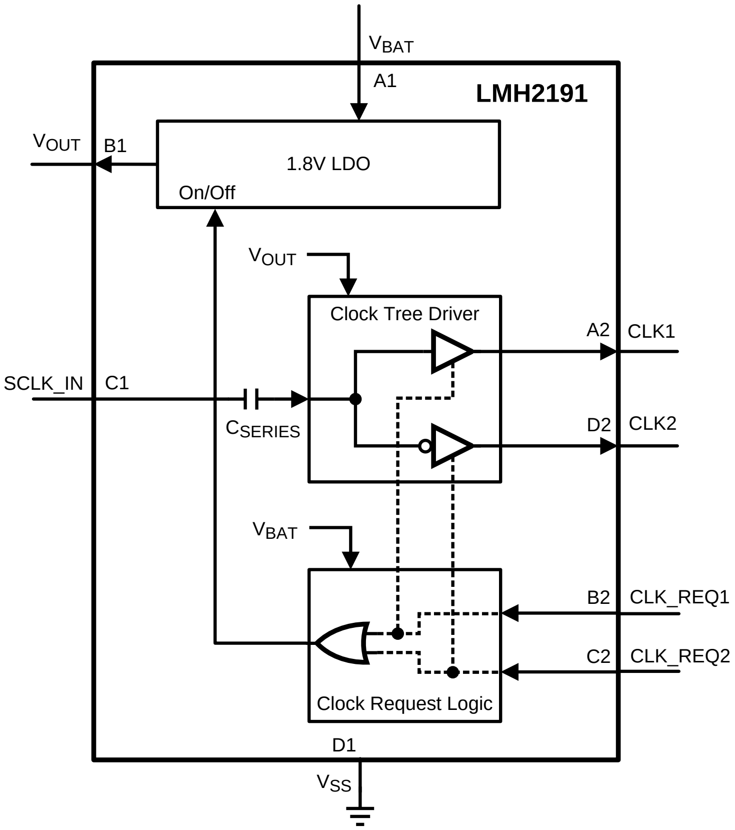


Figure 18. Block Diagram

The LMH2191 clock distribution circuit is comprised of 3 blocks:

- Clock tree driver
- Clock request logic
- Low Dropout Regulator (LDO)

The clock tree driver provides a clean clock to 2 separately connected peripheral devices. Independent clock request inputs allow the peripheral to control when the particular clock should be enabled. Furthermore, both clock request inputs control the LDO output voltage, e.g., when both request inputs are low (no CLK1 and no CLK2 output required), the LDO voltage is disabled. The LDO provides a low-noise, high-PSRR supply voltage that enables low phase noise on the clock outputs, and low quiescent current for portable applications. It can also be used to supply the TCXO. The following sections provide a detailed description of each block.

CLOCK TREE DRIVER

The clock tree driver consists of one input that drives 2 outputs. It is supplied by a high-precision voltage regulator of 1.8V, the LDO. The Clock outputs are enabled when the appropriate Clock Request inputs are logic high.

Clock Tree Driver Input

The source clock input (SCLK_IN) is the input for the clock tree driver. This input has an internally connected coupling capacitor (C_{SERIES}) with a value of 33pF. In shutdown mode (when both CLK_REQ inputs are low), the input stage is completely switched off to prevent unnecessary power consumption when the source clock is still present.

Due to the internal coupling capacitor, the clock signal is DC biased, since the coupling capacitor prevents the internal biasing of the input circuitry to be affected by the external DC voltage. Because of the coupling capacitor, the minimum clock frequency is 10 MHz. It is assumed that the input signal is a sine wave or a typical TCXO waveform (the signal from a TCXO has slow edges), enabling the control loop to adjust to a duty cycle of 50% if the input signal differs slightly from 50% duty cycle. The duty cycle is an important timing parameter for the peripheral equipment. The circuit that adjust the duty cycle is shown in Figure 19.

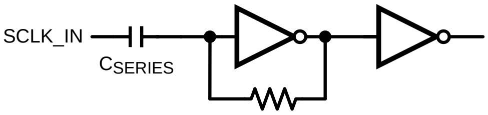


Figure 19. Clock Duty Cycle Regulation

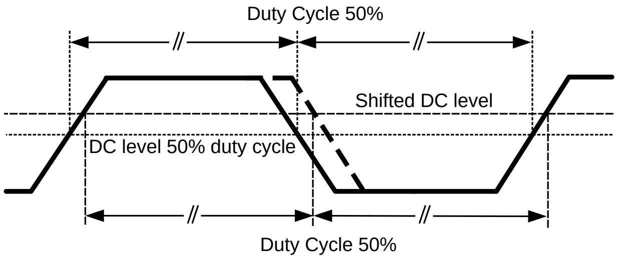


Figure 20. Duty Cycle adjust levels

In order to achieve a duty cycle of 50%, the edges of the incoming clock signal (SCLK_IN) are used to move the switching point to the level that is needed to create the 50% duty cycle. The simplified input circuit consists of an inverter and a feedback resistor. Together with the input series capacitor of about 30 pF, the circuit creates a DC level depending on the duty cycle of the incoming clock signal. When the duty cycle is exactly 50%, the DC level is in the middle of the upper and lower pulse level. When the duty cycle differs from 50%, the DC level shifts slightly to maintain the duty cycle level at 50%. (See Duty Cycle adjust levels of Figure 20.) As explained above, the slow edges of the SCLK_IN signal are important to make the control loop work.

Input Impedance

The input impedance can be split up into two parts: the DC input resistance and the AC input impedance. Due to the used series capacitor in the input signal path the DC resistance is infinite. The AC input impedance is formed by the circuit drawn in Figure 19. This circuit consists of an inverter and a feedback resistor. A signal fed to the input pin is connected to the inverter input which has a high input impedance and is in parallel to the feedback resistor of 30 kΩ. The other pin of the feedback resistor is connected to the output of the inverter which means that the input current is higher than it would be if it were connected to a decoupled supply connection. For this reason the AC input resistance can be much lower than the connected feedback resistor of 30 kΩ. The input resistance is dependant on the amplitude of the input signal. When an input amplitude of 1.8V is used (the same amplitude as the output of the inverter), the input impedance is theoretical half the value of the feedback resistor. When the amplitude of the input signal lowers, the input resistance becomes lower too. With an input signal of $1V_{PP}$, the input impedance will be about 10 kΩ.

Clock Tree Driver Outputs

The LMH2191's clock tree driver outputs have a drive strength that make each output capable of driving a capacitive load up to 50 pF, together with a minimum of EMI. Further reduction of EMI is achieved by the inversion of the CLK2 output. (See Figure 21.) Both the drive strength and the capacitive load make the edges of the output pulse relative slow which is favorable for EMI reduction.

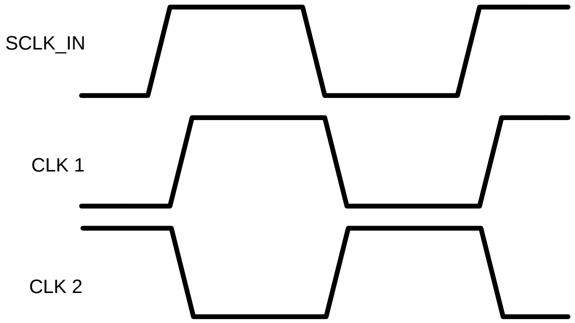


Figure 21. Clock Outputs

CLOCK REQUEST LOGIC

A clock request input is provided for each clock output. This allows the peripheral device to control when it wants to receive a clock. In case the application does not have clock request functionality, the CLKx_REQ can be hard wired to a logic high level to enable the clock output continuously. The clock request inputs have logic levels compatible with 1.8V logic, but can tolerate logic high levels up to V_{BAT}.

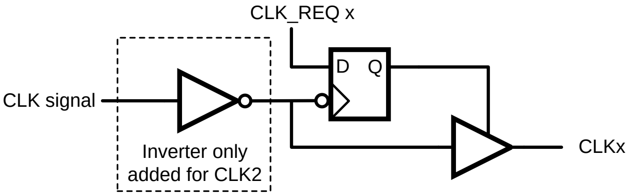


Figure 22. Enabling the output

The clock request logic enables an independent control of the clock tree driver outputs, CLK1 and CLK2, as well as an LDO disable when both request inputs are low.

The on and off switching of the clock output drivers is done synchronously with the clock input in order to prevent glitches at the clock output. For this the clock request signal is connected to the D input of a latch. The Q output of this latch enables the clock output driver (see Figure 22). For the CLK1 output the CLK input signal is connected via an inverter to the clock input of the latch. In this way the latch enables and disables the CLK1 output buffer on the falling edge of the clock signal. For the CLK2 output an extra inverter is inserted prior to the latch circuit, and the CLK2 output buffer is enabled and disabled on the rising edge of the clock input signal (equal to the falling edge of the CLK2 output signal).

LOW DROPOUT REGULATOR

The linear and Low-Dropout regulator (LDO) is used to regulate the input voltage, V_{BAT}, thus generating a well-defined ultra low noise 1.8V supply voltage. This allows the LMH2191 to suppress V_{BAT} supply voltage ripple and noise for the TCXO and the internal Clock Path. Voltage ripple and noise would distort clock edges causing extra phase noise on the distributed clock signal.

The LDO is powered up whenever a Clock Request is active; it supports overheating detection and will switch off in case overheating occurs. The recommended sequence for powering up the LDO is to raise a clock request to a high level with the supply already powered up. Thus the LDO stays in shutdown mode with sub µA current consumption until an output clock is actually needed. The LDO will power up within the turn-on time of about 200 µs (as specified in the data sheet tables). Alternatively, the clock request input can be hard wired to V_{BAT} which powers up the LDO simultaneously with V_{BAT}. A drawback is that the LDO and clock path (and if connected, the TCXO) will always draw current when V_{BAT} is powered up. Also, in this setup, care should be taken with supplies with an excessive long startup time of more than about 25 ms. Under this condition the LDO could exhibit excessive long turn-on delay (order of seconds.)

LAYOUT RECOMMENDATIONS

As with any other device, careful attention must be paid to the board layout. If the board isn't properly designed, the performance of the device can be less than desired. Care should be taken that the SCLK_IN input trace and the output traces of CLK1 and CLK2 are as short as possible to reduce extra capacitive load observed by the clock outputs. Also proper de-coupling close to the device is necessary. Table 1 depicts the advised component values. TI suggests to use the evaluation board, available from the Texas Instruments web site www.ti.com, as a guide for layout and as an aid in device testing and characterization.

Table 1. Recommended Component Values

Symbol	Parameter	Min	Typ	Max	Units
C_{BAT} (1)	Capacitor on V_{BAT}	0.47	1		µF
C_{OUT} (1)	Capacitor on V_{OUT}	1	2.2		
ESR	Equivalent Series Resistance	5		500	mΩ

(1) C_{BAT}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCC's) used in setting electrical characteristics.

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH2191TME/NOPB	ACTIVE	DSBGA	YFX	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5	Samples
LMH2191TMX/NOPB	ACTIVE	DSBGA	YFX	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

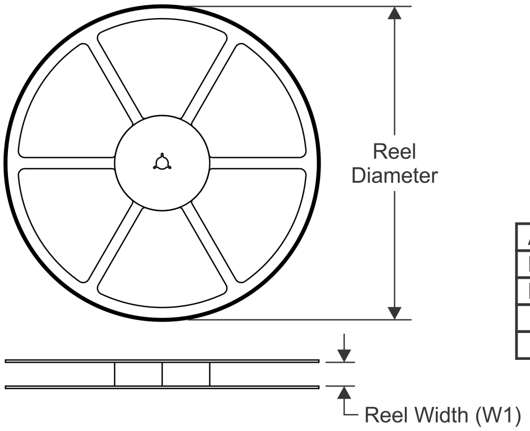
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

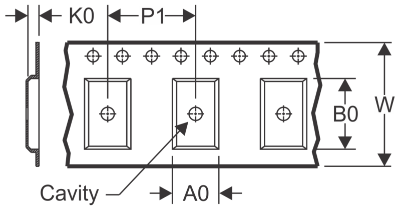
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

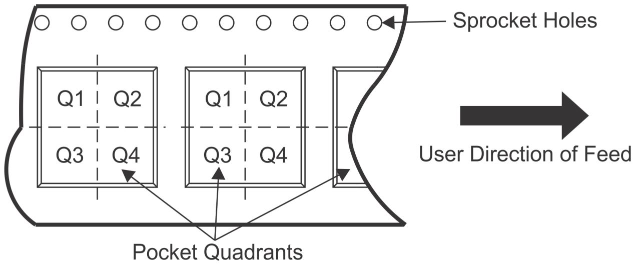

Reel
Diameter
Reel Width (W1)

TAPE DIMENSIONS


K0
P1
B0
W
Cavity
A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

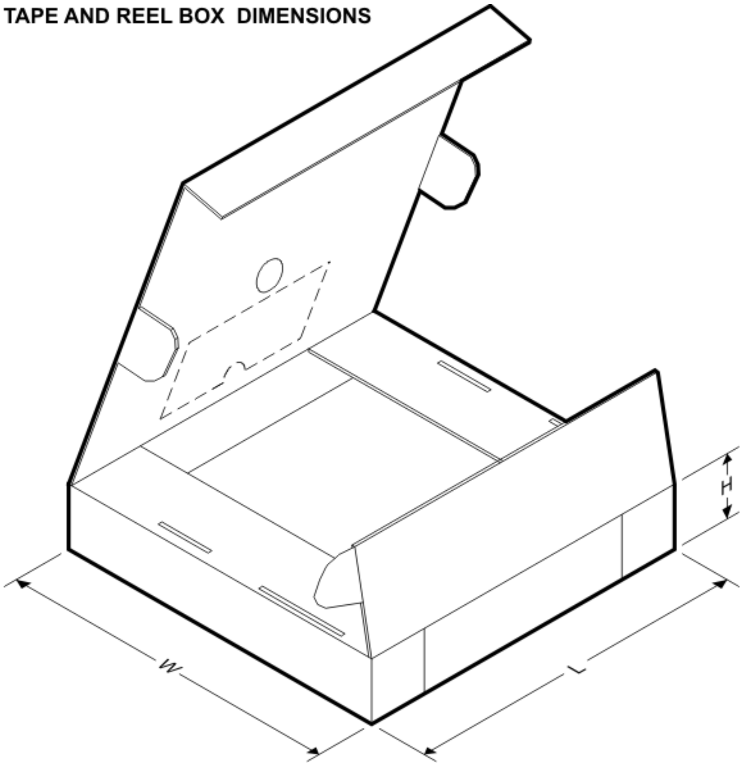
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


Sprocket Holes
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
User Direction of Feed
Pocket Quadrants

*All dimensions are nominal

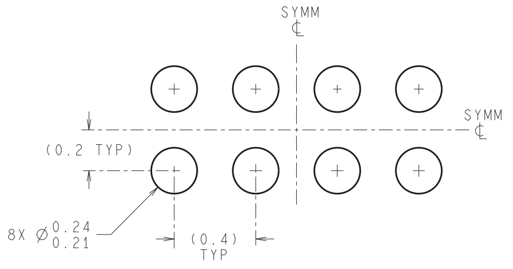
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH2191TME/NOPB	DSBGA	YFX	8	250	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1
LMH2191TMX/NOPB	DSBGA	YFX	8	3000	178.0	8.4	1.24	1.7	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



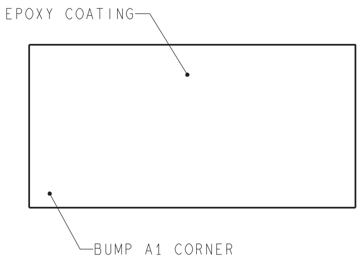
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH2191TME/NOPB	DSBGA	YFX	8	250	210.0	185.0	35.0
LMH2191TMX/NOPB	DSBGA	YFX	8	3000	210.0	185.0	35.0

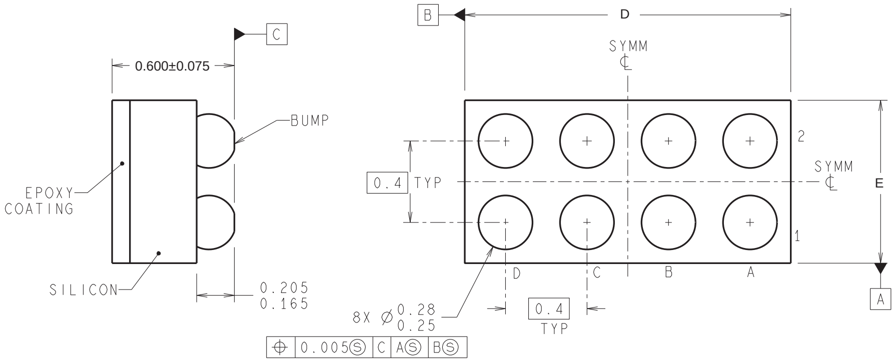

SYMM
℄
SYMM
℄
(0.2 TYP)
8X ∅ 0.24 0.21
(0.4) TYP

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION


EPOXY COATING
BUMP A1 CORNER

TOP SIDE OF PACKAGE


C
0.600±0.075
BUMP
EPOXY COATING
SILICON
0.205 0.165
B
D
SYMM
℄
0.4 TYP
2
SYMM
℄
E
1
D C B A
A
8X ∅ 0.28 0.25
0.4 TYP
⌖ 0.005Ⓢ C AⓈ BⓈ

BOTTOM SIDE OF PACKAGE

TMP08XXX (Rev A)

D: Max = 1.64 mm, Min = 1.58 mm

E: Max = 1.093 mm, Min =1.033 mm

4215093/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, “Designers”) understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers’ applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI’s provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, “TI Resources”) are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer’s company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI’s provision of TI Resources does not expand or otherwise alter TI’s applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED “AS IS” AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers’ own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer’s non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265