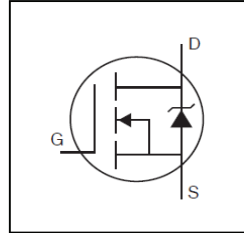


HEXFET® Power MOSFET

Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}	100V
R_{DS(on)} typ.	7.9mΩ
R_{DS(on)} max.	9.3mΩ
I_D	43A

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



TO-220 Full-Pak

G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFI4410ZPbF	TO-220 Full-Pak	Tube	50	IRFI4410ZPbF

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	43	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	30	
I _{DM}	Pulsed Drain Current ①	170	
P _D @ T _C = 25°C	Maximum Power Dissipation	47	W
	Linear Derating Factor	0.3	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
E _{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	310	mJ
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ④	—	3.2	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mount)④	—	65	

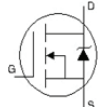
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	95	—	mV/°C	Reference to 25°C , $I_D = 5mA$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	7.9	9.3	mΩ	$V_{GS} = 10V, I_D = 26A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	0.9	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

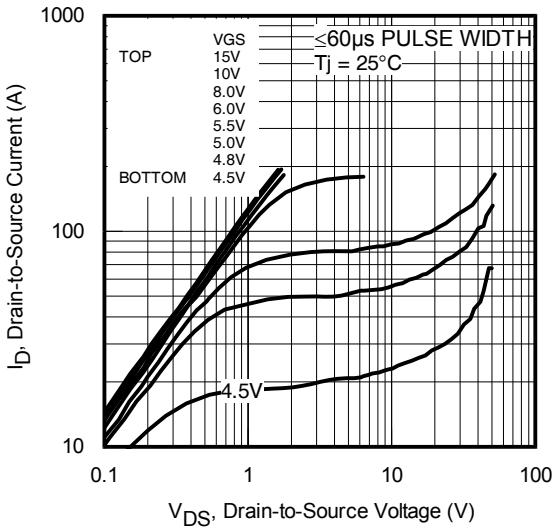
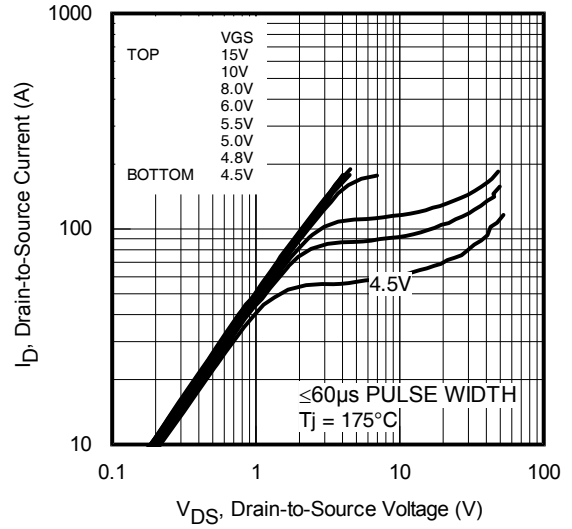
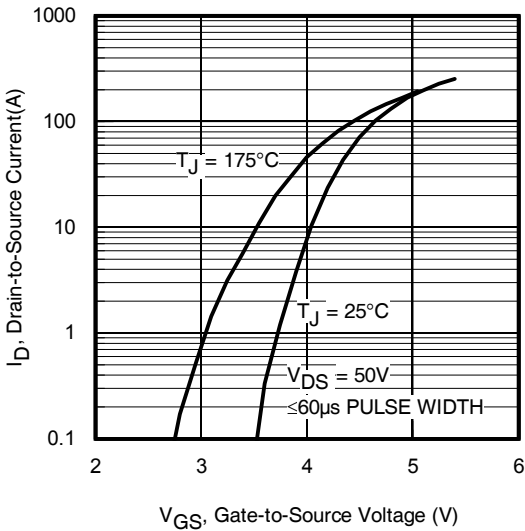
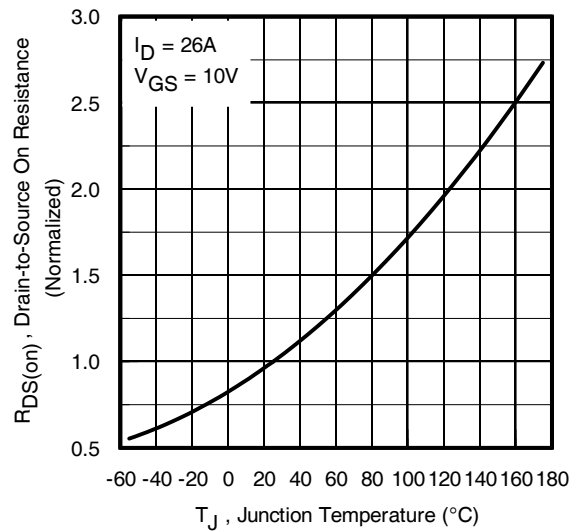
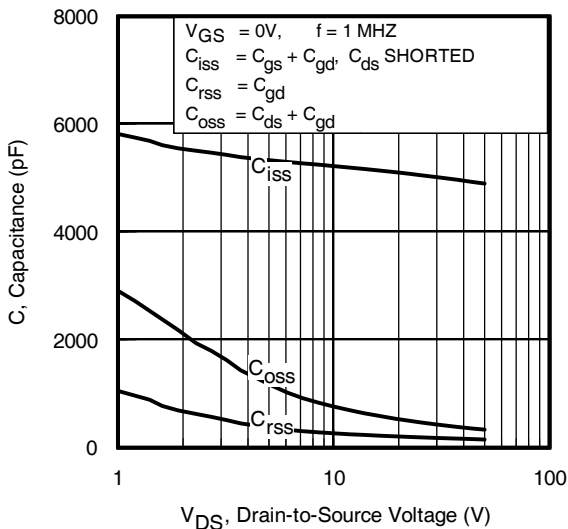
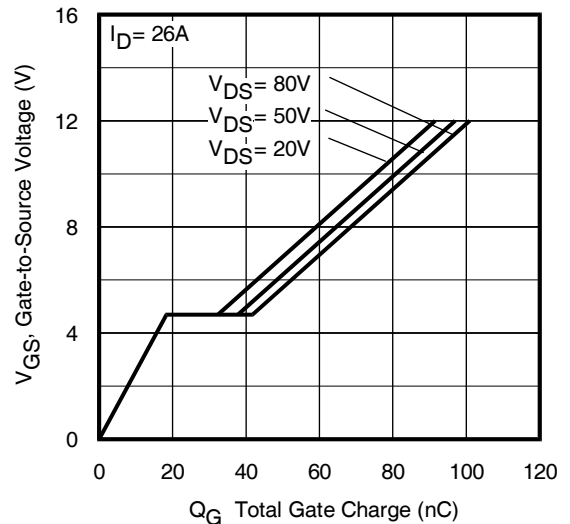
g_{fs}	Forward Trans conductance	80	—	—	S	$V_{DS} = 50V, I_D = 26A$
Q_g	Total Gate Charge	—	81	110	nC	$I_D = 26A$
Q_{gs}	Gate-to-Source Charge	—	18	—		$V_{DS} = 50V$
Q_{gd}	Gate-to-Drain Charge	—	23	—		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = 65V$
t_r	Rise Time	—	27	—		$I_D = 26A$
$t_{d(off)}$	Turn-Off Delay Time	—	43	—		$R_G = 2.7\Omega$
t_f	Fall Time	—	30	—		$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	4910	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	330	—		$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	150	—		$f = 1.0MHz$
$C_{oss\ eff. (ER)}$	Effective Output Capacitance (Energy Related)	—	420	—		$V_{GS}=0V, V_{DS}= 0V \text{ to } 80V$ ⑥ See Fig. 11
$C_{oss\ eff. (TR)}$	Effective Output Capacitance (Time Related)	—	680	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑤

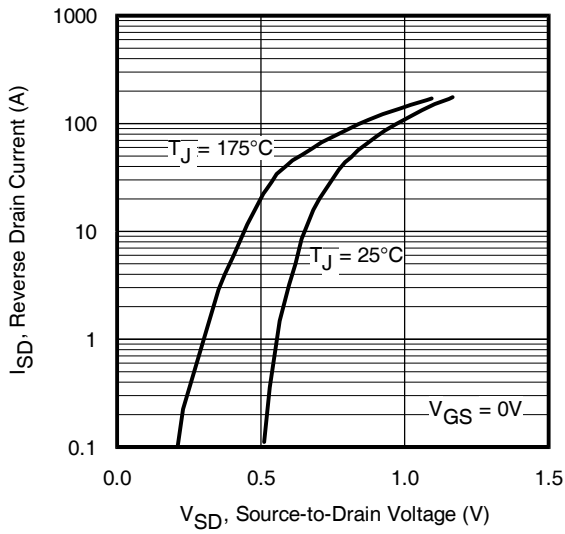
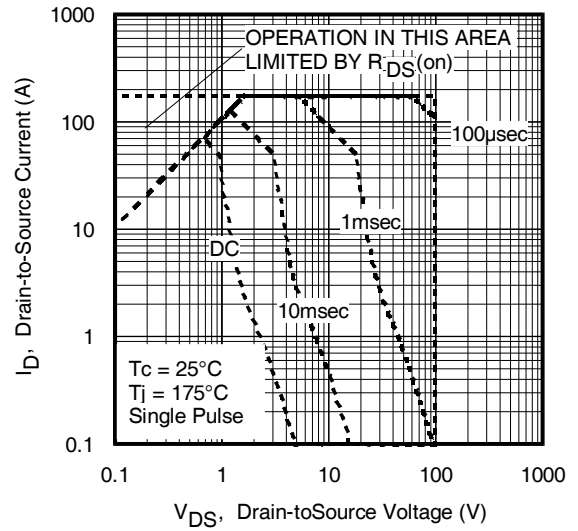
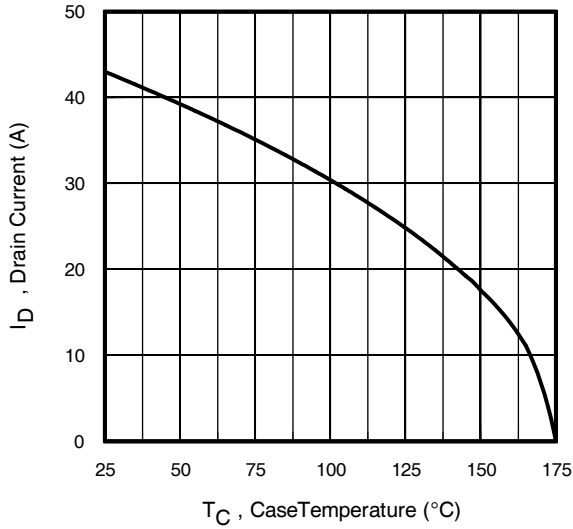
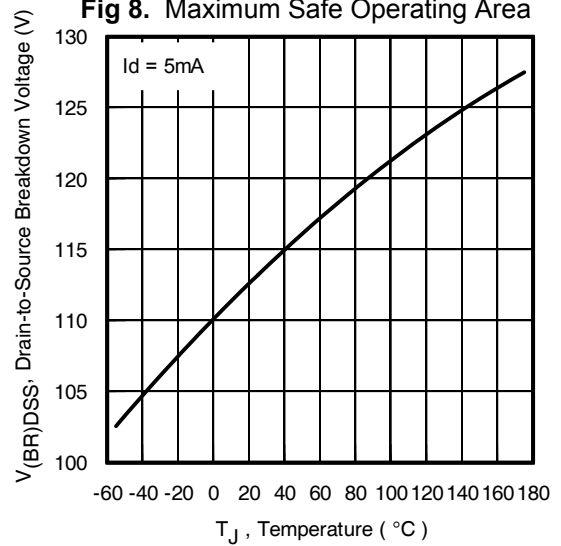
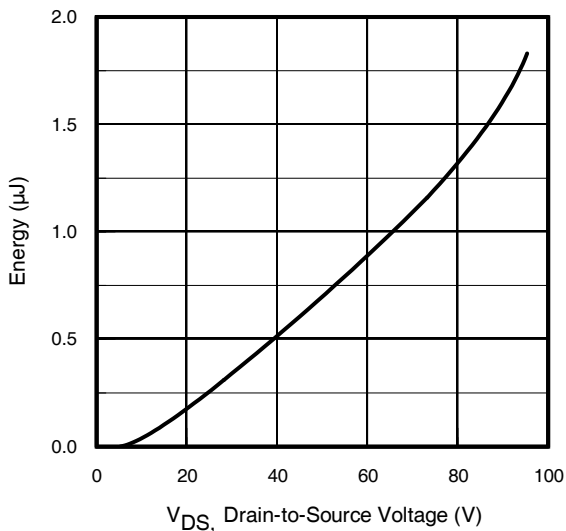
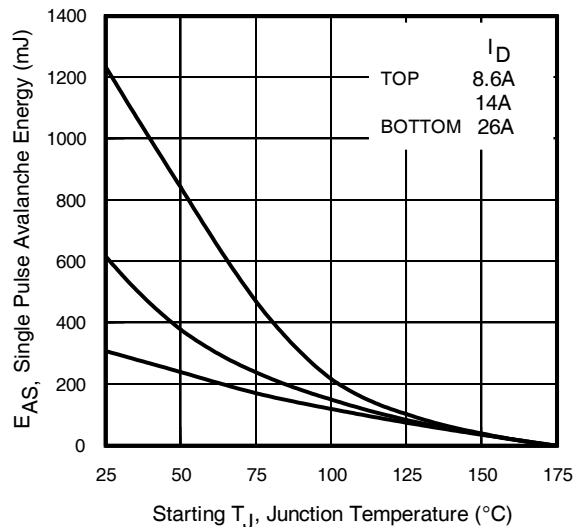
Source-Drain Ratings and Characteristics

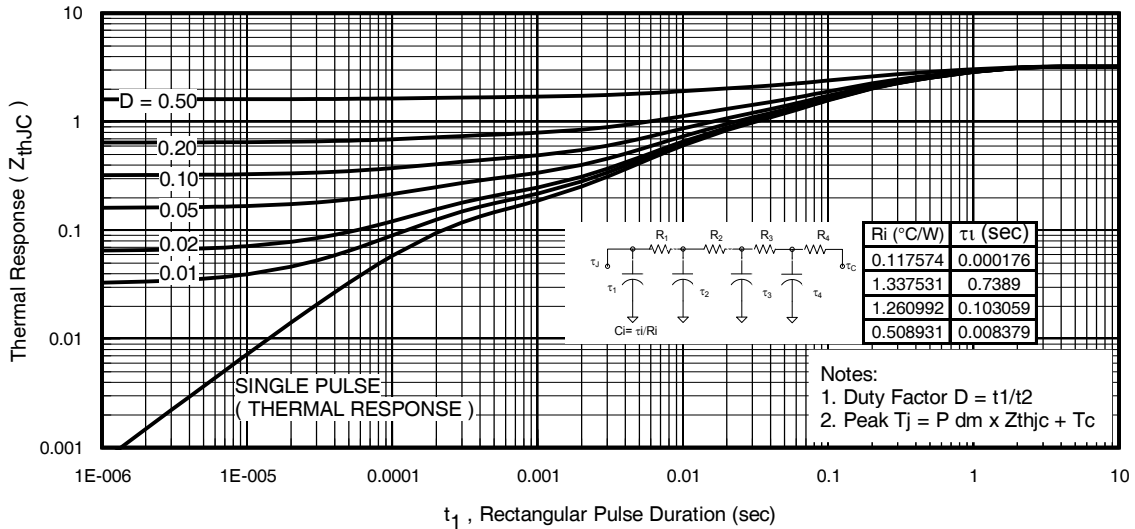
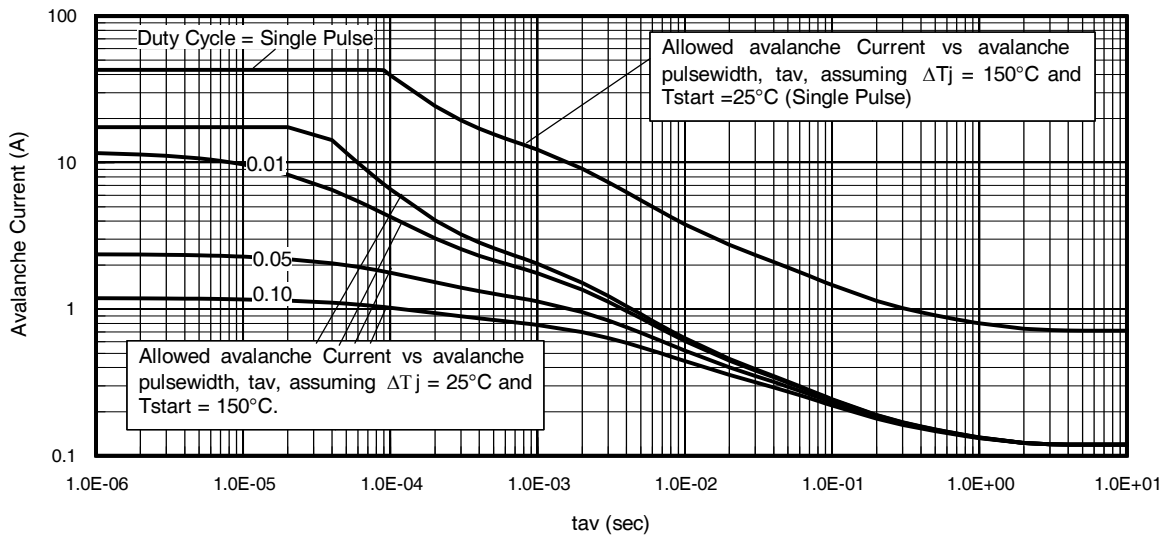
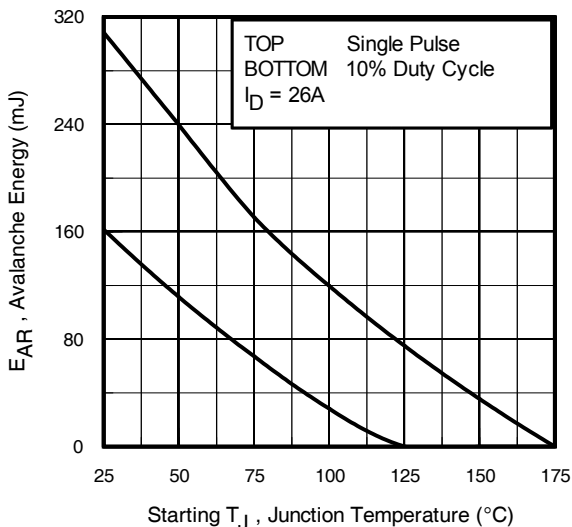
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	43	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	170		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 26A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	47	71	ns	$T_J = 25^\circ\text{C}$
		—	54	81		$T_J = 125^\circ\text{C}$
Q_{rr}	Reverse Recovery Charge	—	110	160	nC	$T_J = 25^\circ\text{C}$ — $V_R = 85V$
		—	140	210		$T_J = 125^\circ\text{C}$ — $I_F = 26A$
I_{RRM}	Reverse Recovery Current	—	2.5	—	A	$T_J = 25^\circ\text{C}$ — $di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.91mH$, $R_G = 25\Omega$, $I_{AS} = 26A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ③ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J approximately 90°C .
- ⑤ $C_{oss\ eff. (TR)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ $C_{oss\ eff. (ER)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

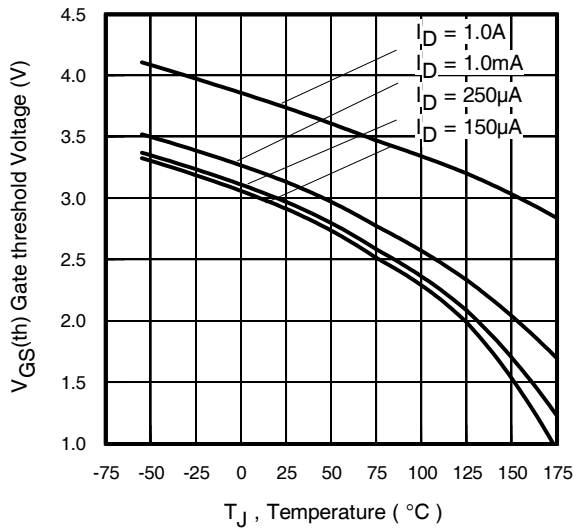
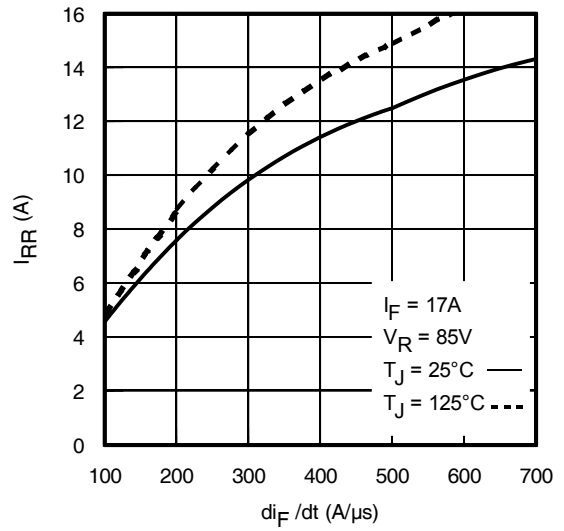
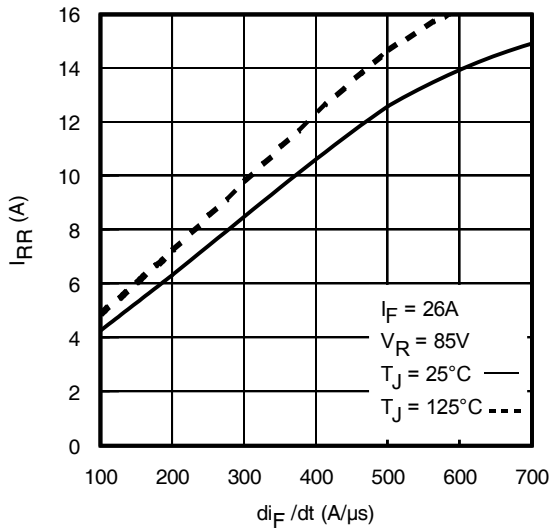
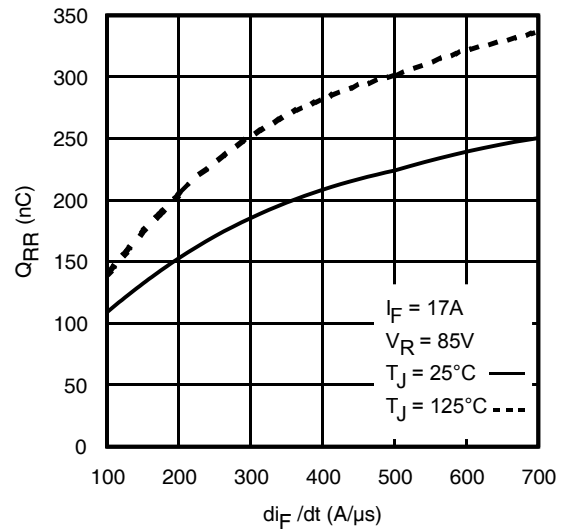
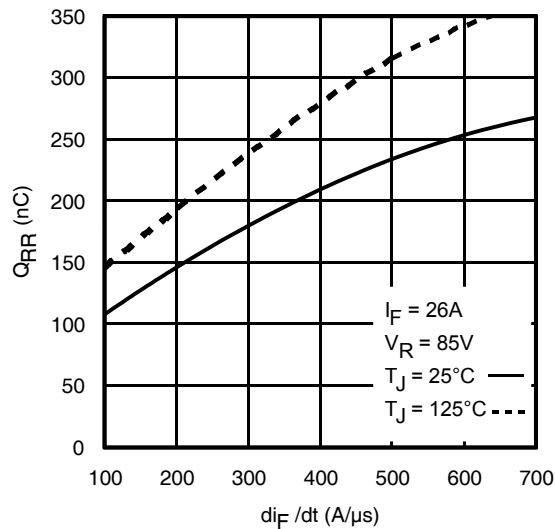

Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

Fig. 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig. 6. Typical Gate Charge vs. Gate-to-Source Voltage

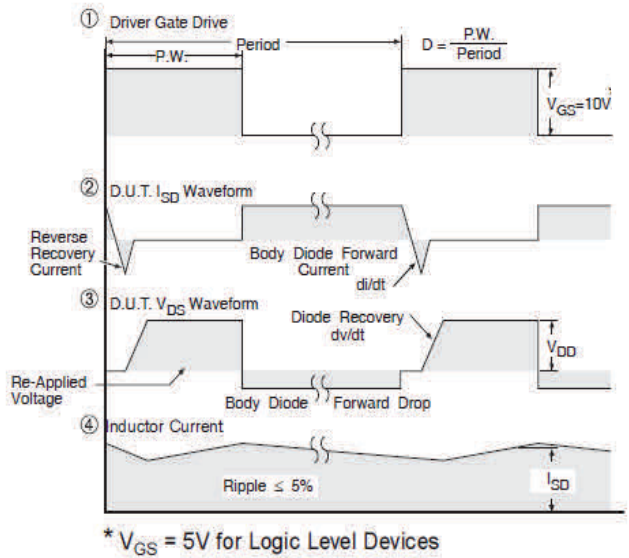
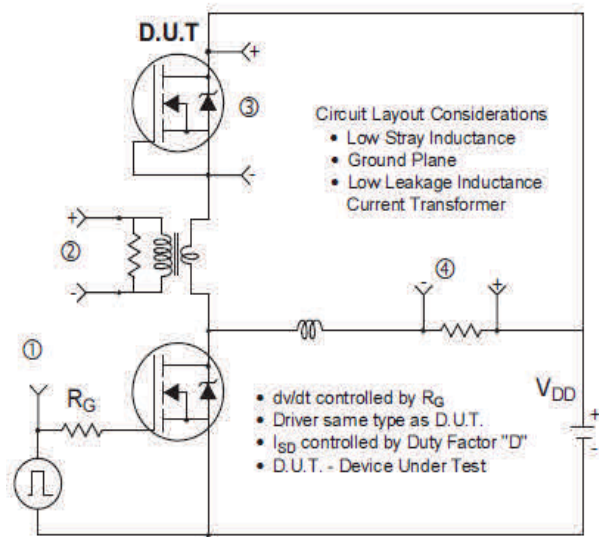
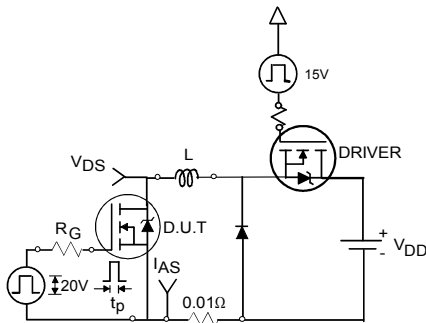
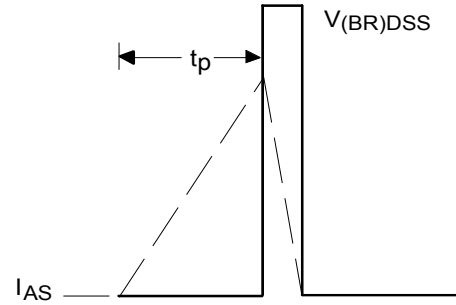
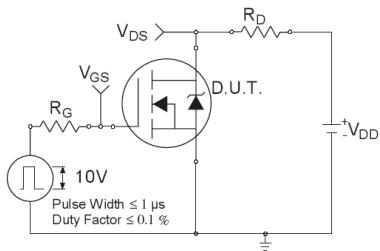
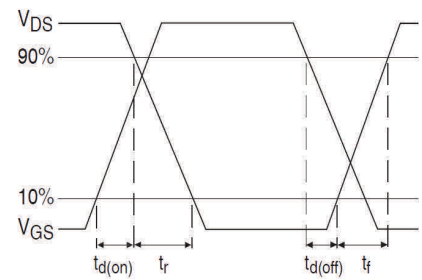
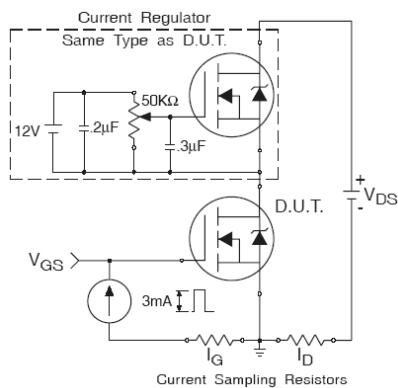
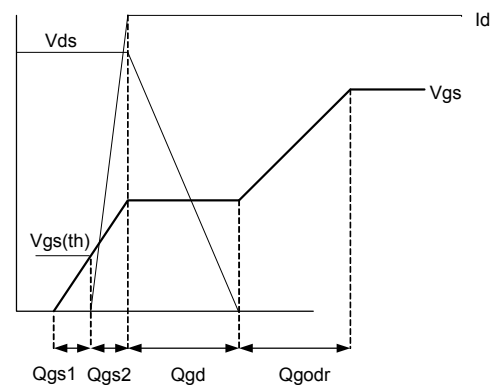

Fig. 7. Typical Source-to-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig. 9. Maximum Drain Current vs. Case Temperature

Fig 10. Drain-to-Source Breakdown Voltage

Fig. 11. Typical C_{OSS} Stored Energy

Fig 12. Maximum Avalanche Energy vs. Drain Current

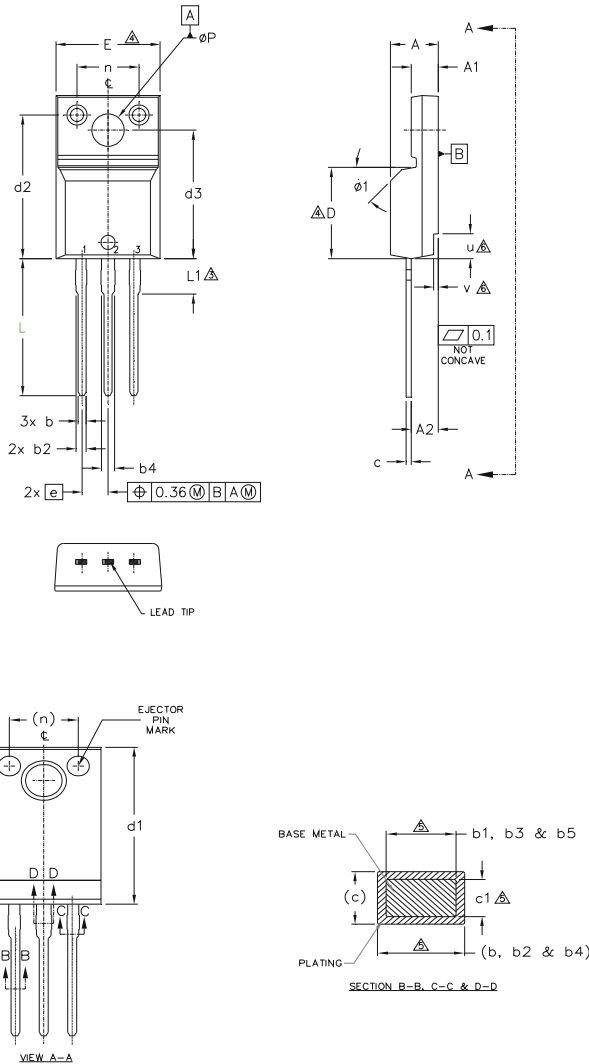

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Single Avalanche Event: Pulse Current vs. Pulse Width

Notes on Repetitive Avalanche Curves , Figures 14, 15: (For further info, see AN-1005 at www.infineon.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)
 $P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$

Fig 15. Maximum Avalanche Energy vs. Temperature


Fig 16. Threshold Voltage vs. Temperature

Fig 17. Typical Recovery Current vs. di_F/dt

Fig 18. Typical Recovery Current vs. di_F/dt

Fig 19. Typical Stored Charge vs. di_F/dt

Fig 20. Typical Stored Charge vs. di_F/dt


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 22a. Unclamped Inductive Test Circuit

Fig 22b. Unclamped Inductive Waveforms

Fig 23a. Switching Time Test Circuit

Fig 23b. Switching Time Waveforms

Fig 24a. Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform

TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

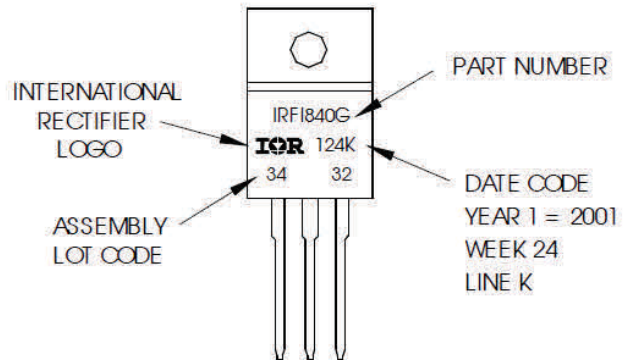
- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
- 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
- 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
- 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	LEAD ASSIGNMENTS HEXFET 1.- GATE 2.- DRAIN 3.- SOURCE
A1	2.57	2.82	.101	.111	
A2	2.51	2.92	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	
b2	0.76	1.27	.030	.050	
b3	0.76	1.22	.030	.048	
b4	1.02	1.52	.040	.060	
b5	1.02	1.47	.040	.058	
c	0.33	0.63	.013	.025	
c1	0.33	0.58	.013	.023	5
D	8.66	9.80	.341	.386	4
d1	15.80	16.13	.622	.635	IGBTs, CoPACK 1.- GATE 2.- COLLECTOR 3.- EMITTER
d2	13.97	14.22	.550	.560	
d3	12.29	12.93	.484	.509	
E	9.63	10.74	.379	.423	4
e	2.54 BSC		.100 BSC		
L	13.21	13.72	.520	.540	3
L1	3.10	3.68	.122	.145	
n	6.05	6.60	.238	.260	6
phi P	3.05	3.45	.120	.136	
u	2.39	2.49	.094	.098	6
v	0.41	0.51	.016	.020	
phi 1	-	45°	-	45°	

TO-220 Full-Pak Part Marking Information

EXAMPLE: THIS IS AN IRFI840G
WITH ASSEMBLY
LOT CODE 3432
ASSEMBLED ON WW 24, 2001
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to website at <http://www.irf.com/package/>

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	TO-220 Full-Pak	N/A
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
04/27/2017	<ul style="list-style-type: none"> Changed datasheet with Infineon logo - all pages. Corrected Package Outline on page 8. Corrected fig 19 & 20 –Y axis title from “A” to “nC” on page 6. Added disclaimer on last page.

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