



The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

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The MB9A110K Series are a highly integrated 32-bit microcontrollers dedicated for embedded controllers with high-performance and low cost.

These series are based on the ARM<sup>®</sup> Cortex<sup>®</sup>-M3 Processor with on-chip Flash memory and SRAM, and has peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (UART, CSIO, I<sup>2</sup>C, LIN).

The products which are described in this datasheet are placed into TYPE5 product categories in "FM3 Family Peripheral Manual".

## Features

### 32-bit ARM<sup>®</sup> Cortex<sup>®</sup>-M3 Core

- Processor version: r2p1
- Up to 40 MHz Frequency Operation
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 48 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

### On-chip Memories

#### [Flash memory]

This Series are based on two independent on-chip Flash memories.

- MainFlash
  - Up to 128 KB
  - Read cycle: 0 wait-cycle
  - Security function for code protection
- WorkFlash
  - 32 KB
  - Read cycle: 0 wait-cycle
  - Security function is shared with code protection

#### [SRAM]

This Series contain a total of up to 16 KB on-chip SRAM. This is composed of two independent SRAM (SRAM0, SRAM1). SRAM0 is connected to I-code bus and D-code bus of Cortex-M3 core. SRAM1 is connected to System bus.

- SRAM0: 8 KB
- SRAM1: 8 KB

### Multi-function Serial Interface (Max 4 channels)

- 2 channels with 16-steps × 9-bits FIFO (ch.0, ch.1), 2 channels without FIFO (ch.3, ch.5)
- Operation mode is selectable from the followings for each channel. (In ch.5, only UART and LIN are available.)
  - UART
  - CSIO
  - LIN
  - I<sup>2</sup>C

#### [UART]

- Full-duplex double buffer
- Selection with or without parity supported
- Built-in dedicated baud rate generator
- External clock available as a serial clock
- Hardware Flow control: Automatically control the transmission by CTS/RTS (only ch.4)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

#### [CSIO]

- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detect function available

**[LIN]**

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/Slave mode supported
- LIN break field generate (can be changed 13 to 16-bit length)
- LIN break delimiter generate (can be changed 1 to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

**[I<sup>2</sup>C]**

Standard mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

**DMA Controller (4 channels)**

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: byte/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

**A/D Converter (Max 8 channels)****[12-bit A/D Converter]**

- Successive Approximation Register type
- Built-in 2 unit
- Conversion time: 1.0 μs @ 5 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

**Base Timer (Max 8 channels)**

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

**General Purpose I/O Port**

This series can use its pins as General Purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up 36 fast General Purpose I/O Ports
- Some pin is 5 V tolerant I/O.  
See "Pin Description" to confirm the corresponding pins.

**Multi-function Timer**

The Multi-function timer is composed of the following blocks.

- 16-bit free-run timer × 3 ch.
- Input capture × 4 ch.
- Output compare × 6 ch.
- A/D activating compare × 3 ch.
- Waveform generator × 3 ch.
- 16-bit PPG timer × 3 ch.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

**Real-time clock (RTC)**

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

### Quadrature Position/Revolution Counter (QPRC)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

### Dual Timer (32/16-bit Down Counter)

The Dual Timer consists of two programmable 32/16-bit down counters. Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

### Watch Counter

The Watch counter is used for wake up from Low Power Consumption mode.

Interval timer: up to 64 s (Max) @ Sub Clock: 32.768 kHz

### External Interrupt Controller Unit

- Up to 6 external interrupt input pin
- Include one non-maskable interrupt (NMI)

### Watchdog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by low-speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power saving mode except RTC and STOP and Deep stand-by RTC and Deep stand-by STOP.

### CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

### Clock and Reset

#### [Clocks]

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main Clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- High-speed internal CR Clock: 4 MHz
- Low-speed internal CR Clock: 100 kHz
- Main PLL Clock

#### [Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low-voltage detector reset
- Clock supervisor reset

### Clock Super Visor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

### Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

### Low Power Consumption Mode

Six Low Power Consumption modes supported.

- SLEEP
- TIMER
- RTC
- STOP
- Deep stand-by RTC
- Deep stand-by STOP

### Debug

Serial Wire JTAG Debug Port (SWJ-DP)

### Power Supply

Wide range voltage: VCC = 2.7 V to 5.5 V

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## 1. Product Lineup

### Memory Size

| Product name         |           | MB9AF111K | MB9AF112K |
|----------------------|-----------|-----------|-----------|
| On-chip Flash memory | MainFlash | 64 KB     | 128 KB    |
|                      | WorkFlash | 32 KB     | 32 KB     |
| On-chip SRAM         | SRAM0     | 8 KB      | 8 KB      |
|                      | SRAM1     | 8 KB      | 8 KB      |
|                      | Total     | 16 KB     | 16 KB     |

### Function

| Product name   |                        | MB9AF111K<br>MB9AF112K   |
|--|------------------------|--|
| Pin count  |                        | 48/52  |
| CPU  | Freq.                  | Cortex-M3<br>40 MHz  |
| Power supply voltage range                                       |                        | 2.7 V to 5.5 V   |
| DMAC   |                        | 4 ch. (Max)  |
| Multi-function Serial Interface (UART/CSIO/LIN/I <sup>2</sup> C) |                        | 4 ch. (Max)<br>with 16-steps × 9-bits FIFO: ch.0, ch.1<br>without FIFO: ch.3, ch.5 (In ch.5, only UART and LIN are available.) |
| Base Timer (PWC/ Reload timer/PWM/PPG)                           |                        | 8 ch. (Max)  |
| MF-Timer   | A/D activation compare | 3 ch.  |
|  | Input capture          | 4 ch.  |
|  | Free-run timer         | 3 ch.  |
|  | Output compare         | 6 ch.  |
|  | Waveform generator     | 3 ch.  |
|  | PPG                    | 3 ch.  |
|  |                        | 1 unit (Max)   |
| QPRC   |                        | 1 ch. (Max)  |
| Dual Timer   |                        | 1 unit   |
| Real-time clock  |                        | 1 unit   |
| Watch Counter  |                        | 1 unit   |
| CRC Accelerator  |                        | Yes  |
| Watchdog timer   |                        | 1 ch. (SW) + 1 ch. (HW)  |
| External Interrupts  |                        | 6 pins (Max) + NMI × 1   |
| General Purpose I/O ports  |                        | 36 pins (Max)  |
| 12-bit A/D converter   |                        | 8 ch. (2 units)  |
| CSV (Clock Super Visor)  |                        | Yes  |
| LVD (Low-Voltage Detector)                                       |                        | 2 ch.  |
| Built-in OSC   | High-speed             | 4 MHz  |
|  | Low-speed              | 100 kHz  |
| Debug Function   |                        | SWJ-DP   |

#### Note:

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use. See "12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Internal CR Oscillation Characteristics" for accuracy of built-in CR.

## 2. Packages

| Package                      | Product name | MB9AF111K<br>MB9AF112K |
|------------------------------|--------------|------------------------|
| LQFP: LQA048 (0.5 mm pitch)  |              | ○                      |
| QFN: VNA048 (0.5 mm pitch)   |              | ○                      |
| LQFP: LQC052 (0.65 mm pitch) |              | ○                      |

○: Supported

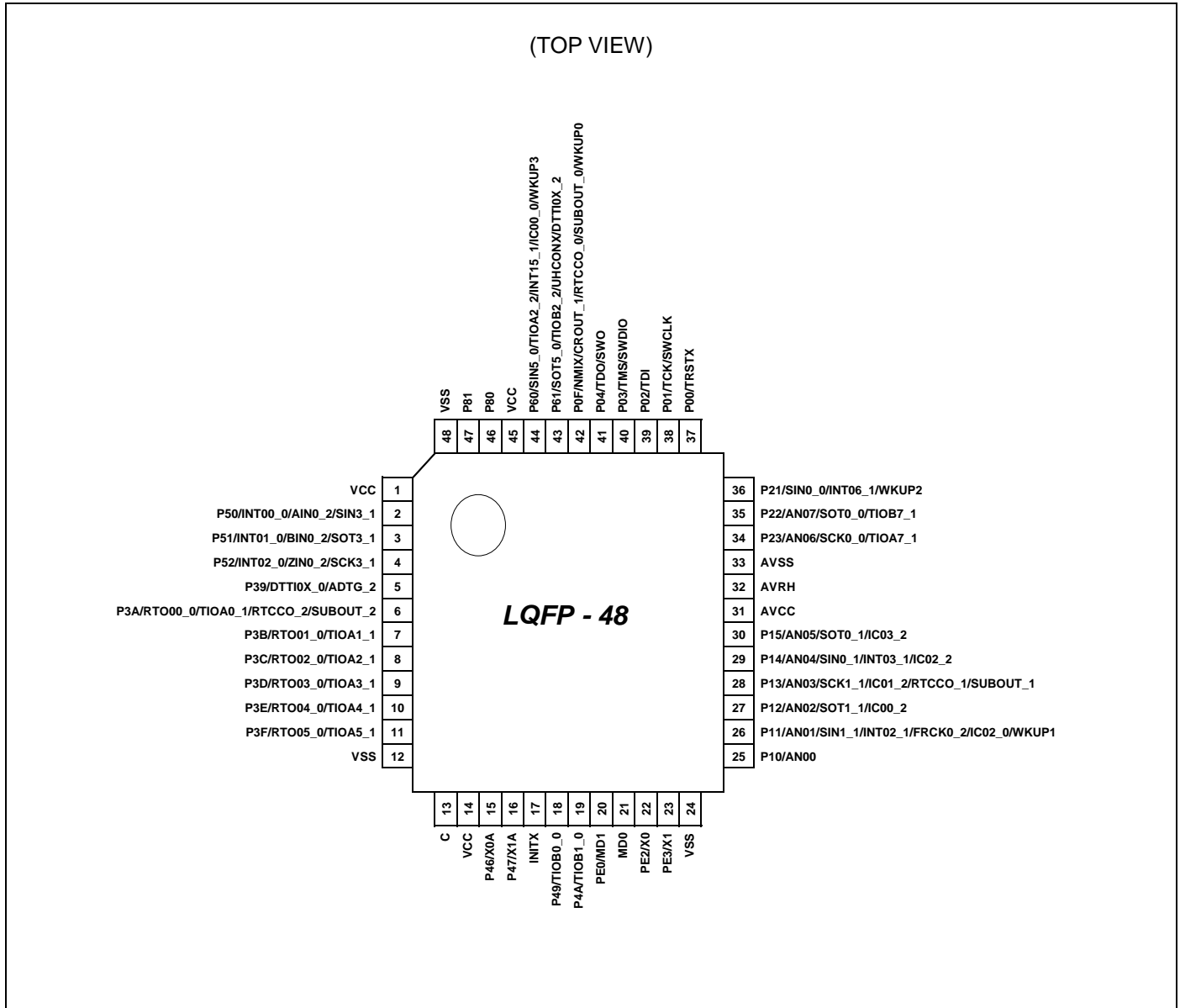
**Note:**

- See "14. Package Dimensions" for detailed information on each package.



### 3. Pin Assignment

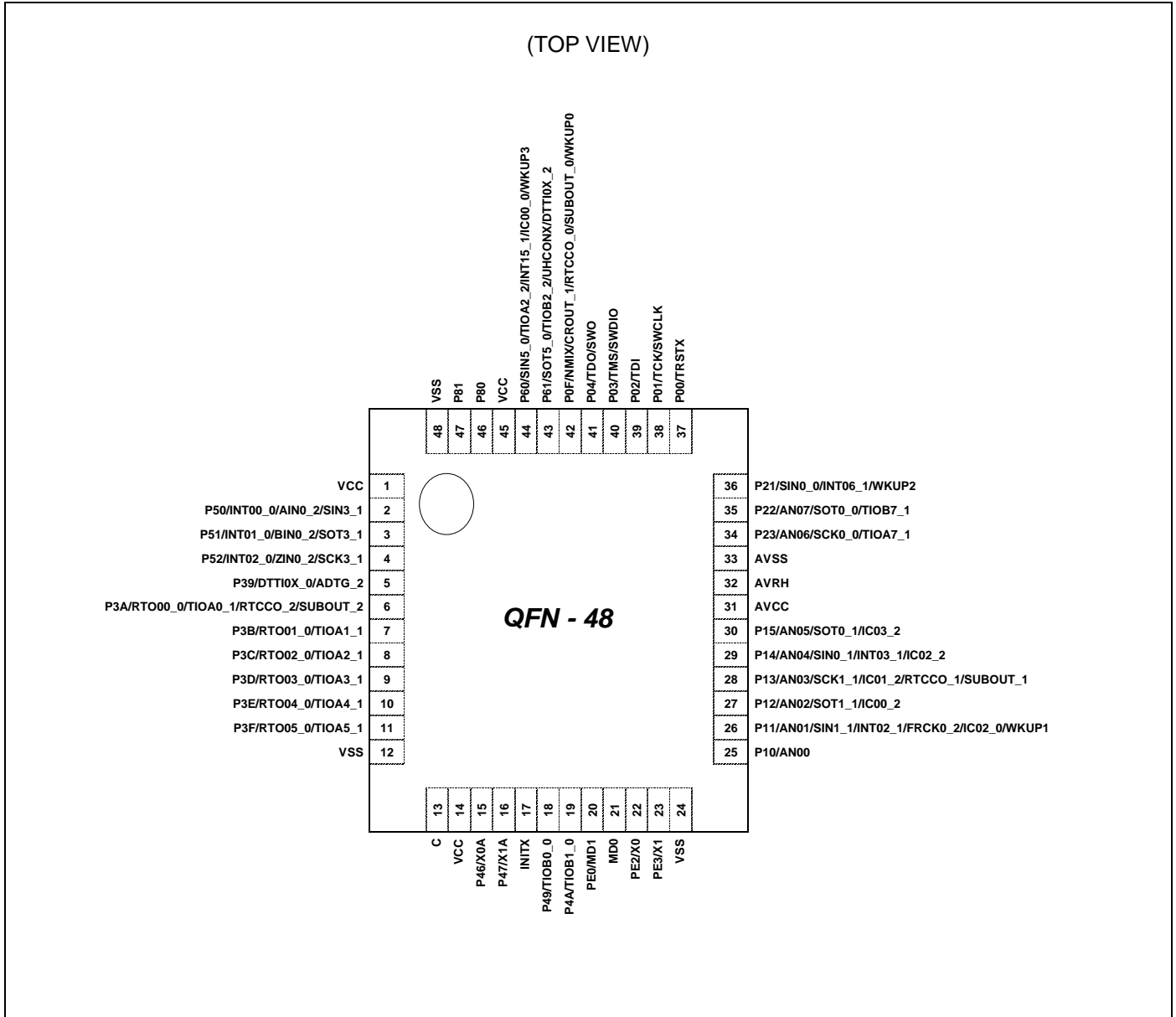
#### LQA048



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

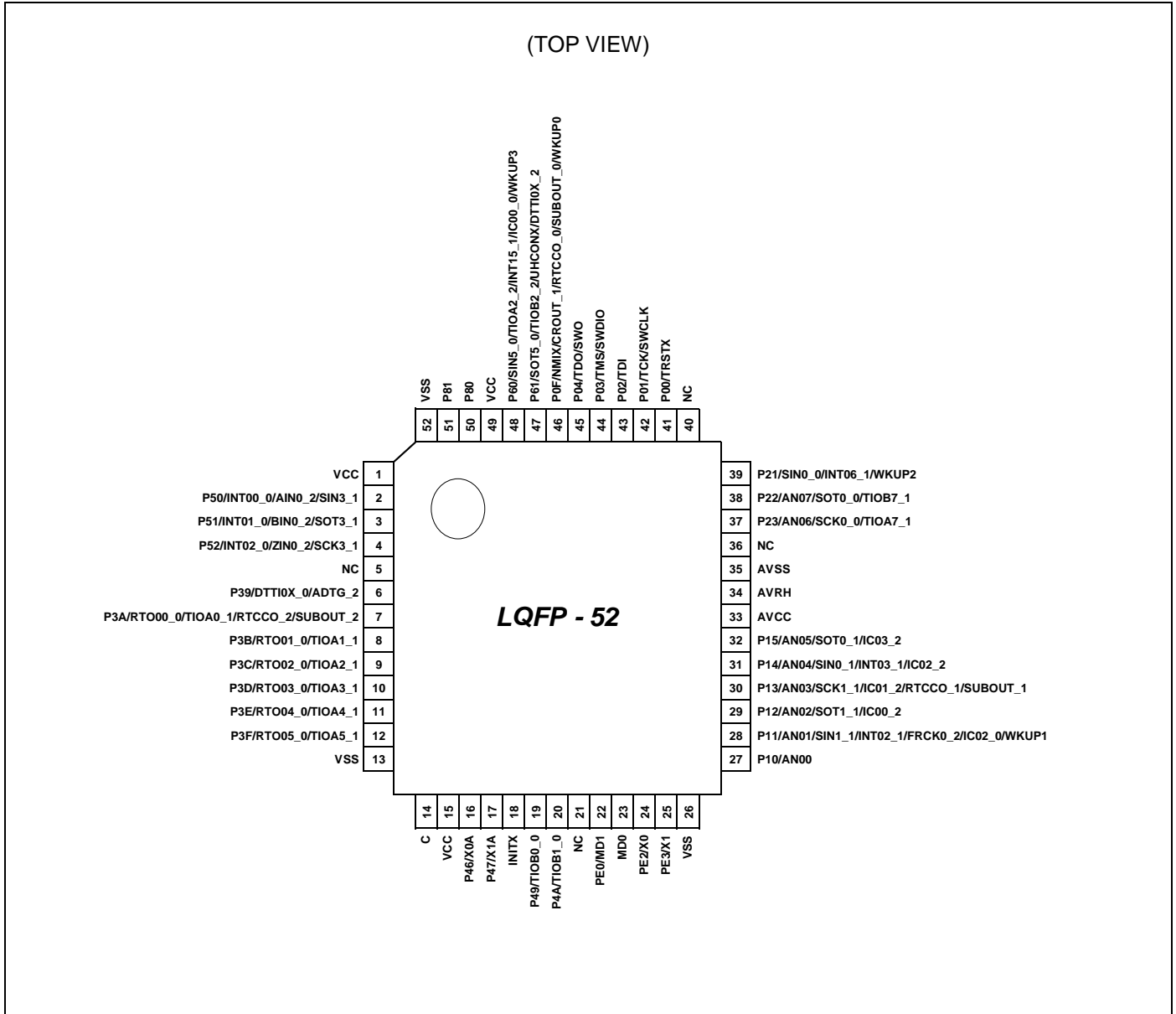
## VNA048



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

## LQC052



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

#### 4. List of Pin Functions

##### List of pin numbers

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

| Pin No            |         | Pin Name | I/O circuit type | Pin state type |
|-------------------|---------|----------|------------------|----------------|
| LQFP-48<br>QFN-48 | LQFP-52 |          |                  |                |
| 1                 | 1       | VCC      | -                |                |
| 2                 | 2       | P50      | I <sup>1</sup>   | H              |
|                   |         | INT00_0  |                  |                |
|                   |         | AIN0_2   |                  |                |
|                   |         | SIN3_1   |                  |                |
| 3                 | 3       | P51      | I <sup>1</sup>   | H              |
|                   |         | INT01_0  |                  |                |
|                   |         | BIN0_2   |                  |                |
|                   |         | SOT3_1   |                  |                |
| 4                 | 4       | P52      | I <sup>1</sup>   | H              |
|                   |         | INT02_0  |                  |                |
|                   |         | ZIN0_2   |                  |                |
|                   |         | SCK3_1   |                  |                |
| -                 | 5       | NC       | -                |                |
| 5                 | 6       | P39      | E                | I              |
|                   |         | DTTI0X_0 |                  |                |
|                   |         | ADTG_2   |                  |                |
| 6                 | 7       | P3A      | G                | I              |
|                   |         | RTO00_0  |                  |                |
|                   |         | TIOA0_1  |                  |                |
|                   |         | RTCCO_2  |                  |                |
|                   |         | SUBOUT_2 |                  |                |
| 7                 | 8       | P3B      | G                | I              |
|                   |         | RTO01_0  |                  |                |
|                   |         | TIOA1_1  |                  |                |
| 8                 | 9       | P3C      | G                | I              |
|                   |         | RTO02_0  |                  |                |
|                   |         | TIOA2_1  |                  |                |
| 9                 | 10      | P3D      | G                | I              |
|                   |         | RTO03_0  |                  |                |
|                   |         | TIOA3_1  |                  |                |
| 10                | 11      | P3E      | G                | I              |
|                   |         | RTO04_0  |                  |                |
|                   |         | TIOA4_1  |                  |                |

| Pin No            |         | Pin Name | I/O circuit type | Pin state type |
|-------------------|---------|----------|------------------|----------------|
| LQFP-48<br>QFN-48 | LQFP-52 |          |                  |                |
| 11                | 12      | P3F      | G                | I              |
|                   |         | RTO05_0  |                  |                |
|                   |         | TIOA5_1  |                  |                |
| 12                | 13      | VSS      | -                |                |
| 13                | 14      | C        | -                |                |
| 14                | 15      | VCC      | -                |                |
| 15                | 16      | P46      | D                | M              |
|                   |         | X0A      |                  |                |
| 16                | 17      | P47      | D                | N              |
|                   |         | X1A      |                  |                |
| 17                | 18      | INITX    | B                | C              |
| 18                | 19      | P49      | E                | I              |
|                   |         | TIOB0_0  |                  |                |
| 19                | 20      | P4A      | E                | I              |
|                   |         | TIOB1_0  |                  |                |
| -                 | 21      | NC       | -                |                |
| 20                | 22      | PE0      | C                | P              |
|                   |         | MD1      |                  |                |
| 21                | 23      | MD0      | J                | D              |
| 22                | 24      | PE2      | A                | A              |
|                   |         | X0       |                  |                |
| 23                | 25      | PE3      | A                | B              |
|                   |         | X1       |                  |                |
| 24                | 26      | VSS      | -                |                |
| 25                | 27      | P10      | F                | K              |
|                   |         | AN00     |                  |                |
| 26                | 28      | P11      | F                | F              |
|                   |         | AN01     |                  |                |
|                   |         | SIN1_1   |                  |                |
|                   |         | INT02_1  |                  |                |
|                   |         | FRCK0_2  |                  |                |
|                   |         | IC02_0   |                  |                |
| WKUP1             |         |          |                  |                |
| 27                | 29      | P12      | F                | K              |
|                   |         | AN02     |                  |                |
|                   |         | SOT1_1   |                  |                |
|                   |         | IC00_2   |                  |                |

| Pin No            |         | Pin Name | I/O circuit type | Pin state type |
|-------------------|---------|----------|------------------|----------------|
| LQFP-48<br>QFN-48 | LQFP-52 |          |                  |                |
| 28                | 30      | P13      | F                | K              |
|                   |         | AN03     |                  |                |
|                   |         | SCK1_1   |                  |                |
|                   |         | IC01_2   |                  |                |
|                   |         | RTCCO_1  |                  |                |
|                   |         | SUBOUT_1 |                  |                |
| 29                | 31      | P14      | F                | L              |
|                   |         | AN04     |                  |                |
|                   |         | SIN0_1   |                  |                |
|                   |         | INT03_1  |                  |                |
|                   |         | IC02_2   |                  |                |
| 30                | 32      | P15      | F                | K              |
|                   |         | AN05     |                  |                |
|                   |         | SOT0_1   |                  |                |
|                   |         | IC03_2   |                  |                |
| 31                | 33      | AVCC     | -                |                |
| 32                | 34      | AVRH     | -                |                |
| 33                | 35      | AVSS     | -                |                |
| -                 | 36      | NC       | -                |                |
| 34                | 37      | P23      | F                | K              |
|                   |         | AN06     |                  |                |
|                   |         | SCK0_0   |                  |                |
|                   |         | TIOA7_1  |                  |                |
| 35                | 38      | P22      | F                | K              |
|                   |         | AN07     |                  |                |
|                   |         | SOT0_0   |                  |                |
|                   |         | TIOB7_1  |                  |                |
| 36                | 39      | P21      | E                | G              |
|                   |         | SIN0_0   |                  |                |
|                   |         | INT06_1  |                  |                |
|                   |         | WKUP2    |                  |                |
| -                 | 40      | NC       | -                |                |
| 37                | 41      | P00      | E                | E              |
|                   |         | TRSTX    |                  |                |
| 38                | 42      | P01      | E                | E              |
|                   |         | TCK      |                  |                |
|                   |         | SWCLK    |                  |                |
| 39                | 43      | P02      | E                | E              |
|                   |         | TDI      |                  |                |
| 40                | 44      | P03      | E                | E              |
|                   |         | TMS      |                  |                |
|                   |         | SWDIO    |                  |                |
| 41                | 45      | P04      | E                | E              |
|                   |         | TDO      |                  |                |
|                   |         | SWO      |                  |                |

| Pin No            |         | Pin Name | I/O circuit type | Pin state type |
|-------------------|---------|----------|------------------|----------------|
| LQFP-48<br>QFN-48 | LQFP-52 |          |                  |                |
| 42                | 46      | P0F      | E                | J              |
|                   |         | NMIX     |                  |                |
|                   |         | CROUT_1  |                  |                |
|                   |         | RTCCO_0  |                  |                |
|                   |         | SUBOUT_0 |                  |                |
|                   |         | WKUP0    |                  |                |
| 43                | 47      | P61      | E                | I              |
|                   |         | SOT5_0   |                  |                |
|                   |         | TIOB2_2  |                  |                |
|                   |         | UHCONX   |                  |                |
|                   |         | DTTIOX_2 |                  |                |
| 44                | 48      | P60      | I <sup>(1)</sup> | G              |
|                   |         | SIN5_0   |                  |                |
|                   |         | TIOA2_2  |                  |                |
|                   |         | INT15_1  |                  |                |
|                   |         | IC00_0   |                  |                |
|                   |         | WKUP3    |                  |                |
| 45                | 49      | VCC      | -                |                |
| 46                | 50      | P80      | H                | O              |
| 47                | 51      | P81      | H                | O              |
| 48                | 52      | VSS      | -                |                |

\*1: 5 V tolerant I/O

**List of pin functions**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

| Module                | Pin name | Function   | Pin No            |         |
|-----------------------|----------|--|-------------------|---------|
|                       |          |  | LQFP-48<br>QFN-48 | LQFP-52 |
| ADC                   | ADTG_2   | A/D converter external trigger input pin                     | 5                 | 6       |
|                       | AN00     | A/D converter analog input pin.<br>ANxx describes ADC ch.xx. | 25                | 27      |
|                       | AN01     |  | 26                | 28      |
|                       | AN02     |  | 27                | 29      |
|                       | AN03     |  | 28                | 30      |
|                       | AN04     |  | 29                | 31      |
|                       | AN05     |  | 30                | 32      |
|                       | AN06     |  | 34                | 37      |
| AN07                  | 35       |  | 38                |         |
| Base Timer<br>0       | TIOA0_1  | Base timer ch.0 TIOA pin                                     | 6                 | 7       |
|                       | TIOB0_0  | Base timer ch.0 TIOB pin                                     | 18                | 19      |
| Base Timer<br>1       | TIOA1_1  | Base timer ch.1 TIOA pin                                     | 7                 | 8       |
|                       | TIOB1_0  | Base timer ch.1 TIOB pin                                     | 19                | 20      |
| Base Timer<br>2       | TIOA2_1  | Base timer ch.2 TIOA pin                                     | 8                 | 9       |
|                       | TIOA2_2  |  | 44                | 48      |
|                       | TIOB2_2  | Base timer ch.2 TIOB pin                                     | 43                | 47      |
| Base Timer<br>3       | TIOA3_1  | Base timer ch.3 TIOA pin                                     | 9                 | 10      |
| Base Timer<br>4       | TIOA4_1  | Base timer ch.4 TIOA pin                                     | 10                | 11      |
| Base Timer<br>5       | TIOA5_1  | Base timer ch.5 TIOA pin                                     | 11                | 12      |
| Base Timer<br>7       | TIOA7_1  | Base timer ch.7 TIOA pin                                     | 34                | 37      |
|                       | TIOB7_1  | Base timer ch.7 TIOB pin                                     | 35                | 38      |
| Debugger              | SWCLK    | Serial wire debug interface clock input pin                  | 38                | 42      |
|                       | SWDIO    | Serial wire debug interface data input/output pin            | 40                | 44      |
|                       | SWO      | Serial wire viewer output pin                                | 41                | 45      |
|                       | TCK      | JTAG test clock input pin                                    | 38                | 42      |
|                       | TDI      | JTAG test data input pin                                     | 39                | 43      |
|                       | TDO      | JTAG debug data output pin                                   | 41                | 45      |
|                       | TMS      | JTAG test mode state input/output pin                        | 40                | 44      |
|                       | TRSTX    | JTAG test reset Input pin                                    | 37                | 41      |
| External<br>Interrupt | INT00_0  | External interrupt request 00 input pin                      | 2                 | 2       |
|                       | INT01_0  | External interrupt request 01 input pin                      | 3                 | 3       |
|                       | INT02_0  | External interrupt request 02 input pin                      | 4                 | 4       |
|                       | INT02_1  |  | 26                | 28      |
|                       | INT03_1  | External interrupt request 03 input pin                      | 29                | 31      |
|                       | INT06_1  | External interrupt request 06 input pin                      | 36                | 39      |
|                       | INT15_1  | External interrupt request 15 input pin                      | 44                | 48      |
|                       | NMIX     | Non-Maskable Interrupt input pin                             | 42                | 46      |



| Module | Pin name | Function                   | Pin No            |         |
|--------|----------|----------------------------|-------------------|---------|
|        |          |                            | LQFP-48<br>QFN-48 | LQFP-52 |
| GPIO   | P00      | General-purpose I/O port 0 | 37                | 41      |
|        | P01      |                            | 38                | 42      |
|        | P02      |                            | 39                | 43      |
|        | P03      |                            | 40                | 44      |
|        | P04      |                            | 41                | 45      |
|        | P0F      |                            | 42                | 46      |
|        | P10      | General-purpose I/O port 1 | 25                | 27      |
|        | P11      |                            | 26                | 28      |
|        | P12      |                            | 27                | 29      |
|        | P13      |                            | 28                | 30      |
|        | P14      |                            | 29                | 31      |
|        | P15      |                            | 30                | 32      |
|        | P21      | General-purpose I/O port 2 | 36                | 39      |
|        | P22      |                            | 35                | 38      |
|        | P23      |                            | 34                | 37      |
|        | P39      | General-purpose I/O port 3 | 5                 | 6       |
|        | P3A      |                            | 6                 | 7       |
|        | P3B      |                            | 7                 | 8       |
|        | P3C      |                            | 8                 | 9       |
|        | P3D      |                            | 9                 | 10      |
|        | P3E      |                            | 10                | 11      |
|        | P3F      |                            | 11                | 12      |
|        | P46      |                            | 15                | 16      |
|        | P47      | General-purpose I/O port 4 | 16                | 17      |
|        | P49      |                            | 18                | 19      |
|        | P4A      |                            | 19                | 20      |
|        | P50      | General-purpose I/O port 5 | 2                 | 2       |
|        | P51      |                            | 3                 | 3       |
|        | P52      |                            | 4                 | 4       |
|        | P60      | General-purpose I/O port 6 | 44                | 48      |
|        | P61      |                            | 43                | 47      |
|        | P80      | General-purpose I/O port 8 | 46                | 50      |
|        | P81      |                            | 47                | 51      |
|        | PE0      | General-purpose I/O port E | 20                | 22      |
|        | PE2      |                            | 22                | 24      |
|        | PE3      |                            | 23                | 25      |

| Module                         | Pin name  | Function  | Pin No.           |         |
|--------------------------------|---|---|-------------------|---------|
|                                |   |   | LQFP-48<br>QFN-48 | LQFP-52 |
| Multi- function<br>Serial<br>0 | SIN0_0  | Multi-function serial interface ch.0 input pin  | 36                | 39      |
|                                | SIN0_1  |   | 29                | 31      |
|                                | SOT0_0<br>(SDA0_0)  | Multi-function serial interface ch.0 output pin.<br>This pin operates as SOT0 when it is used in a<br>UART/CSIO/LIN (operation modes<br>0 to 3) and as SDA0 when it is used in an I <sup>2</sup> C (operation<br>mode 4). | 35                | 38      |
|                                | SOT0_1<br>(SDA0_1)  |   | 30                | 32      |
| SCK0_0<br>(SCL0_0)             | Multi-function serial interface ch.0 clock I/O pin.<br>This pin operates as SCK0 when it is used in a CSIO<br>(operation modes 2) and as SCL0 when it is used in an<br>I <sup>2</sup> C (operation mode 4). | 34  | 37                |         |
| Multi- function<br>Serial<br>1 | SIN1_1  | Multi-function serial interface ch.1 input pin  | 26                | 28      |
|                                | SOT1_1<br>(SDA1_1)  | Multi-function serial interface ch.1 output pin.<br>This pin operates as SOT1 when it is used in a<br>UART/CSIO/LIN (operation modes<br>0 to 3) and as SDA1 when it is used in an I <sup>2</sup> C (operation<br>mode 4). | 27                | 29      |
|                                | SCK1_1<br>(SCL1_1)  | Multi-function serial interface ch.1 clock I/O pin.<br>This pin operates as SCK1 when it is used in a CSIO<br>(operation modes 2) and as SCL1 when it is used in an<br>I <sup>2</sup> C (operation mode 4).               | 28                | 30      |
| Multi- function<br>Serial<br>3 | SIN3_1  | Multi-function serial interface ch.3 input pin  | 2                 | 2       |
|                                | SOT3_1<br>(SDA3_1)  | Multi-function serial interface ch.3 output pin.<br>This pin operates as SOT3 when it is used in a<br>UART/CSIO/LIN (operation modes<br>0 to 3) and as SDA3 when it is used in an I <sup>2</sup> C (operation<br>mode 4). | 3                 | 3       |
|                                | SCK3_1<br>(SCL3_1)  | Multi-function serial interface ch.3 clock I/O pin.<br>This pin operates as SCK3 when it is used in a CSIO<br>(operation modes 2) and as SCL3 when it is used in an<br>I <sup>2</sup> C (operation mode 4).               | 4                 | 4       |
| Multi- function<br>Serial<br>5 | SIN5_0  | Multi-function serial interface ch.5 input pin  | 44                | 48      |
|                                | SOT5_0  | Multi-function serial interface ch.5 output pin.<br>This pin operates as SOT5 when it is used in a<br>UART/LIN (operation modes 0, 1, 3).   | 43                | 47      |

| Module                        | Pin name  | Function  | Pin No            |         |
|-------------------------------|---|---|-------------------|---------|
|                               |   |   | LQFP-48<br>QFN-48 | LQFP-52 |
| Multi- function<br>Timer<br>0 | DTTI0X_0  | Input signal controlling wave form generator outputs RTO00 to RTO05 of multi-function timer 0.                                | 5                 | 6       |
|                               | DTTI0X_2  |   | 43                | 47      |
|                               | FRCK0_2   | 16-bit free-run timer ch.0 external clock input pin   | 26                | 28      |
|                               | IC00_0  | 16-bit input capture ch.0 input pin of multi-function timer 0.<br>ICxx describes channel number.                              | 44                | 48      |
|                               | IC00_2  |   | 27                | 29      |
|                               | IC01_2  |   | 28                | 30      |
|                               | IC02_0  |   | 26                | 28      |
|                               | IC02_2  |   | 29                | 31      |
|                               | IC03_2  |   | 30                | 32      |
|                               | RTO00_0<br>(PPG00_0)  | Wave form generator output pin of multi-function timer 0.<br>This pin operates as PPG00 when it is used in PPG0 output modes. | 6                 | 7       |
|                               | RTO01_0<br>(PPG00_0)  | Wave form generator output pin of multi-function timer 0.<br>This pin operates as PPG00 when it is used in PPG0 output modes. | 7                 | 8       |
|                               | RTO02_0<br>(PPG02_0)  | Wave form generator output pin of multi-function timer 0.<br>This pin operates as PPG02 when it is used in PPG0 output modes. | 8                 | 9       |
|                               | RTO03_0<br>(PPG02_0)  | Wave form generator output pin of multi-function timer 0.<br>This pin operates as PPG02 when it is used in PPG0 output modes. | 9                 | 10      |
|                               | RTO04_0<br>(PPG04_0)  | Wave form generator output pin of multi-function timer 0.<br>This pin operates as PPG04 when it is used in PPG0 output modes. | 10                | 11      |
| RTO05_0<br>(PPG04_0)          | Wave form generator output pin of multi-function timer 0.<br>This pin operates as PPG04 when it is used in PPG0 output modes. | 11  | 12                |         |

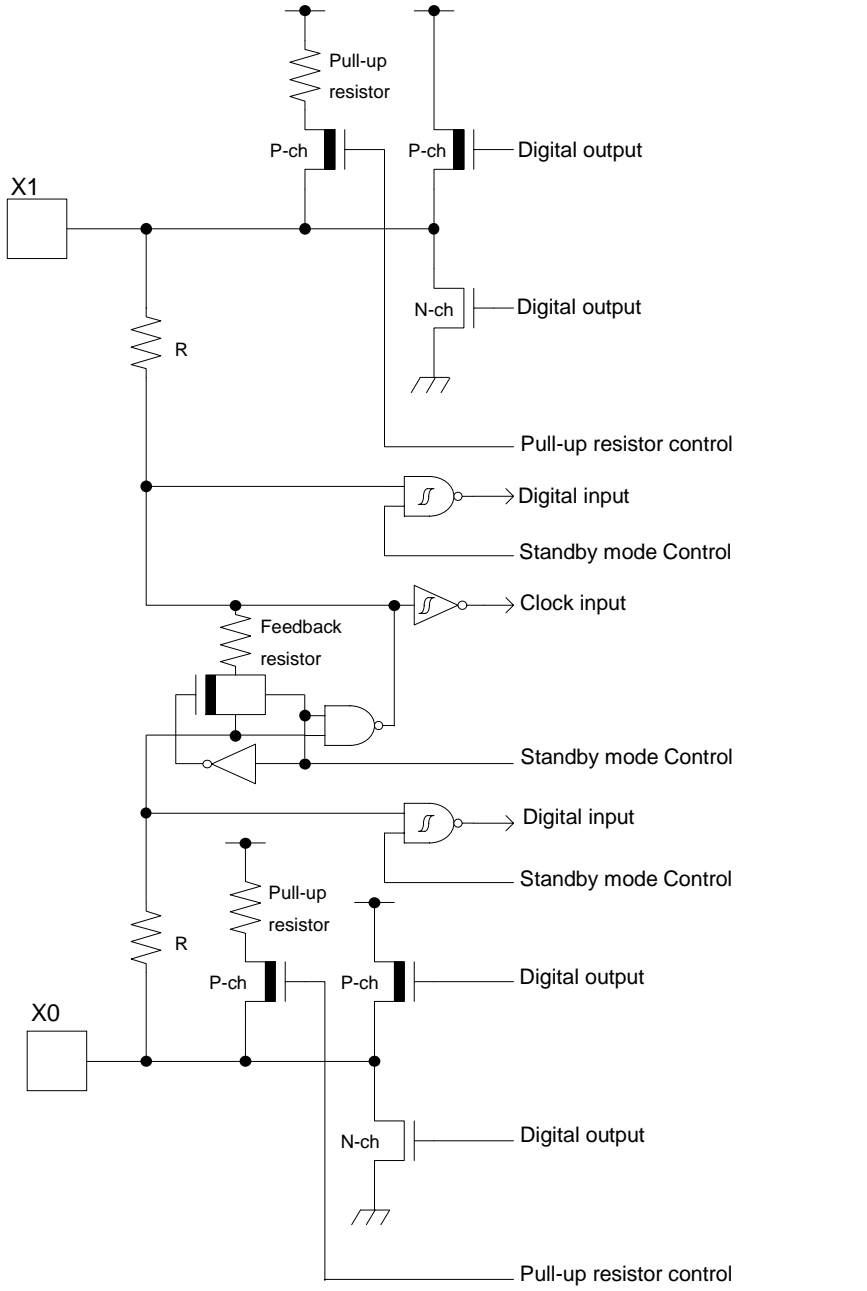
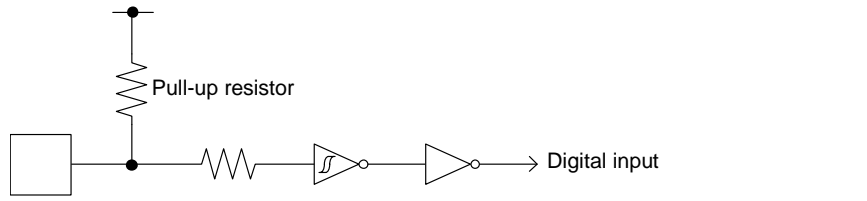
| Module  | Pin name | Function  | Pin No            |         |
|---|----------|---|-------------------|---------|
|   |          |   | LQFP-48<br>QFN-48 | LQFP-52 |
| Quadrature<br>Position/<br>Revolution<br>Counter<br>0 | AIN0_2   | QPRC ch.0 AIN input pin                             | 2                 | 2       |
|   | BIN0_2   | QPRC ch.0 BIN input pin                             | 3                 | 3       |
|   | ZIN0_2   | QPRC ch.0 ZIN input pin                             | 4                 | 4       |
| Real-time clock                                       | RTCCO_0  | 0.5 seconds pulse output pin of Real-time clock pin | 42                | 46      |
|   | RTCCO_1  |   | 28                | 30      |
|   | RTCCO_2  |   | 6                 | 7       |
|   | SUBOUT_0 | Sub clock output pin                                | 42                | 46      |
|   | SUBOUT_1 |   | 28                | 30      |
|   | SUBOUT_2 |   | 6                 | 7       |
| Low Power<br>Consumption<br>Mode                      | WKUP0    | Deep stand-by mode return signal input pin 0        | 42                | 46      |
|   | WKUP1    | Deep stand-by mode return signal input pin 1        | 26                | 28      |
|   | WKUP2    | Deep stand-by mode return signal input pin 2        | 36                | 39      |
|   | WKUP3    | Deep stand-by mode return signal input pin 3        | 44                | 48      |

| Module       | Pin name | Function  | Pin No            |         |
|--------------|----------|---|-------------------|---------|
|              |          |   | LQFP-48<br>QFN-48 | LQFP-52 |
| Reset        | INITX    | External Reset Input.<br>A reset is valid when INITX="L".   | 17                | 18      |
| Mode         | MD0      | Mode 0 pin.<br>During normal operation, MD0="L" must be input.<br>During serial programming to Flash memory, MD0="H" must be input. | 21                | 23      |
|              | MD1      | Mode 1 pin.<br>During serial programming to Flash memory, MD1="L" must be input.  | 20                | 22      |
| Power        | VCC      | Power supply Pin  | 1                 | 1       |
|              | VCC      | Power supply Pin  | 14                | 15      |
|              | VCC      | Power supply Pin  | 45                | 49      |
| GND          | VSS      | GND Pin   | 12                | 13      |
|              | VSS      | GND Pin   | 24                | 26      |
|              | VSS      | GND Pin   | 48                | 52      |
| Clock        | X0       | Main clock (oscillation) input pin  | 22                | 24      |
|              | X0A      | Sub clock (oscillation) input pin   | 15                | 16      |
|              | X1       | Main clock (oscillation) I/O pin  | 23                | 25      |
|              | X1A      | Sub clock (oscillation) I/O pin   | 16                | 17      |
|              | CROUT_1  | Built-in high-speed CR-osc clock output port  | 42                | 46      |
| Analog Power | AVCC     | A/D converter analog power pin  | 31                | 33      |
|              | AVRH     | A/D converter analog reference voltage input pin  | 32                | 34      |
| Analog GND   | AVSS     | A/D converter GND pin   | 33                | 35      |
| C pin        | C        | Power stabilization capacity pin  | 13                | 14      |
| NC pin       | NC       | NC pin.<br>NC pin should be kept open.  | -                 | 5       |
|              | NC       | NC pin.<br>NC pin should be kept open.  | -                 | 21      |
|              | NC       | NC pin.<br>NC pin should be kept open.  | -                 | 36      |
|              | NC       | NC pin.<br>NC pin should be kept open.  | -                 | 40      |

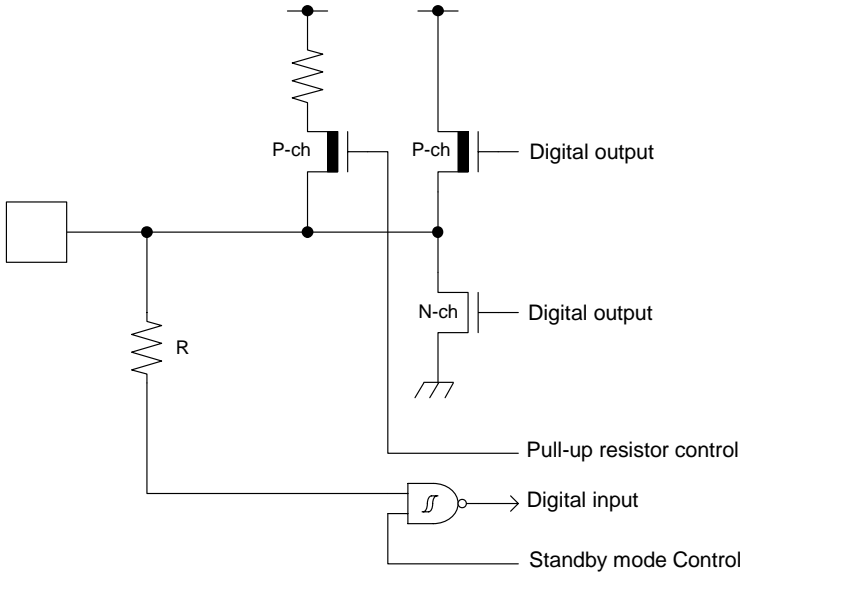
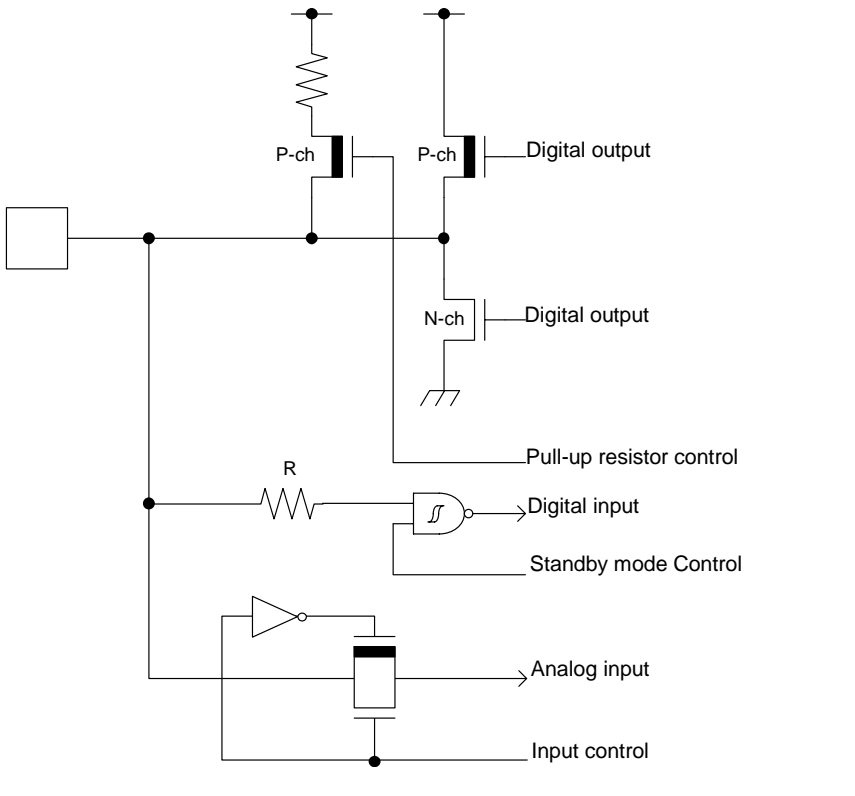
**Note:**

- While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.

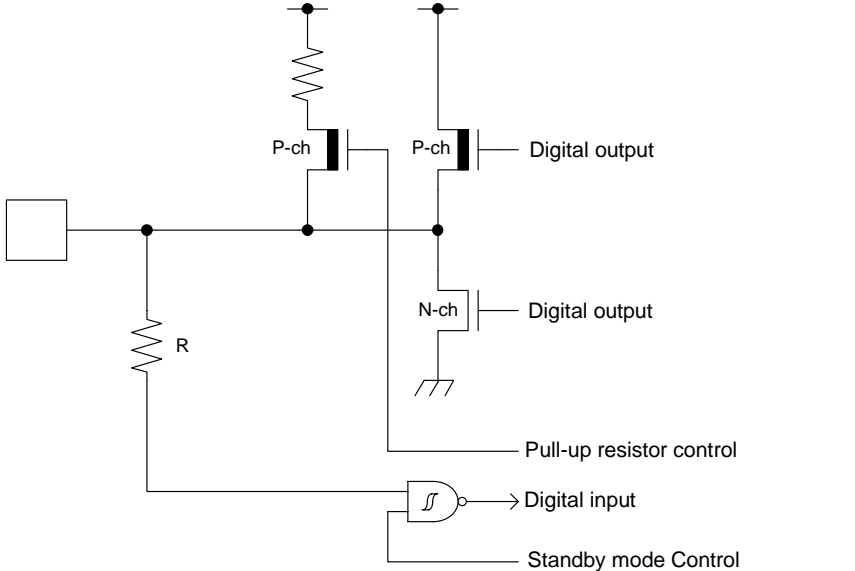
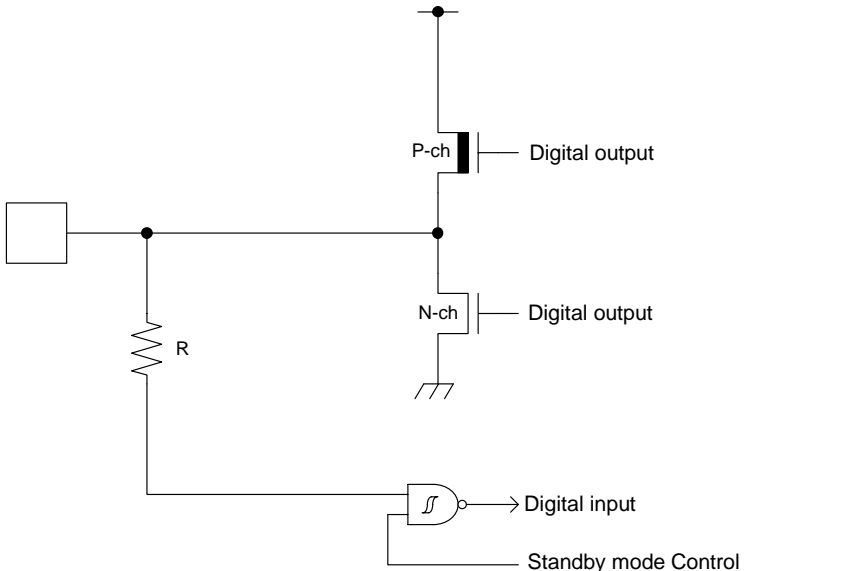
**5. I/O Circuit Type**

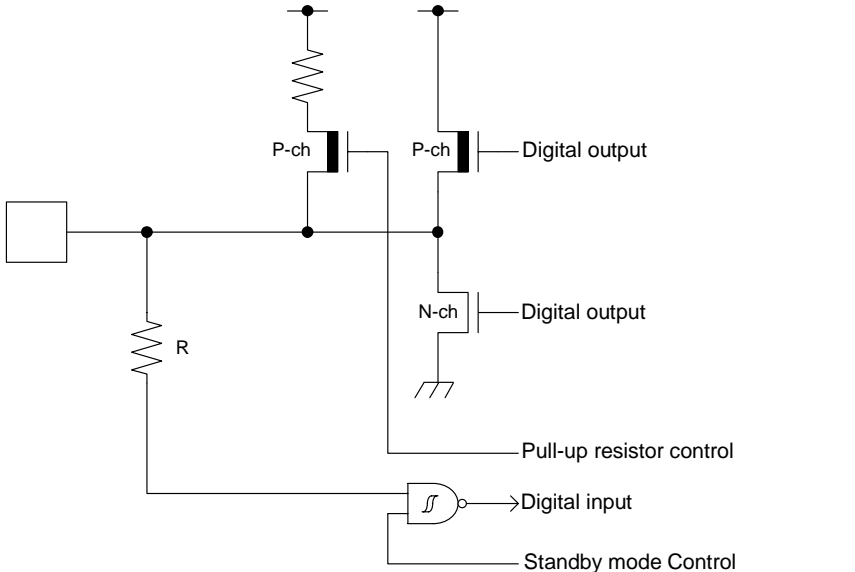
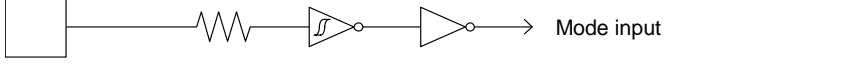
| Type | Circuit  | Remarks   |
|------|--|---|
| A    |   | <p>It is possible to select the main oscillation / GPIO function</p> <p>When the main oscillation is selected.</p> <ul style="list-style-type: none"> <li>- Oscillation feedback resistor : Approximately 1 MΩ</li> <li>- With Standby mode control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>- CMOS level output.</li> <li>- CMOS level hysteresis input</li> <li>- With pull-up resistor control</li> <li>- With standby mode control</li> <li>- Pull-up resistor : Approximately 50 kΩ</li> <li>- <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul> |
| B    |  | <ul style="list-style-type: none"> <li>- CMOS level hysteresis input</li> <li>- Pull-up resistor : Approximately 50 kΩ</li> </ul>   |

| Type | Circuit | Remarks   |
|------|---------|---|
| C    |         | <ul style="list-style-type: none"> <li>- Open drain output</li> <li>- CMOS level hysteresis input</li> </ul>  |
| D    |         | <p>It is possible to select the sub oscillation / GPIO function</p> <p>When the sub oscillation is selected.</p> <ul style="list-style-type: none"> <li>- Oscillation feedback resistor : Approximately 5 MΩ</li> <li>- With Standby mode control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>- CMOS level output.</li> <li>- CMOS level hysteresis input</li> <li>- With pull-up resistor control</li> <li>- With standby mode control</li> <li>- Pull-up resistor : Approximately 50 kΩ</li> <li>- <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> </ul> |

| Type | Circuit   | Remarks  |
|------|---|--|
| E    |   | <ul style="list-style-type: none"> <li>- CMOS level output</li> <li>- CMOS level hysteresis input</li> <li>- With pull-up resistor control</li> <li>- With standby mode control</li> <li>- Pull-up resistor : Approximately 50 kΩ</li> <li>- <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>- When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> <li>- +B input is available</li> </ul>   |
| F    |  | <ul style="list-style-type: none"> <li>- CMOS level output</li> <li>- CMOS level hysteresis input</li> <li>- With input control</li> <li>- Analog input</li> <li>- With pull-up resistor control</li> <li>- With standby mode control</li> <li>- Pull-up resistor : Approximately 50 kΩ</li> <li>- <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>- When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> <li>- +B input is available</li> </ul> |



| Type | Circuit  | Remarks  |
|------|--|--|
| G    |    | <ul style="list-style-type: none"> <li>- CMOS level output</li> <li>- CMOS level hysteresis input</li> <li>- With pull-up resistor control</li> <li>- With standby mode control</li> <li>- Pull-up resistor<br/>: Approximately 50 kΩ</li> <li>- <math>I_{OH} = -12 \text{ mA}</math>, <math>I_{OL} = 12 \text{ mA}</math></li> <li>- +B input is available</li> </ul> |
| H    |  | <ul style="list-style-type: none"> <li>- CMOS level output</li> <li>- CMOS level hysteresis input</li> <li>- With standby mode control</li> <li>- <math>I_{OH} = -20.5 \text{ mA}</math>, <math>I_{OL} = 18.5 \text{ mA}</math></li> </ul>   |

| Type | Circuit  | Remarks   |
|------|--|---|
| I    |  <p>The diagram shows a pull-up resistor R connected to a digital input signal. The input signal is also connected to the gates of two transistors: a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's source is connected to VDD and its drain is connected to the digital output. The N-ch MOSFET's source is connected to ground and its drain is connected to the digital output. A pull-up resistor control signal is connected to the gates of both transistors. A standby mode control signal is connected to the gates of both transistors through an inverter.</p> | <ul style="list-style-type: none"> <li>- CMOS level output</li> <li>- CMOS level hysteresis input</li> <li>- 5 V tolerant</li> <li>- With pull-up resistor control</li> <li>- With standby mode control</li> <li>- Pull-up resistor : Approximately 50 kΩ</li> <li>- <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>- Available to control of PZR registers.</li> </ul> |
| J    |  <p>The diagram shows a resistor connected to a mode input signal. The mode input signal is connected to the input of an inverter, which is then connected to the input of another inverter.</p>   | <p>CMOS level hysteresis input</p>  |

## 6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

### 6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

#### Absolute maximum ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

#### Recommended operating conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

#### Processing and protection of pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

#### Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

**CAUTION:** The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

#### Observance of safety regulations and standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

#### Fail-safe design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

**Precautions related to usage of devices**

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

**6.2 Precautions for Package Mounting**

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress recommended conditions. For detailed information about mount conditions, contact your sales representative.

**Lead insertion type**

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

**Surface mount type**

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

**Lead-free packaging**

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

**Storage of semiconductor devices**

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.  
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

**Baking**

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

**Static electricity**

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).  
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

**6.3 Precautions for Use Environment**

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity  
Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity  
When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil  
Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation  
Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame  
**CAUTION:** Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

## 7. Handling Devices

### Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1  $\mu\text{F}$  be connected as a bypass capacitor between each Power supply pins and GND pins, between AVCC pin and AVSS pin near this device.

### Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/ $\mu\text{s}$  when there is a momentary fluctuation on switching the power supply.

### Crystal oscillator circuit

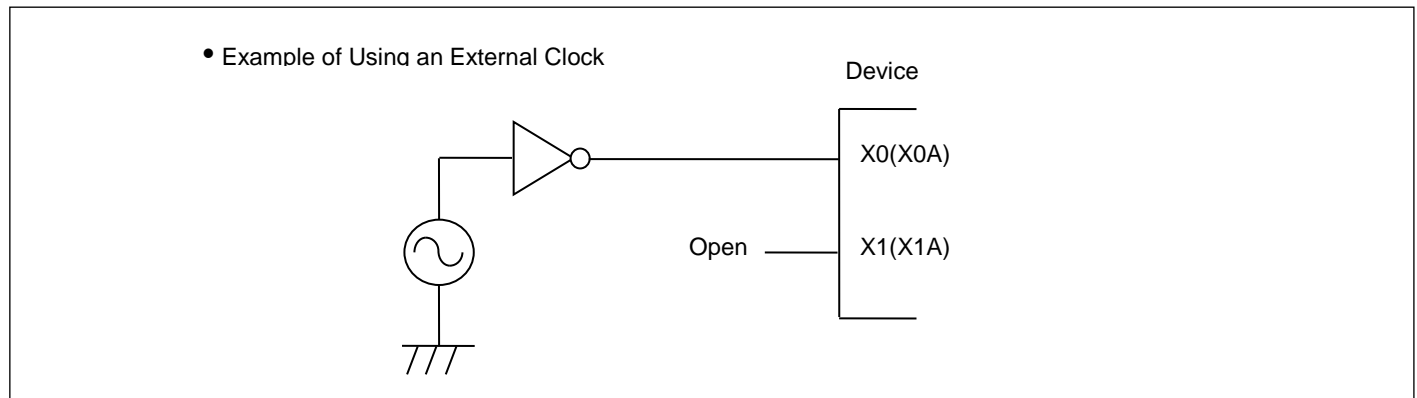
Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

### Using an external clock

When using an external clock, the clock signal should be input to the X0, X0A pin only and the X1, X1A pin should be kept open.

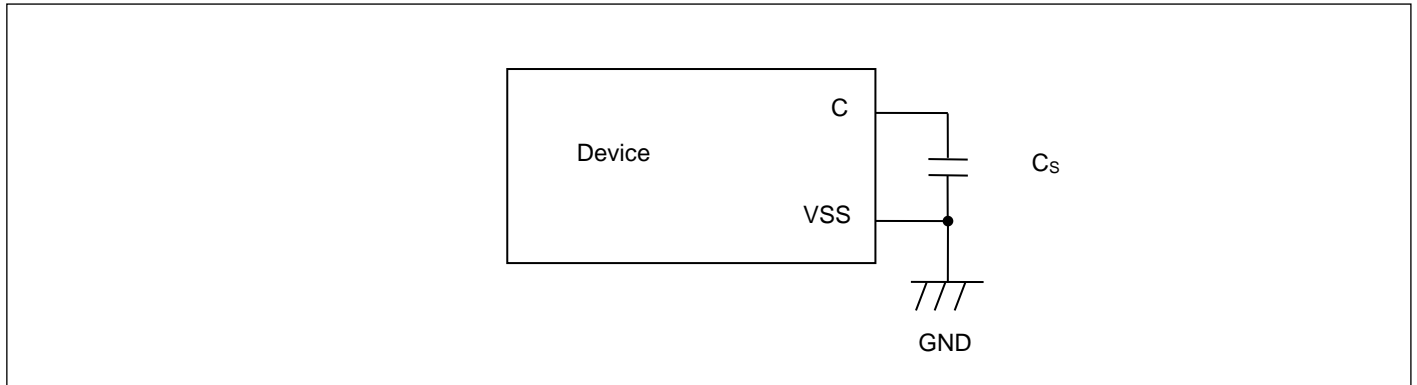


### Handling when using Multi-function serial pin as I<sup>2</sup>C pin

If it is using Multi-function serial pin as I<sup>2</sup>C pins, P-ch transistor of digital output is always disable. However, I<sup>2</sup>C pins need to keep the electrical characteristic like other pins and not to connect to external I<sup>2</sup>C bus system with power OFF.

## C pin

This series contains the regulator. Be sure to connect a smoothing capacitor ( $C_s$ ) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor. A smoothing capacitor of about 4.7  $\mu\text{F}$  would be recommended for this series.



## Mode pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

## NC pins

NC pin should be kept open.

## Notes on power-on

Turn power on/off in the following order or at the same time.  
If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on: VCC → AVCC → AVRH

Turning off: AVRH → AVCC → VCC

## Serial communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

## Differences in features among the products with different memory sizes and between Flash products and MASK products

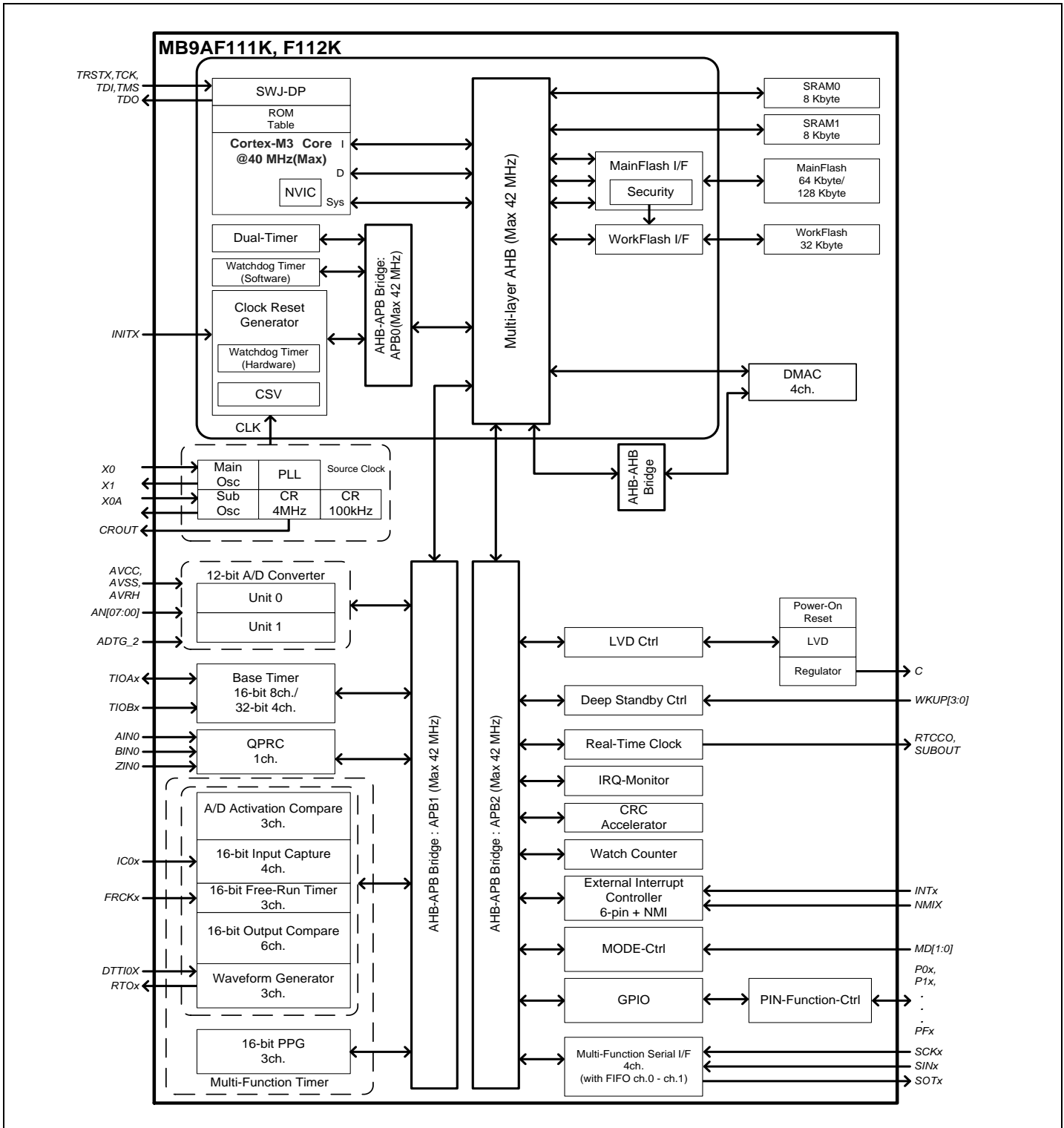
The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

## Pull-up function of 5 V tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

**8. Block Diagram**



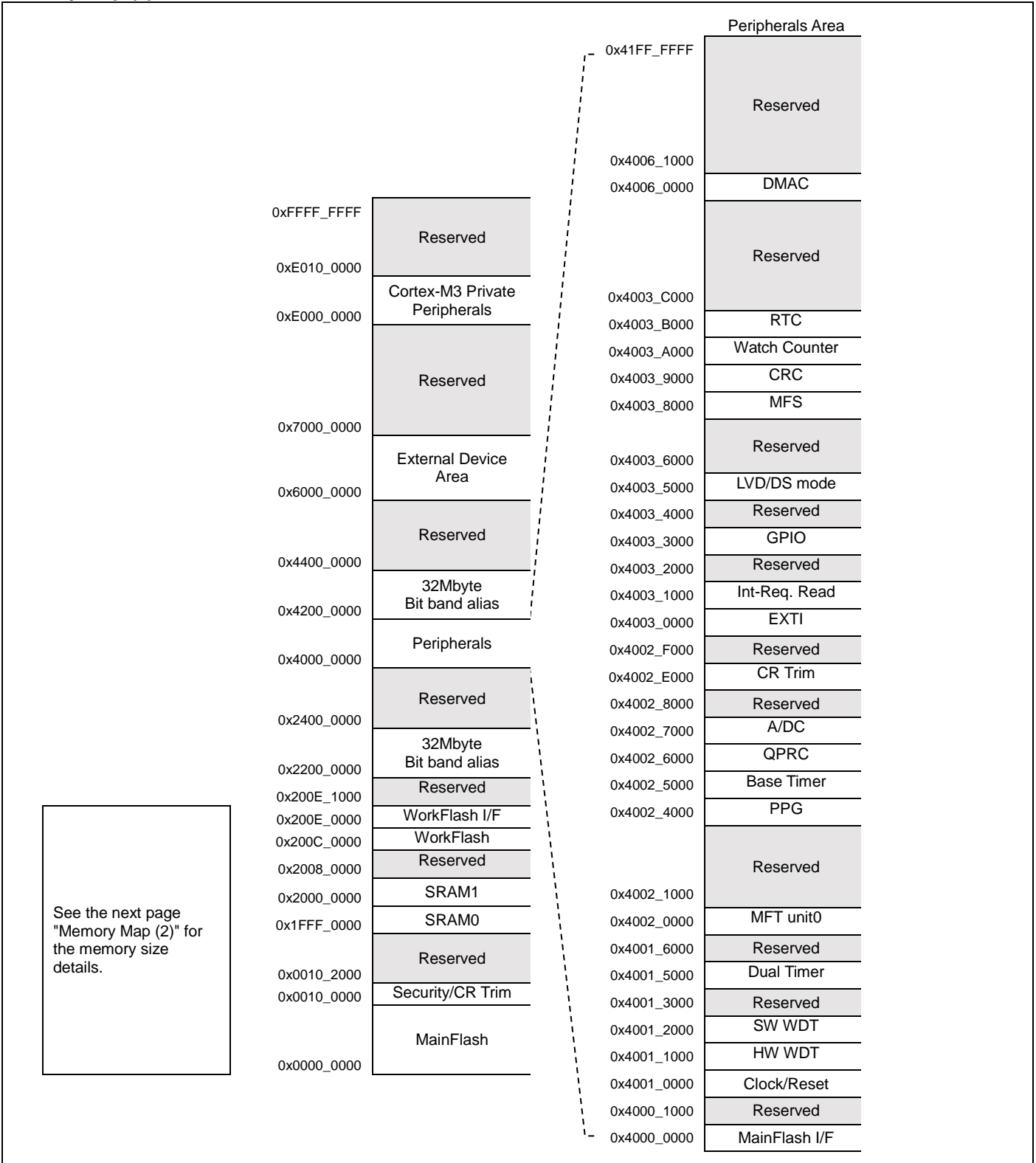
**9. Memory Size**

See “Memory size” in “1. Product Lineup” to confirm the memory size.

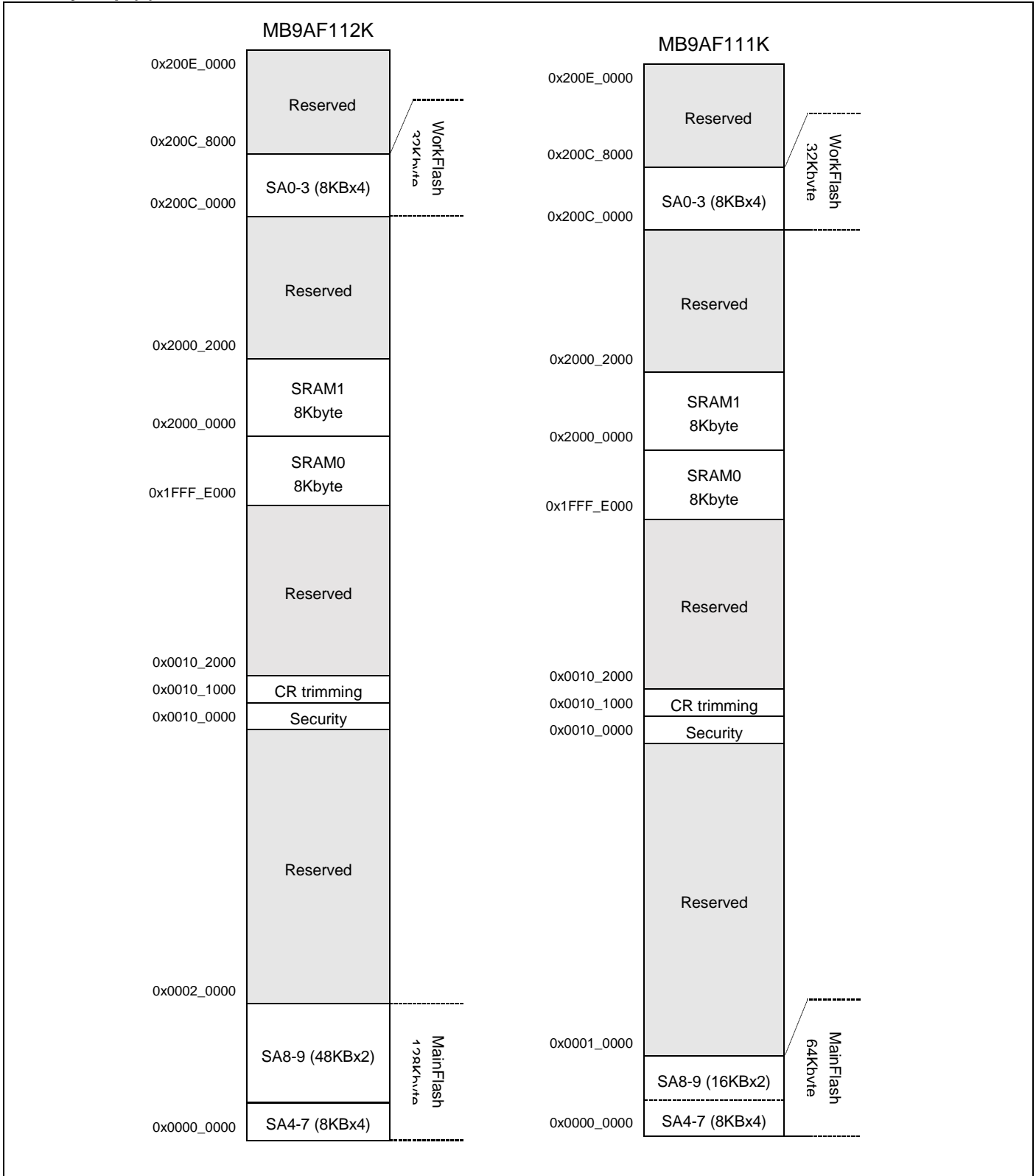


## 10. Memory Map

### Memory Map (1)



## Memory Map (2)



See "MB9A310K/110K Series Flash programming Manual" for sector structure of Flash.

**Peripheral Address Map**

| Start address | End address | Bus                                    | Peripherals                           |                               |
|---------------|-------------|--|---------------------------------------|-------------------------------|
| 0x4000_0000   | 0x4000_0FFF | AHB                                    | MainFlash I/F register                |                               |
| 0x4000_1000   | 0x4000_FFFF |  | Reserved                              |                               |
| 0x4001_0000   | 0x4001_0FFF | APB0                                   | Clock/Reset Control                   |                               |
| 0x4001_1000   | 0x4001_1FFF |  | Hardware Watchdog timer               |                               |
| 0x4001_2000   | 0x4001_2FFF |  | Software Watchdog timer               |                               |
| 0x4001_3000   | 0x4001_4FFF |  | Reserved                              |                               |
| 0x4001_5000   | 0x4001_5FFF |  | Dual-Timer                            |                               |
| 0x4001_6000   | 0x4001_FFFF |  | Reserved                              |                               |
| 0x4002_0000   | 0x4002_0FFF |  | APB1                                  | Multi-function timer unit0    |
| 0x4002_1000   | 0x4002_3FFF | Reserved                               |                                       |                               |
| 0x4002_4000   | 0x4002_4FFF | PPG                                    |                                       |                               |
| 0x4002_5000   | 0x4002_5FFF | Base Timer                             |                                       |                               |
| 0x4002_6000   | 0x4002_6FFF | Quadrature Position/Revolution Counter |                                       |                               |
| 0x4002_7000   | 0x4002_7FFF | A/D Converter                          |                                       |                               |
| 0x4002_8000   | 0x4002_DFFF | Reserved                               |                                       |                               |
| 0x4002_E000   | 0x4002_EFFF | Internal CR trimming                   |                                       |                               |
| 0x4002_F000   | 0x4002_FFFF | Reserved                               |                                       |                               |
| 0x4003_0000   | 0x4003_0FFF | APB2                                   |                                       | External Interrupt Controller |
| 0x4003_1000   | 0x4003_1FFF |  | Interrupt Request Batch-Read Function |                               |
| 0x4003_2000   | 0x4003_2FFF |  | Reserved                              |                               |
| 0x4003_3000   | 0x4003_3FFF |  | GPIO                                  |                               |
| 0x4003_4000   | 0x4003_4FFF |  | Reserved                              |                               |
| 0x4003_5000   | 0x4003_57FF |  | Low Voltage Detector                  |                               |
| 0x4003_5800   | 0x4003_5FFF |  | Deep stand-by mode Controller         |                               |
| 0x4003_6000   | 0x4003_7FFF |  | Reserved                              |                               |
| 0x4003_8000   | 0x4003_8FFF |  | Multi-function serial Interface       |                               |
| 0x4003_9000   | 0x4003_9FFF |  | CRC                                   |                               |
| 0x4003_A000   | 0x4003_AFFF |  | Watch Counter                         |                               |
| 0x4003_B000   | 0x4003_BFFF |  | Real-time clock                       |                               |
| 0x4003_C000   | 0x4003_FFFF |  | Reserved                              |                               |
| 0x4004_0000   | 0x4005_FFFF |  | AHB                                   | Reserved                      |
| 0x4006_0000   | 0x4006_0FFF |  |                                       | DMAC register                 |
| 0x4006_1000   | 0x41FF_FFFF | Reserved                               |                                       |                               |
| 0x200E_0000   | 0x200E_FFFF | WorkFlash I/F register                 |                                       |                               |

## 11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

■ **INITX=0**

This is the period when the INITX pin is the "L" level.

■ **INITX=1**

This is the period when the INITX pin is the "H" level.

■ **SPL=0**

This is the status that standby pin level setting bit (SPL) in standby mode control register (STB\_CTL) is set to "0".

■ **SPL=1**

This is the status that standby pin level setting bit (SPL) in standby mode control register (STB\_CTL) is set to "1".

■ **Input enabled**

Indicates that the input function can be used.

■ **Internal input fixed at "0"**

This is the status that the input function cannot be used. Internal input is fixed at "L".

■ **Hi-Z**

Indicates that the output drive transistor is disabled and the pin is put in the Hi-Z state.

■ **Setting disabled**

Indicates that the setting is disabled.

■ **Maintain previous state**

Maintains the state that was immediately prior to entering the current mode.

If a built-in peripheral function is operating, the output follows the peripheral function.  
If the pin is being used as a port, that output is maintained.

■ **Analog input is enabled**

Indicates that the analog input is enabled.

■ **GPIO selected**

In Deep stand-by mode, pins switch to the general-purpose I/O port.

**List of Pin Status**

| Pin status type | Function group                     | Power-on reset or low-voltage detection state        | INITX input state                  | Device internal reset state        | Run mode or sleep mode state | Timer mode, RTC mode, or sleep mode state  |  | Deep stand-by RTC mode or Deep stand-by STOP mode state  |  | Return from Deep stand-by mode state   |
|-----------------|------------------------------------|--|------------------------------------|------------------------------------|------------------------------|--|--|--|--|--|
|                 |                                    | Power supply unstable                                | Power supply stable                |                                    | Power supply stable          | Power supply stable  |  | Power supply stable  |  | Power supply stable  |
|                 |                                    | -  | INITX = 0                          | INITX = 1                          | INITX = 1                    | INITX = 1  |  | INITX = 1  |  | INITX = 1  |
|                 |                                    | -  | -                                  | -                                  | -                            | SPL = 0  | SPL = 1  | SPL = 0  | SPL = 1  | -  |
| A               | GPIO selected                      | Setting disabled                                     | Setting disabled                   | Setting disabled                   | Maintain previous state      | Maintain previous state  | Hi-Z / Internal input fixed at "0"   | Maintain previous state  | Hi-Z / Internal input fixed at "0"   | Maintain previous state  |
|                 | Main crystal oscillator input pin  | Input enabled  | Input enabled                      | Input enabled                      | Input enabled                | Input enabled  | Input enabled  | Input enabled  | Input enabled  | Input enabled  |
| B               | GPIO selected                      | Setting disabled                                     | Setting disabled                   | Setting disabled                   | Maintain previous state      | Maintain previous state  | Hi-Z / Internal input fixed at "0"   | Maintain previous state  | Hi-Z / Internal input fixed at "0"   | Maintain previous state  |
|                 | Main crystal oscillator output pin | Hi-Z / Internal input fixed at "0" / or Input enable | Hi-Z / Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | Maintain previous state      | Maintain previous state / When oscillation stop <sup>*1</sup> , Hi-Z / Internal input fixed at "0" | Maintain previous state / When oscillation stop <sup>*1</sup> , Hi-Z / Internal input fixed at "0" | Maintain previous state / When oscillation stop <sup>*1</sup> , Hi-Z / Internal input fixed at "0" | Maintain previous state / When oscillation stop <sup>*1</sup> , Hi-Z / Internal input fixed at "0" | Maintain previous state / When oscillation stop <sup>*1</sup> , Hi-Z / Internal input fixed at "0" |
| C               | INITX input pin                    | Pull-up / Input enabled                              | Pull-up / Input enabled            | Pull-up / Input enabled            | Pull-up / Input enabled      | Pull-up / Input enabled  | Pull-up / Input enabled  | Pull-up / Input enabled  | Pull-up / Input enabled  | Pull-up / Input enabled  |
| D               | Mode input pin                     | Input enabled  | Input enabled                      | Input enabled                      | Input enabled                | Input enabled  | Input enabled  | Input enabled  | Input enabled  | Input enabled  |
| E               | JTAG selected                      | Hi-Z   | Pull-up / Input enabled            | Pull-up / Input enabled            | Maintain previous state      | Maintain previous state  | Maintain previous state  | Maintain previous state  | Maintain previous state  | Maintain previous state  |
|                 | GPIO selected                      | Setting disabled                                     | Setting disabled                   | Setting disabled                   |                              |  | Hi-Z / Internal input fixed at "0"   | Maintain previous state  | Hi-Z / Internal input fixed at "0"   | Maintain previous state  |

| Pin status type | Function group                      | Power-on reset or low-voltage detection state | INITX input state   | Device internal reset state                               | Run mode or sleep mode state                              | Timer mode, RTC mode, or sleep mode state                 |   | Deep stand-by RTC mode or Deep stand-by STOP mode state   |   | Return from Deep stand-by mode state                      |
|-----------------|-------------------------------------|---|---|---|---|---|---|---|---|---|
|                 |                                     | Power supply unstable                         | Power supply stable                                       |   | Power supply stable                                       | Power supply stable                                       |   | Power supply stable                                       |   | Power supply stable                                       |
|                 |                                     | -   | INITX = 0   | INITX = 1   | INITX = 1   | INITX = 1   |   | INITX = 1   |   | INITX = 1   |
|                 |                                     | -   | -   | -   | -   | SPL = 0   | SPL = 1   | SPL = 0   | SPL = 1   | -   |
| F               | WKUP enabled                        | Setting disabled                              | Setting disabled  | Setting disabled  | Maintain previous state                                   | Maintain previous state                                   | Maintain previous state                                   | WKUP input enabled  | Hi-Z / WKUP input enabled                                 | GPIO selected   |
|                 | Analog input selected               | Hi-Z  | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled |
|                 | External interrupt enabled selected | Setting disabled                              | Setting disabled  | Setting disabled  | Maintain previous state                                   | Maintain previous state                                   | Maintain previous state                                   | GPIO selected   | Hi-Z / Internal input fixed at "0"                        | GPIO selected   |
|                 | Resource other than above selected  |   |   |   |   |   | Hi-Z / Internal input fixed at "0"                        |   |   |   |
|                 | GPIO selected                       |   |   |   |   |   | Maintain previous state                                   |   |   |   |
| G               | WKUP enabled                        | Setting disabled                              | Setting disabled  | Setting disabled  | Maintain previous state                                   | Maintain previous state                                   | Maintain previous state                                   | WKUP input enabled  | Hi-Z / WKUP input enabled                                 | GPIO selected   |
|                 | External interrupt enabled selected | Setting disabled                              | Setting disabled  | Setting disabled  | Maintain previous state                                   | Maintain previous state                                   | Maintain previous state                                   | GPIO selected   | Hi-Z / Internal input fixed at "0"                        | GPIO selected   |
|                 | Resource other than above selected  | Hi-Z  | Hi-Z / Input enabled                                      | Hi-Z / Input enabled                                      |   |   | Hi-Z / Internal input fixed at "0"                        |   |   |   |
|                 | GPIO selected                       |   |   |   |   |   | Maintain previous state                                   |   |   |   |
| H               | External interrupt enabled selected | Setting disabled                              | Setting disabled  | Setting disabled  | Maintain previous state                                   | Maintain previous state                                   | Maintain previous state                                   | GPIO selected   | Hi-Z / Internal input fixed at "0"                        | GPIO selected   |
|                 | Resource other than above selected  | Hi-Z  | Hi-Z / Input enabled                                      | Hi-Z / Input enabled                                      |   |   | Hi-Z / Internal input fixed at "0"                        |   |   |   |
|                 | GPIO selected                       |   |   |   |   |   | Maintain previous state                                   |   |   |   |

| Pin status type | Function group                      | Power-on reset or low-voltage detection state | INITX input state   | Device internal reset state                               | Run mode or sleep mode state                              | Timer mode, RTC mode, or sleep mode state                 |   | Deep stand-by RTC mode or Deep stand-by STOP mode state   |   | Return from Deep stand-by mode state                      |                                    |
|-----------------|-------------------------------------|---|---|---|---|---|---|---|---|---|------------------------------------|
|                 |                                     | Power supply unstable                         | Power supply stable                                       |   | Power supply stable                                       | Power supply stable                                       |   | Power supply stable                                       |   | Power supply stable                                       |                                    |
|                 |                                     | -   | INITX = 0   | INITX = 1   | INITX = 1   | INITX = 1   |   | INITX = 1   |   | INITX = 1   |                                    |
|                 |                                     | -   | -   | -   | -   | SPL = 0   | SPL = 1   | SPL = 0   | SPL = 1   | -   |                                    |
| I               | Resource selected                   | Hi-Z  | Hi-Z / Input enabled                                      | Hi-Z / Input enabled                                      | Maintain previous state                                   | Maintain previous state                                   | Hi-Z / Internal input fixed at "0"                        | GPIO selected   | Hi-Z / Internal input fixed at "0"                        | GPIO selected   |                                    |
|                 | GPIO selected                       |   | Hi-Z  | Hi-Z / Input enabled                                      | Hi-Z / Input enabled                                      | Maintain previous state                                   | Maintain previous state                                   | Hi-Z / Internal input fixed at "0"                        | Maintain previous state                                   | Hi-Z / Internal input fixed at "0"                        | Maintain previous state            |
| J               | NMIX selected                       | Setting disabled                              | Setting disabled  | Setting disabled  | Maintain previous state                                   | Maintain previous state                                   | Maintain previous state                                   | WKUP input enabled  | Hi-Z / WKUP input enabled                                 | GPIO selected   |                                    |
|                 | Resource other than above selected  | Hi-Z  | Hi-Z / Input enabled                                      | Hi-Z / Input enabled                                      |   |   | Hi-Z / Internal input fixed at "0"                        |   |   |   | Hi-Z / Internal input fixed at "0" |
|                 | GPIO selected                       |   |   |   |   |   |   |   |   |   |                                    |
| K               | Analog input selected               | Hi-Z  | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled |                                    |
|                 | Resource other than above selected  |   | Setting disabled  | Setting disabled  | Setting disabled  | Maintain previous state                                   | Maintain previous state                                   | Hi-Z / Internal input fixed at "0"                        | GPIO selected   | Hi-Z / Internal input fixed at "0"                        | GPIO selected                      |
|                 | GPIO selected                       |   |   |   |   |   |   | Maintain previous state                                   |   |   |                                    |
| L               | Analog input selected               | Hi-Z  | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled | Hi-Z / Internal input fixed at "0" / Analog input enabled |                                    |
|                 | External interrupt enabled selected |   | Setting disabled  | Setting disabled  | Setting disabled  | Maintain previous state                                   | Maintain previous state                                   | Maintain previous state                                   | GPIO selected   | Hi-Z / Internal input fixed at "0"                        | GPIO selected                      |
|                 | Resource other than above selected  |   |   |   |   |   |   | Hi-Z / Internal input fixed at "0"                        |   |   |                                    |
|                 | GPIO selected                       |   |   |   |   |   |   | Maintain previous state                                   |   |   |                                    |

| Pin status type | Function group                    | Power-on reset or low-voltage detection state        | INITX input state                  | Device internal reset state        | Run mode or sleep mode state | Timer mode, RTC mode, or sleep mode state   |   | Deep stand-by RTC mode or Deep stand-by STOP mode state   |   | Return from Deep stand-by mode state  |
|-----------------|-----------------------------------|--|------------------------------------|------------------------------------|------------------------------|---|---|---|---|---|
|                 |                                   | Power supply unstable                                | Power supply stable                |                                    | Power supply stable          | Power supply stable   |   | Power supply stable   |   | Power supply stable   |
|                 |                                   | -  | INITX = 0                          | INITX = 1                          | INITX = 1                    | INITX = 1   |   | INITX = 1   |   | INITX = 1   |
|                 |                                   | -  | -                                  | -                                  | -                            | SPL = 0   | SPL = 1   | SPL = 0   | SPL = 1   | -   |
| M               | GPIO selected                     | Setting disabled                                     | Setting disabled                   | Setting disabled                   | Maintain previous state      | Maintain previous state   | Hi-Z / Internal input fixed at "0"  | Maintain previous state   | Hi-Z / Internal input fixed at "0"  | Maintain previous state   |
|                 | Sub crystal oscillator input pin  | Input enabled  | Input enabled                      | Input enabled                      | Input enabled                | Input enabled   | Input enabled   | Input enabled   | Input enabled   | Input enabled   |
| N               | GPIO selected                     | Setting disabled                                     | Setting disabled                   | Setting disabled                   | Maintain previous state      | Maintain previous state   | Hi-Z / Internal input fixed at "0"  | Maintain previous state   | Hi-Z / Internal input fixed at "0"  | Maintain previous state   |
|                 | Sub crystal oscillator output pin | Hi-Z / Internal input fixed at "0" / or Input enable | Hi-Z / Internal input fixed at "0" | Hi-Z / Internal input fixed at "0" | Maintain previous state      | Maintain previous state /When oscillation stop <sup>*2</sup> , Hi-Z / Internal input fixed at "0" | Maintain previous state /When oscillation stop <sup>*2</sup> , Hi-Z / Internal input fixed at "0" | Maintain previous state /When oscillation stop <sup>*2</sup> , Hi-Z / Internal input fixed at "0" | Maintain previous state /When oscillation stop <sup>*2</sup> , Hi-Z / Internal input fixed at "0" | Maintain previous state /When oscillation stop <sup>*2</sup> , Hi-Z / Internal input fixed at "0" |
| O               | GPIO selected                     | Hi-Z   | Hi-Z / Input enabled               | Hi-Z / Input enabled               | Maintain previous state      | Maintain previous state   | Hi-Z / Internal input fixed at "0"  | Maintain previous state   | Hi-Z / Internal input fixed at "0"  | Maintain previous state   |
| P               | Mode input pin                    | Input enabled  | Input enabled                      | Input enabled                      | Input enabled                | Input enabled   | Input enabled   | Input enabled   | Input enabled   | Input enabled   |
|                 | GPIO selected                     | Setting disabled                                     | Setting disabled                   | Setting disabled                   | Maintain previous state      | Maintain previous state   | Hi-Z / Input enabled  | Maintain previous state   | Hi-Z / Input enabled  | Maintain previous state   |

\*1: Oscillation is stopped at sub timer mode, low-speed CR timer mode, RTC mode, stop mode, deep stand-by RTC mode, and deep stand-by stop mode.

\*2: Oscillation is stopped at stop mode and deep stand-by stop mode



## 12. Electrical Characteristics

### 12.1 Absolute Maximum Ratings

| Parameter  | Symbol               | Rating                |                                     | Unit | Remarks      |
|--|----------------------|-----------------------|-------------------------------------|------|--------------|
|  |                      | Min                   | Max                                 |      |              |
| Power supply voltage <sup>*1, *2</sup>               | V <sub>CC</sub>      | V <sub>SS</sub> - 0.5 | V <sub>SS</sub> + 6.5               | V    |              |
| Analog power supply voltage <sup>*1, *3</sup>        | AV <sub>CC</sub>     | V <sub>SS</sub> - 0.5 | V <sub>SS</sub> + 6.5               | V    |              |
| Analog reference voltage <sup>*1, *3</sup>           | AV <sub>RH</sub>     | V <sub>SS</sub> - 0.5 | V <sub>SS</sub> + 6.5               | V    |              |
| Input voltage  | V <sub>I</sub>       | V <sub>SS</sub> - 0.5 | V <sub>CC</sub> + 0.5<br>(≤ 6.5 V)  | V    |              |
|  |                      | V <sub>SS</sub> - 0.5 | V <sub>SS</sub> + 6.5               | V    | 5 V tolerant |
| Analog pin input voltage                             | V <sub>IA</sub>      | V <sub>SS</sub> - 0.5 | AV <sub>CC</sub> + 0.5<br>(≤ 6.5 V) | V    |              |
| Output voltage                                       | V <sub>O</sub>       | V <sub>SS</sub> - 0.5 | V <sub>CC</sub> + 0.5<br>(≤ 6.5 V)  | V    |              |
| Clamp maximum current                                | I <sub>CLAMP</sub>   | -2                    | +2                                  | mA   | *7           |
| Clamp total maximum current                          | ∑ I <sub>CLAMP</sub> |                       | +20                                 | mA   | *7           |
| "L" level maximum output current <sup>*4</sup>       | I <sub>OL</sub>      | -                     | 10                                  | mA   | 4 mA type    |
|  |                      |                       | 20                                  | mA   | 12 mA type   |
|  |                      |                       | 39                                  | mA   | P80, P81     |
| "L" level average output current <sup>*5</sup>       | I <sub>OLAV</sub>    | -                     | 4                                   | mA   | 4 mA type    |
|  |                      |                       | 12                                  | mA   | 12 mA type   |
|  |                      |                       | 18.5                                | mA   | P80, P81     |
| "L" level total maximum output current               | ∑ I <sub>OL</sub>    | -                     | 100                                 | mA   |              |
| "L" level total average output current <sup>*6</sup> | ∑ I <sub>OLAV</sub>  | -                     | 50                                  | mA   |              |
| "H" level maximum output current <sup>*4</sup>       | I <sub>OH</sub>      | -                     | - 10                                | mA   | 4 mA type    |
|  |                      |                       | - 20                                | mA   | 12 mA type   |
|  |                      |                       | - 39                                | mA   | P80, P81     |
| "H" level average output current <sup>*5</sup>       | I <sub>OHAV</sub>    | -                     | - 4                                 | mA   | 4 mA type    |
|  |                      |                       | - 12                                | mA   | 12 mA type   |
|  |                      |                       | - 20.5                              | mA   | P80, P81     |
| "H" level total maximum output current               | ∑ I <sub>OH</sub>    | -                     | - 100                               | mA   |              |
| "H" level total average output current <sup>*6</sup> | ∑ I <sub>OHAV</sub>  | -                     | - 50                                | mA   |              |
| Power consumption                                    | P <sub>D</sub>       | -                     | 300                                 | mW   |              |
| Storage temperature                                  | T <sub>STG</sub>     | - 55                  | + 150                               | °C   |              |

\*1: These parameters are based on the condition that V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V.

\*2: V<sub>CC</sub> must not drop below V<sub>SS</sub> - 0.5 V.

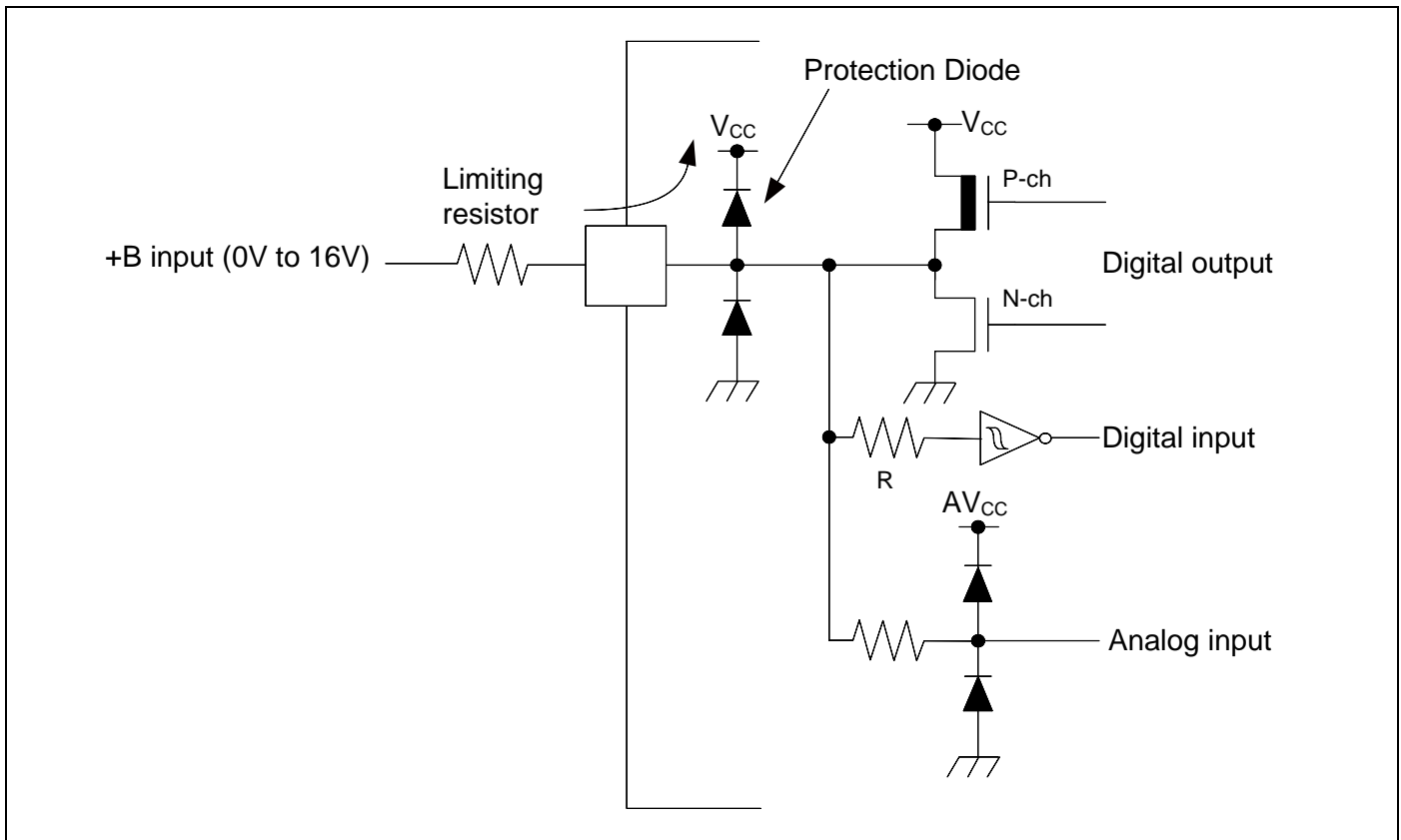
\*3: Ensure that the voltage does not to exceed V<sub>CC</sub> + 0.5 V, for example, when the power is turned on.

\*4: The maximum output current is the peak value for a single pin.

\*5: The average output is the average current for a single pin over a period of 100 ms.

\*6: The total average output current is the average current for all pins over a period of 100 ms.

- \*7:
- See "4. List of Pin Functions" and "5. I/O Circuit Type" about +B input available pin.
  - Use within recommended operating conditions.
  - Use at DC voltage (current) the +B input.
  - The +B signal should always be applied a limiting resistance placed between the +B signal and the device.
  - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the device pin does not exceed rated values, either instantaneously or for prolonged periods.
  - Note that when the device drive current is low, such as in the low-power consumption modes, the +B input potential may pass through the protective diode and increase the potential at the VCC and AVCC pin, and this may affect other devices.
  - Note that if a +B signal is input when the device power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
  - The following is a recommended circuit example (I/O equivalent circuit).



**WARNING:**

- Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 12.2 Recommended Operating Conditions

(V<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V)

| Parameter                   | Symbol           | Conditions | Value             |                  | Unit | Remarks                              |
|-----------------------------|------------------|------------|-------------------|------------------|------|--------------------------------------|
|                             |                  |            | Min               | Max              |      |                                      |
| Power supply voltage        | V <sub>CC</sub>  | -          | 2.7 <sup>*2</sup> | 5.5              | V    |                                      |
| Analog power supply voltage | AV <sub>CC</sub> | -          | 2.7               | 5.5              | V    | AV <sub>CC</sub> =V <sub>CC</sub>    |
| Analog reference voltage    | AV <sub>RH</sub> | -          | 2.7               | AV <sub>CC</sub> | V    |                                      |
| Smoothing capacitor         | C <sub>S</sub>   | -          | 1                 | 10               | μF   | For built-in regulator <sup>*1</sup> |
| Operating temperature       | T <sub>A</sub>   | -          | - 40              | + 105            | °C   |                                      |

\*1: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

\*2: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

### WARNING:

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

## 12.3 DC Characteristics

### 12.3.1 Current Rating

(V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter          | Symbol           | Pin name | Conditions  | Value             |                   | Unit | Remarks |
|--------------------|------------------|----------|---|-------------------|-------------------|------|---------|
|                    |                  |          |   | Typ <sup>*3</sup> | Max <sup>*4</sup> |      |         |
| RUN mode current   | I <sub>CC</sub>  | VCC      | PLL RUN mode<br>CPU: 40 MHz,<br>Peripheral: 40 MHz,<br>MainFlash 0 Wait<br>FRWTR.RWT = 00<br>FSYNDN.SD = 000            | 32                | 41                | mA   | *1, *5  |
|                    |                  |          |   | 21                | 28                |      |         |
|                    |                  |          | High-speed CR RUN mode<br>CPU/ Peripheral: 4 MHz <sup>*2</sup><br>MainFlash 0 Wait<br>FRWTR.RWT = 00<br>FSYNDN.SD = 000 | 3.9               | 7.7               | mA   | *1      |
|                    |                  |          | Sub RUN mode<br>CPU/ Peripheral: 32 kHz<br>MainFlash 0 Wait<br>FRWTR.RWT = 00<br>FSYNDN.SD = 000                        | 0.15              | 3.2               |      |         |
|                    |                  |          | Low-speed CR RUN mode<br>CPU/ Peripheral: 100 kHz<br>MainFlash 0 Wait<br>FRWTR.RWT = 00<br>FSYNDN.SD = 000              | 0.2               | 3.3               | mA   | *1      |
| SLEEP mode current | I <sub>CCS</sub> | VCC      | PLL SLEEP mode<br>Peripheral: 40 MHz  | 10                | 15                |      |         |
|                    |                  |          | High-speed CR SLEEP mode<br>Peripheral: 4 MHz <sup>*2</sup>   | 1.2               | 4.4               | mA   | *1      |
|                    |                  |          | Sub SLEEP mode<br>Peripheral: 32 kHz  | 0.1               | 3.1               |      |         |
|                    |                  |          | Low-speed CR SLEEP mode<br>Peripheral: 100 kHz  | 0.1               | 3.1               | mA   | *1      |

\*1: When all ports are input and are fixed at "0".

\*2: When setting it to 4 MHz by trimming.

\*3: T<sub>A</sub>=+25°C, V<sub>CC</sub>=5.5 V

\*4: T<sub>A</sub>=+105°C, V<sub>CC</sub>=5.5 V

\*5: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

\*6: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

(V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 V to 5.5 V, USBV<sub>CC</sub> = 3.0 V to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                  | Symbol            | Pin name | Conditions              | Value  |                   | Unit | Remarks |        |
|----------------------------|-------------------|----------|-------------------------|--|-------------------|------|---------|--------|
|                            |                   |          |                         | Typ <sup>*2</sup>                                      | Max <sup>*2</sup> |      |         |        |
| TIMER mode current         | I <sub>CCT</sub>  | VCC      | Main TIMER mode         | T <sub>A</sub> = + 25°C, When LVD is off               | 5.2               | 6    | mA      | *1, *3 |
|                            |                   |          |                         | T <sub>A</sub> = + 105°C, When LVD is off              | -                 | 9    | mA      | *1, *3 |
|                            |                   |          | Sub TIMER mode          | T <sub>A</sub> = + 25°C, When LVD is off               | 60                | 230  | μA      | *1, *4 |
|                            |                   |          |                         | T <sub>A</sub> = + 105°C, When LVD is off              | -                 | 3.1  | mA      | *1, *4 |
| RTC mode current           | I <sub>CCR</sub>  |          | RTC mode                | T <sub>A</sub> = + 25°C, When LVD is off               | 50                | 210  | μA      | *1, *4 |
|                            |                   |          |                         | T <sub>A</sub> = + 105°C, When LVD is off              | -                 | 3.1  | mA      | *1, *4 |
| STOP mode current          | I <sub>CCH</sub>  |          | STOP mode               | T <sub>A</sub> = + 25°C, When LVD is off               | 35                | 200  | μA      | *1     |
|                            |                   |          |                         | T <sub>A</sub> = + 105°C, When LVD is off              | -                 | 3    | mA      | *1     |
| Deep stand-by mode current | I <sub>CCRD</sub> | VCC      | Deep stand-by RTC mode  | T <sub>A</sub> = + 25°C, When LVD is off RAM hold off  | 30                | 160  | μA      | *1, *4 |
|                            |                   |          |                         | T <sub>A</sub> = + 25°C, When LVD is off RAM hold on   | 33                | 160  | mA      | *1, *4 |
|                            |                   |          |                         | T <sub>A</sub> = + 105°C, When LVD is off RAM hold off | -                 | 600  | μA      | *1     |
|                            |                   |          |                         | T <sub>A</sub> = + 105°C, When LVD is off RAM hold on  | -                 | 610  | mA      | *1     |
|                            | I <sub>CCHD</sub> |          | Deep stand-by STOP mode | T <sub>A</sub> = + 25°C, When LVD is off RAM hold off  | 20                | 150  | μA      | *1, *4 |
|                            |                   |          |                         | T <sub>A</sub> = + 25°C, When LVD is off RAM hold on   | 23                | 150  | mA      | *1, *4 |
|                            |                   |          |                         | T <sub>A</sub> = + 105°C, When LVD is off RAM hold off | -                 | 600  | μA      | *1     |
|                            |                   |          |                         | T <sub>A</sub> = + 105°C, When LVD is off RAM hold on  | -                 | 610  | mA      | *1     |

\*1: When all ports are input and are fixed at "0".

\*2: V<sub>CC</sub>=5.5 V

\*3: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

\*4: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

**Low-voltage detection current**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter  | Symbol              | Pin name | Conditions  | Value |     | Unit | Remarks       |
|--|---------------------|----------|---|-------|-----|------|---------------|
|  |                     |          |   | Typ   | Max |      |               |
| Low-voltage detection circuit (LVD) power supply current | I <sub>CC</sub> LVD | VCC      | At operation for interrupt<br>V <sub>CC</sub> = 5.5 V | 4     | 7   | μA   | At not detect |

**Flash memory current**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                        | Symbol                | Pin name | Conditions                  | Value |      | Unit | Remarks |
|----------------------------------|-----------------------|----------|-----------------------------|-------|------|------|---------|
|                                  |                       |          |                             | Typ   | Max  |      |         |
| Flash memory write/erase Current | I <sub>CC</sub> FLASH | VCC      | MainFlash<br>At Write/Erase | 11.4  | 13.1 | mA   |         |
|                                  |                       |          | WorkFlash<br>At Write/Erase | 11.4  | 13.1 | mA   |         |

**A/D converter current**

 (V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = AV<sub>RL</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                      | Symbol               | Pin name | Conditions                        | Value |      | Unit | Remarks |
|--------------------------------|----------------------|----------|-----------------------------------|-------|------|------|---------|
|                                |                      |          |                                   | Typ   | Max  |      |         |
| Power supply current           | I <sub>CC</sub> AD   | AVCC     | At 1 unit operation               | 0.57  | 0.72 | mA   |         |
|                                |                      |          | At stop                           | 0.06  | 20   | μA   |         |
| Reference power supply current | I <sub>CC</sub> AVRH | AVRH     | At 1 unit operation<br>AVRH=5.5 V | 1.1   | 1.96 | mA   |         |
|                                |                      |          | At stop                           | 0.06  | 4    | μA   |         |

**12.3.2 Pin Characteristics**

 (V<sub>CC</sub> = AV<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                                  | Symbol           | Pin name  | Conditions   | Value                 |     |                       | Unit | Remarks |
|--|------------------|---|--|-----------------------|-----|-----------------------|------|---------|
|  |                  |   |  | Min                   | Typ | Max                   |      |         |
| "H" level input voltage (hysteresis input) | V <sub>IHS</sub> | CMOS hysteresis input pin, MD0, MD1   | -  | V <sub>CC</sub> × 0.8 | -   | V <sub>CC</sub> + 0.3 | V    |         |
|  |                  | 5V tolerant input pin   | -  | V <sub>CC</sub> × 0.8 | -   | V <sub>SS</sub> + 5.5 | V    |         |
| "L" level input voltage (hysteresis input) | V <sub>ILS</sub> | CMOS hysteresis input pin, MD0, MD1   | -  | V <sub>SS</sub> - 0.3 | -   | V <sub>CC</sub> × 0.2 | V    |         |
|  |                  | 5V tolerant input pin   | -  | V <sub>SS</sub> - 0.3 | -   | V <sub>CC</sub> × 0.2 | V    |         |
| "H" level output voltage                   | V <sub>OH</sub>  | 4mA type  | V <sub>CC</sub> ≥ 4.5 V<br>I <sub>OH</sub> = - 4 mA    | V <sub>CC</sub> - 0.5 | -   | V <sub>CC</sub>       | V    |         |
|  |                  |   | V <sub>CC</sub> < 4.5 V<br>I <sub>OH</sub> = - 2 mA    |                       |     |                       |      |         |
|  |                  | 12mA type   | V <sub>CC</sub> ≥ 4.5 V<br>I <sub>OH</sub> = - 12 mA   | V <sub>CC</sub> - 0.5 | -   | V <sub>CC</sub>       | V    |         |
|  |                  |   | V <sub>CC</sub> < 4.5 V<br>I <sub>OH</sub> = - 8 mA    |                       |     |                       |      |         |
|  |                  | P80/P81   | V <sub>CC</sub> ≥ 4.5 V<br>I <sub>OH</sub> = - 20.5 mA | V <sub>CC</sub> - 0.4 | -   | V <sub>CC</sub>       | V    |         |
|  |                  |   | V <sub>CC</sub> < 4.5 V<br>I <sub>OH</sub> = - 13.0 mA |                       |     |                       |      |         |
| "L" level output voltage                   | V <sub>OL</sub>  | 4mA type  | V <sub>CC</sub> ≥ 4.5 V<br>I <sub>OL</sub> = 4 mA      | V <sub>SS</sub>       | -   | 0.4                   | V    |         |
|  |                  |   | V <sub>CC</sub> < 4.5 V<br>I <sub>OL</sub> = 2 mA      |                       |     |                       |      |         |
|  |                  | 12mA type   | V <sub>CC</sub> ≥ 4.5 V<br>I <sub>OL</sub> = 12 mA     | V <sub>SS</sub>       | -   | 0.4                   | V    |         |
|  |                  |   | V <sub>CC</sub> < 4.5 V<br>I <sub>OL</sub> = 8 mA      |                       |     |                       |      |         |
|  |                  | P80/P81   | V <sub>CC</sub> ≥ 4.5 V<br>I <sub>OL</sub> = 18.5 mA   | V <sub>SS</sub>       | -   | 0.4                   | V    |         |
|  |                  |   | V <sub>CC</sub> < 4.5 V<br>I <sub>OL</sub> = 10.5 mA   |                       |     |                       |      |         |
| Input leak current                         | I <sub>IL</sub>  | -   | -  | - 5                   | -   | +5                    | μA   |         |
| Pull-up resistance value                   | R <sub>PU</sub>  | Pull-up pin   | V <sub>CC</sub> ≥ 4.5 V                                | 25                    | 50  | 100                   | kΩ   |         |
|  |                  |   | V <sub>CC</sub> < 4.5 V                                | 30                    | 80  | 200                   |      |         |
| Input capacitance                          | C <sub>IN</sub>  | Other than V <sub>CC</sub> , V <sub>SS</sub> , AV <sub>CC</sub> , AV <sub>SS</sub> , AVRH | -  | -                     | 5   | 15                    | pF   |         |

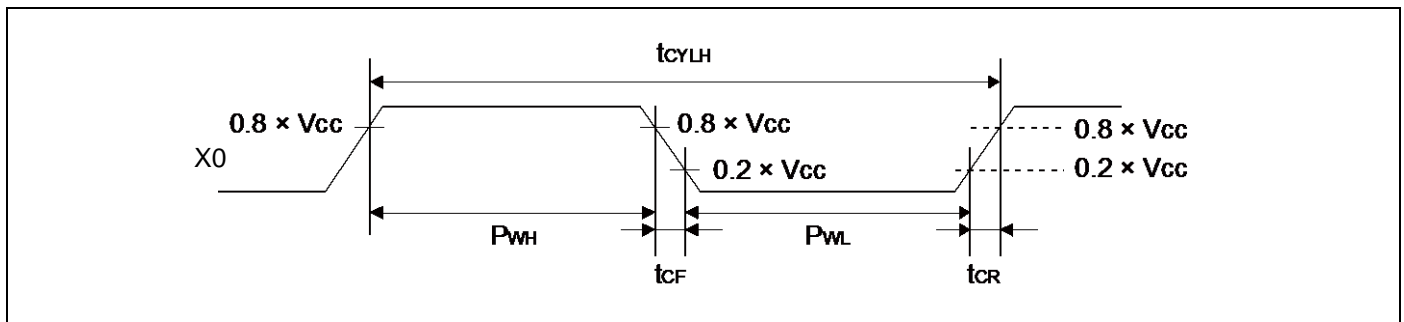
**12.4 AC Characteristics**
**12.4.1 Main Clock Input Characteristics**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter   | Symbol                               | Pin name | Conditions              | Value  |     | Unit | Remarks                              |                           |
|---|--------------------------------------|----------|-------------------------|--|-----|------|--------------------------------------|---------------------------|
|   |                                      |          |                         | Min  | Max |      |                                      |                           |
| Input frequency                                   | F <sub>CH</sub>                      | X0<br>X1 | V <sub>CC</sub> ≥ 4.5 V | 4  | 48  | MHz  | When crystal oscillator is connected |                           |
|   |                                      |          | V <sub>CC</sub> < 4.5 V | 4  | 20  |      |                                      |                           |
|   |                                      |          | V <sub>CC</sub> ≥ 4.5 V | 4  | 48  | MHz  | When using external clock            |                           |
|   |                                      |          | V <sub>CC</sub> < 4.5 V | 4  | 20  |      |                                      |                           |
| Input clock cycle                                 | t <sub>CY LH</sub>                   |          | V <sub>CC</sub> ≥ 4.5 V | 20.83  | 250 | ns   | When using external clock            |                           |
|   |                                      |          | V <sub>CC</sub> < 4.5 V | 50   | 250 |      |                                      |                           |
| Input clock pulse width                           | -                                    |          |                         | PWH/t <sub>CY LH</sub><br>PWL/t <sub>CY LH</sub> | 45  | 55   | %                                    | When using external clock |
| Input clock rise time and fall time               | t <sub>CF</sub> ,<br>t <sub>CR</sub> |          |                         | -  | -   | 5    | ns                                   | When using external clock |
| Internal operating clock frequency* <sup>1</sup>  | F <sub>CM</sub>                      | -        | -                       | -  | 42  | MHz  | Master clock                         |                           |
|   | F <sub>CC</sub>                      | -        | -                       | -  | 42  | MHz  | Base clock (HCLK/FCLK)               |                           |
|   | F <sub>CP0</sub>                     | -        | -                       | -  | 42  | MHz  | APB0 bus clock* <sup>2</sup>         |                           |
|   | F <sub>CP1</sub>                     | -        | -                       | -  | 42  | MHz  | APB1 bus clock* <sup>2</sup>         |                           |
|   | F <sub>CP2</sub>                     | -        | -                       | -  | 42  | MHz  | APB2 bus clock* <sup>2</sup>         |                           |
| Internal operating clock cycle time* <sup>1</sup> | t <sub>CYCC</sub>                    | -        | -                       | 23.8   | -   | ns   | Base clock (HCLK/FCLK)               |                           |
|   | t <sub>CYCP0</sub>                   | -        | -                       | 23.8   | -   | ns   | APB0 bus clock* <sup>2</sup>         |                           |
|   | t <sub>CYCP1</sub>                   | -        | -                       | 23.8   | -   | ns   | APB1 bus clock* <sup>2</sup>         |                           |
|   | t <sub>CYCP2</sub>                   | -        | -                       | 23.8   | -   | ns   | APB2 bus clock* <sup>2</sup>         |                           |

\*1: For more information about each internal operating clock, see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

\*2: For about each APB bus which each peripheral is connected to, see "8. Block Diagram" in this datasheet.

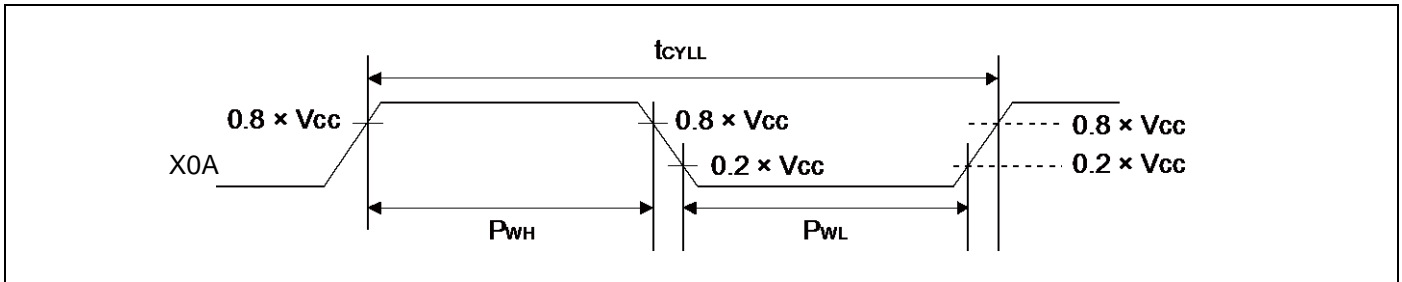




**12.4.2 Sub Clock Input Characteristics**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter               | Symbol               | Pin name   | Conditions            | Value |        |       | Unit | Remarks                              |
|-------------------------|----------------------|------------|-----------------------|-------|--------|-------|------|--------------------------------------|
|                         |                      |            |                       | Min   | Typ    | Max   |      |                                      |
| Input frequency         | 1/ t <sub>CYLL</sub> | X0A<br>X1A | -                     | -     | 32.768 | -     | kHz  | When crystal oscillator is connected |
|                         |                      |            | -                     | 32    | -      | 100   |      | kHz                                  |
| Input clock cycle       | t <sub>CYLL</sub>    |            | -                     | 10    | -      | 31.25 | μs   | When using external clock            |
| Input clock pulse width | -                    |            | PWH/t <sub>CYLL</sub> | 45    | -      | 55    | %    | When using external clock            |
|                         |                      |            | PWL/t <sub>CYLL</sub> |       |        |       |      |                                      |


**12.4.3 Internal CR Oscillation Characteristics**
**High-speed internal CR**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                | Symbol            | Conditions                        | Value |     |      | Unit | Remarks                     |
|--------------------------|-------------------|-----------------------------------|-------|-----|------|------|-----------------------------|
|                          |                   |                                   | Min   | Typ | Max  |      |                             |
| Clock frequency          | F <sub>CRH</sub>  | T <sub>A</sub> = + 25°C           | 3.96  | 4   | 4.04 | MHz  | When trimming <sup>*1</sup> |
|                          |                   | T <sub>A</sub> = 0°C to + 70°C    | 3.84  | 4   | 4.16 |      |                             |
|                          |                   | T <sub>A</sub> = - 40°C to + 85°C | 3.8   | 4   | 4.2  |      |                             |
|                          |                   | T <sub>A</sub> = - 40°C to + 85°C | 3     | 4   | 5    |      | When not trimming           |
| Frequency stability time | t <sub>CRWT</sub> | -                                 | -     | -   | 90   | μs   | *2                          |

\*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

\*2: Frequency stable time is time to stable of the frequency of the High-speed CR clock after the trim value is set. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

**Low-speed internal CR**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter       | Symbol           | Conditions | Value |     |     | Unit | Remarks |
|-----------------|------------------|------------|-------|-----|-----|------|---------|
|                 |                  |            | Min   | Typ | Max |      |         |
| Clock frequency | F <sub>CRL</sub> | -          | 50    | 100 | 150 | kHz  |         |

**12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)**
*(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)*

| Parameter   | Symbol              | Value |     |     | Unit     | Remarks |
|---|---------------------|-------|-----|-----|----------|---------|
|   |                     | Min   | Typ | Max |          |         |
| PLL oscillation stabilization wait time* <sup>1</sup><br>(LOCK UP time) | t <sub>LOCK</sub>   | 100   | -   | -   | μs       |         |
| PLL input clock frequency   | F <sub>PLLI</sub>   | 4     | -   | 16  | MHz      |         |
| PLL multiple rate   | -                   | 13    | -   | 75  | multiple |         |
| PLL macro oscillation clock frequency                                   | F <sub>PLLO</sub>   | 200   | -   | 300 | MHz      |         |
| Main PLL clock frequency* <sup>2</sup>                                  | F <sub>CLKPLL</sub> | -     | -   | 40  | MHz      |         |

\*1: Time from when the PLL starts operating until the oscillation stabilizes.

\*2: For more information about Main PLL clock (CLKPLL), see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

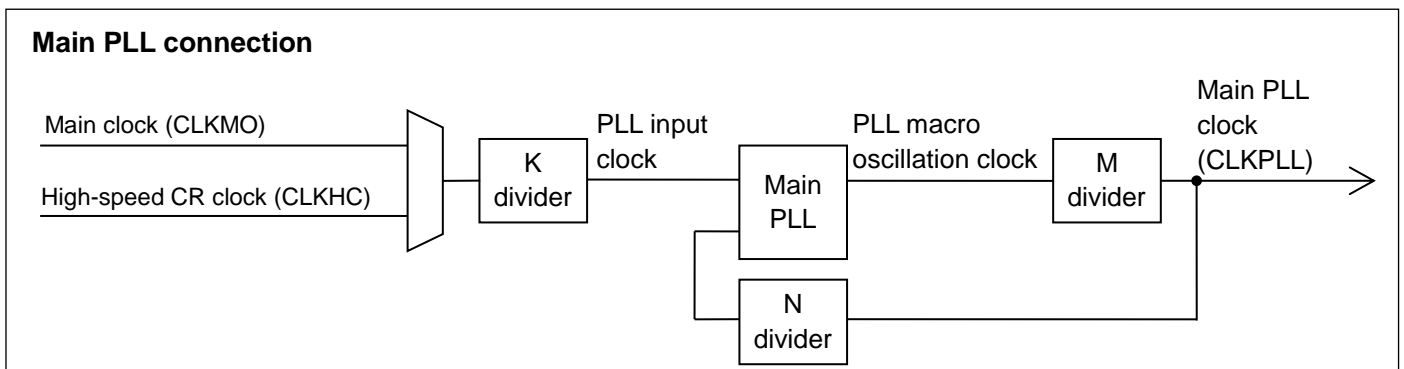
**12.4.5 Operating Conditions of Main PLL (In the case of using high-speed internal CR)**
*(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)*

| Parameter   | Symbol              | Value |     |     | Unit     | Remarks |
|---|---------------------|-------|-----|-----|----------|---------|
|   |                     | Min   | Typ | Max |          |         |
| PLL oscillation stabilization wait time* <sup>1</sup><br>(LOCK UP time) | t <sub>LOCK</sub>   | 100   | -   | -   | μs       |         |
| PLL input clock frequency   | F <sub>PLLI</sub>   | 3.8   | 4   | 4.2 | MHz      |         |
| PLL multiple rate   | -                   | 50    | -   | 71  | multiple |         |
| PLL macro oscillation clock frequency                                   | F <sub>PLLO</sub>   | 190   | -   | 300 | MHz      |         |
| Main PLL clock frequency* <sup>2</sup>                                  | F <sub>CLKPLL</sub> | -     | -   | 42  | MHz      |         |

\*1: Time from when the PLL starts operating until the oscillation stabilizes.

\*2: For more information about Main PLL clock (CLKPLL), see "Chapter 2-1: Clock" in "FM3 Family Peripheral Manual".

When setting PLL multiple rate, please take the accuracy of the built-in high-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.



### 12.4.6 Reset Input Characteristics

( $V_{CC} = 2.7\text{ V to } 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to } +105^\circ\text{C}$ )

| Parameter        | Symbol      | Pin name | Conditions | Value |     | Unit | Remarks |
|------------------|-------------|----------|------------|-------|-----|------|---------|
|                  |             |          |            | Min   | Max |      |         |
| Reset input time | $t_{INITX}$ | INITX    | -          | 500   | -   | ns   |         |

### 12.4.7 Power-on Reset Timing

( $V_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

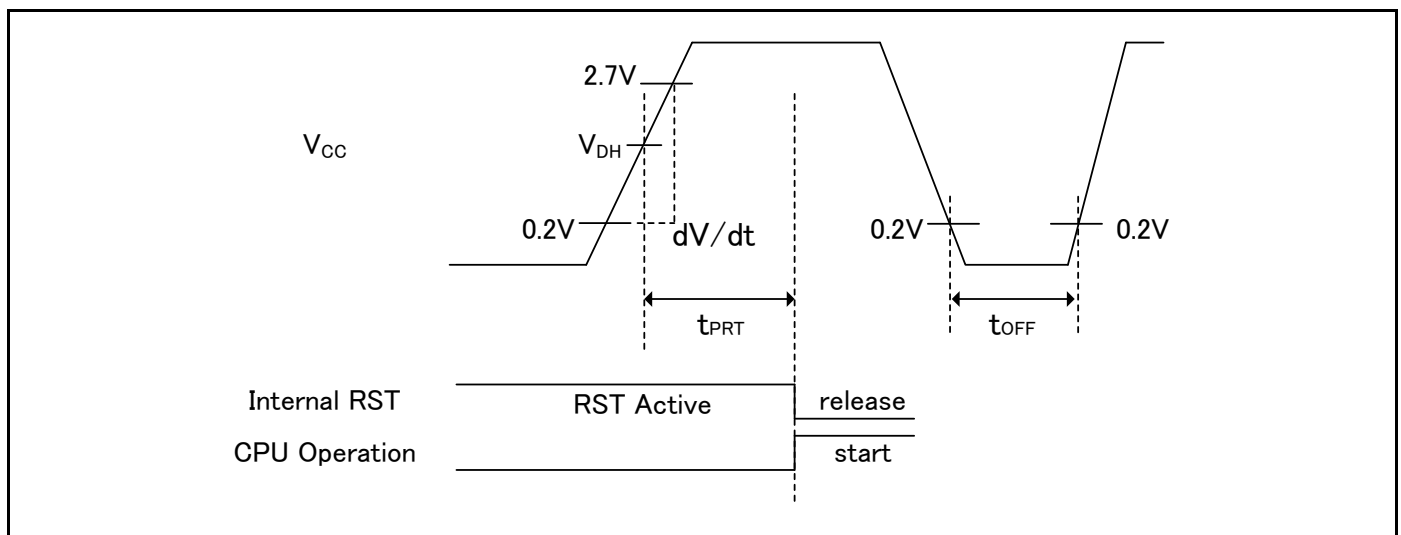
| Parameter                           | Symbol    | Pin Name | Conditions                               | Value |     |      | Unit        | Remarks |
|-------------------------------------|-----------|----------|--|-------|-----|------|-------------|---------|
|                                     |           |          |  | Min   | Typ | Max  |             |         |
| Power supply shut down time         | $t_{OFF}$ | VCC      | -  | 50    | -   | -    | ms          | *1      |
| Power ramp rate                     | $dV/dt$   |          | $V_{CC}: 0.2\text{ V to } 2.70\text{ V}$ | 0.7   | -   | 1000 | mV/ $\mu$ s | *2      |
| Time until releasing Power-on reset | $t_{PRT}$ |          | -  | 0.66  | -   | 0.89 | ms          |         |

\*1:  $V_{CC}$  must be held below 0.2 V for a minimum period of  $t_{OFF}$ . Improper initialization may occur if this condition is not met.

\*2: This  $dV/dt$  characteristic is applied at the power-on of cold start ( $t_{OFF} > 50\text{ ms}$ ).

#### Note:

- $t_{OFF}$  must be satisfied. When  $t_{OFF}$  cannot be satisfied, assert external reset (INITX) at power-up and at any brownout event.

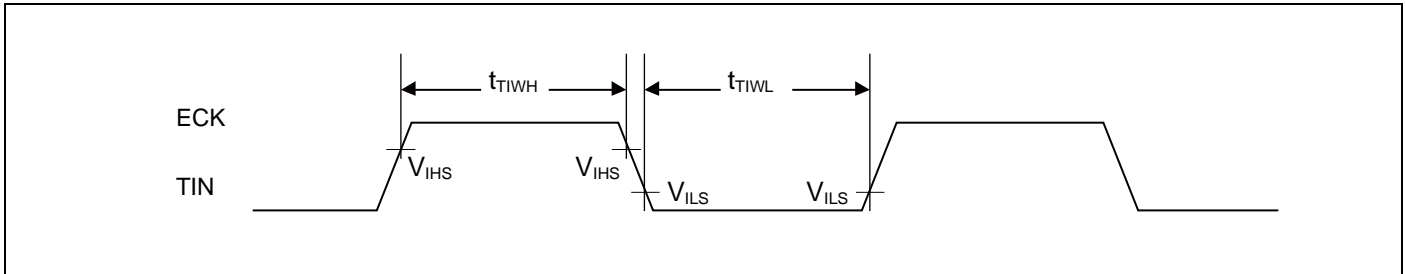


#### Glossary

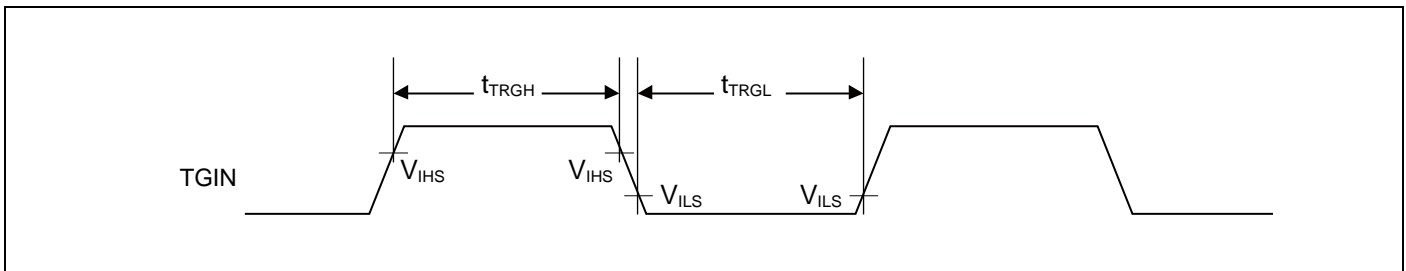
- $V_{DH}$ : detection voltage of Low-Voltage detection reset. See 12.6 Low-voltage Detection Characteristics.

**12.4.8 Base Timer Input Timing**
**Timer input timing**
*(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)*

| Parameter         | Symbol                   | Pin name                                   | Conditions | Value       |     | Unit | Remarks |
|-------------------|--------------------------|--|------------|-------------|-----|------|---------|
|                   |                          |  |            | Min         | Max |      |         |
| Input pulse width | $t_{TIWH}$<br>$t_{TIWL}$ | TIOAn/TIOBn<br>(when using as ECK,<br>TIN) | -          | $2t_{CYCP}$ | -   | ns   |         |


**Trigger input timing**
*(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)*

| Parameter         | Symbol                   | Pin name                               | Conditions | Value       |     | Unit | Remarks |
|-------------------|--------------------------|--|------------|-------------|-----|------|---------|
|                   |                          |  |            | Min         | Max |      |         |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | TIOAn/TIOBn<br>(when using as<br>TGIN) | -          | $2t_{CYCP}$ | -   | ns   |         |


**Note:**

- $t_{CYCP}$  indicates the APB bus clock cycle time.  
About the APB bus number which Base Timer is connected to, see "8. Block Diagram" in this datasheet.

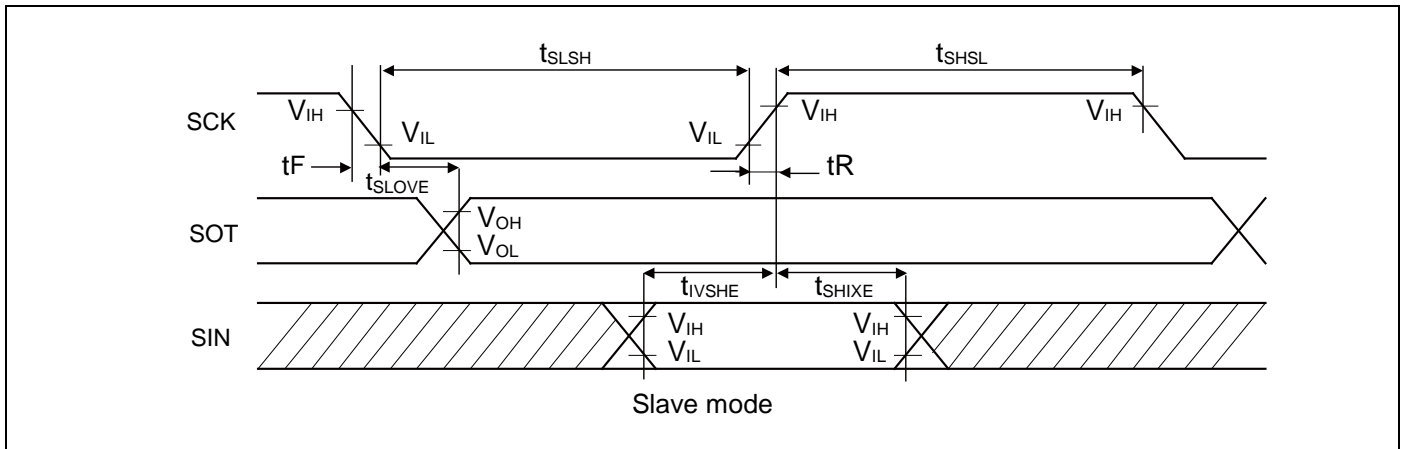
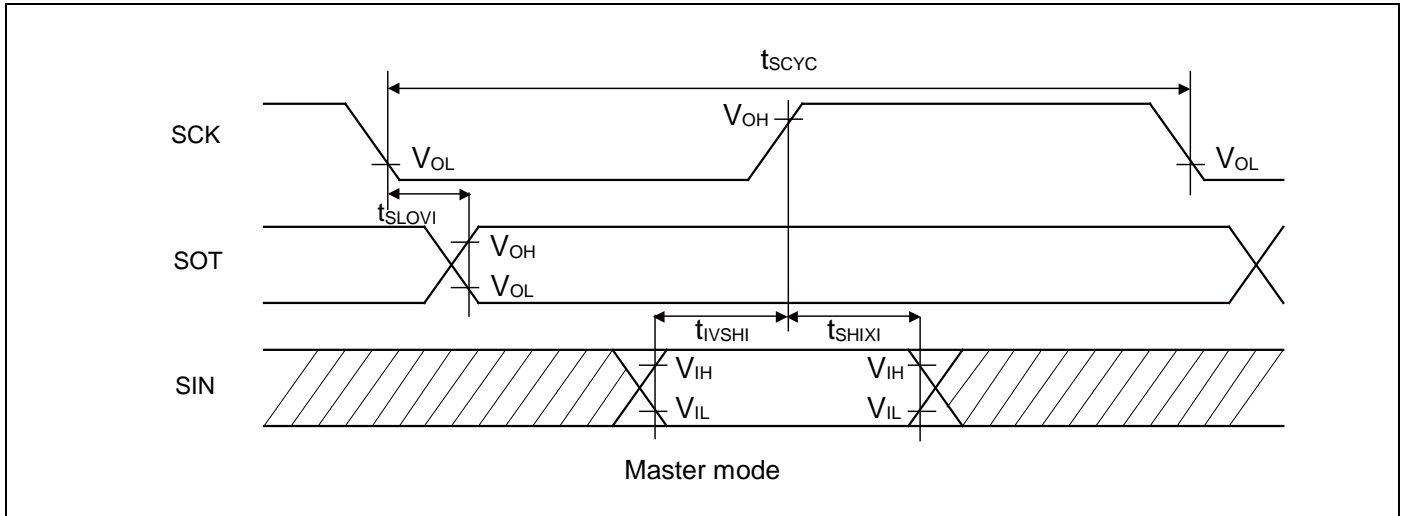
**12.4.9 CSIO/UART Timing**
**CSIO (SPI = 0, SCINV = 0)**

 (V<sub>CC</sub> = 2.7V to 5.5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                    | Symbol             | Pin name     | Conditions  | V <sub>CC</sub> < 4.5 V |     | V <sub>CC</sub> ≥ 4.5 V |      | Unit |
|------------------------------|--------------------|--------------|-------------|-------------------------|-----|-------------------------|------|------|
|                              |                    |              |             | Min                     | Max | Min                     | Max  |      |
| Baud rate                    | -                  | -            | -           | -                       | 8   | -                       | 8    | Mbps |
| Serial clock cycle time      | t <sub>SCYC</sub>  | SCKx         | Master mode | 4t <sub>CYCP</sub>      | -   | 4t <sub>CYCP</sub>      | -    | ns   |
| SCK ↓ → SOT delay time       | t <sub>SLOVI</sub> | SCKx<br>SOTx |             | -30                     | +30 | - 20                    | + 20 | ns   |
| SIN → SCK ↑ setup time       | t <sub>IVSHI</sub> | SCKx<br>SINx |             | 50                      | -   | 30                      | -    | ns   |
| SCK ↑ → SIN hold time        | t <sub>SHIXI</sub> | SCKx<br>SINx |             | 0                       | -   | 0                       | -    | ns   |
| Serial clock "L" pulse width | t <sub>SLSH</sub>  | SCKx         | Slave mode  | 2t <sub>CYCP</sub> - 10 | -   | 2t <sub>CYCP</sub> - 10 | -    | ns   |
| Serial clock "H" pulse width | t <sub>SHSL</sub>  | SCKx         |             | t <sub>CYCP</sub> + 10  | -   | t <sub>CYCP</sub> + 10  | -    | ns   |
| SCK ↓ → SOT delay time       | t <sub>SLOVE</sub> | SCKx<br>SOTx |             | -                       | 50  | -                       | 30   | ns   |
| SIN → SCK ↑ setup time       | t <sub>IVSHE</sub> | SCKx<br>SINx |             | 10                      | -   | 10                      | -    | ns   |
| SCK ↑ → SIN hold time        | t <sub>SHIXE</sub> | SCKx<br>SINx |             | 20                      | -   | 20                      | -    | ns   |
| SCK fall time                | t <sub>F</sub>     | SCKx         |             | -                       | 5   | -                       | 5    | ns   |
| SCK rise time                | t <sub>R</sub>     | SCKx         |             | -                       | 5   | -                       | 5    | ns   |

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram" in this datasheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance = 30 pF.



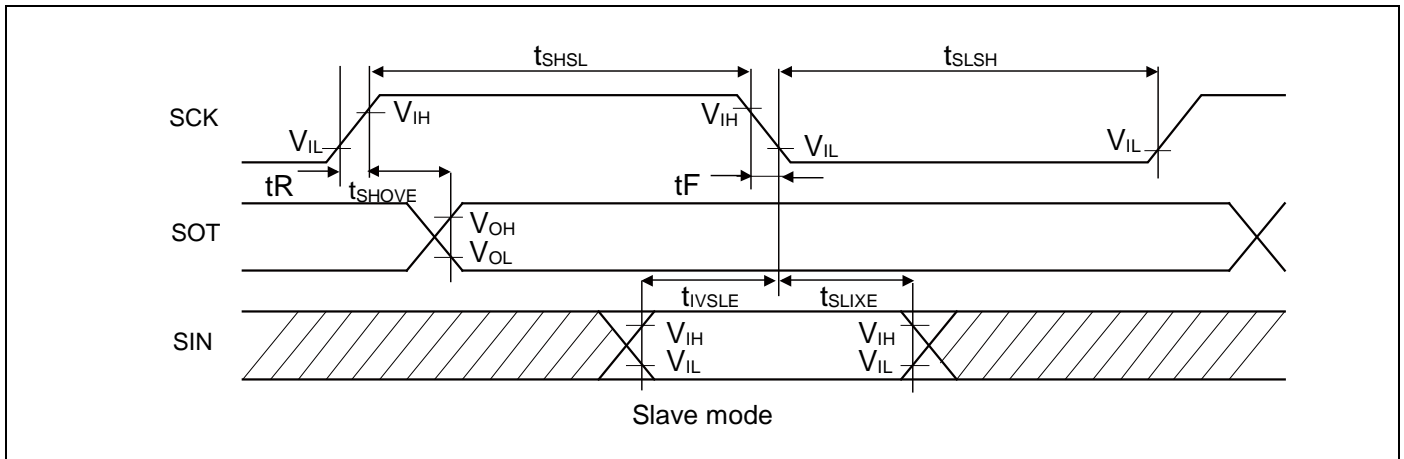
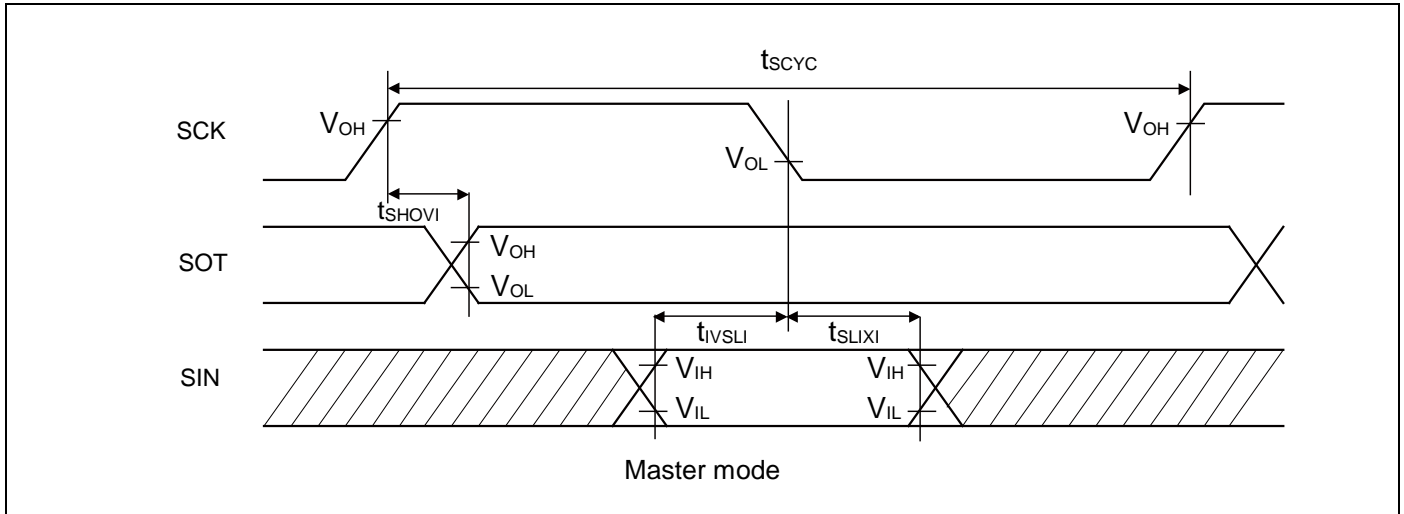
**CSIO (SPI = 0, SCINV = 1)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                    | Symbol             | Pin name     | Conditions  | V <sub>CC</sub> < 4.5 V |     | V <sub>CC</sub> ≥ 4.5 V |      | Unit |
|------------------------------|--------------------|--------------|-------------|-------------------------|-----|-------------------------|------|------|
|                              |                    |              |             | Min                     | Max | Min                     | Max  |      |
| Baud rate                    | -                  | -            | -           | -                       | 8   | -                       | 8    | Mbps |
| Serial clock cycle time      | t <sub>SCYC</sub>  | SCKx         | Master mode | 4t <sub>CYCP</sub>      | -   | 4t <sub>CYCP</sub>      | -    | ns   |
| SCK ↑ → SOT delay time       | t <sub>SHOVI</sub> | SCKx<br>SOTx |             | -30                     | +30 | - 20                    | + 20 | ns   |
| SIN → SCK ↓ setup time       | t <sub>IVSLI</sub> | SCKx<br>SINx |             | 50                      | -   | 30                      | -    | ns   |
| SCK ↓ → SIN hold time        | t <sub>SLIXI</sub> | SCKx<br>SINx |             | 0                       | -   | 0                       | -    | ns   |
| Serial clock "L" pulse width | t <sub>SLSH</sub>  | SCKx         | Slave mode  | 2t <sub>CYCP</sub> - 10 | -   | 2t <sub>CYCP</sub> - 10 | -    | ns   |
| Serial clock "H" pulse width | t <sub>SHSL</sub>  | SCKx         |             | t <sub>CYCP</sub> + 10  | -   | t <sub>CYCP</sub> + 10  | -    | ns   |
| SCK ↑ → SOT delay time       | t <sub>SHOVE</sub> | SCKx<br>SOTx |             | -                       | 50  | -                       | 30   | ns   |
| SIN → SCK ↓ setup time       | t <sub>IVSLE</sub> | SCKx<br>SINx |             | 10                      | -   | 10                      | -    | ns   |
| SCK ↓ → SIN hold time        | t <sub>SLIXE</sub> | SCKx<br>SINx |             | 20                      | -   | 20                      | -    | ns   |
| SCK fall time                | t <sub>F</sub>     | SCKx         |             | -                       | 5   | -                       | 5    | ns   |
| SCK rise time                | t <sub>R</sub>     | SCKx         |             | -                       | 5   | -                       | 5    | ns   |

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram" in this datasheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance = 30 pF.





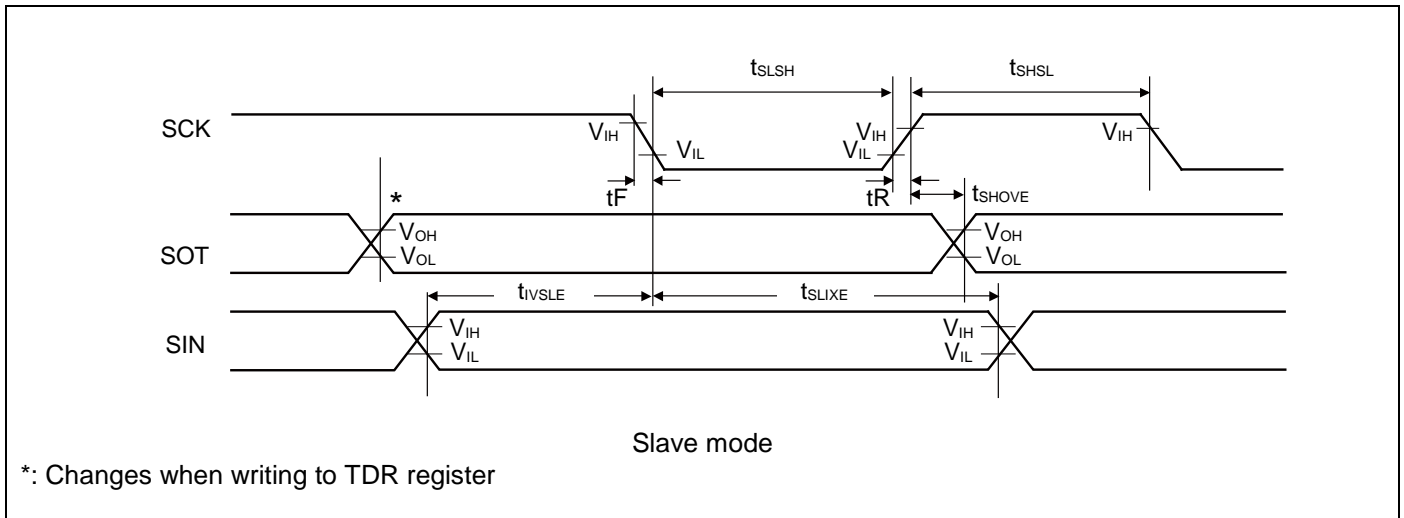
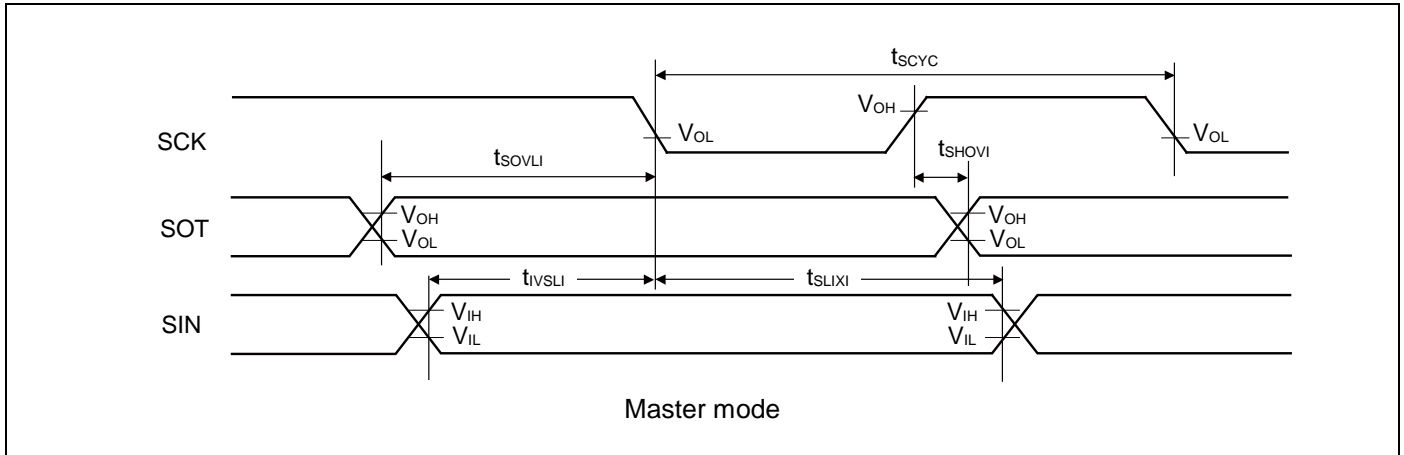
**CSIO (SPI = 1, SCINV = 0)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                    | Symbol             | Pin name     | Conditions             | V <sub>CC</sub> < 4.5 V |                        | V <sub>CC</sub> ≥ 4.5 V |      | Unit |
|------------------------------|--------------------|--------------|------------------------|-------------------------|------------------------|-------------------------|------|------|
|                              |                    |              |                        | Min                     | Max                    | Min                     | Max  |      |
| Baud rate                    | -                  | -            | -                      | -                       | 8                      | -                       | 8    | Mbps |
| Serial clock cycle time      | t <sub>SCYC</sub>  | SCKx         | Master mode            | 4t <sub>CYCP</sub>      | -                      | 4t <sub>CYCP</sub>      | -    | ns   |
| SCK ↑ → SOT delay time       | t <sub>SHOVI</sub> | SCKx<br>SOTx |                        | -30                     | +30                    | - 20                    | + 20 | ns   |
| SIN → SCK ↓ setup time       | t <sub>IVSLI</sub> | SCKx<br>SINx |                        | 50                      | -                      | 30                      | -    | ns   |
| SCK ↓ → SIN hold time        | t <sub>SLIXI</sub> | SCKx<br>SINx |                        | 0                       | -                      | 0                       | -    | ns   |
| SOT → SCK ↓ delay time       | t <sub>SOVLI</sub> | SCKx<br>SOTx |                        | 2t <sub>CYCP</sub> - 30 | -                      | 2t <sub>CYCP</sub> - 30 | -    | ns   |
| Serial clock "L" pulse width | t <sub>LSLH</sub>  | SCKx         |                        | 2t <sub>CYCP</sub> - 10 | -                      | 2t <sub>CYCP</sub> - 10 | -    | ns   |
| Serial clock "H" pulse width | t <sub>SHSL</sub>  | SCKx         | t <sub>CYCP</sub> + 10 | -                       | t <sub>CYCP</sub> + 10 | -                       | ns   |      |
| SCK ↑ → SOT delay time       | t <sub>SHOVE</sub> | SCKx<br>SOTx | Slave mode             | -                       | 50                     | -                       | 30   | ns   |
| SIN → SCK ↓ setup time       | t <sub>IVSLE</sub> | SCKx<br>SINx |                        | 10                      | -                      | 10                      | -    | ns   |
| SCK ↓ → SIN hold time        | t <sub>SLIXE</sub> | SCKx<br>SINx |                        | 20                      | -                      | 20                      | -    | ns   |
| SCK fall time                | t <sub>F</sub>     | SCKx         |                        | -                       | 5                      | -                       | 5    | ns   |
| SCK rise time                | t <sub>R</sub>     | SCKx         |                        | -                       | 5                      | -                       | 5    | ns   |

**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram" in this datasheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance = 30 pF.



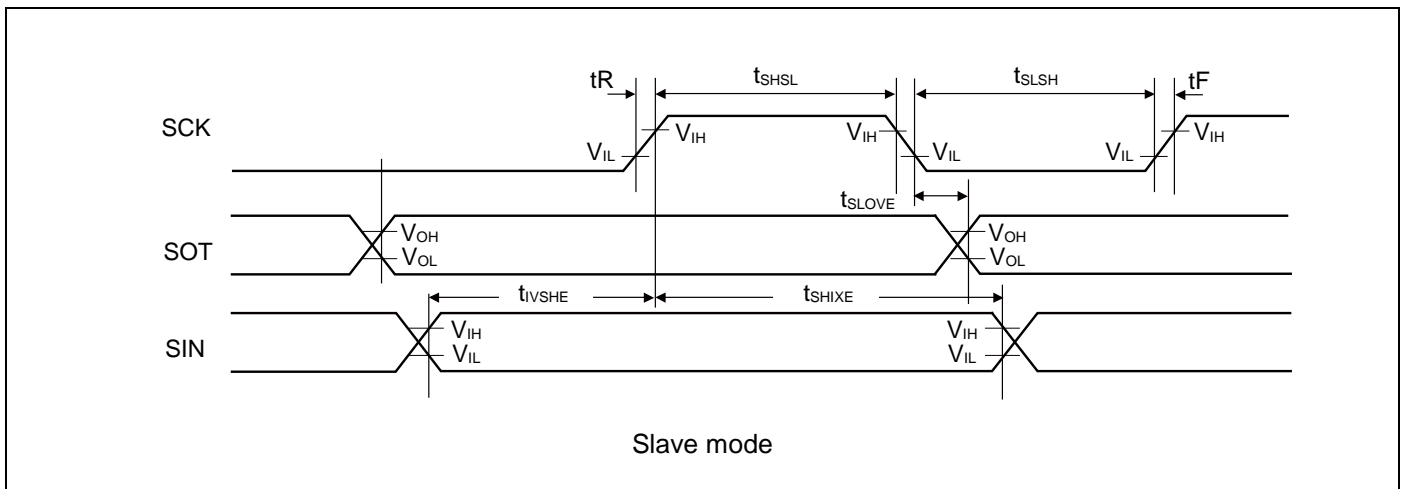
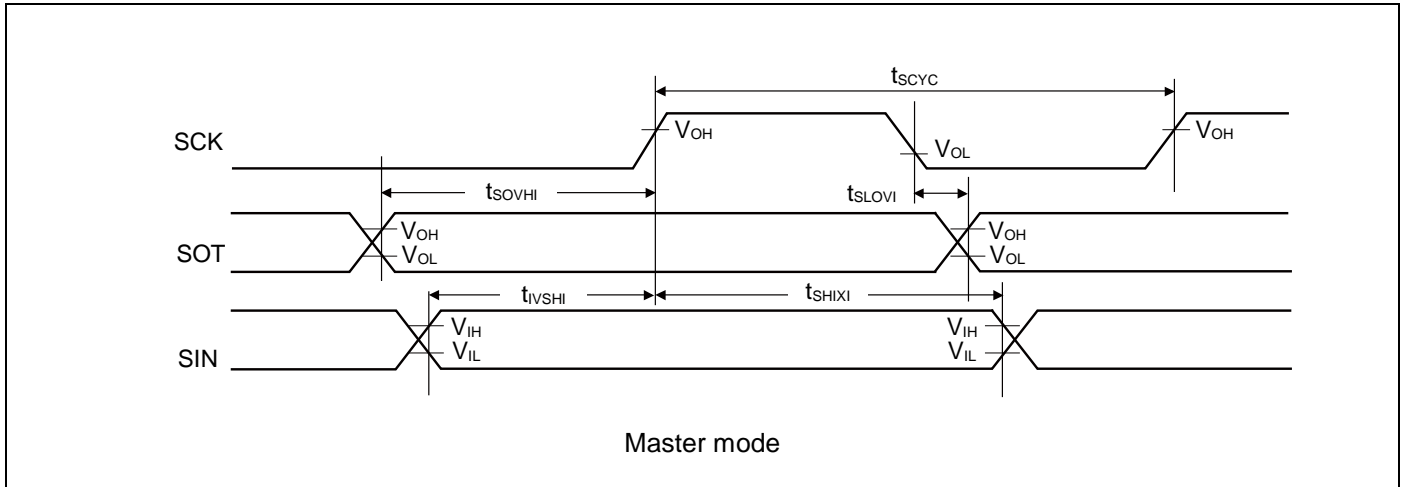
**CSIO (SPI = 1, SCINV = 1)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                    | Symbol             | Pin name     | Conditions  | V <sub>CC</sub> < 4.5 V |     | V <sub>CC</sub> ≥ 4.5 V |      | Unit |
|------------------------------|--------------------|--------------|-------------|-------------------------|-----|-------------------------|------|------|
|                              |                    |              |             | Min                     | Max | Min                     | Max  |      |
| Baud rate                    | -                  | -            | -           | -                       | 8   | -                       | 8    | Mbps |
| Serial clock cycle time      | t <sub>SCYC</sub>  | SCKx         | Master mode | 4t <sub>CYCP</sub>      | -   | 4t <sub>CYCP</sub>      | -    | ns   |
| SCK ↓ → SOT delay time       | t <sub>SLOVI</sub> | SCKx<br>SOTx |             | -30                     | +30 | - 20                    | + 20 | ns   |
| SIN → SCK ↑ setup time       | t <sub>IVSHI</sub> | SCKx<br>SINx |             | 50                      | -   | 30                      | -    | ns   |
| SCK ↑ → SIN hold time        | t <sub>SHIXI</sub> | SCKx<br>SINx |             | 0                       | -   | 0                       | -    | ns   |
| SOT → SCK ↑ delay time       | t <sub>SOVHI</sub> | SCKx<br>SOTx |             | 2t <sub>CYCP</sub> - 30 | -   | 2t <sub>CYCP</sub> - 30 | -    | ns   |
| Serial clock "L" pulse width | t <sub>SLSH</sub>  | SCKx         | Slave mode  | 2t <sub>CYCP</sub> - 10 | -   | 2t <sub>CYCP</sub> - 10 | -    | ns   |
| Serial clock "H" pulse width | t <sub>SHSL</sub>  | SCKx         |             | t <sub>CYCP</sub> + 10  | -   | t <sub>CYCP</sub> + 10  | -    | ns   |
| SCK ↓ → SOT delay time       | t <sub>SLOVE</sub> | SCKx<br>SOTx |             | -                       | 50  | -                       | 30   | ns   |
| SIN → SCK ↑ setup time       | t <sub>IVSHE</sub> | SCKx<br>SINx |             | 10                      | -   | 10                      | -    | ns   |
| SCK ↑ → SIN hold time        | t <sub>SHIXE</sub> | SCKx<br>SINx |             | 20                      | -   | 20                      | -    | ns   |
| SCK fall time                | t <sub>F</sub>     | SCKx         |             | -                       | 5   | -                       | 5    | ns   |
| SCK rise time                | t <sub>R</sub>     | SCKx         |             | -                       | 5   | -                       | 5    | ns   |

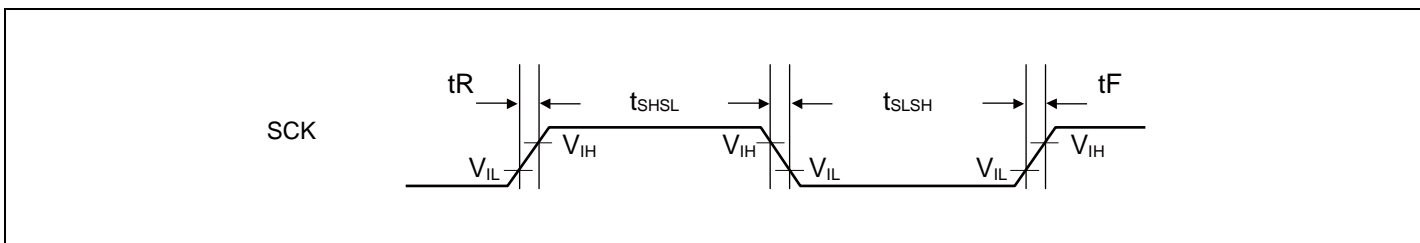
**Notes:**

- The above characteristics apply to CLK synchronous mode.
- t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
About the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram" in this datasheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance = 30 pF.


**UART external clock input (EXT = 1)**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                    | Symbol            | Conditions             | Min                    | Max | Unit | Remarks |
|------------------------------|-------------------|------------------------|------------------------|-----|------|---------|
| Serial clock "L" pulse width | t <sub>SLSH</sub> | C <sub>L</sub> = 30 pF | t <sub>CYCP</sub> + 10 | -   | ns   |         |
| Serial clock "H" pulse width | t <sub>SHSL</sub> |                        | t <sub>CYCP</sub> + 10 | -   | ns   |         |
| SCK fall time                | t <sub>F</sub>    |                        | -                      | 5   | ns   |         |
| SCK rise time                | t <sub>R</sub>    |                        | -                      | 5   | ns   |         |



## 12.4.10 External Input Timing

(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter         | Symbol                                 | Pin name | Conditions | Value                            |  | Unit | Remarks                     |                           |
|-------------------|--|----------|------------|----------------------------------|--|------|-----------------------------|---------------------------|
|                   |  |          |            | Min                              | Max                                    |      |                             |                           |
| Input pulse width | t <sub>INH</sub> ,<br>t <sub>INL</sub> | ADTG     | -          | 2t <sub>CYCP</sub> <sup>*1</sup> | -                                      | ns   | A/D converter trigger input |                           |
|                   |  | FRCKx    |            |                                  |  |      | Free-run timer input clock  |                           |
|                   |  | ICxx     |            |                                  |  |      | Input capture               |                           |
|                   |  | DTTlxX   | -          | 2t <sub>CYCP</sub> <sup>*1</sup> | -                                      | ns   | Wave form generator         |                           |
|                   |  | INTxx    | *2         | -                                | 2t <sub>CYCP</sub> + 100 <sup>*1</sup> | -    | ns                          | External interrupt<br>NMI |
|                   |  | NMIX     |            |                                  |  |      |                             |                           |
|                   |  | WKUPx    | *4         | -                                | 820                                    | -    | ns                          | Deep stand-by wake up     |

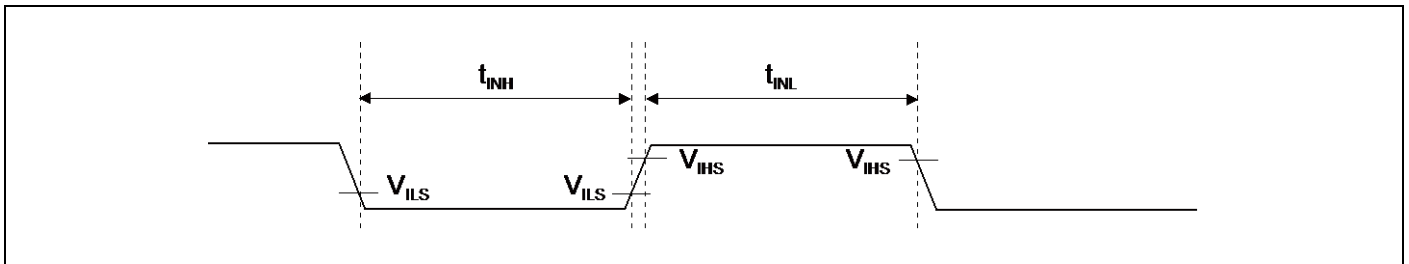
\*1: t<sub>CYCP</sub> indicates the APB bus clock cycle time.

About the APB bus number which A/D converter, Multi-function Timer, External interrupt are connected to, see "8. Block Diagram" in this datasheet.

\*2: When in Run mode, in Sleep mode.

\*3: When in Stop mode, in RTC mode, in Timer mode.

\*4: When in deep stand-by Stop mode, in deep stand-by RTC mode.



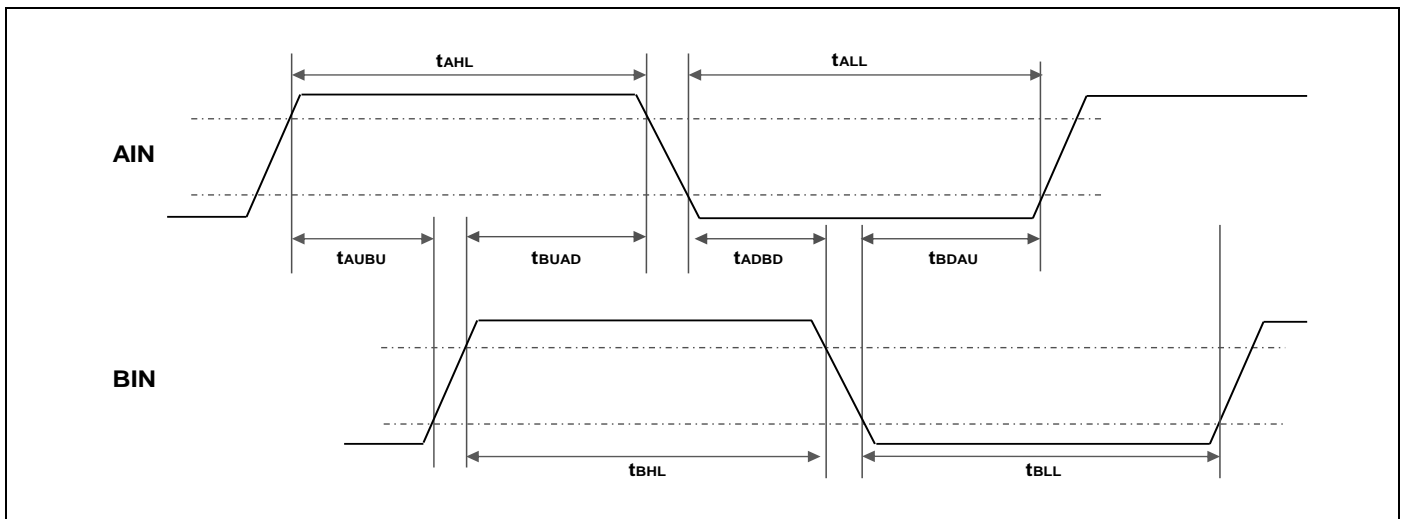
## 12.4.11 Quadrature Position/Revolution Counter timing

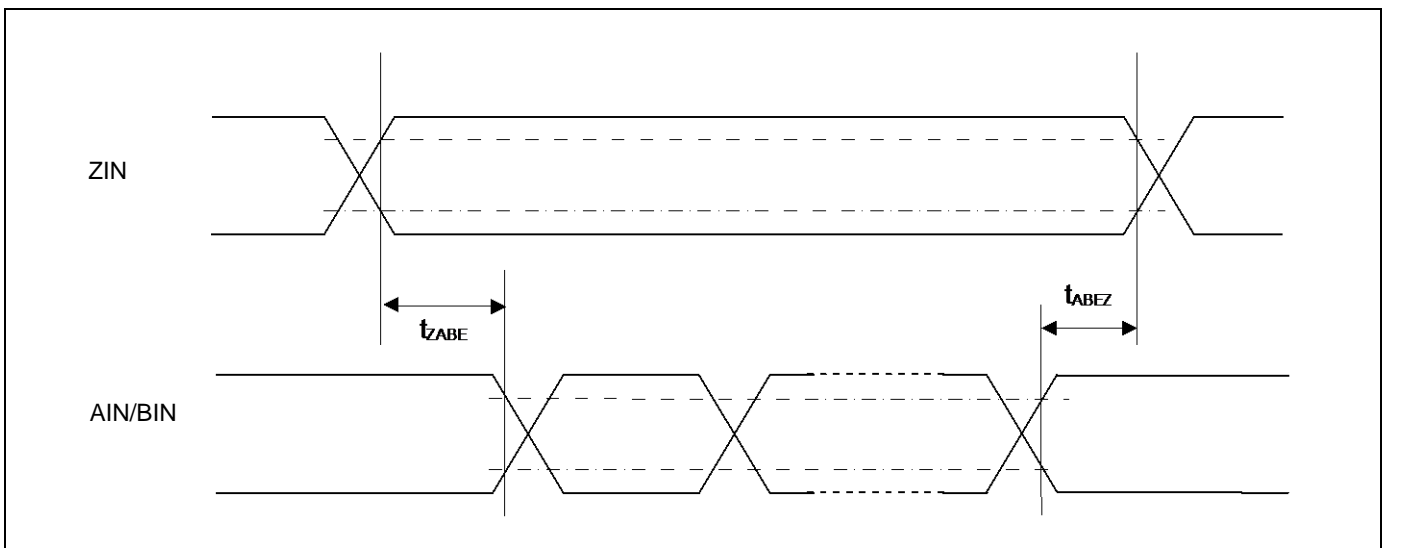
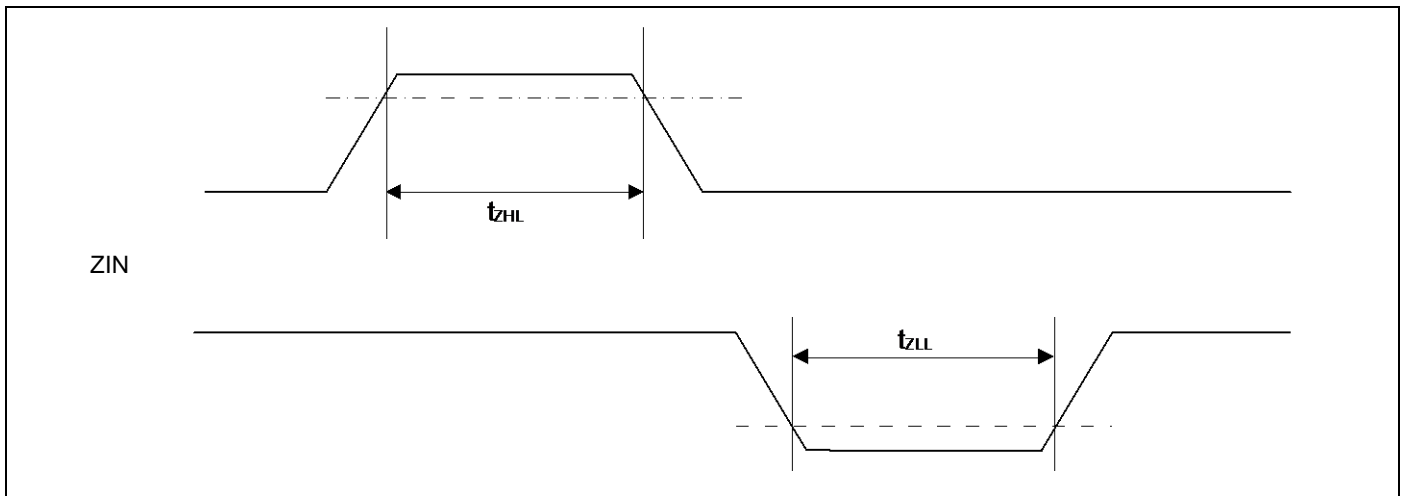
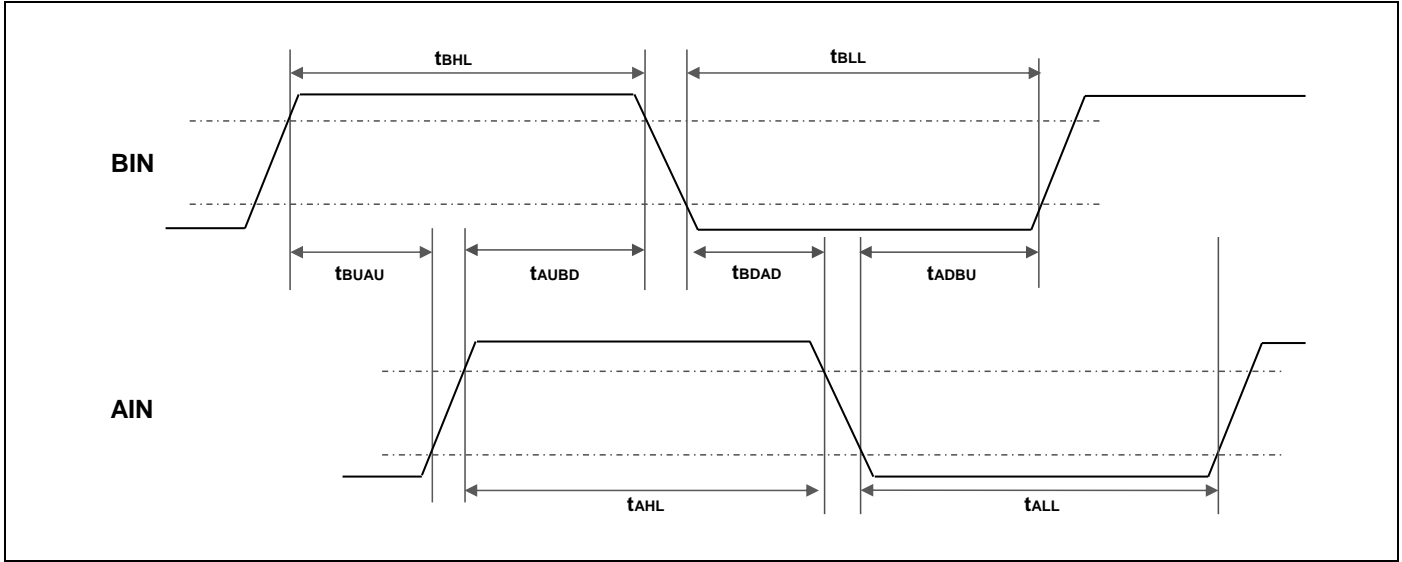
( $V_{CC} = 2.7\text{ V to } 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to } +105^\circ\text{C}$ )

| Parameter  | Symbol     | Conditions           | Value            |     | Unit |
|--|------------|----------------------|------------------|-----|------|
|  |            |                      | Min              | Max |      |
| AIN pin "H" width                                    | $t_{AHL}$  | -                    | $2t_{CYCP}^{*1}$ | -   | ns   |
| AIN pin "L" width                                    | $t_{ALL}$  | -                    |                  |     |      |
| BIN pin "H" width                                    | $t_{BHL}$  | -                    |                  |     |      |
| BIN pin "L" width                                    | $t_{BLL}$  | -                    |                  |     |      |
| BIN rise time from AIN pin "H" level                 | $t_{AUBU}$ | PC_Mode2 or PC_Mode3 |                  |     |      |
| AIN fall time from BIN pin "H" level                 | $t_{BUAD}$ | PC_Mode2 or PC_Mode3 |                  |     |      |
| BIN fall time from AIN pin "L" level                 | $t_{ADBD}$ | PC_Mode2 or PC_Mode3 |                  |     |      |
| AIN rise time from BIN pin "L" level                 | $t_{BDAU}$ | PC_Mode2 or PC_Mode3 |                  |     |      |
| AIN rise time from BIN pin "H" level                 | $t_{BUAU}$ | PC_Mode2 or PC_Mode3 |                  |     |      |
| BIN fall time from AIN pin "H" level                 | $t_{AUBD}$ | PC_Mode2 or PC_Mode3 |                  |     |      |
| AIN fall time from BIN pin "L" level                 | $t_{BDAD}$ | PC_Mode2 or PC_Mode3 |                  |     |      |
| BIN rise time from AIN pin "L" level                 | $t_{ADBU}$ | PC_Mode2 or PC_Mode3 |                  |     |      |
| ZIN pin "H" width                                    | $t_{ZHL}$  | QCR:CGSC="0"         |                  |     |      |
| ZIN pin "L" width                                    | $t_{ZLL}$  | QCR:CGSC="0"         |                  |     |      |
| AIN/BIN rise and fall time from determined ZIN level | $t_{ZABE}$ | QCR:CGSC="1"         |                  |     |      |
| Determined ZIN level from AIN/BIN rise and fall time | $t_{ABEZ}$ | QCR:CGSC="1"         |                  |     |      |

\*1:  $t_{CYCP}$  indicates the APB bus clock cycle time.

About the APB bus number which Quadrature Position/Revolution Counter is connected to, see "8. Block Diagram" in this datasheet.





## 12.4.12 I<sup>2</sup>C Timing

(V<sub>CC</sub> = 2.7 V to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter  | Symbol             | Conditions  | Standard-mode |                                   | Fast-mode |                                   | Unit | Remarks |  |
|--|--------------------|---|---------------|-----------------------------------|-----------|-----------------------------------|------|---------|--|
|  |                    |   | Min           | Max                               | Min       | Max                               |      |         |  |
| SCL clock frequency  | F <sub>SCL</sub>   |   | 0             | 100                               | 0         | 400                               | kHz  |         |  |
| (Repeated) START condition hold time<br>SDA ↓ → SCL ↓              | t <sub>HDSTA</sub> | C <sub>L</sub> = 30 pF,<br>R = (V <sub>p</sub> /I <sub>OL</sub> ) <sup>*1</sup> | 4.0           | -                                 | 0.6       | -                                 | μs   |         |  |
| SCLclock "L" width   | t <sub>LOW</sub>   |   | 4.7           | -                                 | 1.3       | -                                 | μs   |         |  |
| SCLclock "H" width   | t <sub>HIGH</sub>  |   | 4.0           | -                                 | 0.6       | -                                 | μs   |         |  |
| (Repeated) START setup time<br>SCL ↑ → SDA ↓                       | t <sub>SUSTA</sub> |   | 4.7           | -                                 | 0.6       | -                                 | μs   |         |  |
| Data hold time<br>SCL ↓ → SDA ↓ ↑                                  | t <sub>HDDAT</sub> |   | 0             | 3.45 <sup>*2</sup>                | 0         | 0.9 <sup>*3</sup>                 | μs   |         |  |
| Data setup time<br>SDA ↓ ↑ → SCL ↑                                 | t <sub>SUDAT</sub> |   | 250           | -                                 | 100       | -                                 | ns   |         |  |
| STOP condition setup time<br>SCL ↑ → SDA ↑                         | t <sub>SUSTO</sub> |   | 4.0           | -                                 | 0.6       | -                                 | μs   |         |  |
| Bus free time between<br>"STOP condition" and<br>"START condition" | t <sub>BUF</sub>   |   | 4.7           | -                                 | 1.3       | -                                 | μs   |         |  |
| Noise filter   | t <sub>SP</sub>    |   | -             | 2 t <sub>CYCP</sub> <sup>*4</sup> | -         | 2 t <sub>CYCP</sub> <sup>*4</sup> | -    | ns      |  |

\*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively.

V<sub>p</sub> indicates the power supply voltage of the pull-up resistance and I<sub>OL</sub> indicates V<sub>OL</sub> guaranteed current.

\*2: The maximum t<sub>HDDAT</sub> must satisfy that it doesn't extend at least "L" period (t<sub>LOW</sub>) of device's SCL signal.

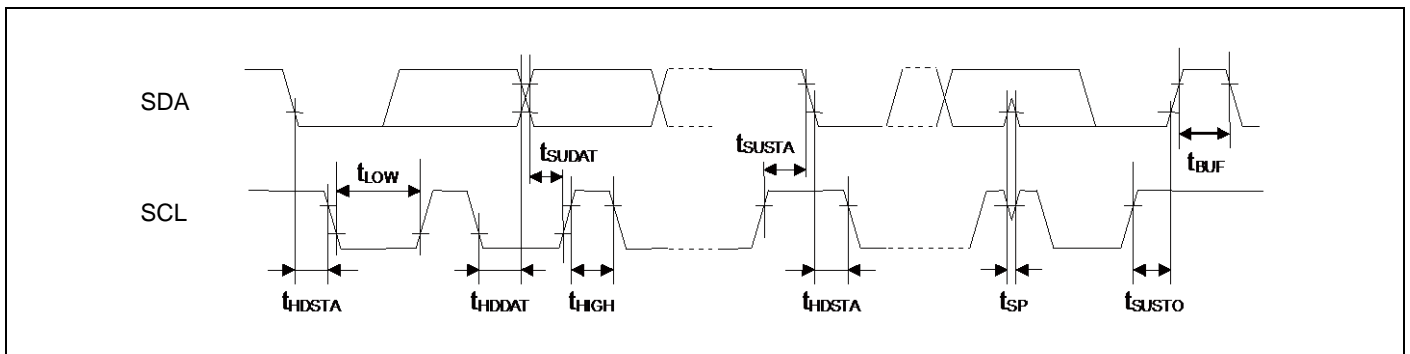
\*3: Fast-mode I<sup>2</sup>C bus device can be used on Standard-mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of "t<sub>SUDAT</sub> ≥ 250 ns".

\*4: t<sub>CYCP</sub> is the APB bus clock cycle time.

About the APB bus number that I<sup>2</sup>C is connected to, see "8. Block Diagram" in this datasheet.

To use Standard-mode, set the APB bus clock at 2 MHz or more.

To use Fast-mode, set the APB bus clock at 8 MHz or more.





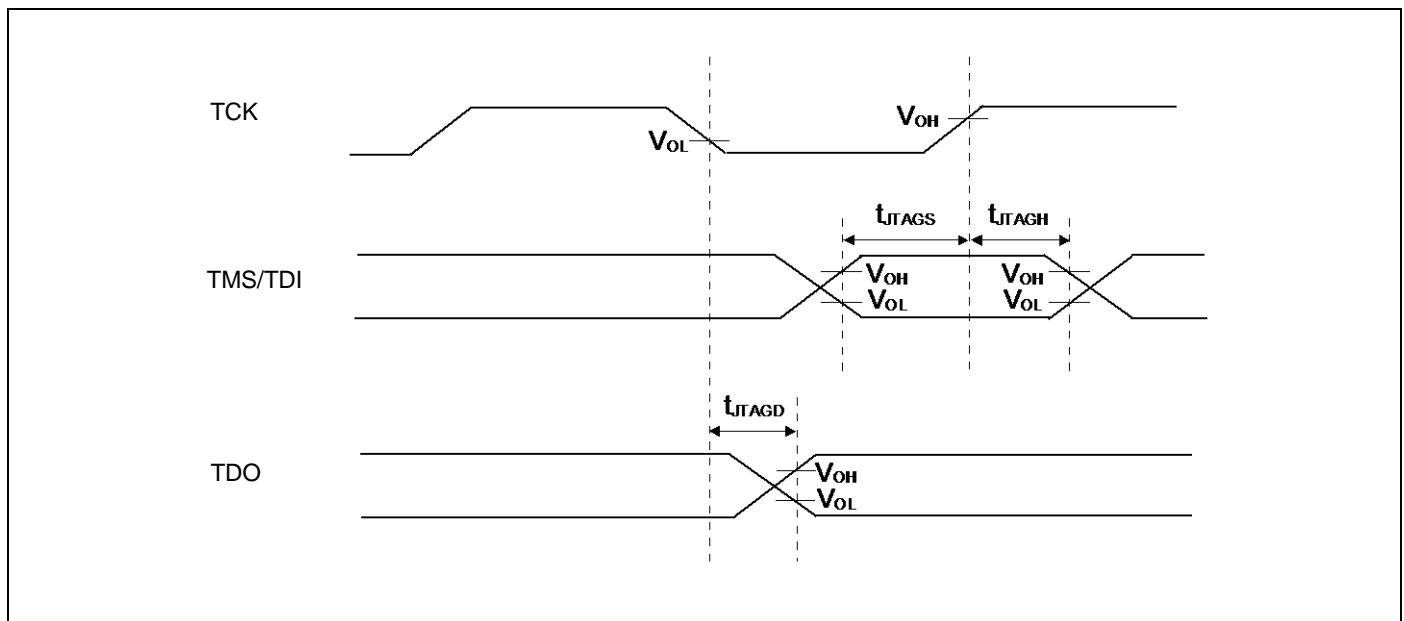
## 12.4.13 JTAG Timing

( $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ )

| Parameter           | Symbol             | Pin name         | Conditions                 | Value |     | Unit | Remarks |
|---------------------|--------------------|------------------|----------------------------|-------|-----|------|---------|
|                     |                    |                  |                            | Min   | Max |      |         |
| TMS, TDI setup time | $t_{JT\text{AGS}}$ | TCK,<br>TMS, TDI | $V_{CC} \geq 4.5\text{ V}$ | 15    | -   | ns   |         |
|                     |                    |                  | $V_{CC} < 4.5\text{ V}$    |       |     |      |         |
| TMS, TDI hold time  | $t_{JT\text{AGH}}$ | TCK,<br>TMS, TDI | $V_{CC} \geq 4.5\text{ V}$ | 15    | -   | ns   |         |
|                     |                    |                  | $V_{CC} < 4.5\text{ V}$    |       |     |      |         |
| TDO delay time      | $t_{JT\text{AGD}}$ | TCK,<br>TDO      | $V_{CC} \geq 4.5\text{ V}$ | -     | 25  | ns   |         |
|                     |                    |                  | $V_{CC} < 4.5\text{ V}$    | -     | 45  |      |         |

**Note:**

- When the external load capacitance = 30 pF.



## 12.5 12-bit A/D Converter

### Electrical characteristics for the A/D converter

( $V_{CC} = AV_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ )

| Parameter                                     | Symbol    | Pin name | Value      |     |           | Unit          | Remarks               |
|---|-----------|----------|------------|-----|-----------|---------------|-----------------------|
|   |           |          | Min        | Typ | Max       |               |                       |
| Resolution                                    | -         | -        | -          | -   | 12        | bit           |                       |
| Integral nonlinearity                         | -         | -        | - 4.5      | -   | + 4.5     | LSB           | AVRH = 2.7 V to 5.5 V |
| Differential nonlinearity                     | -         | -        | -2.5       | -   | + 2.5     | LSB           |                       |
| Zero transition voltage                       | $V_{ZT}$  | ANxx     | - 20       | -   | + 20      | mV            |                       |
| Full-scale transition voltage                 | $V_{FST}$ | ANxx     | AVRH - 20  | -   | AVRH + 20 | mV            |                       |
| Conversion time                               | -         | -        | $1.0^{*1}$ | -   | -         | $\mu\text{s}$ | AVCC $\geq$ 4.5 V     |
|   |           |          | $1.2^{*1}$ | -   | -         |               | AVCC < 4.5 V          |
| Sampling time                                 | $T_s$     | -        | *2         | -   | -         | ns            | AVCC $\geq$ 4.5 V     |
|   |           |          | *2         | -   | -         |               | AVCC < 4.5 V          |
| Compare clock cycle <sup>*3</sup>             | $T_{cck}$ | -        | 50         | -   | 2000      | ns            |                       |
| State transition time to operation permission | $T_{stt}$ | -        | -          | -   | 1.0       | $\mu\text{s}$ |                       |
| Analog input capacity                         | $C_{AIN}$ | -        | -          | -   | 12.9      | pF            |                       |
| Analog input resistance                       | $R_{AIN}$ | -        | -          | -   | 2         | k $\Omega$    | AVCC $\geq$ 4.5 V     |
|   |           |          |            |     | 3.8       |               | AVCC < 4.5 V          |
| Interchannel disparity                        | -         | -        | -          | -   | 4         | LSB           |                       |
| Analog port input leak current                | -         | ANxx     | -          | -   | 5         | $\mu\text{A}$ |                       |
| Analog input voltage                          | -         | ANxx     | AVSS       | -   | AVRH      | V             |                       |
| Reference voltage                             | -         | AVRH     | 2.7        | -   | AVCC      | V             |                       |

\*1: Conversion time is the value of sampling time ( $T_s$ ) + compare time ( $T_c$ ).

The condition of the minimum conversion time is the following.

AVCC  $\geq$  4.5 V, HCLK=40 MHz sampling time: 300 ns, compare time: 700 ns

AVCC < 4.5 V, HCLK=40 MHz sampling time: 500 ns, compare time: 700 ns

Ensure that it satisfies the value of sampling time ( $T_s$ ) and compare clock cycle ( $T_{cck}$ ).

For setting of sampling time and compare clock cycle, see "Chapter 1-1: A/D Converter" in "FM3 Family Peripheral Manual Analog Macro Part".

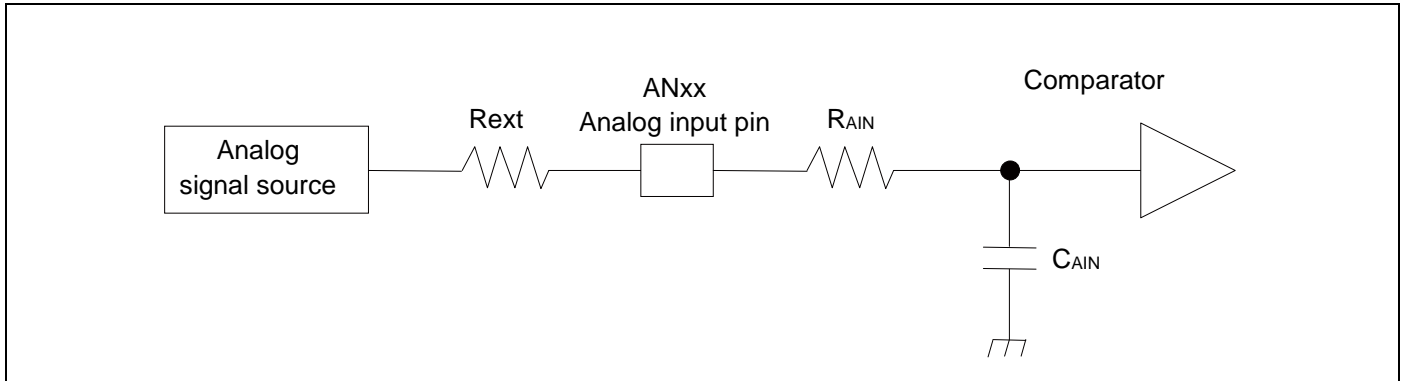
The A/D Converter register is set at APB bus clock timing. The sampling clock and compare clock are set at Base clock (HCLK).

About the APB bus number which the A/D Converter is connected to, see "8. Block Diagram" in this datasheet.

\*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1).

\*3: Compare time ( $T_c$ ) is the value of (Equation 2).



(Equation 1)  $T_s \geq (R_{AIN} + R_{ext}) \times C_{AIN} \times 9$

T<sub>s</sub>: Sampling time

R<sub>AIN</sub>: Input resistance of A/D = 2 kΩ at 4.5 V ≤ AV<sub>CC</sub> ≤ 5.5 V

Input resistance of A/D = 3.8 kΩ at 2.7 V ≤ AV<sub>CC</sub> ≤ 4.5 V

C<sub>AIN</sub>: Input capacity of A/D = 12.9 pF at 2.7 V ≤ AV<sub>CC</sub> ≤ 5.5 V

R<sub>ext</sub>: Output impedance of external circuit

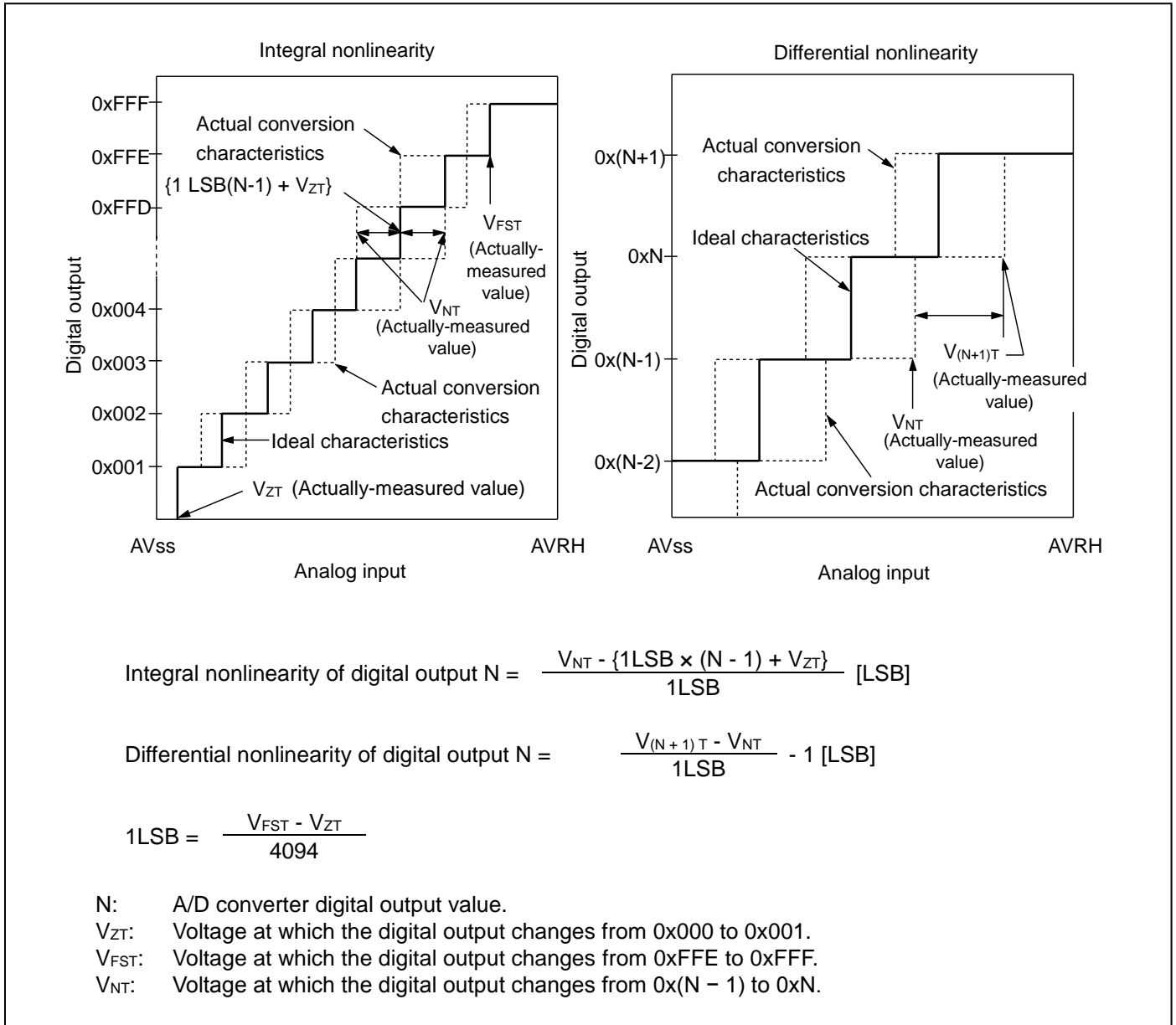
(Equation 2)  $T_c = T_{cck} \times 14$

T<sub>c</sub>: Compare time

T<sub>cck</sub>: Compare clock cycle

**Definition of 12-bit A/D converter terms**

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ←→ 0b000000000001) and the full-scale transition point (0b111111111110 ←→ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



**12.6 Low-Voltage Detection Characteristics**
**12.6.1 Low-Voltage Detection Reset**

 (T<sub>A</sub> = - 40°C to + 105°C)

| Parameter        | Symbol | Conditions | Value |      |      | Unit | Remarks            |
|------------------|--------|------------|-------|------|------|------|--------------------|
|                  |        |            | Min   | Typ  | Max  |      |                    |
| Detected voltage | VDL    | -          | 2.25  | 2.45 | 2.65 | V    | When voltage drops |
| Released voltage | VDH    | -          | 2.30  | 2.50 | 2.70 | V    | When voltage rises |

**12.6.2 Interrupt of Low-voltage Detection**

 (T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                   | Symbol            | Conditions  | Value |     |  | Unit | Remarks            |
|-----------------------------|-------------------|-------------|-------|-----|--|------|--------------------|
|                             |                   |             | Min   | Typ | Max                                    |      |                    |
| Detected voltage            | VDL               | SVHI = 0000 | 2.58  | 2.8 | 3.02                                   | V    | When voltage drops |
| Released voltage            | VDH               |             | 2.67  | 2.9 | 3.13                                   | V    | When voltage rises |
| Detected voltage            | VDL               | SVHI = 0001 | 2.76  | 3.0 | 3.24                                   | V    | When voltage drops |
| Released voltage            | VDH               |             | 2.85  | 3.1 | 3.34                                   | V    | When voltage rises |
| Detected voltage            | VDL               | SVHI = 0010 | 2.94  | 3.2 | 3.45                                   | V    | When voltage drops |
| Released voltage            | VDH               |             | 3.04  | 3.3 | 3.56                                   | V    | When voltage rises |
| Detected voltage            | VDL               | SVHI = 0011 | 3.31  | 3.6 | 3.88                                   | V    | When voltage drops |
| Released voltage            | VDH               |             | 3.40  | 3.7 | 3.99                                   | V    | When voltage rises |
| Detected voltage            | VDL               | SVHI = 0100 | 3.40  | 3.7 | 3.99                                   | V    | When voltage drops |
| Released voltage            | VDH               |             | 3.50  | 3.8 | 4.10                                   | V    | When voltage rises |
| Detected voltage            | VDL               | SVHI = 0111 | 3.68  | 4.0 | 4.32                                   | V    | When voltage drops |
| Released voltage            | VDH               |             | 3.77  | 4.1 | 4.42                                   | V    | When voltage rises |
| Detected voltage            | VDL               | SVHI = 1000 | 3.77  | 4.1 | 4.42                                   | V    | When voltage drops |
| Released voltage            | VDH               |             | 3.86  | 4.2 | 4.53                                   | V    | When voltage rises |
| Detected voltage            | VDL               | SVHI = 1001 | 3.86  | 4.2 | 4.53                                   | V    | When voltage drops |
| Released voltage            | VDH               |             | 3.96  | 4.3 | 4.64                                   | V    | When voltage rises |
| LVD stabilization wait time | T <sub>LVDW</sub> | -           | -     | -   | 2240 × t <sub>CYCP</sub> <sup>*1</sup> | μs   |                    |

 \*1: t<sub>CYCP</sub> indicates the APB2 bus clock cycle time.

**12.7 MainFlash Memory Write/Erase Characteristics**
**12.7.1 Write / Erase time**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                     |              | Value             |                   | Unit | Remarks                                     |
|-------------------------------|--------------|-------------------|-------------------|------|---|
|                               |              | Typ <sup>*1</sup> | Max <sup>*1</sup> |      |   |
| Sector erase time             | Large Sector | 0.7               | 3.7               | s    | Includes write time prior to internal erase |
|                               | Small Sector | 0.3               | 1.1               |      |   |
| Half word (16-bit) write time |              | 12                | 384               | μs   | Not including system-level overhead time    |
| Chip erase time               |              | 3.8               | 16.2              | s    | Includes write time prior to internal erase |

\*1: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

**12.7.2 Erase/write cycles and data hold time**

| Erase/write cycles (cycle) | Data hold time (year) |
|----------------------------|-----------------------|
| 1,000                      | 20 <sup>*1</sup>      |
| 10,000                     | 10 <sup>*1</sup>      |
| 100,000                    | 5 <sup>*1</sup>       |

\*1: At average + 85°C

**12.8 WorkFlash Memory Write/Erase Characteristics**
**12.8.1 Write / Erase time**

 (V<sub>CC</sub> = 2.7 V to 5.5 V, T<sub>A</sub> = - 40°C to + 105°C)

| Parameter                     |  | Value             |                   | Unit | Remarks                                     |
|-------------------------------|--|-------------------|-------------------|------|---|
|                               |  | Typ <sup>*1</sup> | Max <sup>*1</sup> |      |   |
| Sector erase time             |  | 0.3               | 1.5               | s    | Includes write time prior to internal erase |
| Half word (16-bit) write time |  | 20                | 384               | μs   | Not including system-level overhead time    |
| Chip erase time               |  | 1.2               | 6                 | s    | Includes write time prior to internal erase |

\*1: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

**12.8.2 Erase/write cycles and data hold time**

| Erase/write cycles (cycle) | Data hold time (year) |
|----------------------------|-----------------------|
| 1,000                      | 20 <sup>*1</sup>      |
| 10,000                     | 10 <sup>*1</sup>      |

\*1: At average + 85°C

## 12.9 Return Time from Low-Power Consumption Mode

### 12.9.1 Return Factor: Interrupt/WKUP

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

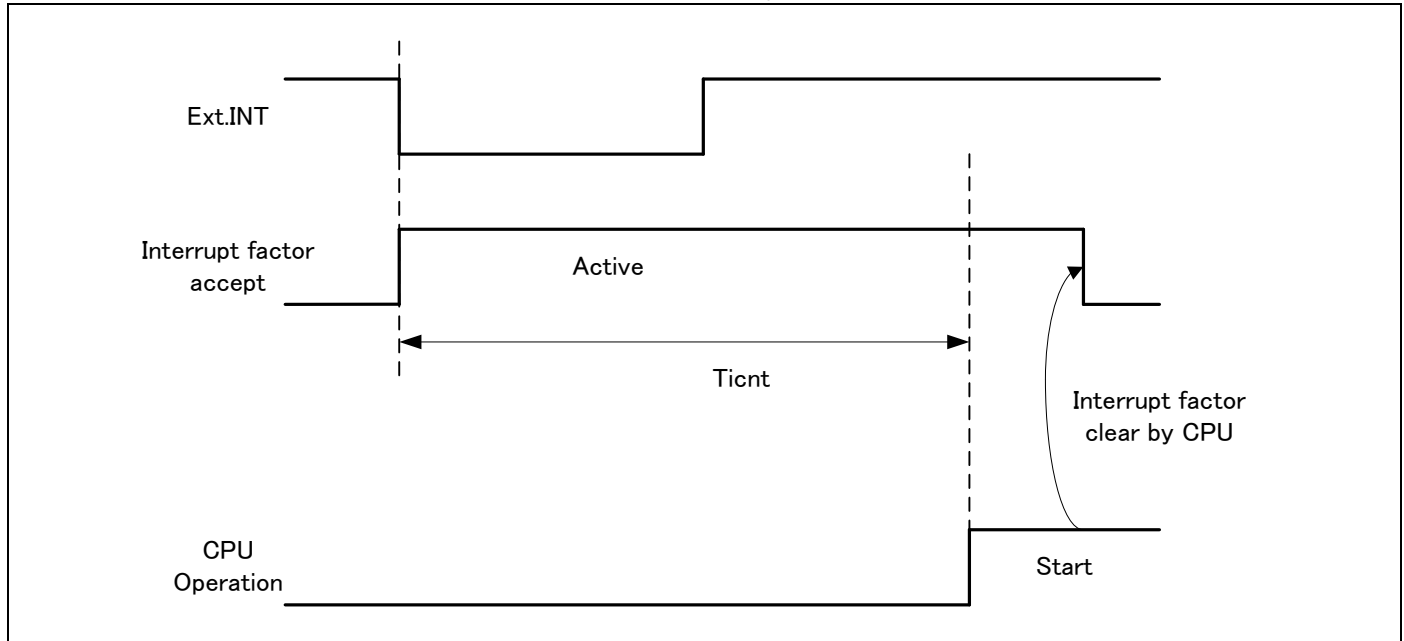
#### Return count time

( $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ )

| Parameter   | Symbol | Value |       | Unit          | Remarks |
|---|--------|-------|-------|---------------|---------|
|   |        | Typ   | Max*1 |               |         |
| SLEEP mode  | Ticnt  | tcycc |       | ns            |         |
| High-speed CR TIMER mode,<br>Main TIMER mode,<br>PLL TIMER mode |        | 40    | 80    | $\mu\text{s}$ |         |
| Low-speed CR TIMER mode   |        | 370   | 740   | $\mu\text{s}$ |         |
| Sub TIMER mode  |        | 699   | 929   | $\mu\text{s}$ |         |
| STOP mode   |        | 505   | 834   | $\mu\text{s}$ |         |

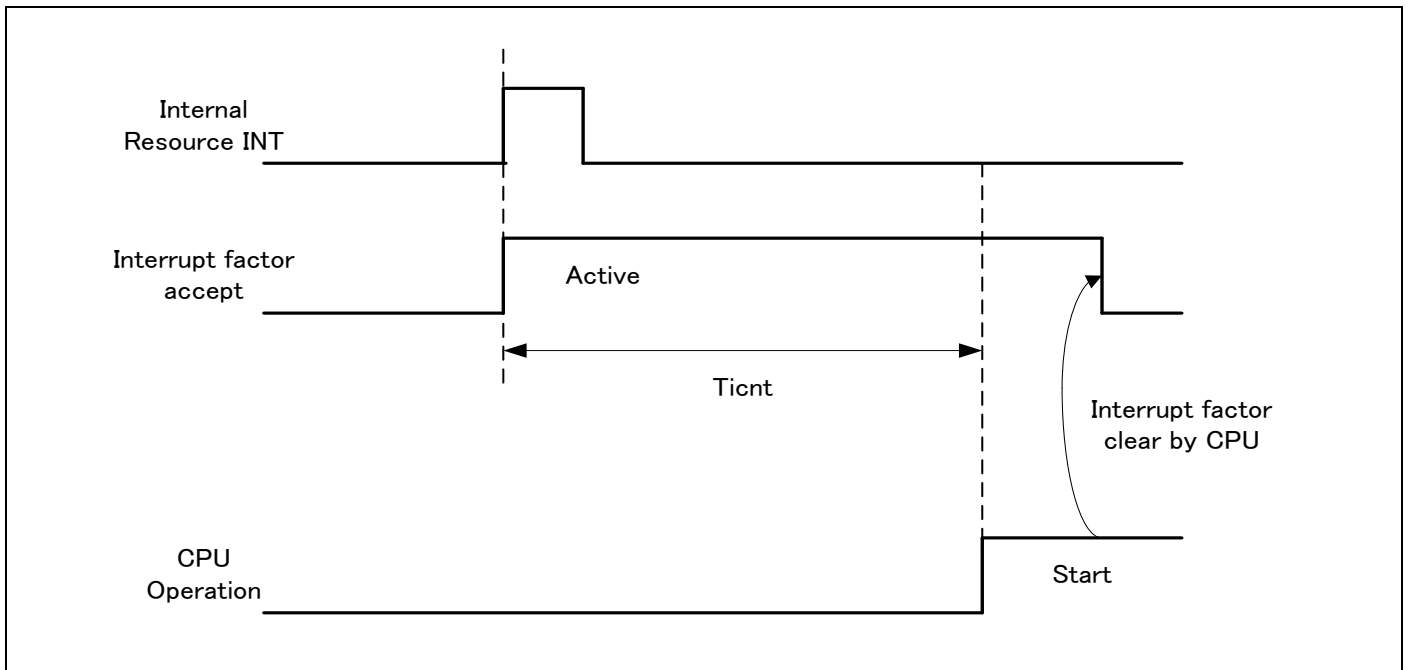
\*1: The maximum value depends on the accuracy of built-in CR.

#### Operation example of return from Low-Power consumption mode (by external interrupt\*1)



\*1: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt<sup>\*1</sup>)



\*1: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

**Notes:**

- The return factor is different in each Low-Power consumption modes. See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual about the return factor from Low-Power consumption mode.
- When interrupt recovers, the operation mode that CPU recovers depends on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual".



**12.9.2 Return Factor: Reset**

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

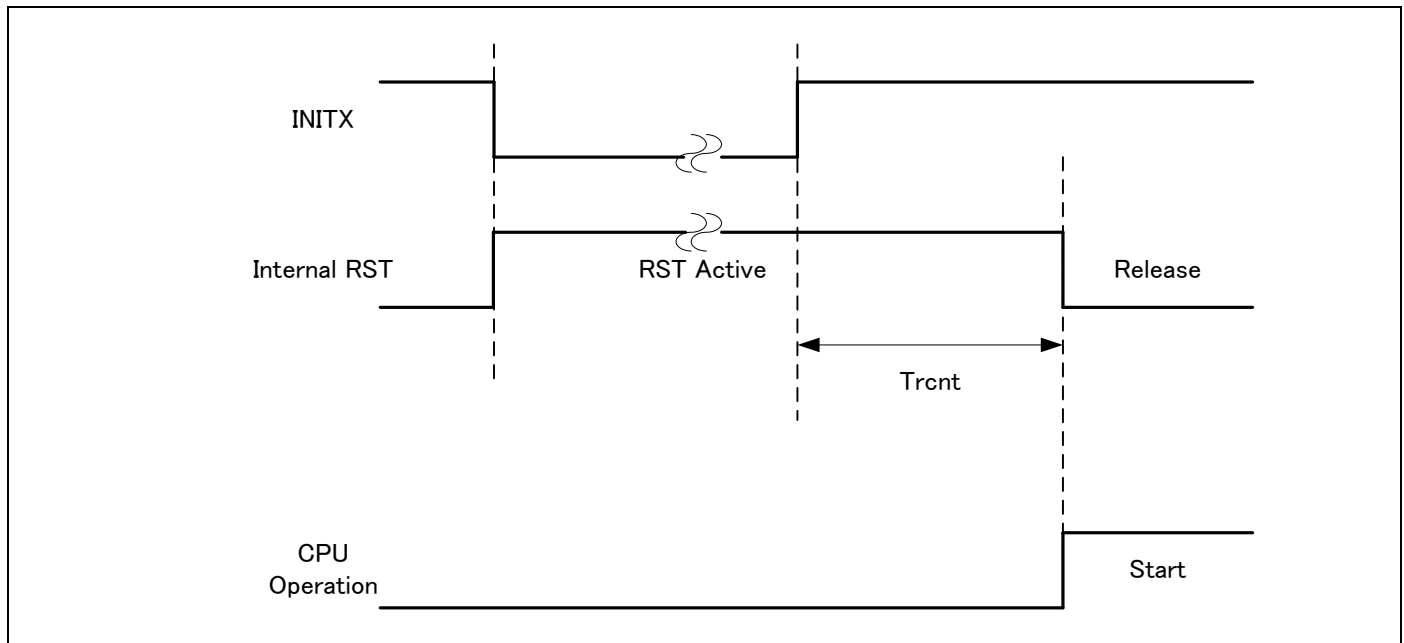
**Return count time**

( $V_{CC} = 2.7\text{ V to }5.5\text{ V}$ ,  $T_A = -40^{\circ}\text{C to }+105^{\circ}\text{C}$ )

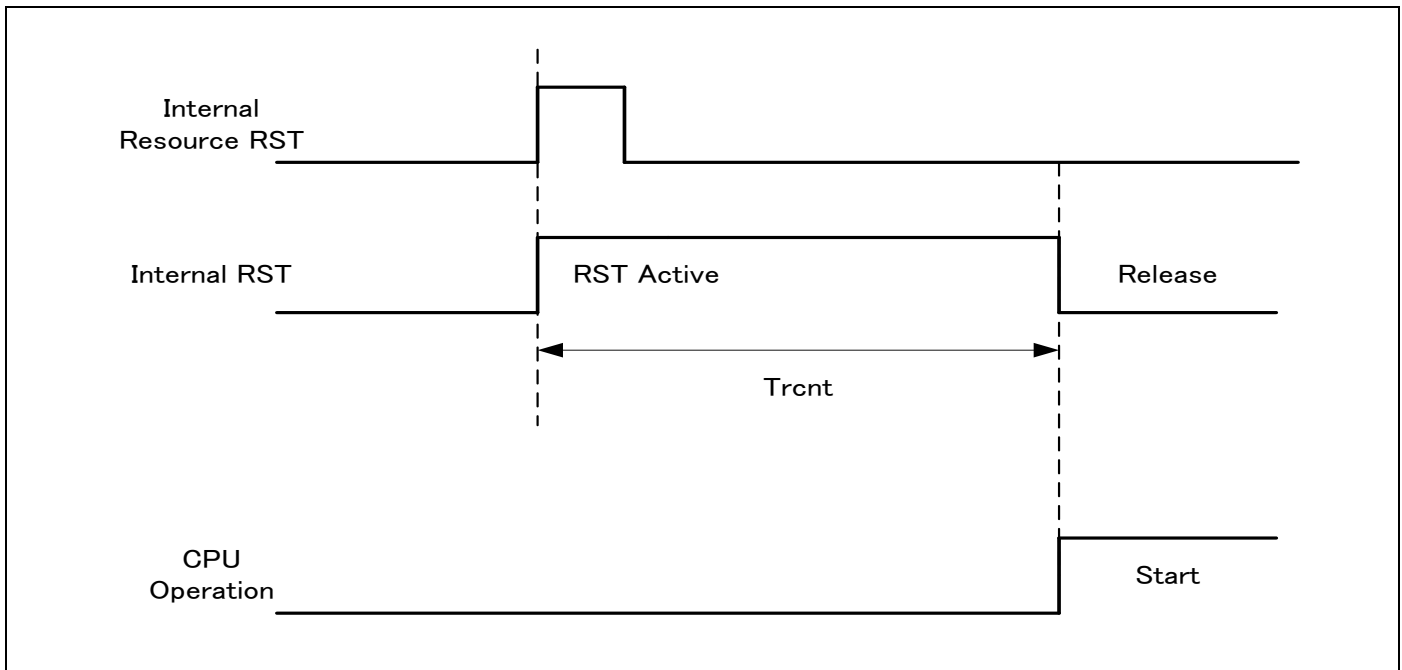
| Parameter   | Symbol | Value |                   | Unit | Remarks |
|---|--------|-------|-------------------|------|---------|
|   |        | Typ   | Max <sup>*1</sup> |      |         |
| SLEEP mode  | Trcnt  | 365   | 554               | μs   |         |
| High-speed CR TIMER mode,<br>Main TIMER mode,<br>PLL TIMER mode |        | 365   | 554               | μs   |         |
| Low-speed CR TIMER mode   |        | 555   | 934               | μs   |         |
| Sub TIMER mode  |        | 608   | 976               | μs   |         |
| STOP mode   |        | 475   | 774               | μs   |         |

\*1: The maximum value depends on the accuracy of built-in CR.

**Operation example of return from Low-Power consumption mode (by INITX)**



## Operation example of return from low power consumption mode (by internal resource reset<sup>\*1</sup>)



\*1: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

### Notes:

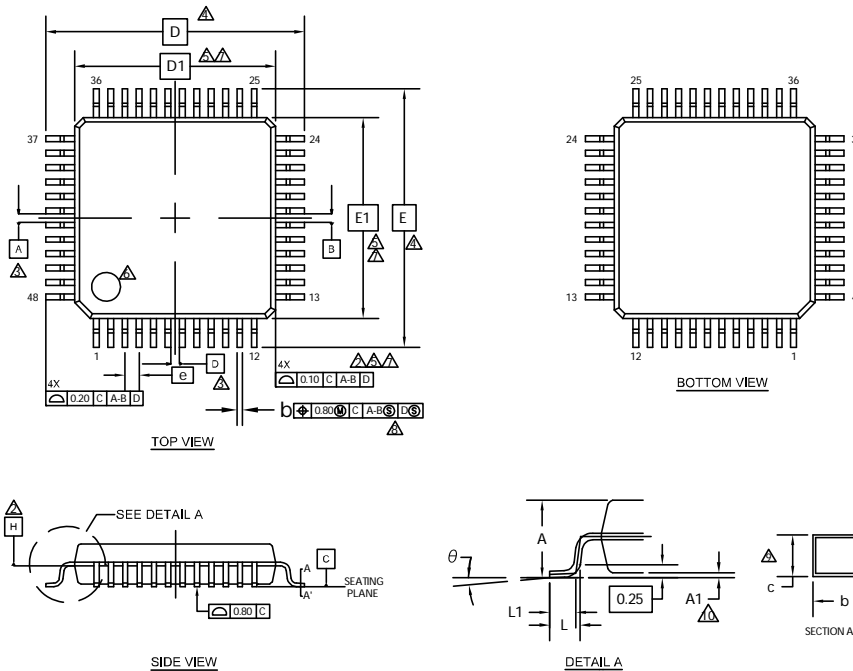
- The return factor is different in each Low-Power consumption modes. See "Chapter 6: Low Power Consumption Mode" and "Operations of Standby Modes" in FM3 Family Peripheral Manual.
- When interrupt recovers, the operation mode that CPU recovers depends on the state before the Low-Power consumption mode transition. See "Chapter 6: Low Power Consumption Mode" in "FM3 Family Peripheral Manual".
- The time during the power-on reset/low-voltage detection reset is excluded. See "12.4.7. Power-on Reset Timing in 12.4. AC Characteristics in 12. Electrical Characteristics" for the detail on the time during the power-on reset/low-voltage detection reset.
- When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.
- The internal resource reset means the watchdog reset and the CSV reset.

**13. Ordering Information**

| Part number          | On-chip Flash memory        | On-chip SRAM | Package   | Packing |
|----------------------|-----------------------------|--------------|---|---------|
| MB9AF111KPMC-G-JNE2  | Main: 64 KB<br>Work: 32 KB  | 16 KB        | Plastic • LQFP<br>48-pin (0.5 mm pitch),<br>(LQA048)  | Tray    |
| MB9AF112KPMC-G-JNE2  | Main: 128 KB<br>Work: 32 KB | 16 KB        |   |         |
| MB9AF111KPMC1-G-JNE2 | Main: 64 KB<br>Work: 32 KB  | 16 KB        | Plastic • LQFP<br>52-pin (0.65 mm pitch),<br>(LQC052) |         |
| MB9AF112KPMC1-G-JNE2 | Main: 128 KB<br>Work: 32 KB | 16 KB        |   |         |
| MB9AF111KQN-G-AVE2   | Main: 64 KB<br>Work: 32 KB  | 16 KB        | Plastic • QFN<br>48-pin (0.5 mm pitch),<br>(VNA048)   |         |
| MB9AF112KQN-G-AVE2   | Main: 128 KB<br>Work: 32 KB | 16 KB        |   |         |

## 14. Package Dimensions

| Package Type             | Package Code |
|--------------------------|--------------|
| LQFP 48pin (0.5mm pitch) | LQA048       |



| SYMBOL   | DIMENSIONS |      |      |
|----------|------------|------|------|
|          | MIN.       | NOM. | MAX. |
| A        | —          | —    | 1.70 |
| A1       | 0.00       | —    | 0.20 |
| b        | 0.15       | —    | 0.27 |
| c        | 0.09       | —    | 0.20 |
| D        | 9.00 BSC   |      |      |
| D1       | 7.00 BSC   |      |      |
| e        | 0.50 BSC   |      |      |
| E        | 9.00 BSC   |      |      |
| E1       | 7.00 BSC   |      |      |
| L        | 0.45       | 0.60 | 0.75 |
| L1       | 0.30       | 0.50 | 0.70 |
| $\theta$ | 0°         | —    | 8°   |

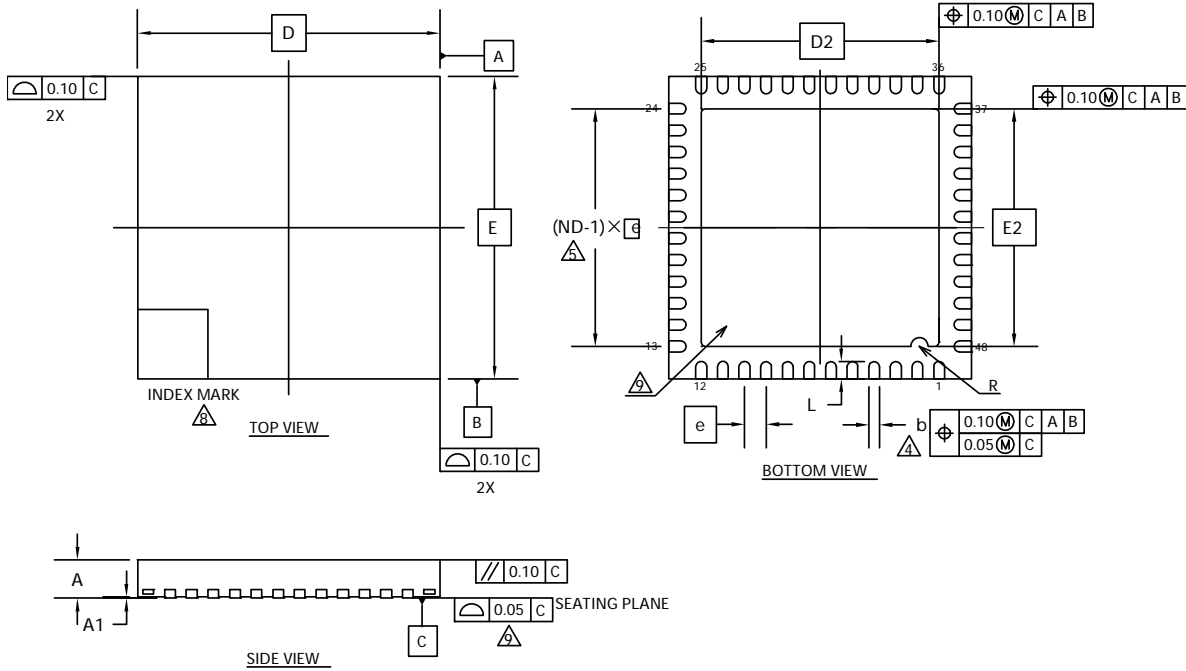
### NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 48 LEAD LQFP  
7.0X7.0X1.7 MM LQA048 REV\*\*

002-13731 \*\*

|                         |                     |
|-------------------------|---------------------|
| <b>Package Type</b>     | <b>Package Code</b> |
| QFN 48pin (0.5mm pitch) | VNA048              |



| SYMBOL | DIMENSIONS |      |      |
|--------|------------|------|------|
|        | MIN.       | NOM. | MAX. |
| A      | —          | —    | 0.90 |
| A1     | 0.00       | —    | 0.05 |
| D      | 7.00 BSC   |      |      |
| E      | 7.00 BSC   |      |      |
| b      | 0.20       | 0.25 | 0.30 |
| D2     | 5.50 BSC   |      |      |
| E2     | 5.50 BSC   |      |      |
| e      | 0.50 BSC   |      |      |
| R      | 0.20 REF   |      |      |
| L      | 0.35       | 0.40 | 0.45 |

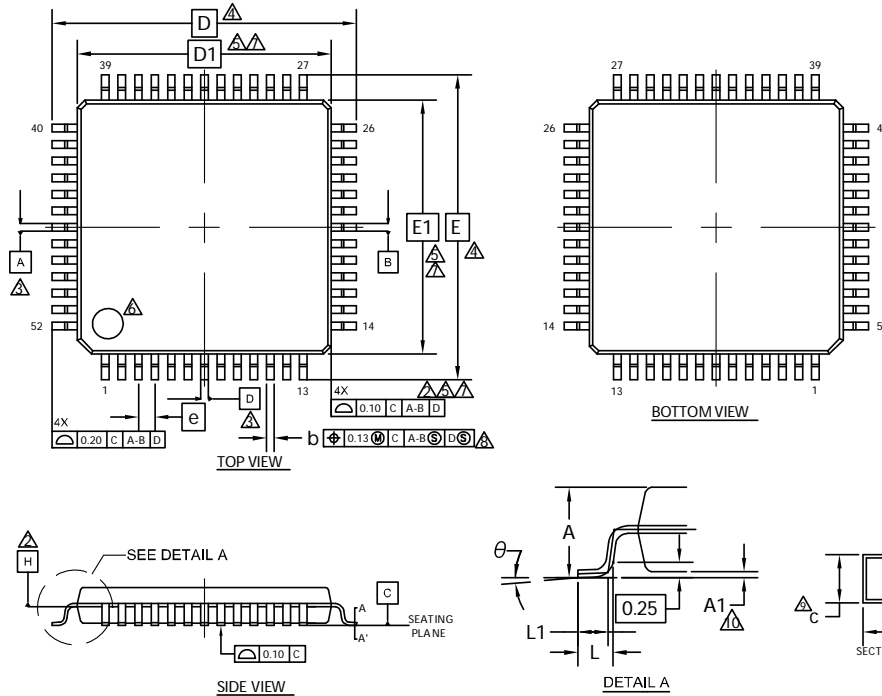
**NOTE**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
- N IS THE TOTAL NUMBER OF TERMINALS.
- △ DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
- △ ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
- MAX. PACKAGE WARPAGE IS 0.05mm.
- MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
- △ PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
- △ BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- JEDEC SPECIFICATION NO. REF: N/A

PACKAGE OUTLINE, 48 LEAD QFN  
7.0K7.0K0.9MMVNA048 5.5X5.5MM EPAD (\$AWN) REV\*\*

002-15528 \*\*

| Package Type              | Package Code |
|---------------------------|--------------|
| LQFP 52pin (0.65mm pitch) | LQC052       |



| SYMBOL   | DIMENSION |      |       |
|----------|-----------|------|-------|
|          | MIN.      | NOM. | MAX.  |
| A        | —         | —    | 1.70  |
| A1       | 0.00      | —    | 0.20  |
| b        | 0.265     | 0.30 | 0.365 |
| c        | 0.09      | —    | 0.20  |
| D        | 12.00 BSC |      |       |
| D1       | 10.00 BSC |      |       |
| e        | 0.65 BSC  |      |       |
| E        | 12.00 BSC |      |       |
| E1       | 10.00 BSC |      |       |
| L        | 0.45      | 0.60 | 0.75  |
| L1       | 0.30      | 0.50 | 0.70  |
| $\theta$ | 0°        | —    | 8°    |

### NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

## 15. Major Changes

Spanion Publication Number: DS706-00030

| Page         | Section   | Change Results   |
|--------------|---|--|
| Revision 1.0 |   |  |
| -            | -   | PRELIMINARY → Datasheet  |
| 7            | PRODUCT LINEUP<br>Function  | Added the pin count.   |
| 8            | PACKAGES  | Revised from "Planning".   |
| 23           | I/O CIRCUIT TYPE  | Corrected the following description to "TypeB".<br>Digital output → Digital input  |
| 34           | BLOCK DIAGRAM   | Corrected the following description.<br>· AHB (Max 40MHz) → AHB (Max 42MHz)<br>· APB0 (Max 40MHz) → APB0 (Max 42MHz)<br>· APB1 (Max 40MHz) → APB1 (Max 42MHz)<br>· APB2 (Max 40MHz) → APB2 (Max 42MHz)<br>Deleted the description for "USB Clock Ctrl / PLL".                |
| 45, 46       | ELECTRICAL CHARACTERISTICS<br>3. DC Characteristics<br>(1) Current Rating                   | Revised the value of "TBD".<br>Corrected the value.<br>- Power supply current (I <sub>CCR</sub> )<br>Typ: 60 → 50<br>- Power supply current (I <sub>CCRD</sub> ) (RAM hold off)<br>Typ: 45 → 30<br>- Power supply current (I <sub>CCRD</sub> ) (RAM hold on)<br>Typ: 48 → 33 |
| 61           | (9) External Input Timing   | Revised the value of "TBD".  |
| 66           | 5. 12-bit A/D Converter<br>Electrical characteristics for the A/D converter                 | Deleted "(Preliminary value)".<br>Corrected the value of "Compare clock cycle".<br>Max: 10000 → 2000   |
| 70           | 7. MainFlash Memory Write/Erase<br>Characteristics<br>Erase/write cycles and data hold time | Deleted "(targeted value)".  |
|              | 8. WorkFlash Memory Write/Erase<br>Characteristics<br>Erase/write cycles and data hold time |  |
| Revision 1.1 |   |  |
| -            | -   | Company name and layout design change  |
| Revision 2.0 |   |  |
| 25           | I/O Circuit Type  | Added the description of I <sup>2</sup> C to the type of E and F   |
| 25, 26       | I/O Circuit Type  | Added about +B input   |
| 32           | Handling Devices  | Added "Stabilizing power supply voltage"   |
| 32           | Handling Devices<br>Crystal oscillator circuit  | Added the following description<br>"Evaluate oscillation of your using crystal oscillator by your mount board."  |
| 33           | Handling Devices<br>C Pin   | Changed the description  |
| 34           | Block Diagram   | Modified the block diagram   |
| 35           | Memory Map<br>Memory map(1)   | Modified the area of "External Device Area"  |
| 36           | Memory Map<br>Memory map(2)   | Added the summary of Flash memory sector and the note  |
| 43, 44       | Electrical Characteristics<br>1. Absolute Maximum Ratings                                   | Added the Clamp maximum current<br>Added the output current of P80 and P81<br>Added about +B input   |
| 45           | Electrical Characteristics<br>2. Recommended Operation Conditions                           | Modified the minimum value of Analog reference voltage<br>Added Smoothing capacitor<br>Added the note about less than the minimum power supply voltage   |
| 46-48        | Electrical Characteristics<br>3. DC Characteristics<br>(1) Current rating                   | Changed the table format<br>Added Main TIMER mode current<br>Added Flash Memory Current<br>Moved A/D Converter Current   |

| Page  | Section   | Change Results   |
|-------|---|--|
| 51    | Electrical Characteristics<br>4. AC Characteristics<br>(1) Main Clock Input Characteristics   | Added Master clock at Internal operating clock frequency   |
| 52    | Electrical Characteristics<br>4. AC Characteristics<br>(3) Built-in CR Oscillation Characteristics                                      | Added Frequency stability time at Built-in high-speed CR   |
| 53    | Electrical Characteristics<br>4. AC Characteristics<br>(4-1) Operating Conditions of Main PLL<br>(4-2) Operating Conditions of Main PLL | Added Main PLL clock frequency<br>Added the figure of Main PLL connection  |
| 54    | Electrical Characteristics<br>4. AC Characteristics<br>(6) Power-on Reset Timing  | Added Time until releasing Power-on reset<br>Changed the figure of timing  |
| 56-63 | Electrical Characteristics<br>4. AC Characteristics<br>(7) CSIO/UART Timing   | Modified from UART Timing to CSIO/UART Timing<br>Changed from Internal shift clock operation to Master mode<br>Changed from External shift clock operation to Slave mode   |
| 69    | Electrical Characteristics<br>5. 12bit A/D Converter  | Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage<br>Added Conversion time at AVcc < 4.5 V<br>Modified Stage transition time to operation permission<br>Modified the minimum value of Reference voltage |
| 74-77 | Electrical Characteristics<br>9. Return Time from Low-Power Consumption Mode  | Added Return Time from Low-Power Consumption Mode  |
| 78    | Ordering Information  | Changed the description of part number   |

Note: Please see “Document History” about later revised information.



## Document History

Document Title: MB9A110K Series 32-bit ARM® Cortex®-M3, FM3 Microcontroller

Document Number: 002-05627

| Revision | ECN     | Orig. of Change | Submission Date | Description of Change  |
|----------|---------|-----------------|-----------------|--|
| **       | –       | TOYO            | 02/20/2015      | Migrated to Cypress and assigned document number 002-05627.<br>No change to document contents or format.   |
| *A       | 5226072 | TOYO            | 04/18/2016      | Updated to Cypress format.   |
| *B       | 5561750 | YSKA            | 03/22/2017      | <p>Changed an explanation from “from 01 to 99” to “from 00 to 99” in Real-Time Clock (RTC) (Page 2) of Features, and Deleted “Second/A day of the week” of interrupt function.</p> <p>Changed package code as the following in chapter :</p> <ul style="list-style-type: none"> <li><a href="#">2. Packages</a></li> <li><a href="#">3. Pin Assignment</a></li> <li><a href="#">13. Ordering Information</a></li> <li><a href="#">14. Package Dimensions.</a></li> </ul> <p>FTP-48P-M49 -&gt; LQA048, LCC-48P-M73 -&gt; VNA048,<br/>FPT-52P-M02 -&gt; LQC052</p> <p>Corrected “J-TAG” to “JTAG” in <a href="#">4. List of Pin Functions</a>.</p> <p>Added Note for JTAG pin in <a href="#">4. List of Pin Functions</a>.</p> <p>Changed remark [1] to “When all ports are input and are fixed at “0”.” in <a href="#">12.3.1 Current Rating</a>.</p> <p>Changed Parameter “Power supply rising time (<math>t_{VCCR}</math>)” to “Power ramp rate (dV/dt)” in <a href="#">12.4.7 Power-on Reset Timing</a>, Changed the minimum to 0.7mV/μs, Changed the maximum to 1000mV/μs, and Added remarks and note.</p> <p>Corrected “Analog port input current” to “Analog port input leak current” in <a href="#">12.5 12-bit A/D Converter</a>.</p> <p>Added the Baud rate spec in “12.4.9 CSIO/UART Timing”(Page 52, 54, 56, 58)</p> |

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