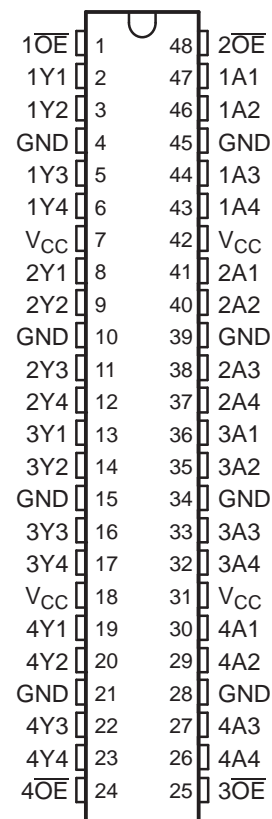


## FEATURES

- Member of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

SN54LVT16244B . . . WD PACKAGE  
SN74LVT16244B . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVT16244BGRDR	VD244B
	FBGA – ZRD (Pb-free)		SN74LVT16244BZRDR	
	SSOP – DL	Tube of 25	SN74LVT16244BDL	LVT16244B
			SN74LVT16244BDLG4	
		Reel of 1000	SN74LVT16244BDLR 74LVT16244BDLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVT16244BDGGR	LVT16244B
			74LVT16244BDGGRG4	
	TVSOP – DGV	Reel of 2000	SN74LVT16244BDGVR	VD244B
			74LVT16244BDGVRE4	
	VFBGA – GQL	Reel of 1000	SN74LVT16244BGQLR	VD244B
SN74LVT16244BZQLR				
VFBGA – ZQL (Pb-free)	Reel of 1000	SN74LVT16244BZQLR	VD244B	
		SN74LVT16244BZQLR		
-55°C to 125°C	CFP – WD	Tube	SNJ54LVT16244BWD	SNJ54LVT16244BWD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN54LVT16244B, SN74LVT16244B 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS716E—MARCH 2000—REVISED DECEMBER 2006

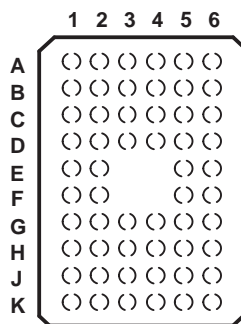
## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The 'LVT16244B devices are 16-bit buffers and line drivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable ( $\overline{OE}$ ) inputs.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**GQL OR ZQL PACKAGE  
(TOP VIEW)**

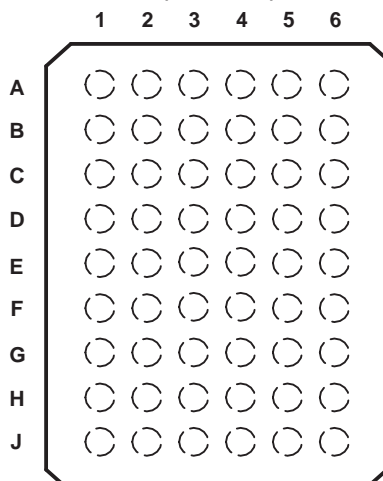


**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
<b>A</b>	1 $\overline{OE}$	NC	NC	NC	NC	2 $\overline{OE}$
<b>B</b>	1Y2	1Y1	GND	GND	1A1	1A2
<b>C</b>	1Y4	1Y3	$V_{CC}$	$V_{CC}$	1A3	1A4
<b>D</b>	2Y2	2Y1	GND	GND	2A1	2A2
<b>E</b>	2Y4	2Y3			2A3	2A4
<b>F</b>	3Y1	3Y2			3A2	3A1
<b>G</b>	3Y3	3Y4	GND	GND	3A4	3A3
<b>H</b>	4Y1	4Y2	$V_{CC}$	$V_{CC}$	4A2	4A1
<b>J</b>	4Y3	4Y4	GND	GND	4A4	4A3
<b>K</b>	4 $\overline{OE}$	NC	NC	NC	NC	3 $\overline{OE}$

(1) NC – No internal connection

**GRD OR ZRD PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(54-Ball GRD/ZRD Package)**

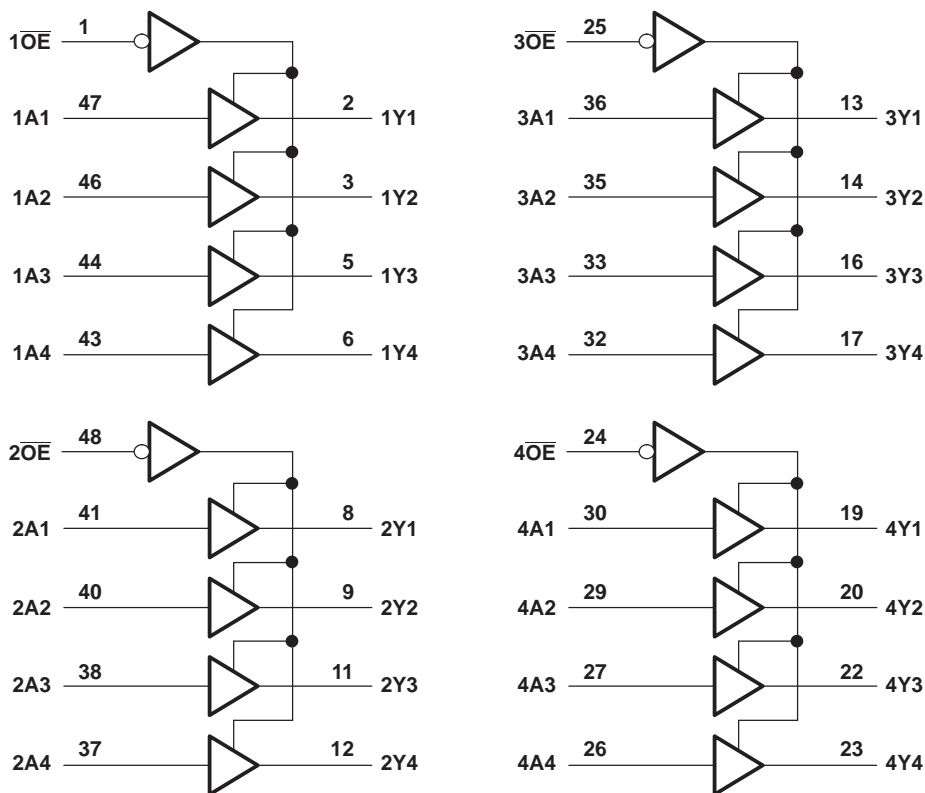
	1	2	3	4	5	6
<b>A</b>	1Y1	NC	1 $\overline{OE}$	2 $\overline{OE}$	NC	1A1
<b>B</b>	1Y3	1Y2	NC	NC	1A2	1A3
<b>C</b>	2Y1	1Y4	$V_{CC}$	$V_{CC}$	1A4	2A1
<b>D</b>	2Y3	2Y2	GND	GND	2A2	2A3
<b>E</b>	3Y1	2Y4	GND	GND	2A4	3A1
<b>F</b>	3Y3	3Y2	GND	GND	3A2	3A3
<b>G</b>	4Y1	3Y4	$V_{CC}$	$V_{CC}$	3A4	4A1
<b>H</b>	4Y3	4Y2	NC	NC	4A2	4A3
<b>J</b>	4Y4	NC	4 $\overline{OE}$	3 $\overline{OE}$	NC	4A4

(1) NC – No internal connection

**FUNCTION TABLE  
(EACH 4-BIT BUFFER)**

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers shown are for the DGG, DGV, DL, and WD packages.

# SN54LVT16244B, SN74LVT16244B 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS716E—MARCH 2000—REVISED DECEMBER 2006

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Voltage range applied to any output in the high state <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>O</sub>	Current into any output in the low state	SN54LVT16244B	96	mA
		SN74LVT16244B	128	
I <sub>O</sub>	Current into any output in the high state <sup>(3)</sup>	SN54LVT16244B	48	mA
		SN74LVT16244B	64	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(4)</sup>	DGG package	70	°C/W
		DGV package	58	
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
T <sub>stg</sub>	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This current flows only when the output is in the high state and V<sub>O</sub> > V<sub>CC</sub>.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

		SN54LVT16244B <sup>(2)</sup>		SN74LVT16244B		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage		5.5		5.5	V
I <sub>OH</sub>	High-level output current		-24		-32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate	200		200		μs/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(2) Product preview

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16244B <sup>(1)</sup>			SN74LVT16244B			UNIT	
			MIN	TYP <sup>(2)</sup>	MAX	MIN	TYP <sup>(2)</sup>	MAX		
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$		-1.2			-1.2			V	
$V_{OH}$	$V_{CC} = 2.7\text{ to }3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC} - 0.2$			$V_{CC} - 0.2$			V	
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4			2.4				
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2			2				
$I_{OH} = -32\text{ mA}$										
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$	0.2			0.2			V	
		$I_{OL} = 24\text{ mA}$	0.5			0.5				
		$I_{OL} = 16\text{ mA}$	0.4			0.4				
	$V_{CC} = 3\text{ V}$	$I_{OL} = 32\text{ mA}$	0.5			0.5				
		$I_{OL} = 48\text{ mA}$	0.55			0.55				
		$I_{OL} = 64\text{ mA}$				0.55				
$I_I$	$V_{CC} = 0\text{ or }3.6\text{ V}$ , $V_I = 5.5\text{ V}$		50			10			$\mu\text{A}$	
	Control inputs	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$		$\pm 1$			$\pm 1$			
		Data inputs	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$	1			1		
$V_I = 0$	-5			-5						
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$					$\pm 100$			$\mu\text{A}$	
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$		5			5			$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$		-5			-5			$\mu\text{A}$	
$I_{OZPU}$	$V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $\overline{OE} = \text{don't care}$		$\pm 100^{(3)}$			$\pm 100$			$\mu\text{A}$	
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $\overline{OE} = \text{don't care}$		$\pm 100^{(3)}$			$\pm 100$			$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high	0.19			0.19			mA	
		Outputs low	5			5				
		Outputs disabled	0.19			0.19				
$\Delta I_{CC}^{(4)}$	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$		0.2			0.2			mA	
$C_i$	$V_I = 3\text{ V or }0$		4			4			pF	
$C_o$	$V_O = 3\text{ V or }0$		9			9			pF	

(1) Product preview

 (2) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

 (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

# SN54LVT16244B, SN74LVT16244B 3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS716E—MARCH 2000—REVISED DECEMBER 2006

## Switching Characteristics

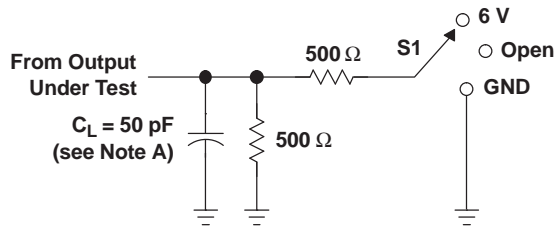
over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16244B <sup>(1)</sup>				SN74LVT16244B				UNIT	
			$V_{CC} = 3.3$ V $\pm 0.3$ V		$V_{CC} = 2.7$ V		$V_{CC} = 3.3$ V $\pm 0.3$ V			$V_{CC} = 2.7$ V		
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(2)</sup>	MAX	MIN		MAX
$t_{PLH}$	A	Y	1.1	4.4	4.6		1.2	2.3	3.2	3.7		ns
$t_{PHL}$			1.1	3.6	3.9		1.2	2	3.2	3.7		
$t_{PZH}$	$\overline{OE}$	Y	1.1	4.6	5.4		1.2	2.6	4	5		ns
$t_{PZL}$			1.1	5.4	6.2		1.2	2.7	4	5		
$t_{PHZ}$	$\overline{OE}$	Y	1.6	5.7	6.2		2.2	3.3	4.5	5		ns
$t_{PLZ}$			1.2	5	4.7		2	3.1	4.2	4.4		
$t_{sk(LH)}$									0.5			ns
$t_{sk(HL)}$									0.5			

(1) Product preview

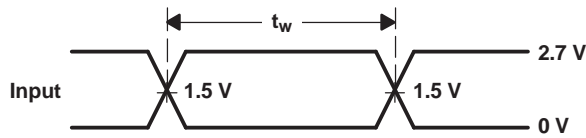
(2) All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$ .

PARAMETER MEASUREMENT INFORMATION

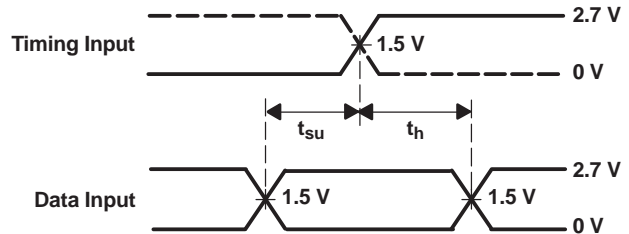


LOAD CIRCUIT

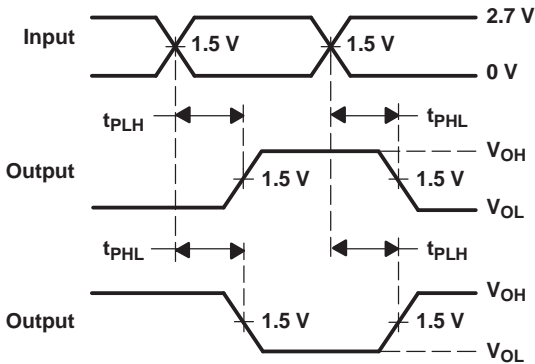
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



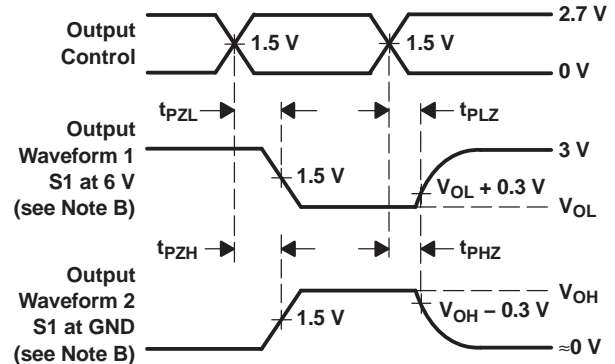
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVT16244BDGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16244B	<a href="#">Samples</a>
SN74LVT16244BDGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16244B	<a href="#">Samples</a>
SN74LVT16244BDGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VD244B	<a href="#">Samples</a>
SN74LVT16244BDL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16244B	<a href="#">Samples</a>
SN74LVT16244BDLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16244B	<a href="#">Samples</a>
SN74LVT16244BDLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVT16244B	<a href="#">Samples</a>
SN74LVT16244BZQLR	LIFEBUY	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	VD244B	
SN74LVT16244BZRDR	LIFEBUY	BGA MICROSTAR JUNIOR	ZRD	54	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	VD244B	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT16244BDGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVT16244BDGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVT16244BDLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVT16244BZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74LVT16244BZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	330.0	16.4	5.8	8.3	1.55	8.0	16.0	Q1

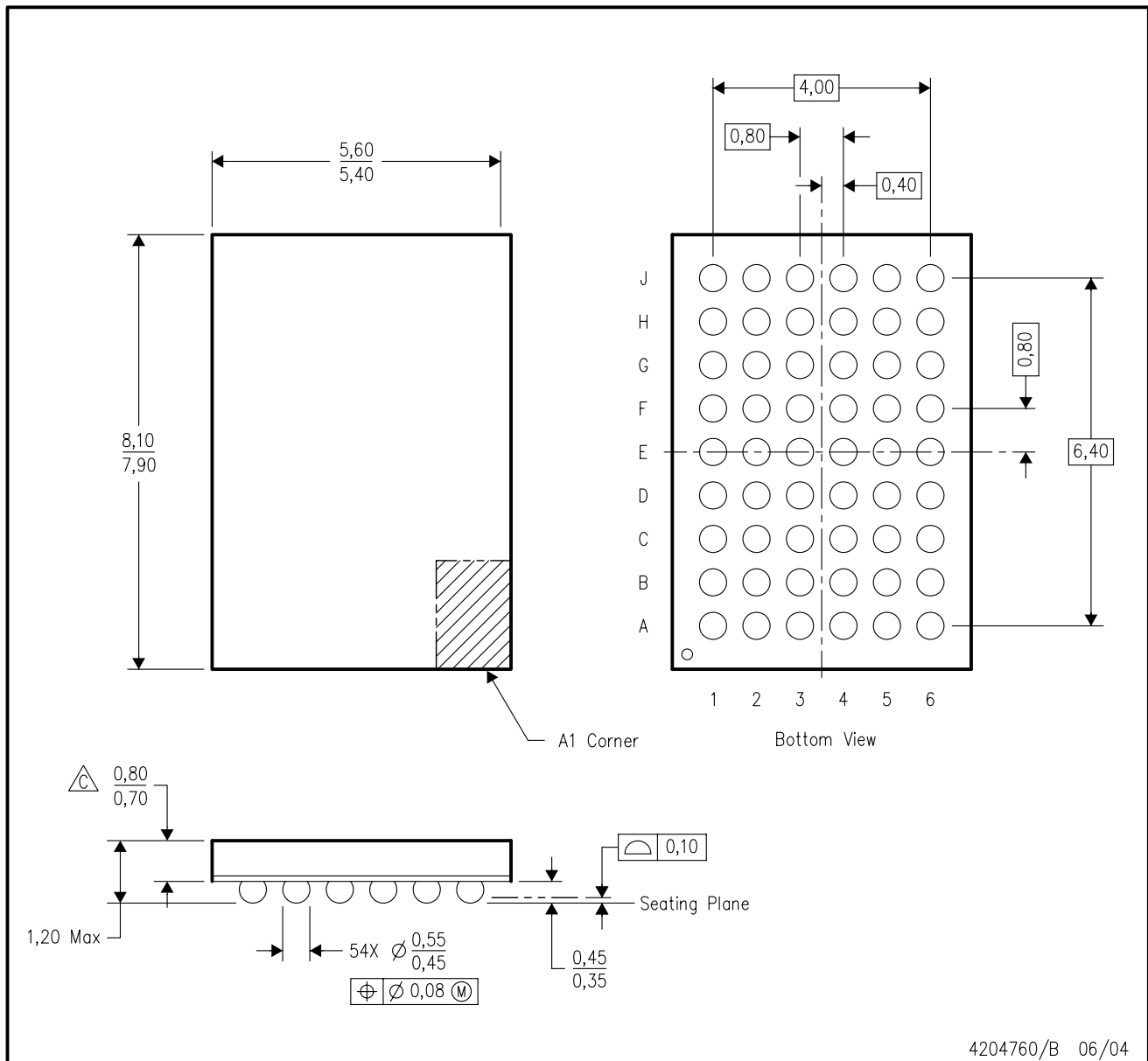
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT16244BDGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVT16244BDGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74LVT16244BDLR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74LVT16244BZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	350.0	350.0	43.0
SN74LVT16244BZRDR	BGA MICROSTAR JUNIOR	ZRD	54	1000	350.0	350.0	43.0

ZRD (R-PBGA-N54)

PLASTIC BALL GRID ARRAY

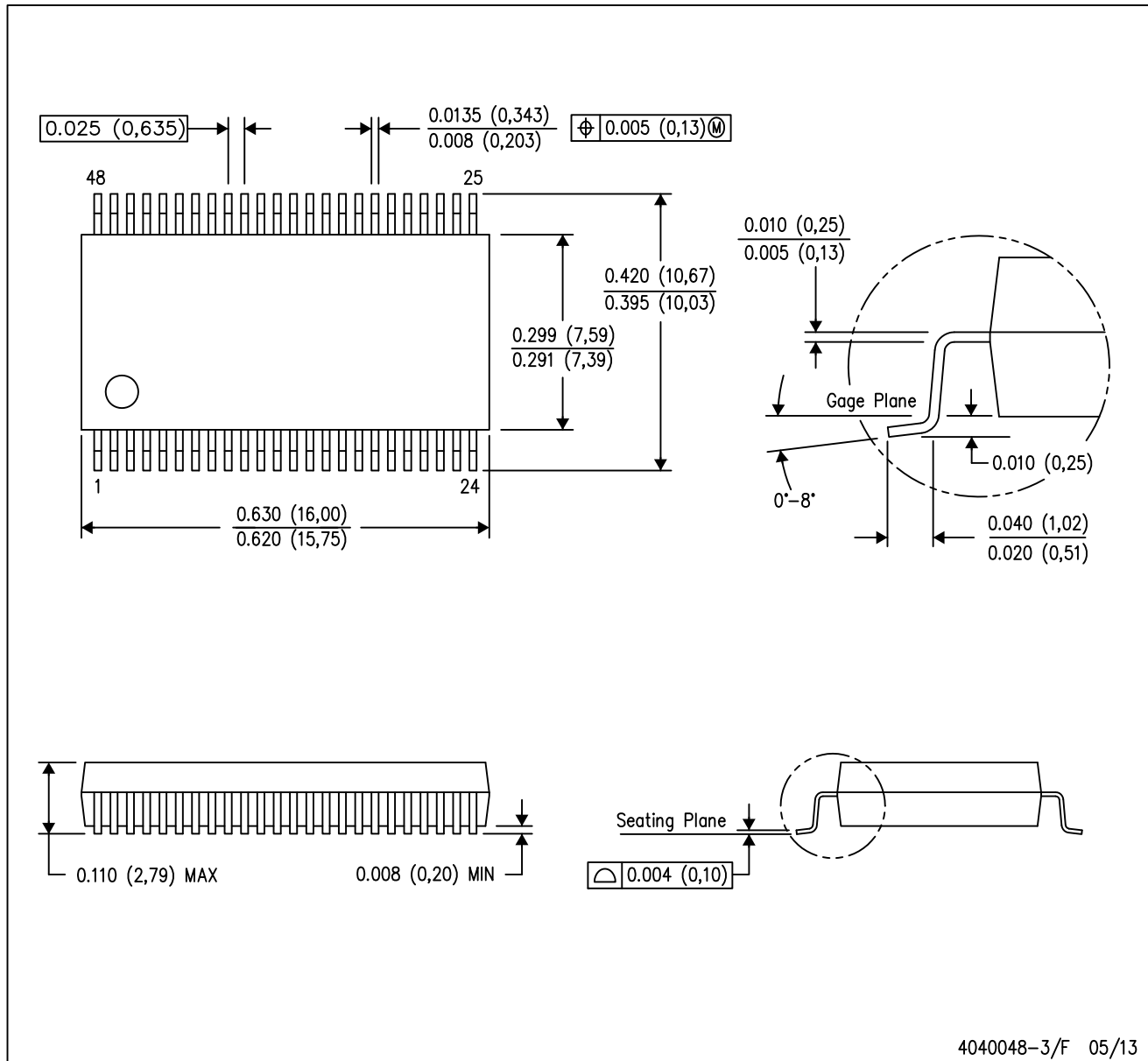


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-205 variation DD.
  - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

DGV (R-PDSO-G\*\*)

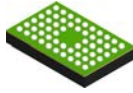
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

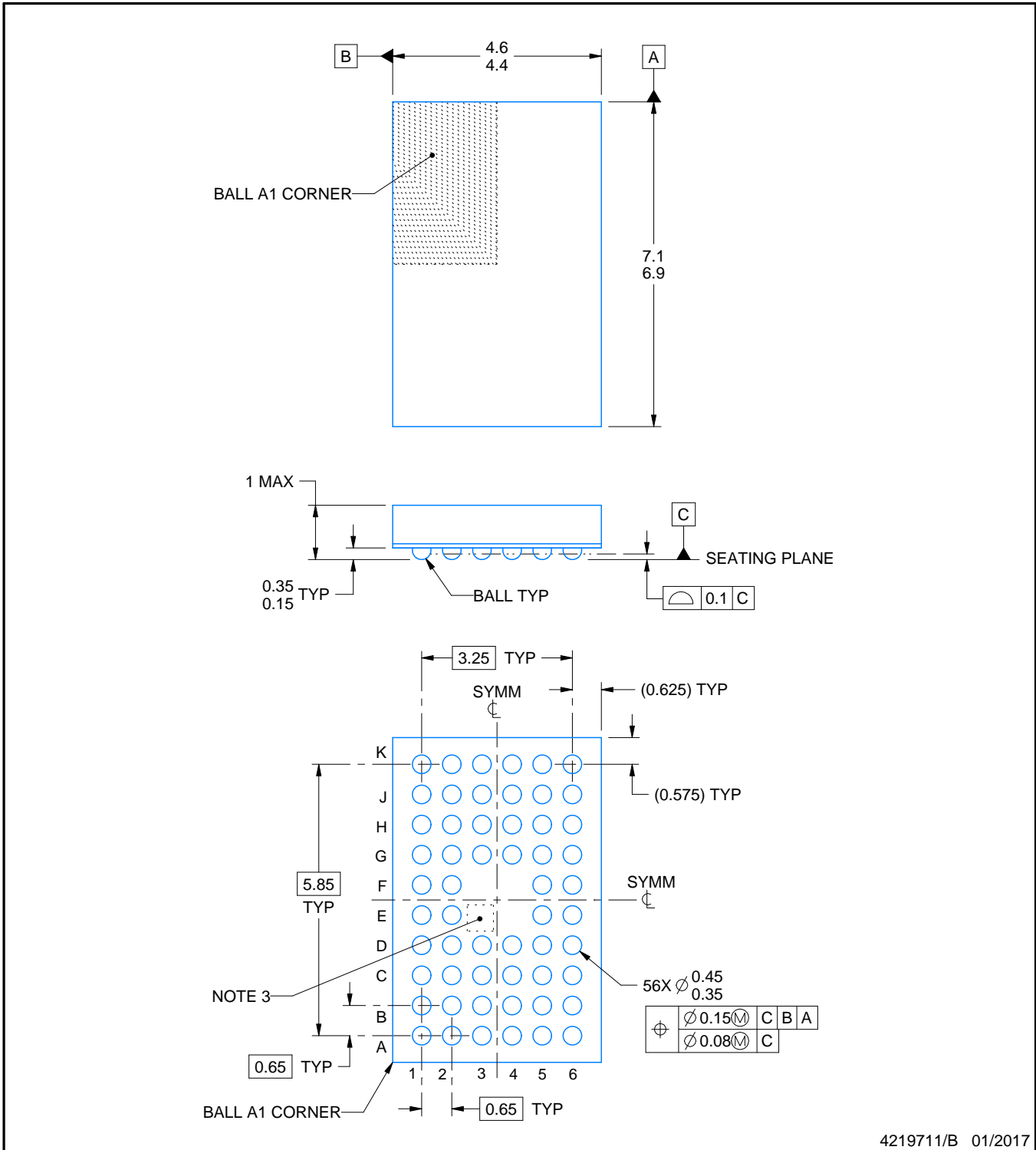
# ZQL0056A



# PACKAGE OUTLINE

## JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



4219711/B 01/2017

### NOTES:

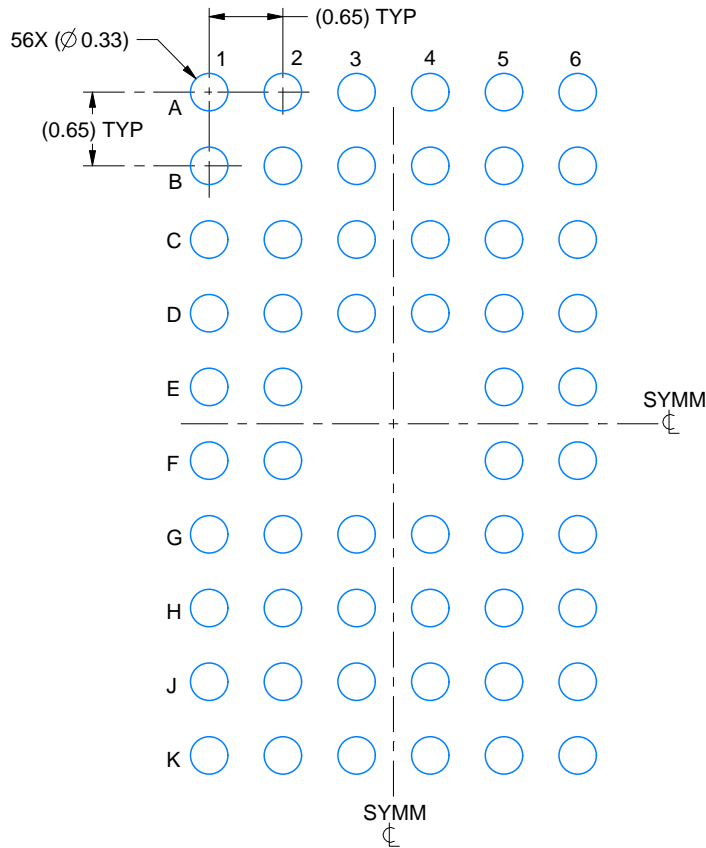
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. No metal in this area, indicates orientation.

# EXAMPLE BOARD LAYOUT

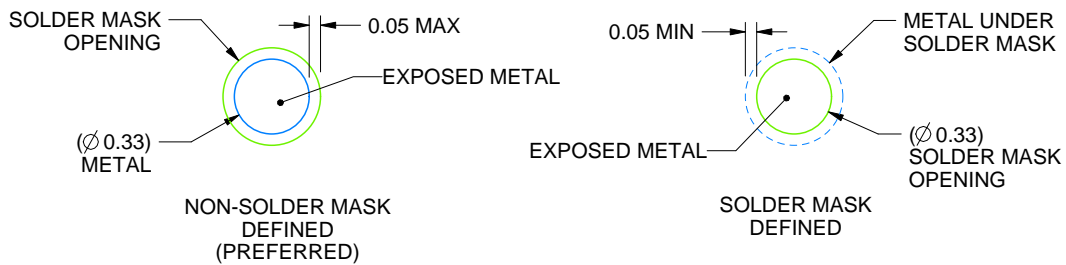
ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

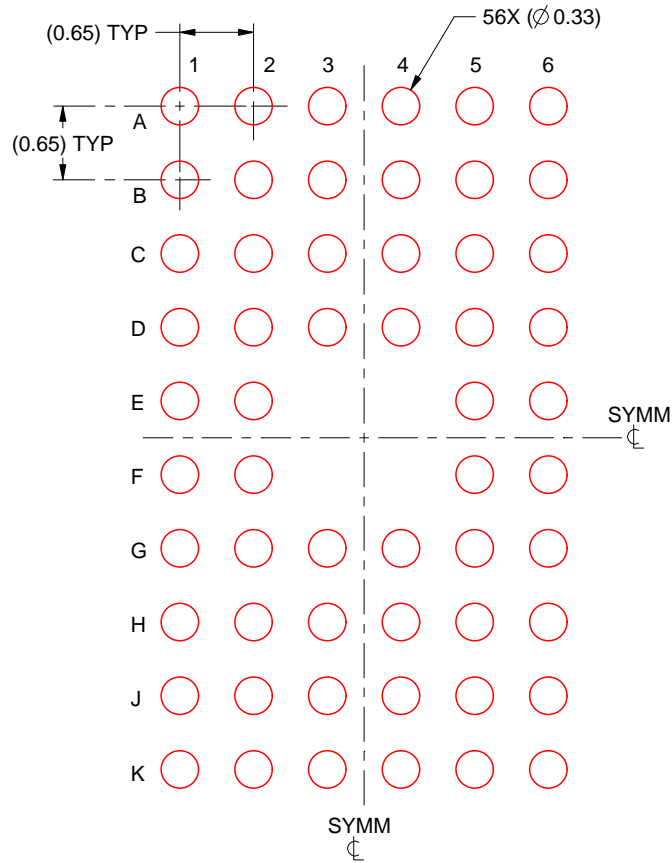


# EXAMPLE STENCIL DESIGN

ZQL0056A

JRBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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