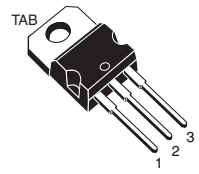
STP80NF12

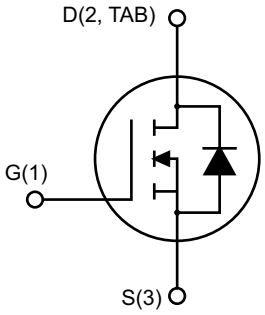
N-channel 120 V, 0.013 Ω typ., 80 A, STripFET™ II Power MOSFET in a TO-220 package

Datasheet - production data



TO-220

Figure 1. Internal schematic diagram



Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STP80NF12	120 V	< 0.018 Ω	80 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

Application

- Switching applications

Description

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for telecom and computer applications. It is also intended for any applications with low gate drive requirements.

Table 1. Device summary

Order code	Marking	Package	Packaging
STP80NF12	P80NF12	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	120	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D	Drain current (continuous) at T_C=100 °C	60	A
I_{DM}(2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	300	W
	Derating factor	2.0	W/°C
dv/dt (3)	Peak diode recovery voltage slope	10	V/ns
E_{AS} (4)	Single pulse avalanche energy	350	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Limited by package
2. Pulse width limited by safe operating area
3. I_{SD} < 80 A, di/dt < 300 A/µs, V_{DD}= 80% $V_{(BR)DSS}$
4. Starting T_J = 25 °C, I_D = 40 A, V_{DD} = 50 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case max	0.5	°C/W
R_{thJA}	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	120			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating @125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 40 A		0.013	0.018	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15 V, I_D = 40 A	-	80		S
C_{iss}	Input capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	4300		pF
C_{oss}	Output capacitance		-	600		pF
C_{rss}	Reverse transfer capacitance		-	230		pF
Q_{gs}	Total gate charge	V_{DD} = 80 V, I_D = 80 A V_{GS} =10 V	-	140	189	nC
Q_{gs}	Gate-source charge		-	23		nC
Q_{gd}	Gate-drain charge		-	51		nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 50 V, I_D= 40 A, R_G=4.7 Ω, V_{GS}=10 V See *Figure 13*	-	40	-	ns
t_r	Rise time		-	145	-	ns
$t_{d(off)}$	Turn-off delay time		-	134	-	ns
t_f	Fall time		-	115	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-	-	80	A
I_{SDM} (1)	Source-drain current (pulsed)		-	-	320	A
V_{SD} (2)	Forward on voltage	I_{SD}=80 A, V_{GS}=0	-	-	1.3	V
t_{rr}	Reverse recovery time	I_{SD}=80 A, di/dt = 100 A/µs, V_{DD}=35 V, T_J = 150 °C	-	155		ns
Q_{rr}	Reverse recovery charge		-	0.85		µC
I_{RRM}	Reverse recovery current		-	11		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

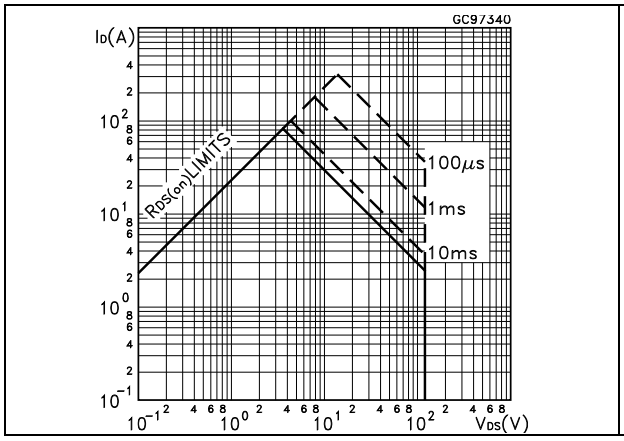


Figure 3. Thermal impedance

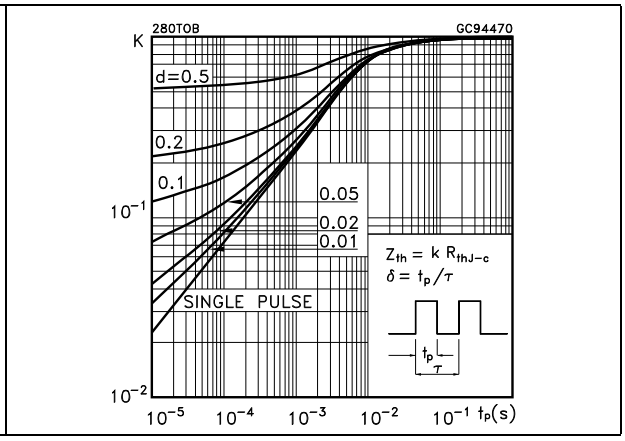


Figure 4. Output characteristics

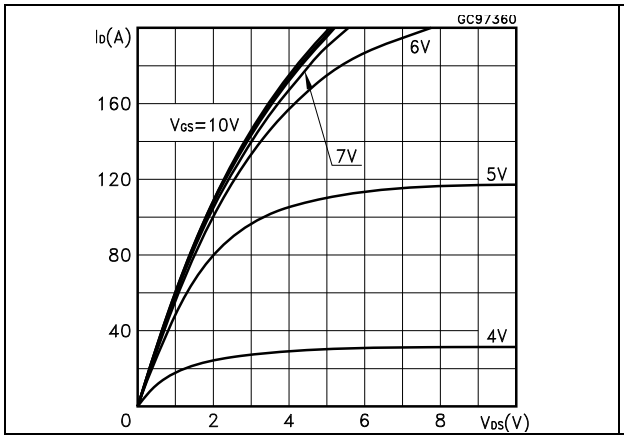


Figure 5. Transfer characteristics

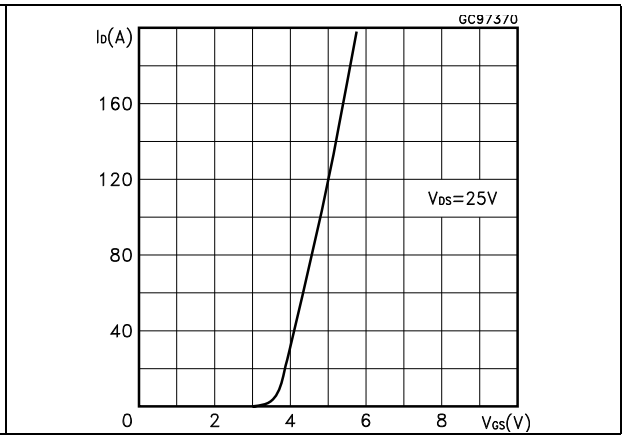


Figure 6. Normalized B_{VDSS} vs. temperature

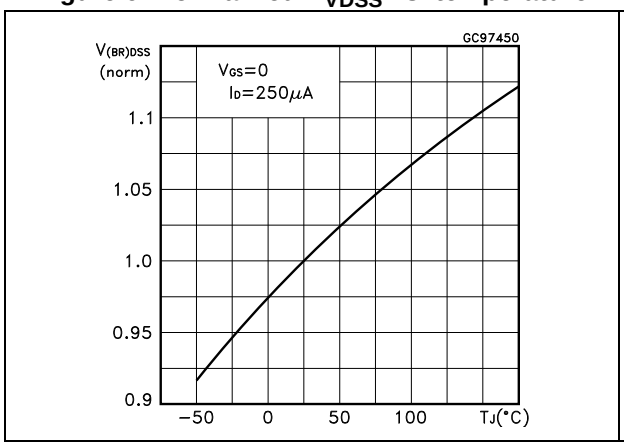


Figure 7. Static drain-source on resistance

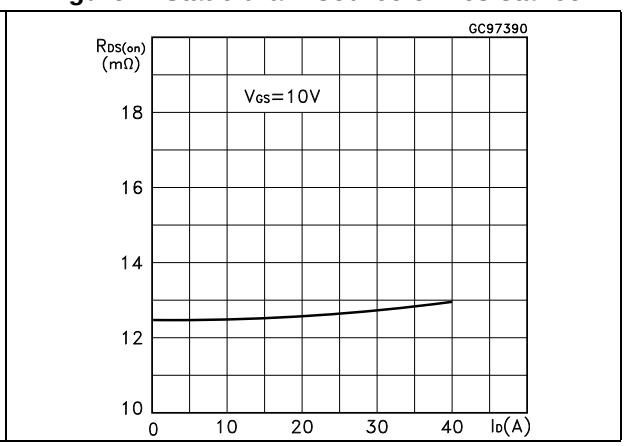


Figure 8. Gate charge vs. gate-source voltage

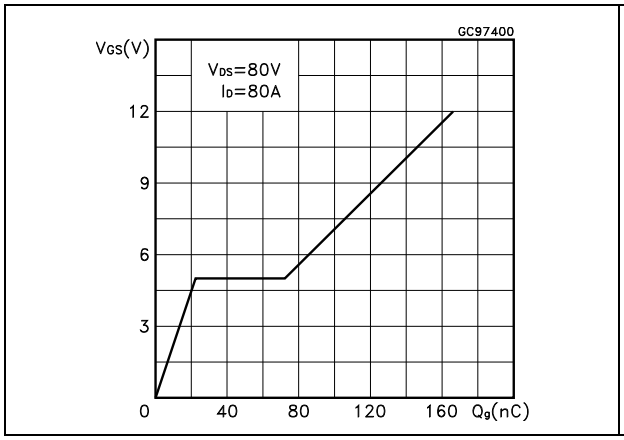


Figure 9. Capacitance variations

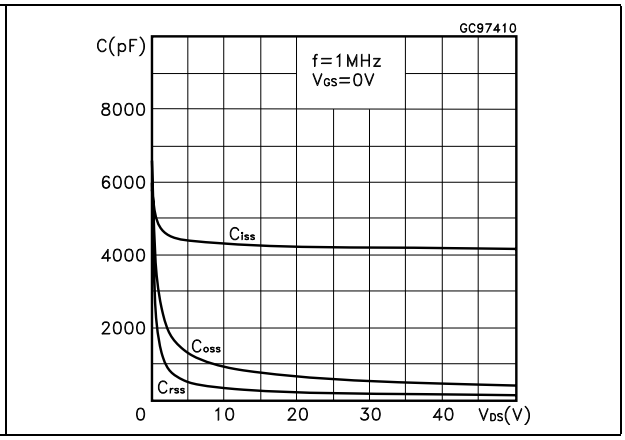


Figure 10. Normalized gate threshold voltage vs. temperature

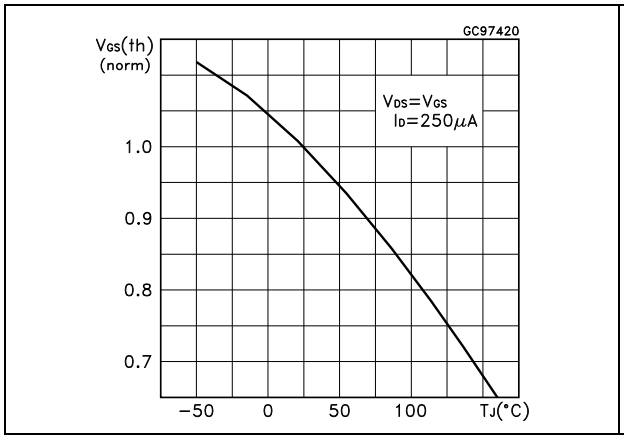


Figure 11. Normalized on resistance vs. temperature

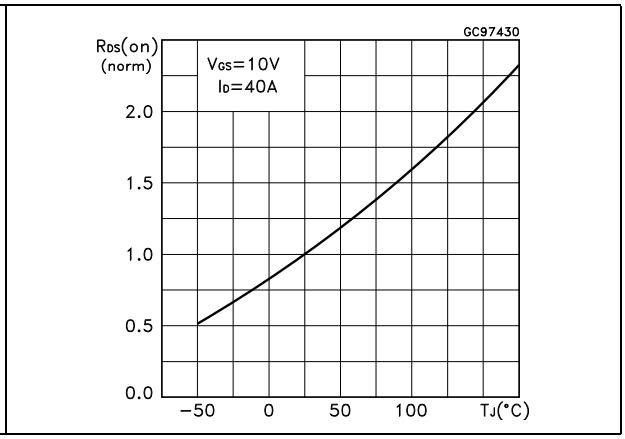
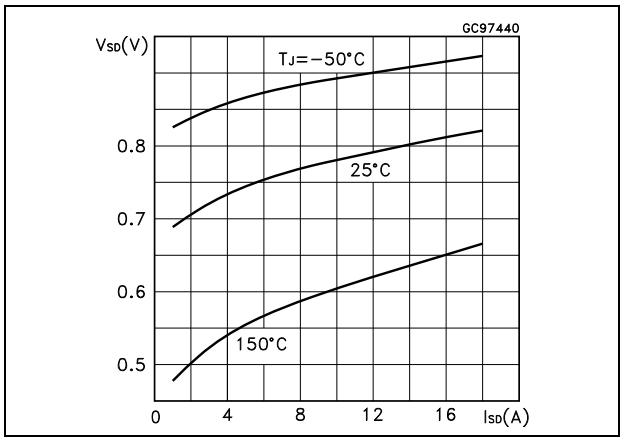


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

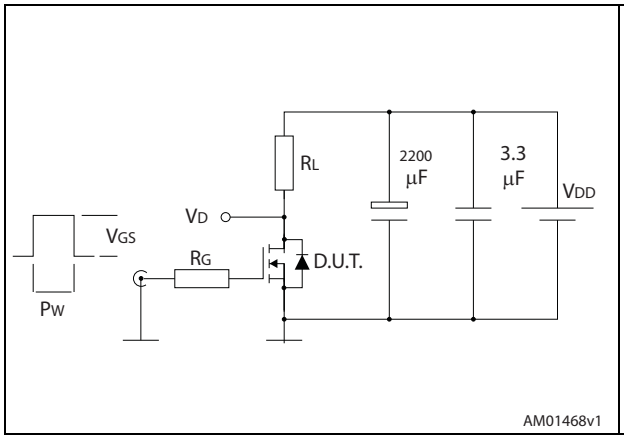


Figure 14. Gate charge test circuit

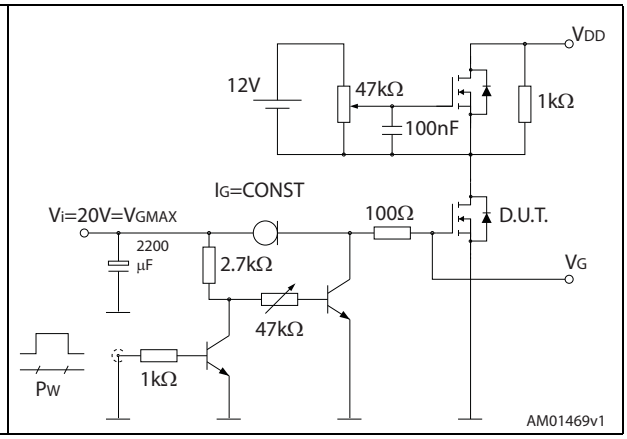


Figure 15. Test circuit for inductive load switching and diode recovery times

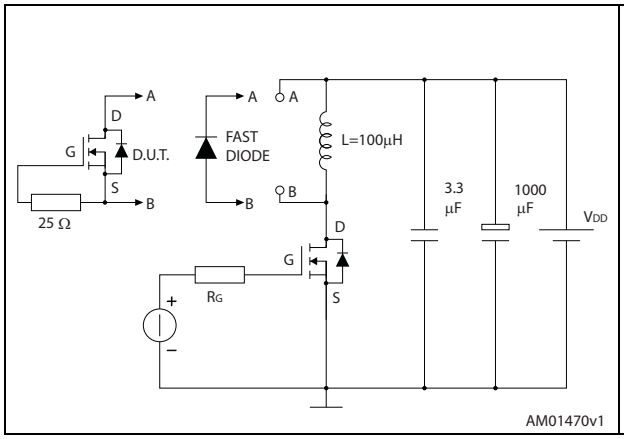


Figure 16. Unclamped inductive load test circuit

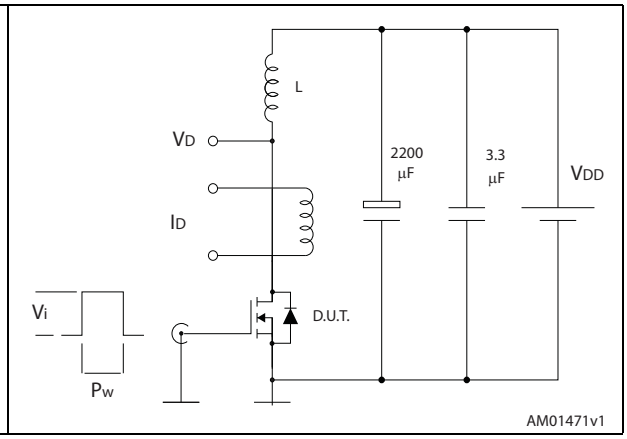


Figure 17. Unclamped inductive waveform

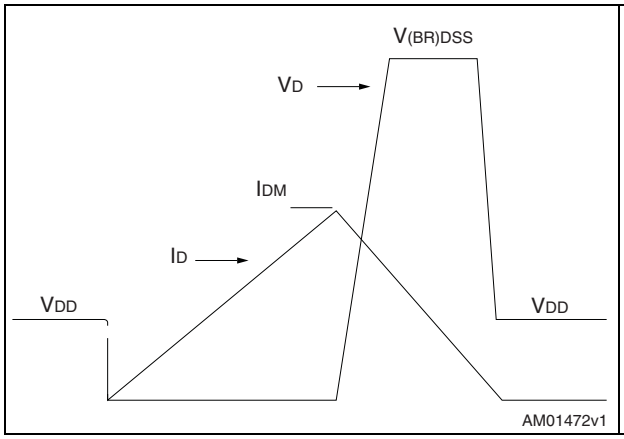
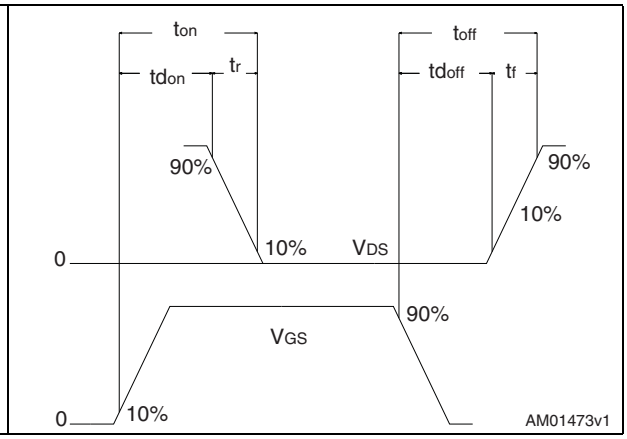


Figure 18. Switching time waveform



4 Package mechanical data

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Figure 19. TO-220 type A drawing

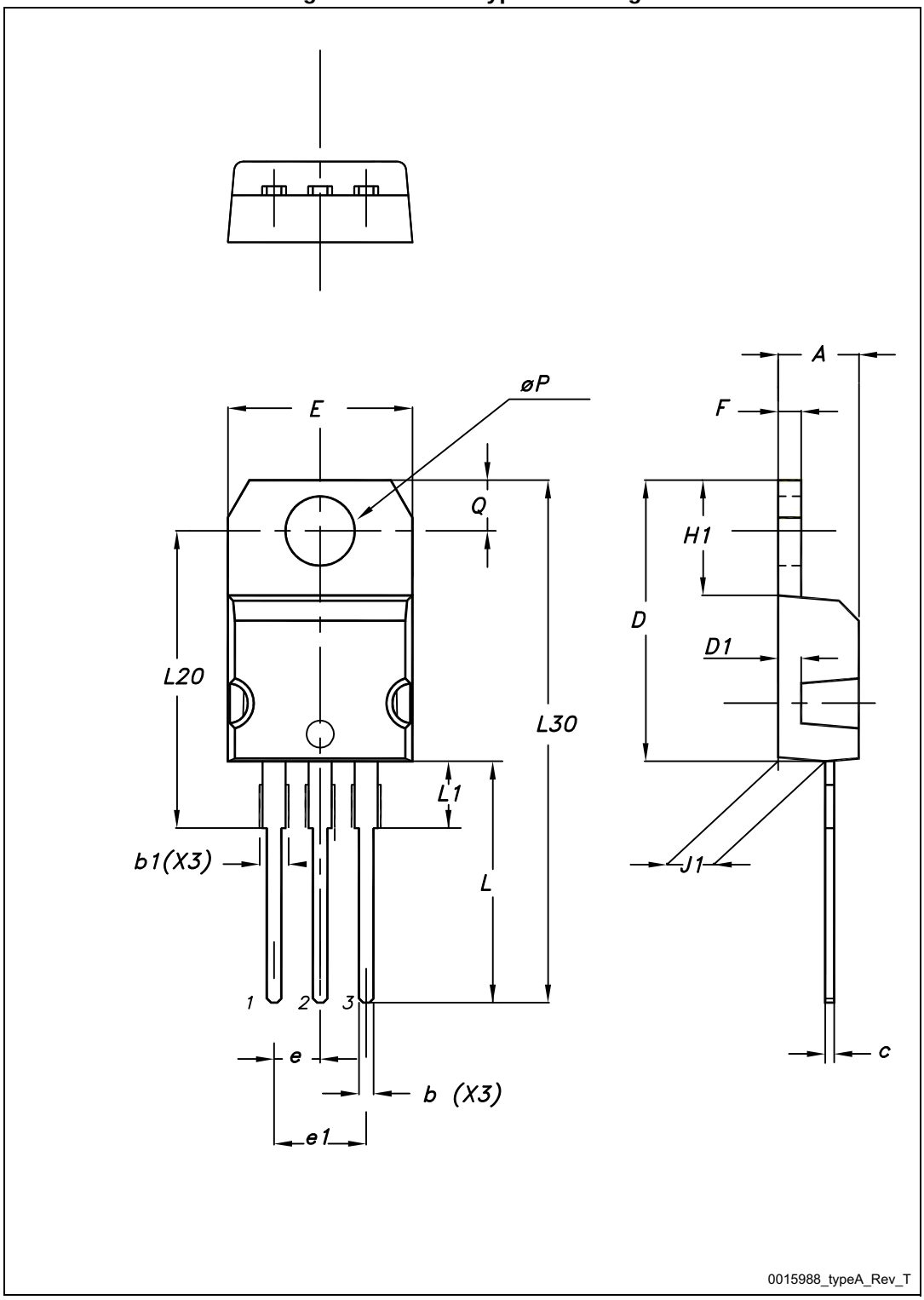

Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 9. Revision history

Date	Revision	Changes
21-Jun-2004	2	Preliminary version
24-Jul-2006	3	The document has been reformatted, SOA updated
31-Jan-2007	4	Typo mistake on *Table 2*.
10-Apr-2007	5	Typo mistake on *Table 2* and *Table 3*
19-Apr-2007	6	Corrected value on *Table 4*
17-Nov-2008	7	Inserted E_{AS} value on *Table 2*.
26-Feb-2014	8	Updated: *Section 4: Package mechanical data* Inserted E_{AS} value on *Table 2*. Added value V_{GS} on *Table 4*

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