14-Bit, 20/40/65/80 MSPS, 1.8 V Analog-to-Digital Converter

Data Sheet **AD9649**

FEATURES

- 1.8 V analog supply operation
- 1.8 V to 3.3 V output supply
- SNR
  - 74.3 dBFS at 9.7 MHz input
  - 71.5 dBFS at 200 MHz input
- SFDR
  - 93 dBc at 9.7 MHz input
  - 80 dBc at 200 MHz input
- Low power
  - 45 mW at 20 MSPS
  - 87 mW at 80 MSPS
- Differential input with 700 MHz bandwidth
- On-chip voltage reference and sample-and-hold circuit
- 2 V p-p differential analog input
- DNL = ±0.35 LSB
- Serial port control options
  - Offset binary, gray code, or twos complement data format
  - Integer 1, 2, or 4 input clock divider
  - Built-in selectable digital test pattern generation
  - Energy-saving power-down modes
  - Data clock out (DCO) with programmable clock and data alignment

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers
  - GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA
- Smart antenna systems
- Battery-powered instruments
- Handheld scope meters
- Portable medical imaging
- Ultrasound
- Radar/LIDAR

FUNCTIONAL BLOCK DIAGRAM

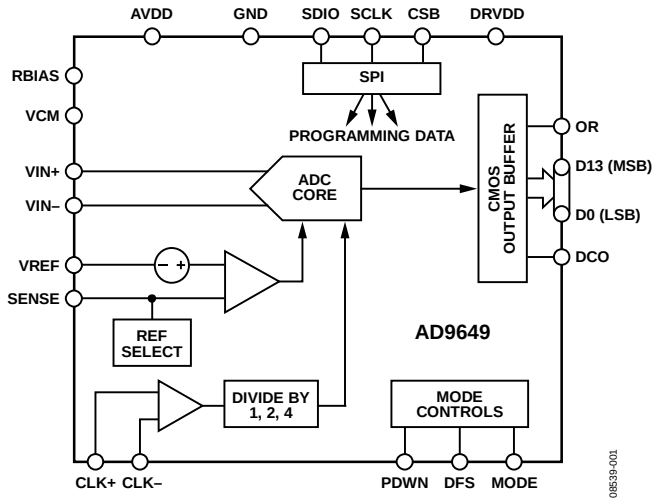

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD9649 operates from a single 1.8 V analog power supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
2. The sample-and-hold circuit maintains excellent performance for input frequencies up to 200 MHz and is designed for low cost, low power, and ease of use.
3. A standard serial port interface (SPI) supports various product features and functions, such as data output formatting, internal clock divider, power-down, DCO, data output (D13 to D0) timing and offset adjustments, and voltage reference modes.
4. The AD9649 is packaged in a 32-lead RoHS-compliant LFCSP that is pin compatible with the AD9629 12-bit ADC and the AD9609 10-bit ADC, enabling a simple migration path between 10-bit and 14-bit converters sampling from 20 MSPS to 80 MSPS.

Rev. B

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REVISION HISTORY

2/2017—Rev. A to Rev. B

Added Endnote 1, Table 16 ... 28
Changes to Power and Ground Recommendations Section ... 30
Added Soft Reset Section ... 30

6/2015—Rev. 0 to Rev. A

Change to Product Highlights Section ... 1
Changes to Figure 3 and Table 8 ... 10
Updated Outline Dimensions ... 32
Changes to Ordering Guide ... 32

10/2009—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9649 is a monolithic, single channel 1.8 V supply, 14-bit, 20/40/65/80 MSPS analog-to-digital converter (ADC). It features a high performance sample-and-hold circuit and an on-chip voltage reference.

The product uses multistage differential pipeline architecture with output error correction logic to provide 14-bit accuracy at 80 MSPS data rates and to guarantee no missing codes over the full operating temperature range.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

A differential clock input with optional 1, 2, or 4 divide ratios controls all internal conversion cycles.

The digital output data is presented in offset binary, gray code, or twos complement format. A data output clock (DCO) is provided to ensure proper latch timing with receiving logic. Both 1.8 V and 3.3 V CMOS levels are supported.

The AD9649 is available in a 32-lead RoHS-compliant LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

Table 1.

		AD9649-20/AD9649-40			AD9649-65			AD9649-80			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			14			Bits
ACCURACY											
No Missing Codes	Full		Guaranteed			Guaranteed			Guaranteed		
Offset Error	Full	−0.40	+0.05	+0.50	−0.40	+0.05	+0.50	−0.40	+0.05	+0.50	% FSR
Gain Error[1]	Full		−1.5			−1.5			−1.5		% FSR
Differential Nonlinearity (DNL)[2]	Full			±0.50			+0.55			±0.65	LSB
	25°C		±0.25			±0.3			±0.35		LSB
Integral Nonlinearity (INL)[2]	Full			±1.30			±1.30			±1.75	LSB
	25°C		±0.50			±0.50			±0.60		LSB
TEMPERATURE DRIFT											
Offset Error	Full		±2			±2			±2		ppm/°C
INTERNAL VOLTAGE REFERENCE											
Output Voltage (1 V Mode)	Full	0.984	0.996	1.008	0.984	0.996	1.008	0.984	0.996	1.008	V
Load Regulation Error at 1.0 mA	Full		2			2			2		mV
INPUT-REFERRED NOISE											
VREF = 1.0 V	25°C		0.98			0.98			0.98		LSB rms
ANALOG INPUT											
Input Span, VREF = 1.0 V	Full		2			2			2		V p-p
Input Capacitance[3]	Full		6			6			6		pF
Input Common-Mode Voltage	Full		0.9			0.9			0.9		V
Input Common-Mode Range	Full	0.5		1.3	0.5		1.3	0.5		1.3	V
REFERENCE INPUT RESISTANCE	Full		7.5			7.5			7.5		kΩ
POWER SUPPLIES											
Supply Voltage											
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7		3.6	1.7		3.6	1.7		3.6	V
Supply Current											
IAVDD[2]	Full		25.0/31.3	27.3/33.7		41.0	44.0		47.0	50.0	mA
IDRVDD[2] (1.8 V)	Full		1.6/2.9			4.7			5.6		mA
IDRVDD[2] (3.3 V)	Full		3.0/5.3			8.4			10.2		mA
POWER CONSUMPTION											
DC Input	Full		45.2/57.2			75.2			86.8		mW
Sine Wave Input[2] (DRVDD = 1.8 V)	Full		47.9/61.6	51.8/65.8		82.3	87.5		94.7	100	mW
Sine Wave Input[2] (DRVDD = 3.3 V)	Full		54.9/73.8			101.5			118.3		mW
Standby Power[4]	Full		34/34			34			34		mW
Power-Down Power	Full		0.5			0.5			0.5		mW

[1] Measured with 1.0 V external reference.
[2] Measured with a 10 MHz input frequency at rated sample rate, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between one differential input pin and ground.
[4] Standby power is measured with a dc input and the CLK+, CLK− active.

AC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

Table 2.

		AD9649-20/AD9649-40			AD9649-65			AD9649-80			
Parameter[1]	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)											
f_{IN} = 9.7 MHz	25°C		74.7			74.5			74.3		dBFS
f_{IN} = 30.5 MHz	25°C		74.4			74.3			74.1		dBFS
	Full	73.1			73.6						dBFS
f_{IN} = 70 MHz	25°C		73.7			73.7			73.6		dBFS
	Full							72.7			dBFS
f_{IN} = 200 MHz	25°C		71.5			71.5			71.5		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)											
f_{IN} = 9.7 MHz	25°C		74.6			74.4			74.1		dBFS
f_{IN} = 30.5 MHz	25°C		74.3			74.2			74.0		dBFS
	Full	73.0			73.5						dBFS
f_{IN} = 70 MHz	25°C		73.6			73.6			73.5		dBFS
	Full							72.6			dBFS
f_{IN} = 200 MHz	25°C		70.0			70.0			70.0		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)											
f_{IN} = 9.7 MHz	25°C		12.0			12.0			12.0		Bits
f_{IN} = 30.5 MHz	25°C		12.0			12.0			12.0		Bits
f_{IN} = 70 MHz	25°C		11.9			11.9			11.9		Bits
f_{IN} = 200 MHz	25°C		11.3			11.3			11.3		Bits
WORST SECOND OR THIRD HARMONIC											
f_{IN} = 9.7 MHz	25°C		−95			−95			−93		dBc
f_{IN} = 30.5 MHz	25°C		−95			−95			−93		dBc
	Full			−82			−83				dBc
f_{IN} = 70 MHz	25°C		−94			−94			−92		dBc
	Full									−82	dBc
f_{IN} = 200 MHz	25°C		−80			−80			−80		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)											
f_{IN} = 9.7 MHz	25°C		95			95			93		dBc
f_{IN} = 30.5 MHz	25°C		94			94			93		dBc
	Full	82			83						dBc
f_{IN} = 70 MHz	25°C		93			93			92		dBc
	Full							82			dBc
f_{IN} = 200 MHz	25°C		80			80			80		dBc
WORST OTHER (HARMONIC OR SPUR)											
f_{IN} = 9.7 MHz	25°C		−100			−100			−100		dBc
f_{IN} = 30.5 MHz	25°C		−100			−100			−100		dBc
	Full			−90			−90				dBc
f_{IN} = 70 MHz	25°C		−100			−100			−100		dBc
	Full									−90	dBc
f_{IN} = 200 MHz	25°C		−95			−95			−95		dBc
TWO-TONE SFDR											
f_{IN} = 30.5 MHz (−7 dBFS), 32.5 MHz (−7 dBFS)	25°C		90			90			90		dBc
ANALOG INPUT BANDWIDTH	25°C		700			700			700		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

Table 3.

		AD9649-20/AD9649-40/AD9649-65/AD9649-80			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Unit**
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.2		3.6	V p-p
Input Voltage Range	Full	GND − 0.3		AVDD + 0.2	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full	8	10	12	kΩ
Input Capacitance	Full		4		pF
LOGIC INPUTS (SCLK/DFS, MODE, SDIO/PDWN)[1]					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−50		−75	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		30		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (CSB)[2]					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		135	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
DIGITAL OUTPUTS					
DRVDD = 3.3 V					
High Level Output Voltage (I_{OH})					
I_{OH} = 50 µA	Full	3.29			V
I_{OH} = 0.5 mA	Full	3.25			V
Low Level Output Voltage (I_{OL})					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V
DRVDD = 1.8 V					
High Level Output Voltage (I_{OH})					
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage (I_{OL})					
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V

[1] Internal 30 kΩ pull-down.
[2] Internal 30 kΩ pull-up.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

Table 4.

		AD9649-20/AD9649-40			AD9649-65			AD9649-80			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS											
Input Clock Rate	Full			80/160			260			320	MHz
Conversion Rate[1]	Full	3		20/40	3		65	3		80	MSPS
CLK Period, Divide-by-1 Mode (t_{CLK})	Full	50/25			15.38			12.5			ns
CLK Pulse Width High (t_{CH})			25.0/12.5			7.69			6.25		ns
Aperture Delay (t_A)	Full		1.0			1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1			0.1		ps rms
DATA OUTPUT PARAMETERS											
Data Propagation Delay (t_{PD})	Full		3			3			3		ns
DCO Propagation Delay (t_{DCO})	Full		3			3			3		ns
DCO to Data Skew (t_{SKEW})	Full		0.1			0.1			0.1		ns
Pipeline Delay (Latency)	Full		8			8			8		Cycles
Wake-Up Time[2]	Full		350			350			350		µs
Standby	Full		600/400			300			260		ns
OUT-OF-RANGE RECOVERY TIME	Full		2			2			2		Cycles

[1] Conversion rate is the clock rate after the CLK divider.
[2] Wake-up time is dependent on the value of the decoupling capacitors.

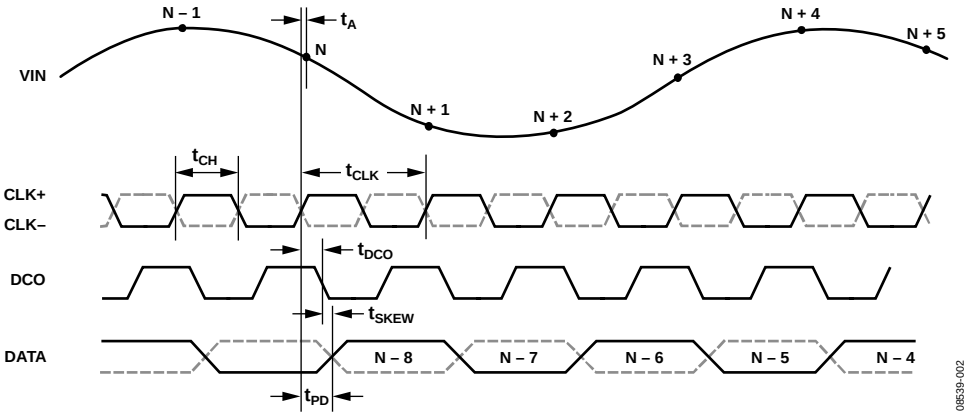


Figure 2. CMOS Output Data Timing

TIMING SPECIFICATIONS

Table 5.

Parameter	Conditions	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
AVDD to AGND[1]	−0.3 V to +2.0 V
DRVDD to AGND[1]	−0.3 V to +3.9 V
VIN+, VIN− to AGND[1]	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND[1]	−0.3 V to AVDD + 0.2 V
VREF to AGND[1]	−0.3 V to AVDD + 0.2 V
SENSE to AGND[1]	−0.3 V to AVDD + 0.2 V
VCM to AGND[1]	−0.3 V to AVDD + 0.2 V
RBIAS to AGND[1]	−0.3 V to AVDD + 0.2 V
CSB to AGND[1]	−0.3 V to DRVDD + 0.3 V
SCLK/DFS to AGND[1]	−0.3 V to DRVDD + 0.3 V
SDIO/PDWN to AGND[1]	−0.3 V to DRVDD + 0.3 V
MODE/OR to AGND[1]	−0.3 V to DRVDD + 0.3 V
D0 through D13 to AGND[1]	−0.3 V to DRVDD + 0.3 V
DCO to AGND[1]	−0.3 V to DRVDD + 0.3 V
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

[1] AGND refers to the analog ground of the customer's PCB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The exposed paddle is the only ground connection for the chip and must be soldered to the analog ground plane of the user's PCB. Soldering the exposed paddle to the user's board also increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
32-Lead LFCSP 5 mm × 5 mm	0	37.1	3.1	20.7	0.3	°C/W
	1.0	32.4			0.5	°C/W
	2.5	29.1			0.8	°C/W

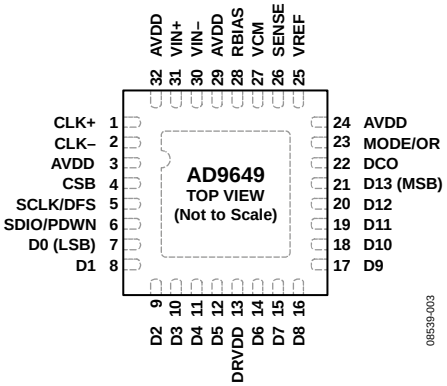
[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PADDLE. THE EXPOSED PADDLE IS THE ONLY GROUND CONNECTION. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	EPAD	Exposed Paddle. The exposed paddle is the only ground connection. It must be soldered to the analog ground of the PCB to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.
1, 2	CLK+, CLK–	Differential Encode Clock for PECL, LVDS, or 1.8 V CMOS Inputs.
3, 24, 29, 32	AVDD	1.8 V Supply Pin for the ADC CORE Domain.
4	CSB	SPI Chip Select. Active low enable, 30 kΩ internal pull-up.
5	SCLK/DFS	SPI Clock Input in SPI Mode (SCLK). 30 kΩ internal pull-down. Data Format Select in Non-SPI Mode (DFS). Static control of data output format. 30 kΩ internal pull-down. DFS high = twos complement output; DFS low = offset binary output.
6	SDIO/PDWN	SPI Data Input/Output (SDIO). Bidirectional SPI data I/O with 30 kΩ internal pull-down. Non-SPI Mode Power-Down (PDWN). Static control of chip power-down with 30 kΩ internal pull-down. See Table 14 for details.
7 to 12, 14 to 21	D0 (LSB) to D13 (MSB)	ADC Digital Outputs.
13	DRVDD	1.8 V to 3.3 V Supply Pin for Output Driver Domain.
22	DCO	Data Clock Digital Output.
23	MODE/OR	Chip Mode Select Input in SPI Mode (MODE). Out-of-Range Digital Output in SPI Mode or in Non-SPI Mode (OR). Default = out-of-range (OR) digital output (SPI Register 0x2A, Bit 0 = 1). Option = chip mode select input (SPI Register 0x2A, Bit 0 = 0). Chip power-down (SPI Register 0x08, Bits[7:5] = 100). Chip stand-by (SPI Register 0x08, Bits[7:5] = 101). Normal operation, output disabled (SPI Register 0x08, Bits[7:5] = 110). Normal operation, output enabled (SPI Register 0x08, Bits[7:5] = 111). In non-SPI mode, the pin operates only as an out-of-range (OR) digital output.
25	VREF	1.0 V Voltage Reference Input/Output. See Table 10.
26	SENSE	Reference Mode Selection. See Table 10.
27	VCM	Analog Output Voltage at Mid AVDD Supply. Sets common mode of the analog inputs.
28	RBIAS	Set Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
30, 31	VIN–, VIN+	ADC Analog Inputs.

TYPICAL PERFORMANCE CHARACTERISTICS

AD9649-80

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

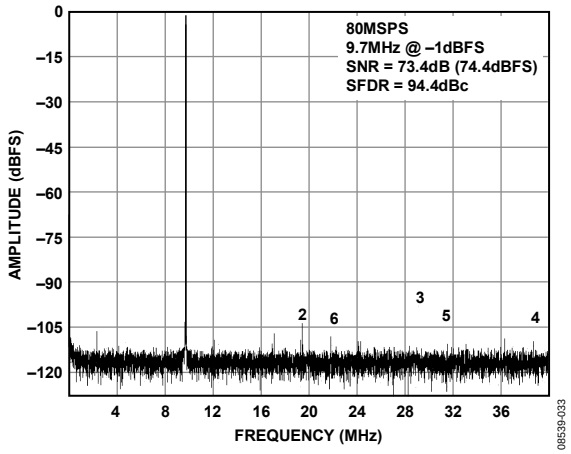


Figure 4. AD9649-80 Single-Tone FFT with f_{IN} = 9.7 MHz

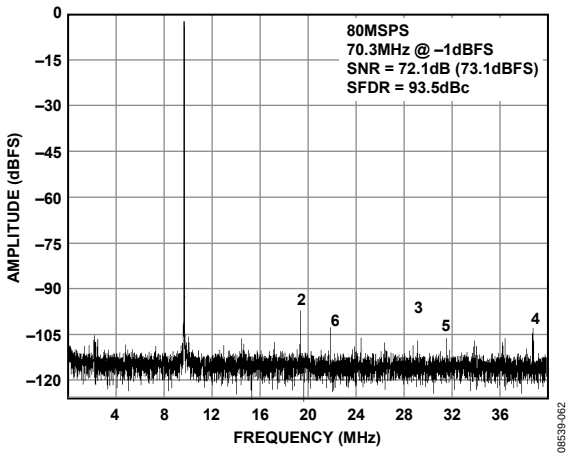


Figure 5. AD9649-80 Single-Tone FFT with f_{IN} = 70.3 MHz

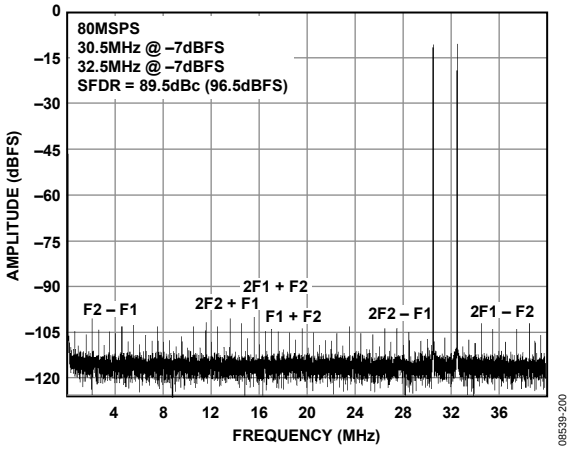


Figure 6. AD9649-80 Two-Tone FFT with f_{IN1} = 30.5 MHz and f_{IN2} = 32.5 MHz

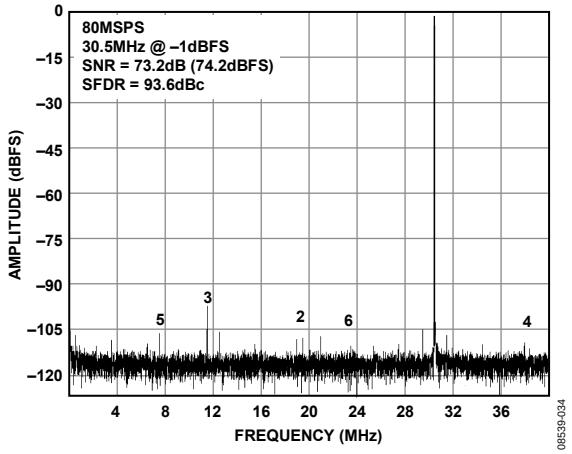


Figure 7. AD9649-80 Single-Tone FFT with f_{IN} = 30.5 MHz

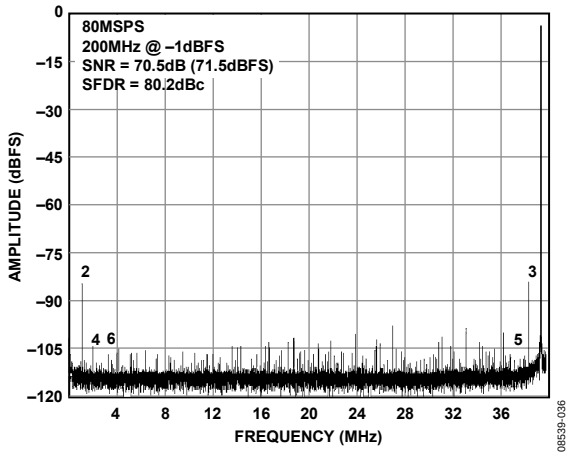


Figure 8. AD9649-80 Single-Tone FFT with f_{IN} = 200 MHz

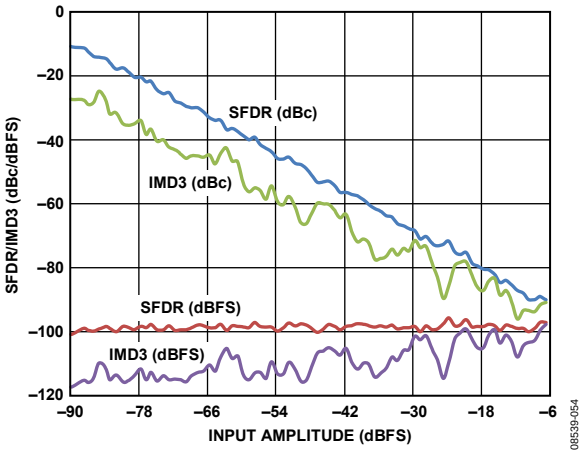


Figure 9. AD9649-80 Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with f_{IN1} = 30.5 MHz and f_{IN2} = 32.5 MHz

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

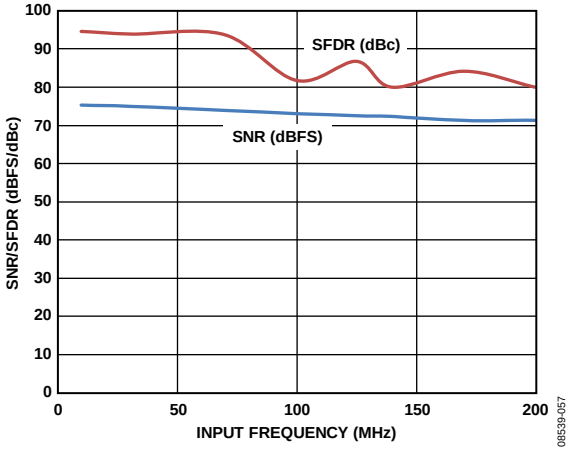


Figure 10. AD9649-80 SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

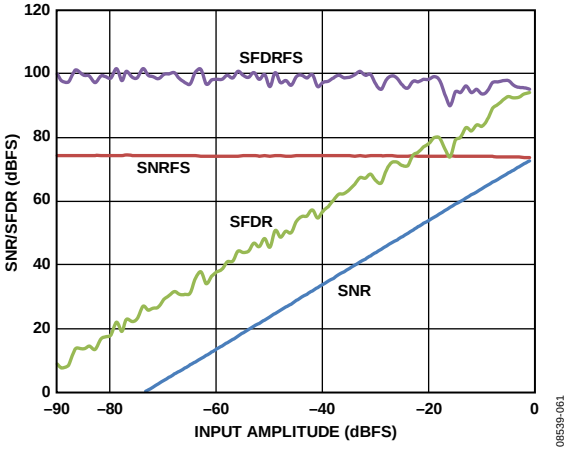


Figure 13. AD9649-80 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

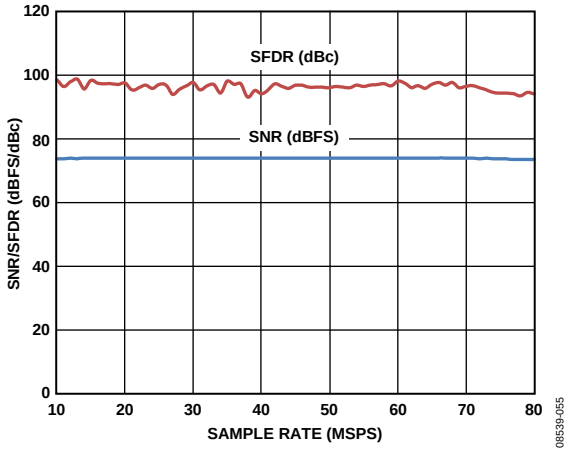


Figure 11. AD9649-80 SNR/SFDR vs. Sample Rate with AIN = 9.7 MHz

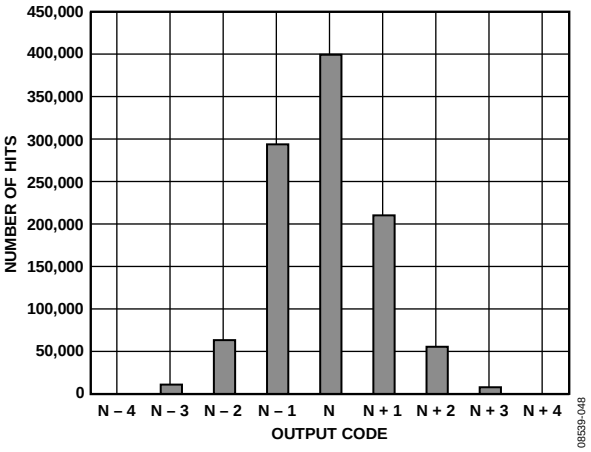


Figure 14. AD9649-80 Grounded Input Histogram

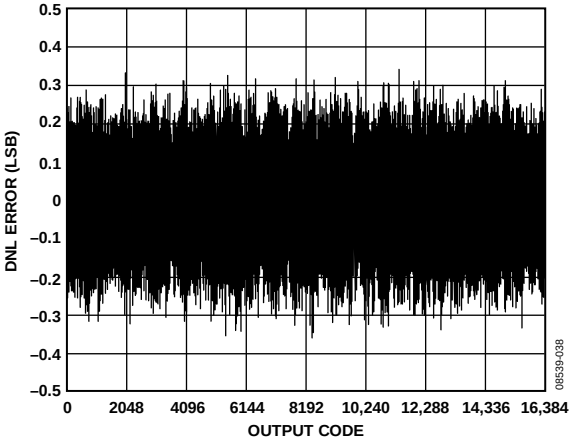


Figure 12. AD9649-80 DNL Error with f_{IN} = 9.7 MHz

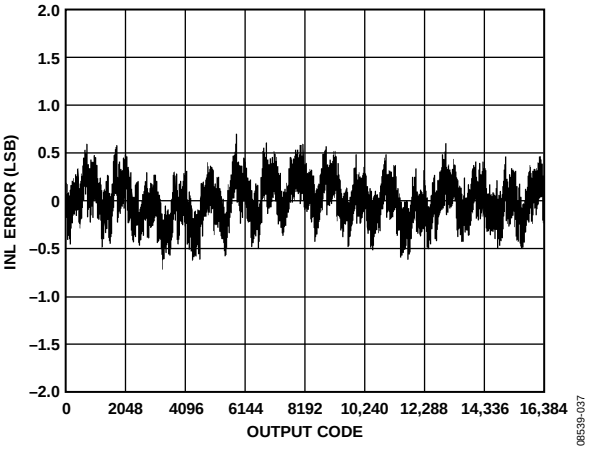


Figure 15. AD9649-80 INL with f_{IN} = 9.7 MHz

AD9649-65

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

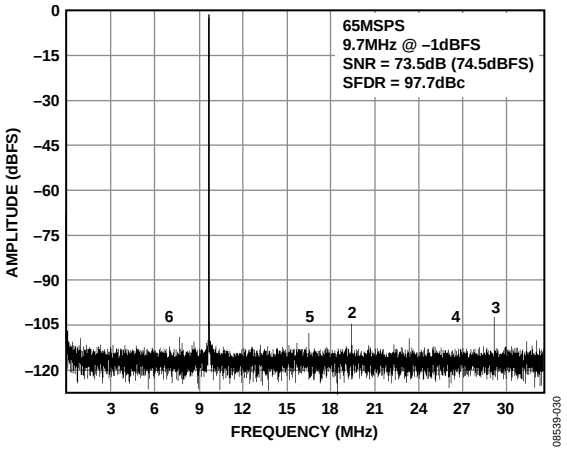


Figure 16. AD9649-65 Single-Tone FFT with f_{IN} = 9.7 MHz

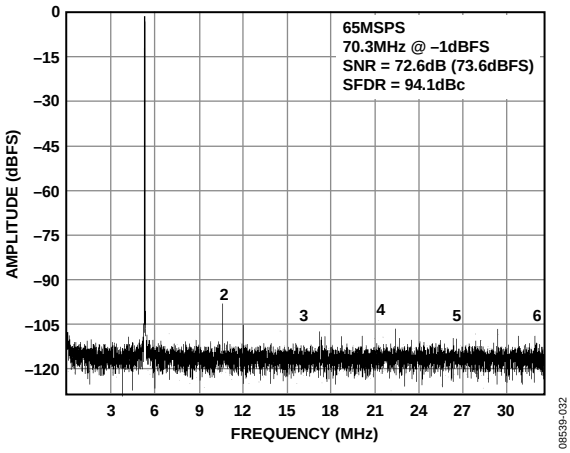


Figure 17. AD9649-65 Single-Tone FFT with f_{IN} = 70.3 MHz

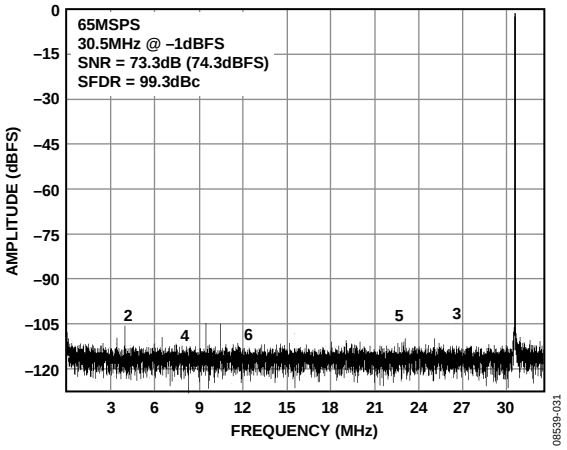


Figure 18. AD9649-65 Single-Tone FFT with f_{IN} = 30.5 MHz

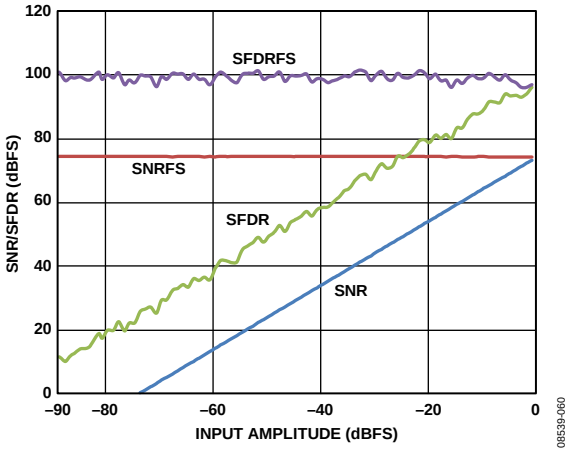


Figure 19. AD9649-65 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

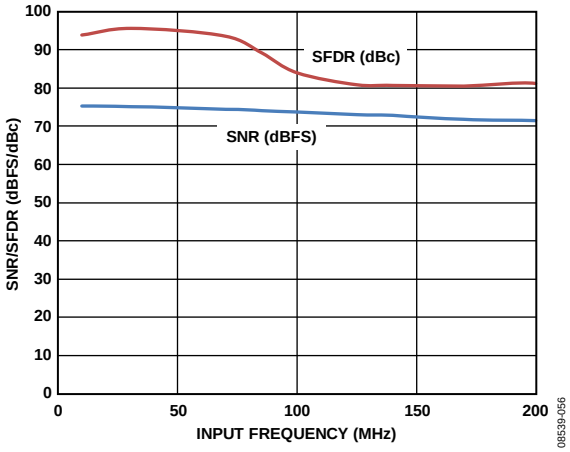


Figure 20. AD9649-65 SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

AD9649-40

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

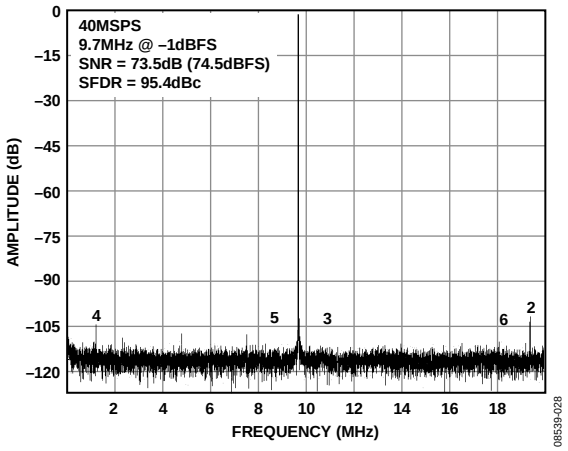


Figure 21. AD9649-40 Single-Tone FFT with f_{IN} = 9.7 MHz

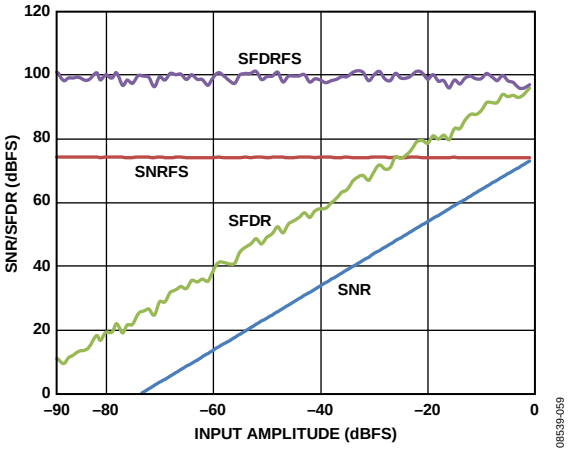


Figure 23. AD9649-40 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

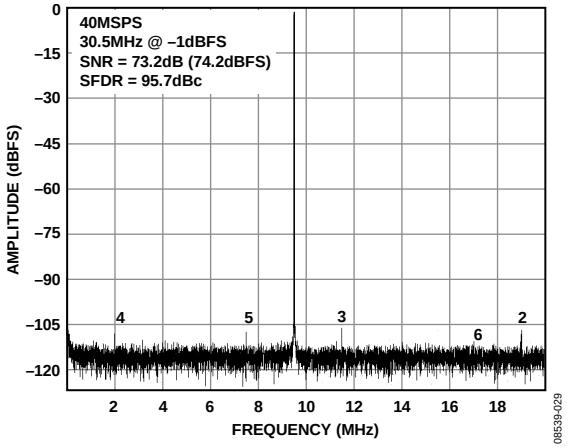


Figure 22. AD9649-40 Single-Tone FFT with f_{IN} = 30.5 MHz

AD9649-20

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = −1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

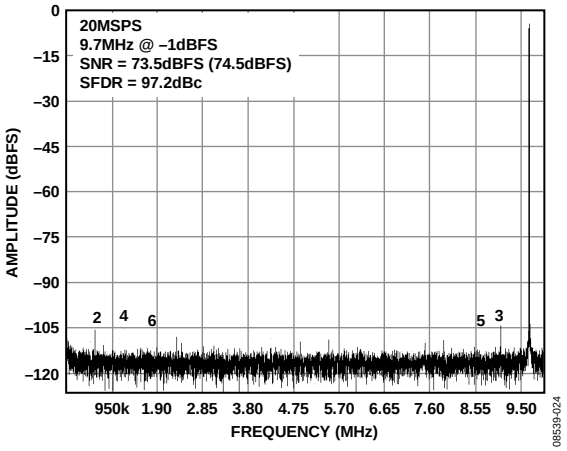


Figure 24. AD9649-20 Single-Tone FFT with f_{IN} = 9.7 MHz

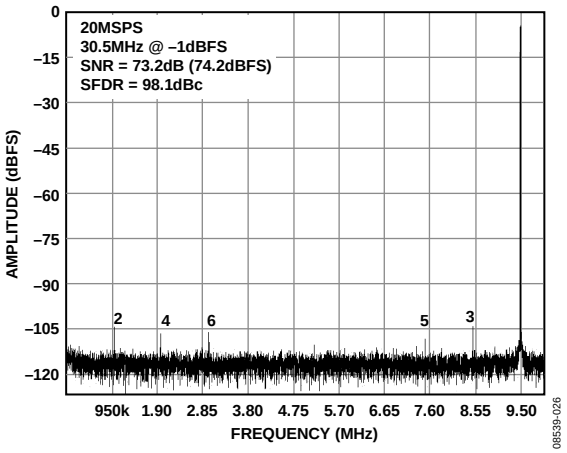


Figure 25. AD9649-20 Single-Tone FFT with f_{IN} = 30.5 MHz

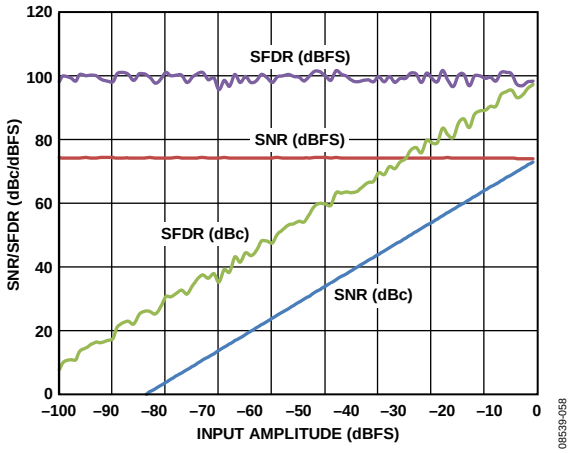


Figure 26. AD9649-20 SNR/SFDR vs. Input Amplitude (AIN) with f_{IN} = 9.7 MHz

EQUIVALENT CIRCUITS

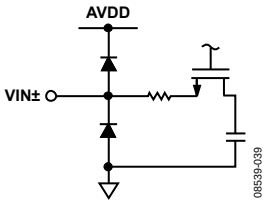


Figure 27. Equivalent Analog Input Circuit

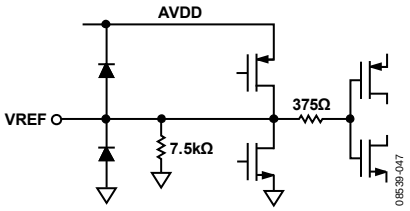


Figure 28. Equivalent VREF Circuit

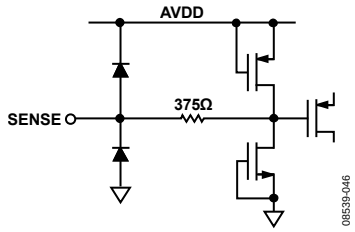


Figure 29. Equivalent SENSE Circuit

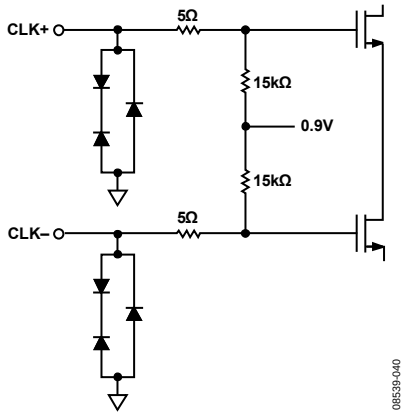


Figure 30. Equivalent Clock Input Circuit

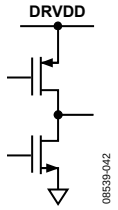


Figure 31. Equivalent D0 to D13 and OR Digital Output Circuit

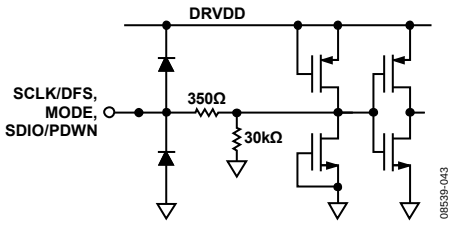


Figure 32. Equivalent SCLK/DFS, MODE and SDIO/PDWN Input Circuit

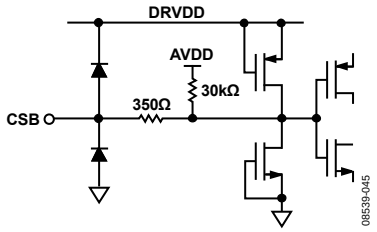


Figure 33. Equivalent CSB Input Circuit

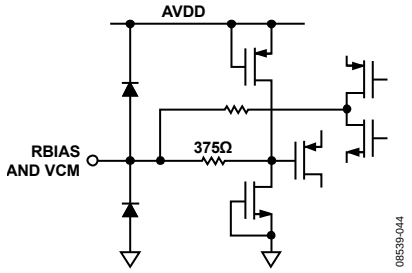


Figure 34. Equivalent RBIAS, VCM Circuit

THEORY OF OPERATION

The AD9649 architecture consists of a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample, whereas the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the CMOS output buffers. The output buffers are powered from a separate (DRVDD) supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9649 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

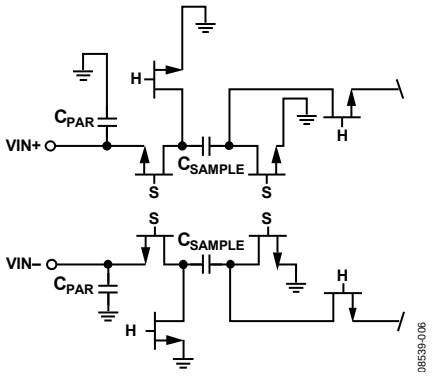


Figure 35. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 35). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

Input Common Mode

The analog inputs of the AD9649 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide an external dc bias. Setting the device so that VCM = AVDD/2 is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 36 and Figure 37.

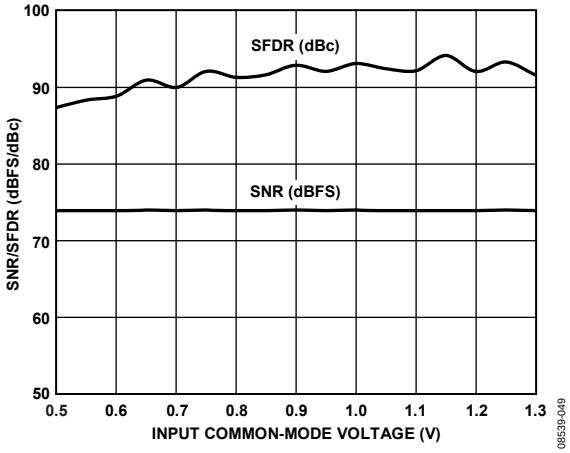


Figure 36. SNR/SFDR vs. Input Common-Mode Voltage, f_{IN} = 32.1 MHz, f_S = 80 MSPS

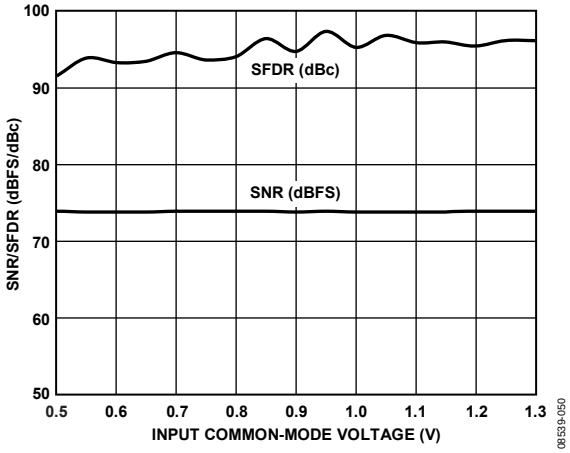


Figure 37. SNR/SFDR vs. Input Common-Mode Voltage, f_{IN} = 10.3 MHz, f_S = 20 MSPS

An on-board, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section.

Differential Input Configurations

Optimum performance is achieved while driving the AD9649 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCM pin of the AD9649 (see Figure 38), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

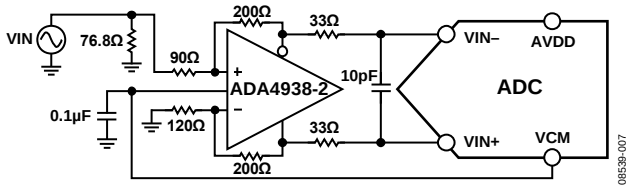


Figure 38. Differential Input Configuration Using the ADA4938-2

For baseband applications below ~10 MHz where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 39. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

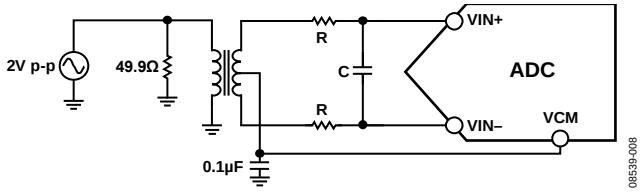


Figure 39. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9649. For applications above ~10 MHz where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 41).

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver. An example is shown in Figure 42. See the AD8352 data sheet for more information.

In any configuration, the value of Shunt Capacitor C is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 9 displays the suggested values to set the RC network. However, these values are dependent on the input signal and should be used only as a starting guide.

Table 9. Example RC Network

Frequency Range (MHz)	R Series (Ω Each)	C Differential (pF)
0 to 70	33	22
70 to 200	125	Open

Single-Ended Input Configuration

A single-ended input can provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the source impedances on each input are matched, there should be little effect on SNR performance. Figure 40 shows a typical single-ended input configuration.

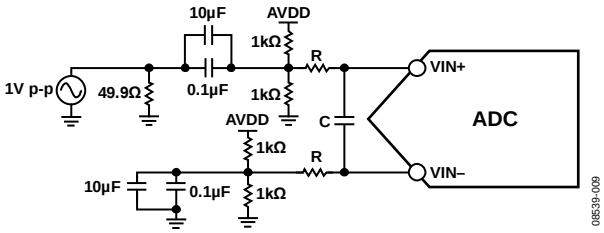


Figure 40. Single-Ended Input Configuration

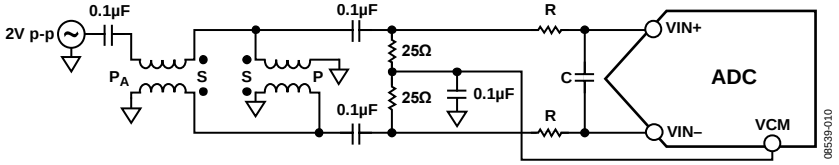


Figure 41. Differential Double Balun Input Configuration

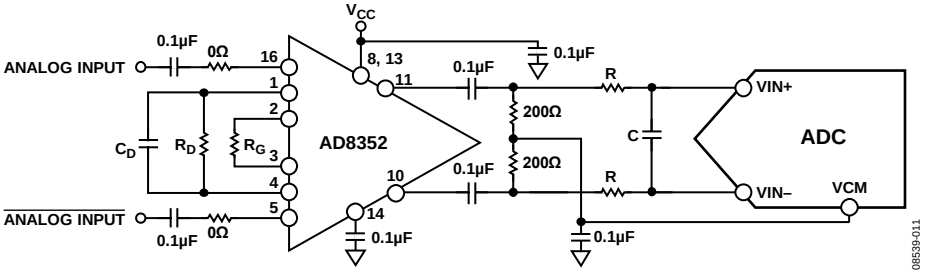


Figure 42. Differential Input Configuration Using the AD8352

VOLTAGE REFERENCE

A stable and accurate 1.0 V voltage reference is built into the AD9649. The VREF can be configured using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the sections that follow. The Reference Decoupling section describes the best practices PCB layout of the reference.

Internal Reference Connection

A comparator within the AD9649 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 10. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 43), setting VREF to 1.0 V.

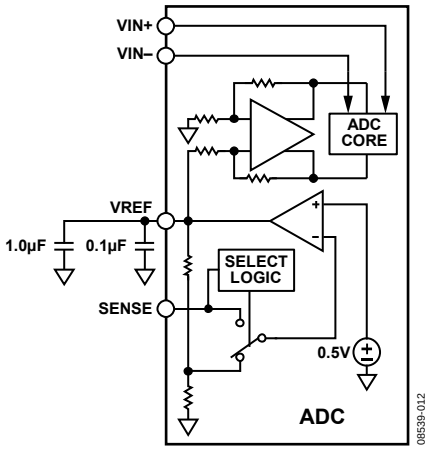


Figure 43. Internal Reference Configuration

If the internal reference of the AD9649 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 44 shows how the internal reference voltage is affected by loading.

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 45 shows the typical drift characteristics of the internal reference in 1.0 V mode.

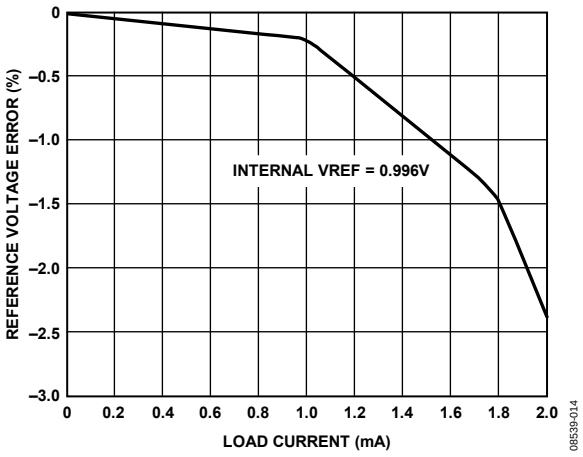


Figure 44. VREF Accuracy vs. Load Current

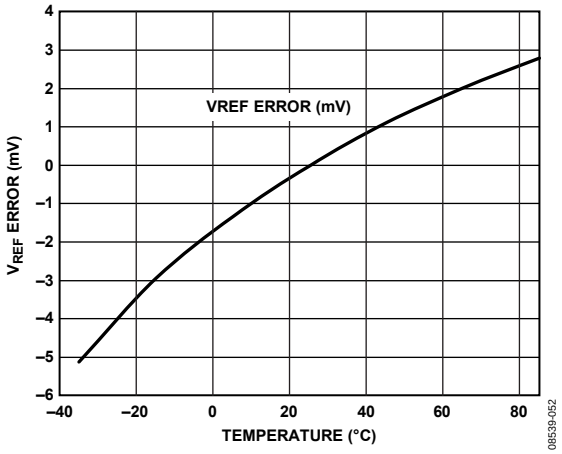


Figure 45. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 28). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.0 V.

Table 10. Reference Configuration Summary

Selected Mode	SENSE Voltage (V)	Resulting VREF (V)	Resulting Differential Span (V p-p)
Fixed Internal Reference	AGND to 0.2	1.0 internal	2.0
Fixed External Reference	AVDD	1.0 applied to external VREF pin	2.0

CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the AD9649 sample clock inputs, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 46) and require no external bias.

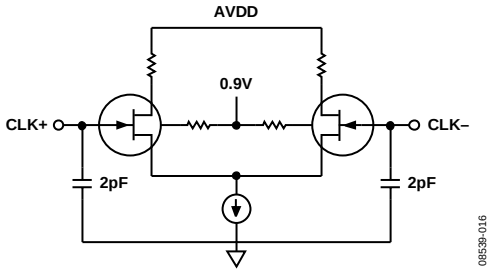


Figure 46. Equivalent Clock Input Circuit

Clock Input Options

The AD9649 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of great concern, as described in the Jitter Considerations section.

Figure 47 and Figure 48 show two preferred methods for clocking the AD9649. The CLK inputs support up to 4× the rated sample rate when using the internal clock divider feature. A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

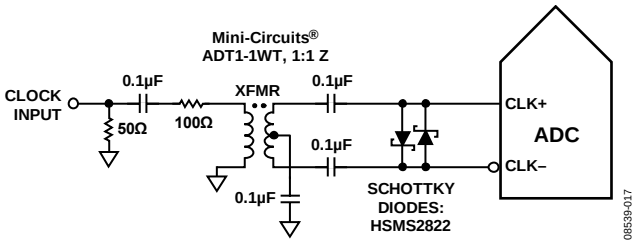


Figure 47. Transformer-Coupled Differential Clock (3 MHz to 200 MHz)

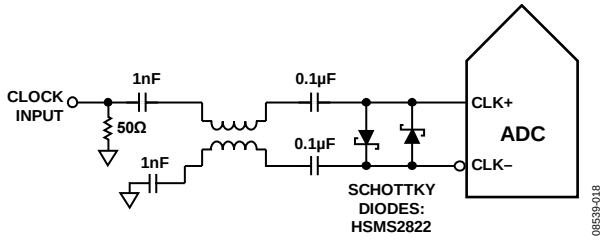


Figure 48. Balun-Coupled Differential Clock (Up to 4× Rated Sample Rate)

The RF balun configuration is recommended for clock frequencies between 80 MHz and 320 MHz, and the RF transformer is recommended for clock frequencies from 3 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the AD9649 to ~0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9649 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 49. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-4/AD9517-4 clock drivers offer excellent jitter performance.

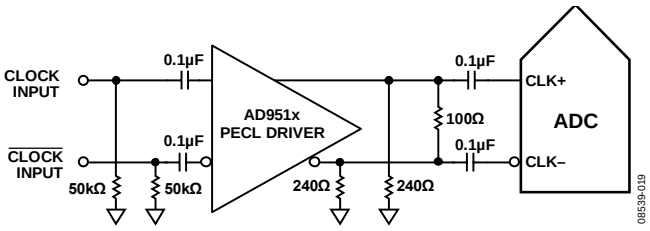


Figure 49. Differential PECL Sample Clock (Up to 4× Rated Sample Rate)

A third option is to ac couple a differential LVDS signal to the sample clock input pins as shown in Figure 50. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-4/AD9517-4 clock drivers offer excellent jitter performance.

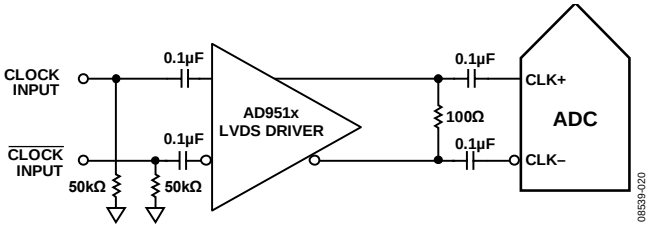


Figure 50. Differential LVDS Sample Clock (Up to 4× Rated Sample Rate)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK− pin to ground with a 0.1 µF capacitor (see Figure 51).

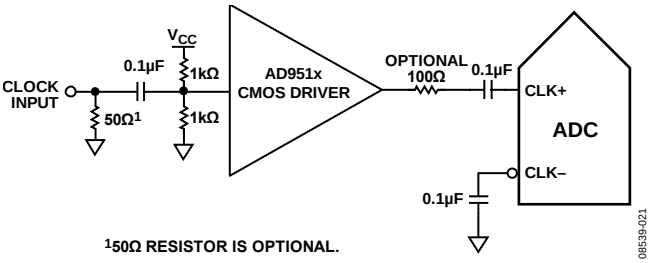


Figure 51. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9649 contains an input clock divider with the ability to divide the input clock by integer values of 1, 2, or 4.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a 50% duty cycle clock with ±5% tolerance is required to maintain optimum dynamic performance, as shown in Figure 52.

Jitter on the rising edge of the clock input can also impact dynamic performance and should be minimized, as discussed in the Jitter Considerations section of this datasheet.

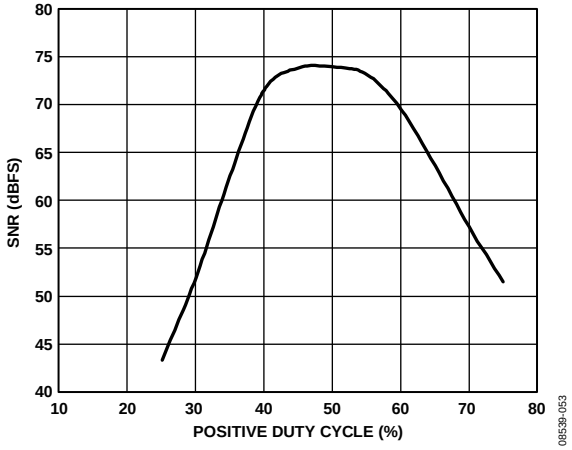


Figure 52. SNR vs. Clock Duty Cycle

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR from the low frequency SNR (SNR_{LF}) at a given input frequency (f_{INPUT}) due to jitter (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{INPUT} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the previous equation, the rms aperture jitter represents the clock input jitter specification. IF undersampling applications are particularly sensitive to jitter, as illustrated in Figure 53.

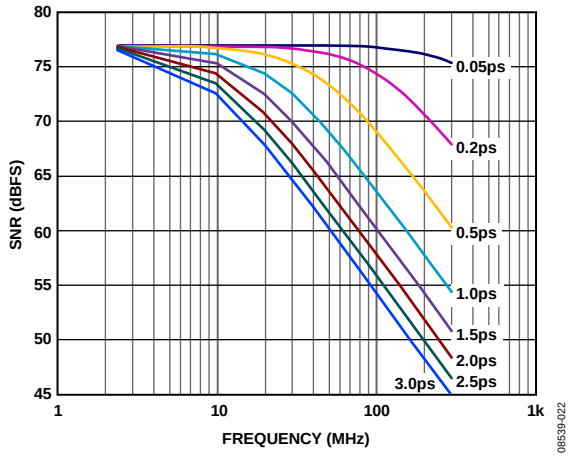


Figure 53. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases in which aperture jitter may affect the dynamic range of the AD9649. To avoid modulating the clock signal with digital noise, keep power supplies for clock drivers separate from the ADC output driver supplies. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step.

For more information, see the AN-501 Application Note and the AN-756 Application Note.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 54, the analog core power dissipated by the AD9649 is proportional to its sample rate. The digital power dissipation of the CMOS outputs are determined primarily by the strength of the digital drivers and the load on each output bit.

The maximum DRVDD current (I_{DRVDD}) can be calculated as

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where N is the number of output bits (15, in the case of the AD9649).

This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency of $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits that are switching, which is determined by the sample rate and the characteristics of the analog input signal.

Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 54 was taken using the same operating conditions as those used for the Typical Performance Characteristics, with a 5 pF load on each output driver.

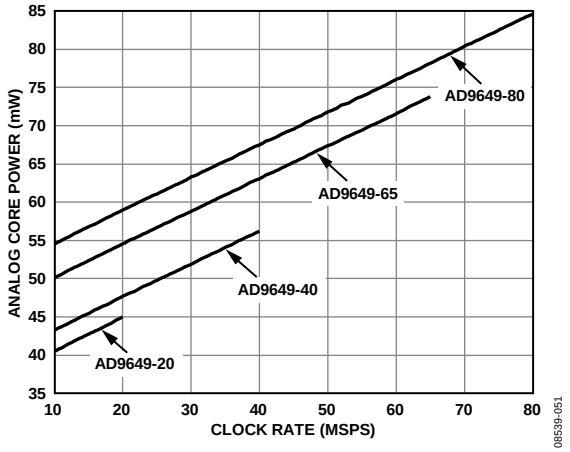


Figure 54. Analog Core Power vs. Clock Rate

In SPI mode, the AD9649 can be placed in power-down mode directly via the SPI port or by using the programmable external MODE pin. In non-SPI mode, power-down is achieved by asserting the PDWN pin high. In this state, the ADC typically dissipates 500 µW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin (or the MODE pin in SPI mode) low returns the AD9649 to normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details.

DIGITAL OUTPUTS

The AD9649 output drivers can be configured to interface with 1.8 V to 3.3 V CMOS logic families. Output data can also be multiplexed onto a single output bus to reduce the total number of traces required.

The CMOS output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies and may affect converter performance.

Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

The output data format can be selected to be either offset binary or twos complement by setting the SCLK/DFS pin when operating in the external pin mode (see Table 11).

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

Table 11. SCLK/DFS and SDIO/PDWN Mode Selection (External Pin Mode)

Voltage at Pin	SCLK/DFS	SDIO/PDWN
GND	Offset binary (default)	Normal operation (default)
DRVDD	Twos complement	Outputs disabled

Digital Output Enable Function (OEB)

When using the SPI interface, the data outputs and DCO can be independently three-stated by using the programmable external MODE pin. The OEB function of the MODE pin is enabled via Bits[6:5] of Register 0x08.

If the MODE pin is configured to operate in traditional OEB mode and the MODE pin is low, the output data drivers and DCOs are enabled. If the MODE pin is high, the output data drivers and DCOs are placed in a high impedance state. This OEB function is not intended for rapid access to the data bus. Note that the MODE pin is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

TIMING

The AD9649 provides latched data with a pipeline delay of eight clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

Minimize the length of the output data lines and loads placed on them to reduce transients within the AD9649. These transients may degrade converter dynamic performance.

The lowest typical conversion rate of the AD9649 is 3 MSPS. At clock rates below 3 MSPS, dynamic performance may degrade.

Data Clock Output (DCO)

The AD9649 provides a data clock output (DCO) signal that is intended for capturing the data in an external register. The CMOS data outputs are valid on the rising edge of DCO, unless the DCO clock polarity has been changed via the SPI. See Figure 2 for a graphical timing description.

Table 12. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode	OR
VIN+ – VIN–	< –VREF – 0.5 LSB	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ – VIN–	= –VREF	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ – VIN–	= 0	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ – VIN–	= +VREF – 1.0 LSB	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ – VIN–	> +VREF – 0.5 LSB	11 1111 1111 1111	01 1111 1111 1111	1

BUILT-IN SELF-TEST (BIST) AND OUTPUT TEST

The AD9649 includes a built-in test feature designed to enable verification of the integrity of each channel, as well as facilitate board-level debugging. Also included is a built-in self-test (BIST) feature that verifies the integrity of the digital datapath of the AD9649. Various output test options are also provided to place predictable values on the outputs of the AD9649.

BUILT-IN SELF-TEST (BIST)

The BIST is a thorough test of the digital portion of the selected AD9649 signal path. Perform the BIST test after a reset to ensure that the part is in a known state. During the BIST test, data from an internal pseudorandom noise (PN) source is driven through the digital datapath of both channels, starting at the ADC block output. At the datapath output, CRC logic calculates a signature from the data. The BIST sequence runs for 512 cycles and then stops. When the BIST sequence is complete, the BIST compares the signature results with a predetermined value. If the signatures match, the BIST sets Bit 0 of Register 0x24, signifying that the test passed. If the BIST test failed, Bit 0 of Register 0x24 is cleared. The outputs are connected during this test so that the PN sequence can be observed as it runs. Writing the value 0x05 to Register 0x0E runs the BIST, enabling Bit 0 (BIST enable) of Register 0x0E and resetting the PN sequence generator, Bit 2 (BIST init) of Register 0x0E. Upon completion of the BIST, Bit 0 of Register 0x24 is automatically cleared. The PN sequence can be continued from its last value by writing a 0 in Bit 2 of Register 0x0E. However, if the PN sequence is not reset, the signature calculation does not equal the predetermined value at the end of the test. The user must then rely on verifying the output data.

OUTPUT TEST MODES

The output test options are described in Table 16 at Address 0x0D. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

SERIAL PORT INTERFACE (SPI)

The AD9649 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK (SCLK/DFS, the SDIO (SDIO/PDWN), and the CSB (see Table 13). The SCLK (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) is an active-low control that enables or disables the read and write cycles.

Table 13. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active-low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 55 and Table 5.

Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits, as shown in Figure 55.

All data is composed of 8-bit words. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB-first mode or in LSB-first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

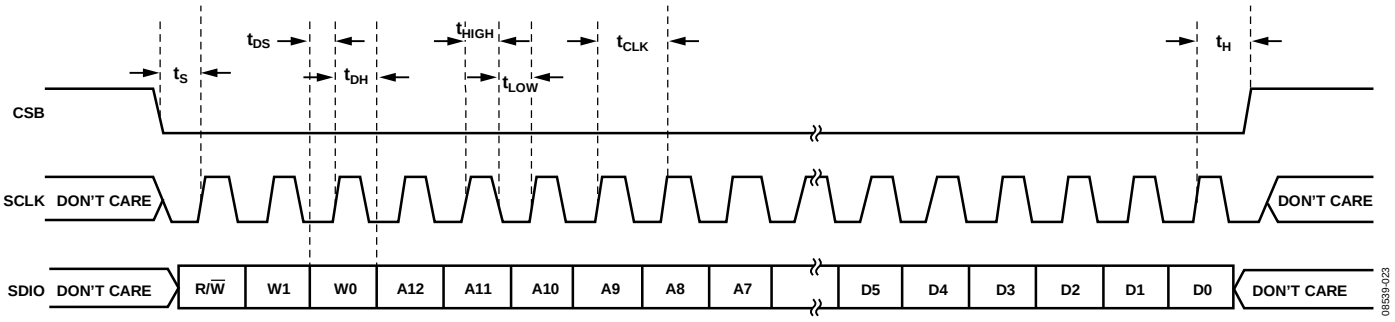


Figure 55. Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 13 constitute the physical interface between the programming device of the user and the serial port of the AD9649. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. For detailed information about one method for SPI configuration, refer to the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9649 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

The SDIO/PDWN and SCLK/DFS pins serve a dual function when the SPI interface is not being used. When the pins are strapped to DRVDD or ground during device power-on, they are associated with a specific function. The Digital Outputs section describes the strappable functions supported on the AD9649.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/PDWN pin and the SCLK/DFS pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the power-down and output data format feature control. In this mode, connect the CSB chip select to DRVDD, which disables the serial port interface.

Table 14. Mode Selection

Pin	External Voltage	Configuration
SDIO/PDWN	DRVDD	Chip power-down mode
	AGND (default)	Normal operation (default)
SCLK/DFS	DRVDD	Twos complement enabled
	AGND (default)	Offset binary enabled

SPI ACCESSIBLE FEATURES

Table 15 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9649 part-specific features are described in detail in Table 16.

Table 15. Features Accessible Using the SPI

Feature	Description
Modes	Allows the user to set either power-down mode or standby mode
Offset Adjust	Allows the user to digitally adjust the converter offset
Test Mode	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set up outputs
Output Phase	Allows the user to set the output clock polarity
Output Delay	Allows the user to vary the DCO delay

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table (see Table 16) contains eight bit locations. The memory map is roughly divided into four sections: the chip configuration registers (Address 0x00 to Address 0x02); the device transfer registers (Address 0xFF); the program registers, including setup, control, and test (Address 0x08 to Address 0x2A); and the digital feature control registers (Address 0x101).

Table 16 documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x2A, the OR/MODE select register, has a hexadecimal default value of 0x01. This means that in Address 0x2A, Bits[7:1] = 0, and Bit 0 = 1. This setting is the default OR/MODE setting. The default value results in the programmable external MODE/OR pin (Pin 23) functioning as an out-of-range digital output. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI.* This document details the functions controlled by Register 0x00 to Register 0xFF. The remaining register, Register 0x101, is documented in the Memory Map Register Descriptions section that follows Table 16.

OPEN LOCATIONS

All address and bit locations that are not included in the SPI map are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x2A). If the entire address location is open, it is omitted from the SPI map (for example, Address 0x13) and should not be written.

DEFAULT VALUES

After the AD9649 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table (see Table 16).

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Address 0x08 to Address 0x18 are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and then the bit autoclears.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 16 are not currently supported for this device.

Table 16.

Addr. (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Def. Value (Hex)	Default Notes/ Comments
Chip configuration registers											
0x00	SPI port configuration	0	LSB first	Soft reset[1]	1	1	Soft reset[1]	LSB first	0	0x18	The nibbles are mirrored so that LSB or MSB first mode registers correctly, regardless of shift mode.
0x01	Chip ID	8-bit chip ID, Bits[7:0] AD9649 = 0x6F								Read only	Unique chip ID used to differentiate devices; read only.
0x02	Chip grade	Open	Speed grade ID, Bits[6:4] (identify device variants of chip ID) 20 MSPS = 000 40 MSPS = 001 65 MSPS = 010 80 MSPS = 011			Open				Read only	Unique speed grade ID used to differentiate devices; read only.
Device transfer registers											
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Transfer	0x00	Synchronously transfers data from the master shift register to the slave.
Program registers											
0x08	Modes	External Pin 23 MODE input enable	External Pin 23 function when high 00 = full power-down 01 = standby 10 = normal mode, output disabled 11 = normal mode, output enabled		Open	Open	Open	00 = chip run 01 = full power-down 10 = standby 11 = chip wide digital reset		0x00	Determines various generic modes of chip operation.
0x0B	Clock divide	Open					Clock divider, Bits[2:0] Clock divide ratio 000 = divide-by-1 001 = divide-by-2 011 = divide-by-4			0x00	The divide ratio is the value + 1.
0x0D	Test mode	User test mode 00 = single 01 = alternate 10 = single once 11 = alternate once		Reset PN long gen	Reset PN short gen	Output test mode, Bits[3:0] (local) 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN 23 sequence 0110 = PN 9 sequence 0111 = 1/0 word toggle 1000 = user input 1001 = 1/0 bit toggle 1010 = 1× sync 1011 = one bit high 1100 = mixed bit frequency				0x00	When set, the test data is placed on the output pins in place of normal data.
0x0E	BIST enable	Open	Open	Open	Open	Open	BIST init	Open	BIST enable	0x00	When Bit 0 is set, the built-in self-test function is initiated.
0x10	Offset adjust	8-bit device offset adjustment, Bits[7:0] (local) Offset adjust in LSBs from +127 to −128 (twos complement format)								0x00	Device offset trim.

Addr. (Hex)	Register Name	(MSB) Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Def. Value (Hex)	Default Notes/ Comments
0x14	Output mode	00 = 3.3 V CMOS 10 = 1.8 V CMOS		Open	Output disable	Open	Output invert	00 = offset binary 01 = twos complement 10 = gray code 11 = offset binary		0x00	Configures the outputs and the format of the data.
0x15	Output adjust	3.3 V DCO drive strength 00 = 1 stripe (default) 01 = 2 stripes 10 = 3 stripes 11 = 4 stripes		1.8 V DCO drive strength 00 = 1 stripe 01 = 2 stripes 10 = 3 stripes (default) 11 = 4 stripes		3.3 V data drive strength 00 = 1 stripe (default) 01 = 2 stripes 10 = 3 stripes 11 = 4 stripes		1.8 V data drive strength 00 = 1 stripe 01 = 2 stripes 10 = 3 stripes (default) 11 = 4 stripes		0x22	Determines CMOS output drive strength properties.
0x16	Output phase	DCO output polarity 0 = normal 1 = inv	Open	Open	Open	Open	Input clock phase adjust, Bits[2:0] (Value is number of input clock cycles of phase delay) 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles 111 = 7 input clock cycles			0x00	On devices that use global clock divide, determines which phase of the divider output is used to supply the output clock; internal latching is unaffected.
0x17	Output delay	Enable DCO delay	Open	Enable data delay	Open		DCO/data delay, Bits[2:0] 000 = 0.56 ns 001 = 1.12 ns 010 = 1.68 ns 011 = 2.24 ns 100 = 2.80 ns 101 = 3.36 ns 110 = 3.92 ns 111 = 4.48 ns			0x00	Sets the fine output delay of the output clock but does not change internal timing.
0x19	USER_PATT1_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined Pattern 1 LSB.
0x1A	USER_PATT1_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined Pattern 1 MSB.
0x1B	USER_PATT2_LSB	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User-defined Pattern 2 LSB.
0x1C	USER_PATT2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User-defined Pattern 2 MSB.
0x24	BIST signature LSB	BIST signature, Bits[7:0]								0x00	Least significant byte of BIST signature, read only.
0x2A	OR/MODE select	Open	Open	Open	Open	Open	Open	Open	0 = MODE 1 = OR (default)	0x01	Selects I/O functionality in conjunction with Address 0x08 for MODE (input) or OR (output) on External Pin 23.
Digital feature-control register											
0x101	USR2	1	Open	Open	Open	Enable GCLK detect	Run GCLK	Open	Disable SDIO pull-down	0x88	Enables internal oscillator for clock rates of <5 MHz.

[1.] See the Soft Reset section for limitations on use of soft reset.

MEMORY MAP REGISTER DESCRIPTIONS

For additional information about functions controlled in Register 0x00 to Register 0xFF, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

USR2 (Register 0x101)

Bit 3—Enable GCLK Detect

Normally set high, Bit 3 enables a circuit that detects encode rates below ~5 MSPS. When a low encode rate is detected, an internal oscillator, GCLK, is enabled, ensuring the proper operation of several circuits. If set low, the detector is disabled.

Bit 2—Run GCLK

Bit 2 enables the GCLK oscillator. For some applications with encode rates below 10 MSPS, it may be preferable to set this bit high to supersede the GCLK detector.

Bit 0—Disable SDIO Pull-Down

Bit 0 can be set high to disable the internal 30 kΩ pull-down on the SDIO pin, which can be used to limit the loading when many devices are connected to the SPI bus.

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting the design and layout of the AD9649 as a system, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

Power and Ground Recommendations

When connecting power to the AD9649, it is strongly recommended that two separate supplies be used. Use one 1.8 V supply for analog (AVDD); use a separate 1.8 V to 3.3 V supply for the digital output supply (DRVDD). If a common 1.8 V AVDD and DRVDD supply must be used, the AVDD and DRVDD domains must be isolated with a ferrite bead or filter choke and separate decoupling capacitors. Several different decoupling capacitors can be used to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

A single PCB ground plane should be sufficient when using the AD9649. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

When powering down the AD9649, power off AVDD and DRVDD simultaneously, or DRVDD must be removed before AVDD.

Exposed Paddle Thermal Heat Sink Recommendations

The exposed paddle (Pin 0) is the only ground connection for the AD9649; therefore, it must be connected to analog ground (AGND) on the customer's PCB. To achieve the best electrical and thermal performance, mate an exposed (no solder mask) continuous copper plane on the PCB to the AD9649 exposed paddle, Pin 0.

The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. Fill or plug these vias with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and the PCB, a silkscreen should be overlaid to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. For detailed information about packaging and PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

Encode Clock

For optimum dynamic performance, use a low jitter encode clock source with a 50% duty cycle (±5%) to clock the AD9649.

VCM

The VCM pin should be decoupled to ground with a 0.1 µF capacitor, as shown in Figure 39.

RBIAS

The AD9649 requires that a 10 kΩ resistor be placed between the RBIAS pin and ground. This resistor sets the master current reference of the ADC core and should have at least a 1% tolerance.

Reference Decoupling

Externally decouple the VREF pin to ground with a low ESR, 1.0 µF capacitor in parallel with a low ESR, 0.1 µF ceramic capacitor.

SPI Port

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9649 to keep these signals from transitioning at the converter inputs during critical sampling periods.

Soft Reset

In applications with DRVDD ≥ 2.75 V, do not perform soft reset (Register 0x00 Bit 2 and Bit 5 = 1). Soft reset restores AD9649 defaults already available at power-up and is not needed.

OUTLINE DIMENSIONS

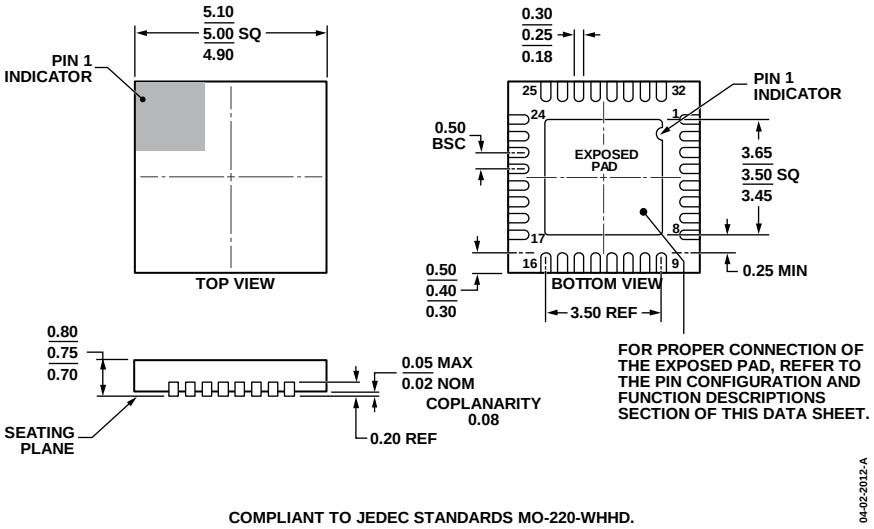


Figure 56. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 mm × 5 mm Body, Very Very Thin Quad
(CP-32-11)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD9649BCPZ-80	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-11
AD9649BCPZRL7-80	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-11
AD9649BCPZ-65	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-11
AD9649BCPZRL7-65	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-11
AD9649BCPZ-40	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-11
AD9649BCPZRL7-40	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-11
AD9649BCPZ-20	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-11
AD9649BCPZRL7-20	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-11
AD9649-80EBZ		Evaluation Board	
AD9649-65EBZ		Evaluation Board	
AD9649-40EBZ		Evaluation Board	
AD9649-20EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] For the AD9649BCPZ models, the exposed paddle (Pin 0) is the only GND connection on the chip and must be connected to the PCB AGND.

NOTES

D08539-0-2/17(B)

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

AD9649-40EBZ AD9649-65EBZ AD9649BCPZ-40 AD9649BCPZ-65 AD9649BCPZ-20 AD9649BCPZ-80 AD9649BCPZRL7-40 AD9649-20EBZ AD9649BCPZRL7-65 AD9649-80EBZ AD9649BCPZRL7-80 AD9649BCPZRL7-20