TPS22961 3.5-V, 6-A, Ultra-low Resistance Load Switch

1 Features

- Integrated Single Channel Load Switch
- VBIAS Voltage Range: 3 V to 5.5 V
- Input Voltage Range: 0.8 V to 3.5 V
- Ultra low R_{ON} Resistance
  – R_{ON} = 4.4 mΩ at V_{IN} = 1.05 V (V_{BIAS} = 5 V)
- 6A Maximum Continuous Switch Current
- Low Quiescent Current < 1 µA (max)
- Low Control Input Threshold Enables use of 1.2-V/1.8-V/2.5-V/3.3-V Logic
- Controlled Slew Rate
  – t_R = 4.2 µs at V_{IN} = 1.05 V (V_{BIAS} = 5 V)
- Quick Output Discharge (QOD)
- SON 8-terminal Package with Thermal Pad
- ESD Performance Tested per JESD 22
  – 2-kV HBM and 1-kV CDM

2 Applications

- Ultrabook™/Notebooks
- Desktops
- Servers
- Set-top Boxes
- Telecom Systems
- Tablet PC

3 Description

The TPS22961 is a small, ultra-low R_{ON}, single channel load switch with controlled turn on. The device contains an N-channel MOSFET that can operate over an input voltage range of 0.8 V to 3.5 V and supports a maximum continuous current of 6 A.

The combination of ultra-low R_{ON} and high current capability of the device makes it ideal for driving processor rails with very tight voltage dropout tolerances. Quick rise time of the device allows for power rails to come up quickly when the device is enabled, thereby reducing response time for power distribution. The switch can be independently controlled via the ON terminal, which is capable of interfacing directly with low-voltage control signals originating from microcontrollers or low voltage discrete logic. The device further reduces the total solution size by integrating a 260 Ω pull-down transistor for quick output discharge (QOD) when the switch is turned off.

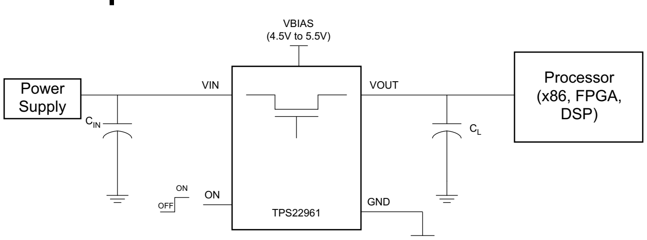
The TPS22961 is available in a small, space-saving 3 mm x 3 mm 8-SON package (DNY) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
TPS22961	WSON (8)	3.00 mm x 3.00 mm

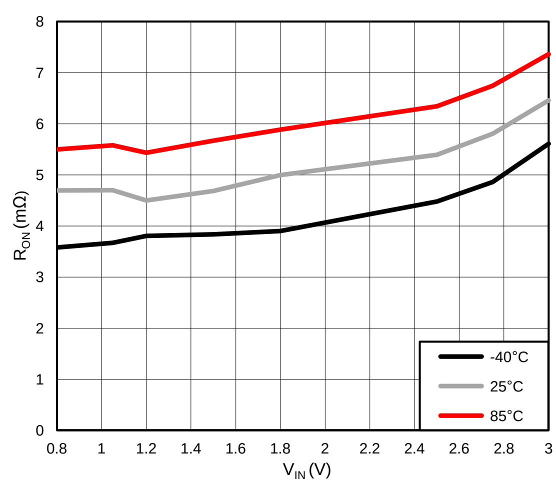
(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Typical Application: driving high current core rails for a processor

R_{ON} vs V_{IN} (V_{BIAS} = 5 V, I_{OUT} = –200 mA)



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5 Revision History

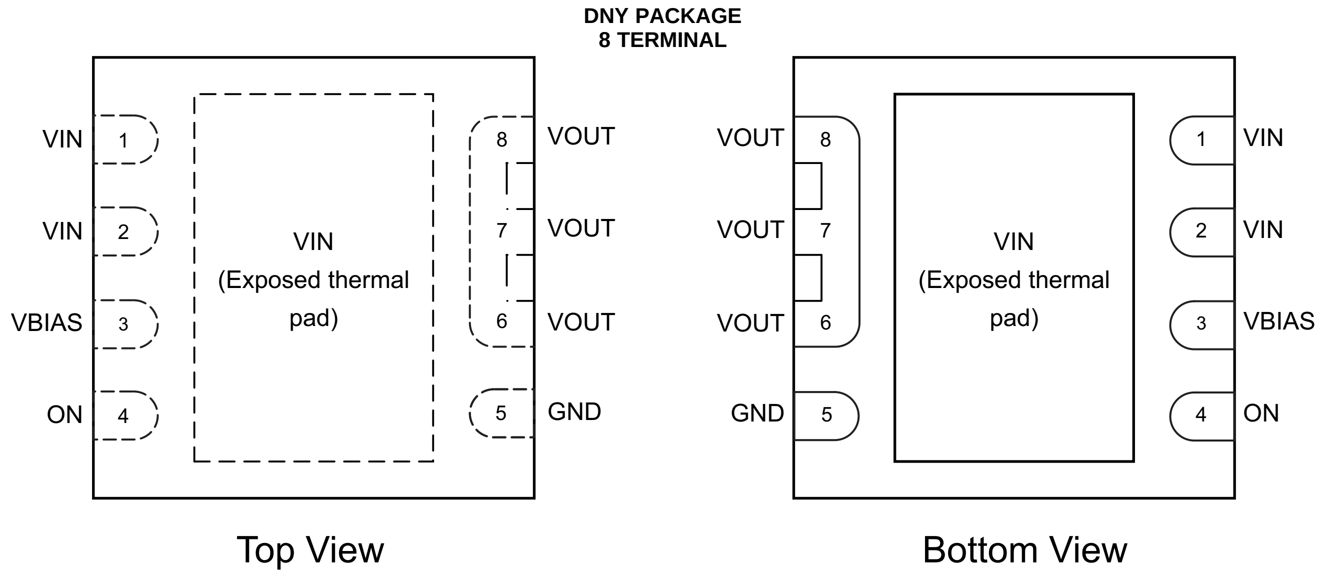
Changes from Revision A (February 2014) to Revision B **Page**

- Fixed caption error in Filtered Output curve. ... 18

Changes from Original (February 2014) to Revision A **Page**

- Initial release of full version. ... 1

6 Terminal Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1, 2	I	Switch input. Place ceramic bypass capacitor(s) between this terminal and GND. See *Detailed Description* section for more information.
VIN	Exposed thermal Pad	I	Switch input. Place ceramic bypass capacitor(s) between this terminal and GND. See *Detailed Description* section for more information.
VBIAS	3	I	Bias voltage. Power supply to the device.
ON	4	I	Active high switch control input. Do not leave floating.
GND	5	–	Ground.
VOUT	6, 7, 8	O	Switch output. Place ceramic bypass capacitor(s) between this terminal and GND. See *Detailed Description* section for more information.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	–0.3	4	V
V_{BIAS}	Bias voltage range	–0.3	6	V
V_{OUT}	Output voltage range	–0.3	4	V
V_{ON}	ON pin voltage range	–0.3	6	V
I_{MAX}	Maximum Continuous Switch Current		6	A
I_{PLS}	Maximum Pulsed Switch Current, pulse < 300 µs, 2% duty cycle		8	A
T_A	Operating free-air temperature range	–40	85	°C
T_J	Maximum junction temperature		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{STG}	Storage temperature range	–65	150	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
V_{ESD} [(1)]	Human-Body Model (HBM)[(2)]		2	kV
	Charged-Device Model (CDM)[(3)]		1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		0.8	V_{BIAS} – 1.95	V
V_{BIAS}	Bias voltage range		3	5.5	V
V_{ON}	ON voltage range		0	5.5	V
V_{OUT}	Output voltage range			V_{IN}	V
$V_{IH, ON}$	High-level voltage, ON	V_{BIAS} = 3 V to 5.5 V	1.2	5.5	V
$V_{IL, ON}$	Low-level voltage, ON	V_{BIAS} = 3 V to 5.5 V	0	0.5	V
C_{IN}	Input Capacitor		1[(1)]		µF

(1) Refer to *Detailed Description* section.

7.4 Thermal Information

THERMAL METRIC[(1)]		TPS22961	UNIT
		DNY	
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	44.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.4	
θ_{JB}	Junction-to-board thermal resistance	17.6	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	17.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics, V_{BIAS} = 5.0 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ 85°C (full) and V_{BIAS} = 5.0 V. Typical values are for T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = 3 V, V_{ON} = V_{BIAS} = 5.0 V		Full		0.6	1	µA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V		Full		0.6	1	µA
$I_{SD, VIN}$	V_{IN} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 3.0 V	Full		0.0009	0.1	µA
			V_{IN} = 2.5 V			0.0008	0.1	
			V_{IN} = 2.0 V			0.0007	0.1	
			V_{IN} = 1.05 V			0.0007	0.1	
			V_{IN} = 0.8 V			0.0006	0.1	
I_{ON}	ON terminal input leakage current	V_{ON} = 5.5 V		Full			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5.0 V	V_{IN} = 3.0 V	25°C		6.5	8	mΩ
				Full			8.8	
			V_{IN} = 2.5 V	25°C		5.3	6.3	mΩ
				Full			7.2	
			V_{IN} = 2.0 V	25°C		4.8	5.8	mΩ
				Full			6.7	
			V_{IN} = 1.05 V	25°C		4.4	5.3	mΩ
				Full			6.2	
			V_{IN} = 0.8 V	25°C		4.3	5.3	mΩ
				Full			6.1	
R_{PD}	Output pulldown resistance	V_{IN} = 5.0 V, V_{ON} = 0 V, V_{OUT} = 1 V		Full		260	300	Ω

7.6 Electrical Characteristics, V_{BIAS} = 3.0 V

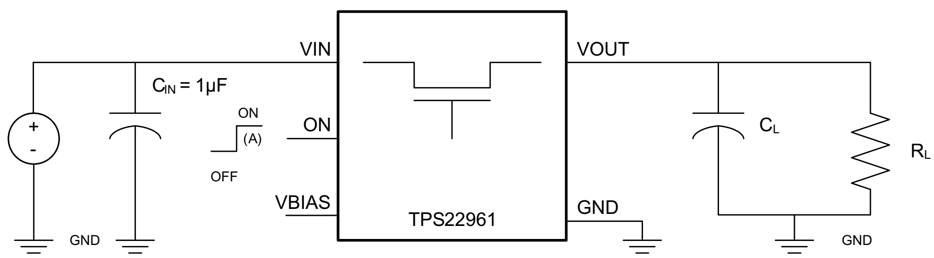
Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ 85°C (full) and V_{BIAS} = 3.0 V. Typical values are for T_A = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0, V_{IN} = 1 V, V_{ON} = V_{BIAS} = 3.0 V		Full		0.3	1	µA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V		Full		0.3	1	µA
$I_{SD, VIN}$	V_{IN} shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 1.05 V	Full		0.001	0.1	µA
			V_{IN} = 0.8 V			0.0008	0.1	
I_{ON}	ON terminal input leakage current	V_{ON} = 5.5 V		Full			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 3.0 V	V_{IN} =1.05 V	25°C		6.7	8.4	mΩ
				Full			9.2	
			V_{IN} = 0.8 V	25°C		5.8	7.0	mΩ
				Full			7.9	
R_{PD}	Output pull-down resistance	V_{IN} = 3V, V_{ON} = 0 V, V_{OUT} = 1 V		Full		260	300	Ω

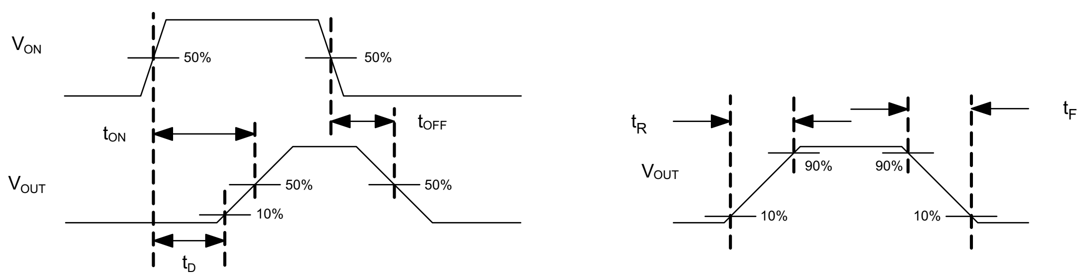
7.7 Switching Characteristics

Refer to the timing test circuit in Figure 1 (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = 2.5 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF		10.0		µs
t_{OFF}	Turn-off time			3.5		
t_R	V_{OUT} rise time			6.3		
t_F	V_{OUT} fall time			2.0		
t_D	Delay time			8.1		
V_{IN} = 1.05 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	L = 2.2 µH (DCR = 0.33 Ω), C = 2 x 22 µF (Refer to *Typical Application Powering Rails Sensitive to Ringing and Overvoltage due to Fast Rise Time* and Figure 31)	8.1	11.3	17.3	µs
t_{OFF}	Turn-off time			13700		
t_R	V_{OUT} rise time		5	9.5	12.5	
t_F	V_{OUT} fall time			44200		
t_D	Delay time		6.7	9.3	12.5	
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF		9.7		µs
t_{OFF}	Turn-off time			6.0		
t_R	V_{OUT} rise time			3.2		
t_F	V_{OUT} fall time			1.8		
t_D	Delay time			8.1		
V_{IN} = 1.05 V, V_{ON} = 5 V, V_{BIAS} = 3.0 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF		19.1		µs
t_{OFF}	Turn-off time			4.7		
t_R	V_{OUT} rise time			9.0		
t_F	V_{OUT} fall time			2.0		
t_D	Delay time			15.6		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 3.0 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF		19.0		µs
t_{OFF}	Turn-off time			5.4		
t_R	V_{OUT} rise time			7.0		
t_F	V_{OUT} fall time			1.9		
t_D	Delay time			15.7		



Timing Test Circuit

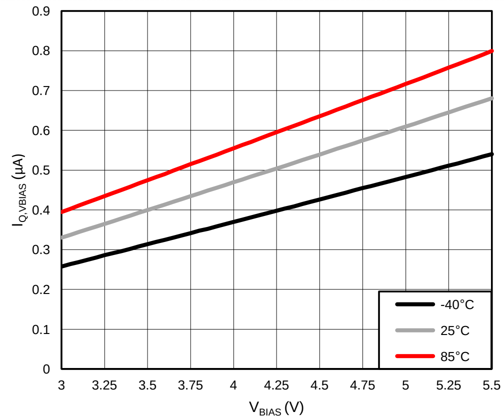


Timing Waveforms

(A) Rise and fall times of the control signal is 100ns.

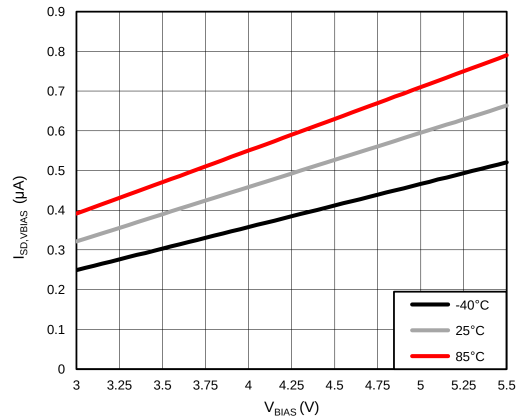
Figure 1. Switching Characteristics Measurement Setup and Definitions

7.8 Typical Characteristics



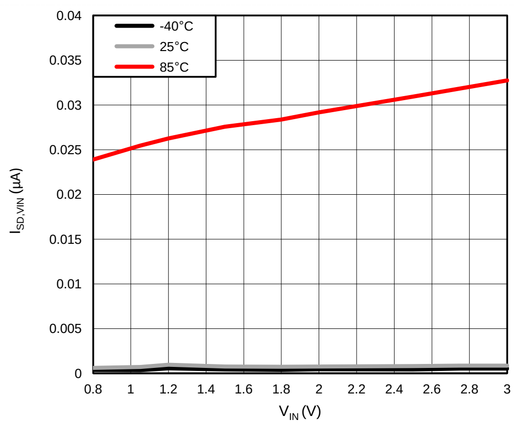
V_{IN} = 1.05 V V_{ON} = 5 V I_{OUT} = 0 A

Figure 2. $I_{Q,VBIAS}$ vs V_{BIAS}



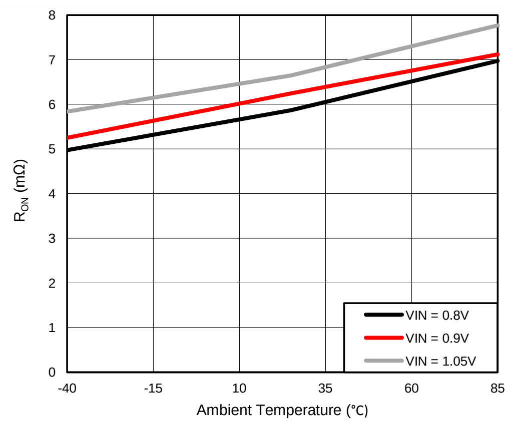
V_{ON} = 0 V V_{OUT} = 0 V

Figure 3. $I_{SD,VBIAS}$ vs V_{BIAS}



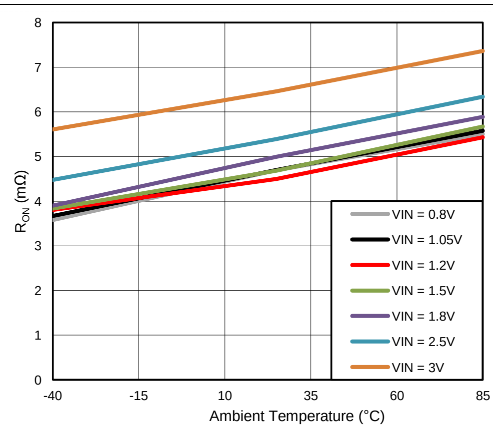
V_{BIAS} = 5 V V_{ON} = 0 V V_{OUT} = 0 V

Figure 4. $I_{SD,VIN}$ vs V_{IN}



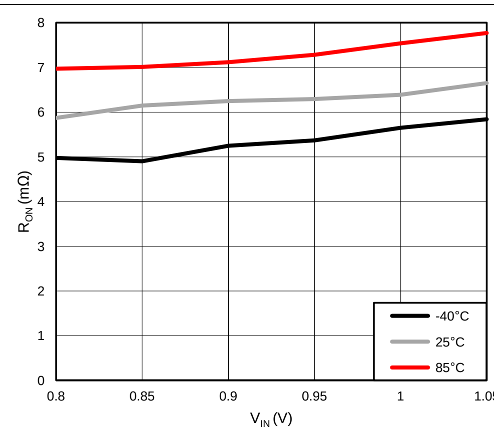
V_{BIAS} = 3 V V_{ON} = 5 V I_{OUT} = –200 mA

Figure 5. R_{ON} vs Ambient Temperature



V_{BIAS} = 5 V V_{ON} = 5 V I_{OUT} = –200 mA

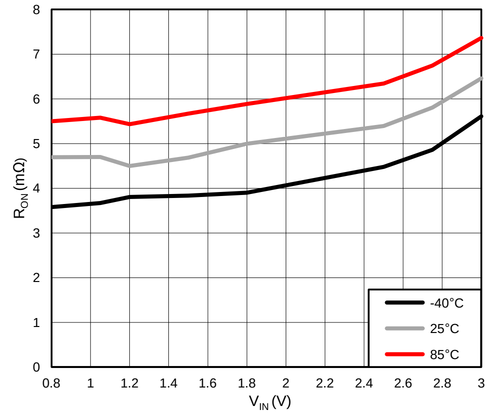
Figure 6. R_{ON} vs Ambient Temperature



V_{BIAS} = 3 V V_{ON} = 5 V I_{OUT} = –200 mA

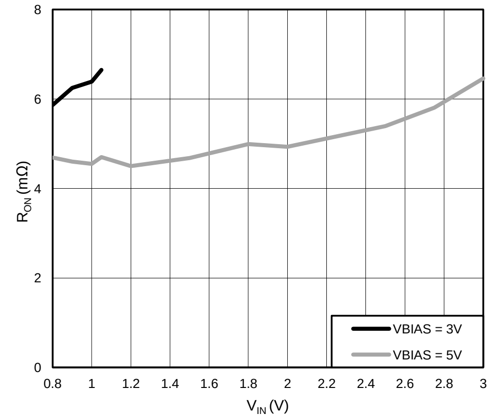
Figure 7. R_{ON} vs V_{IN}

Typical Characteristics (continued)



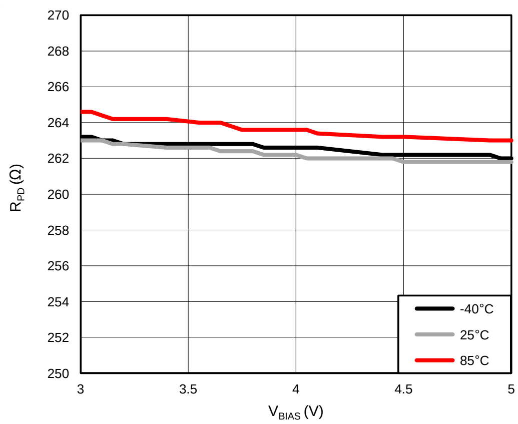
V_{BIAS} = 5 V V_{ON} = 5 V I_{OUT} = –200 mA

Figure 8. R_{ON} vs V_{IN}



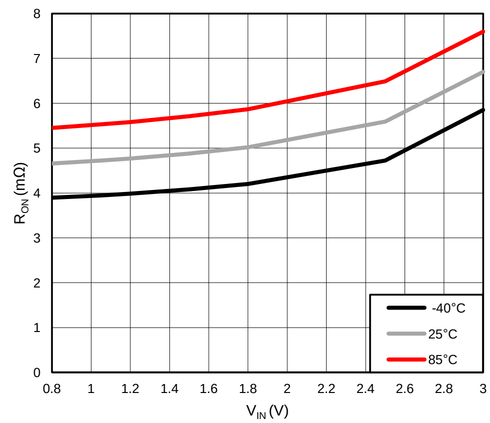
T_A = 25°C V_{ON} = 5 V I_{OUT} = –200 mA

Figure 9. R_{ON} vs V_{IN}



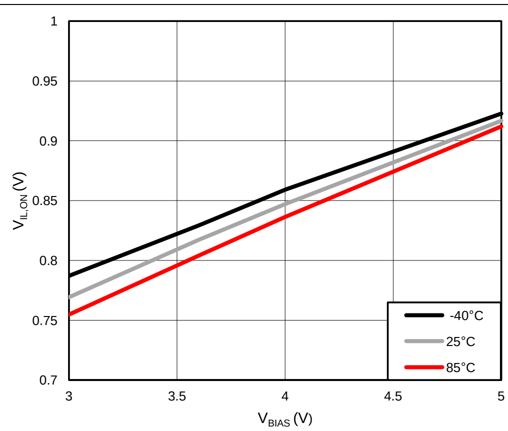
V_{ON} = 0 V V_{IN} = 1.05 V V_{OUT} = 1 V

Figure 10. R_{PD} vs V_{BIAS}



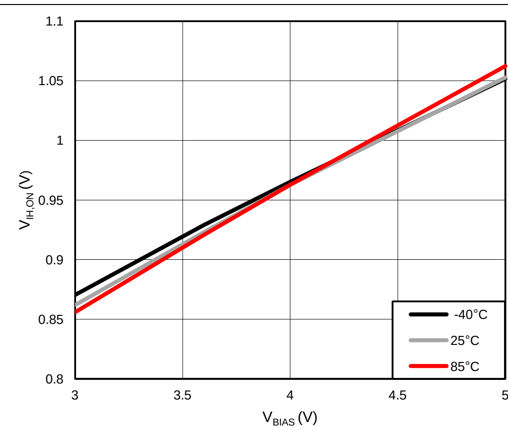
V_{BIAS} = 5 V V_{ON} = 5 V I_{OUT} = –6 A

Figure 11. R_{ON} vs V_{IN} at 6A load



V_{IN} = V_{BIAS} – 2 V

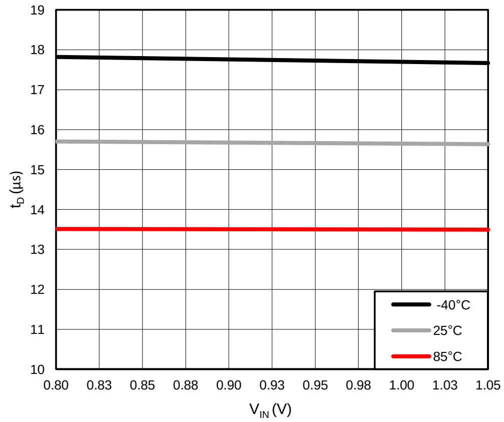
Figure 12. $V_{IL,ON}$ vs V_{BIAS}



V_{IN} = V_{BIAS} – 2 V

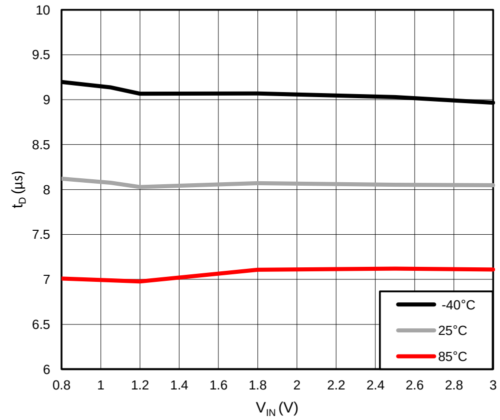
Figure 13. $V_{IH,ON}$ vs V_{BIAS}

Typical Characteristics (continued)



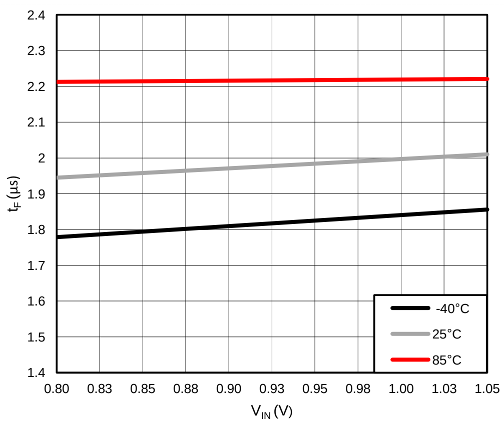
V_{BIAS} = 3 V R_L = 10 Ω C_L = 0.1 µF

Figure 14. t_D vs V_{IN}



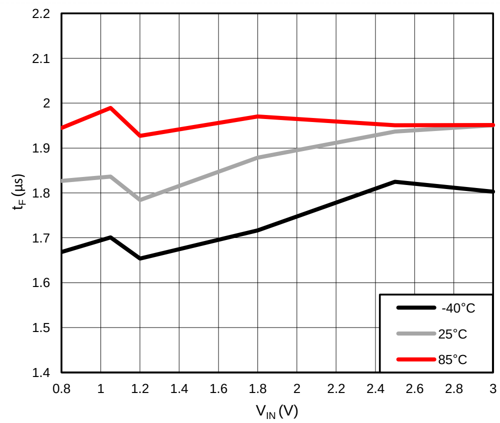
V_{BIAS} = 5 V R_L = 10 Ω C_L = 0.1 µF

Figure 15. t_D vs V_{IN}



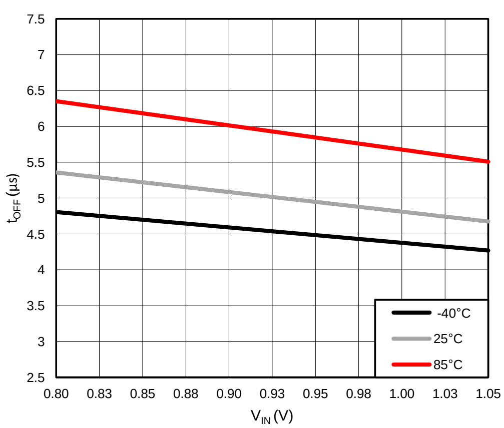
V_{BIAS} = 3 V R_L = 10 Ω C_L = 0.1 µF

Figure 16. t_F vs V_{IN}



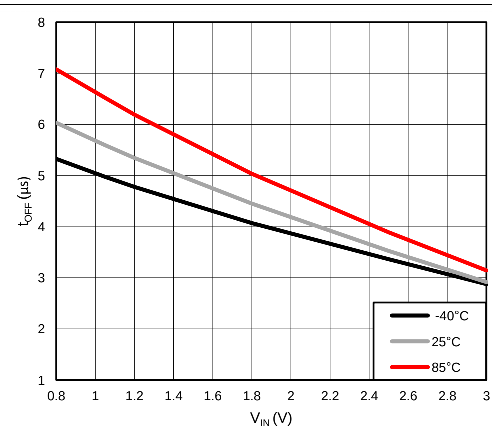
V_{BIAS} = 5 V R_L = 10 Ω C_L = 0.1 µF

Figure 17. t_F vs V_{IN}



V_{BIAS} = 3 V R_L = 10 Ω C_L = 0.1 µF

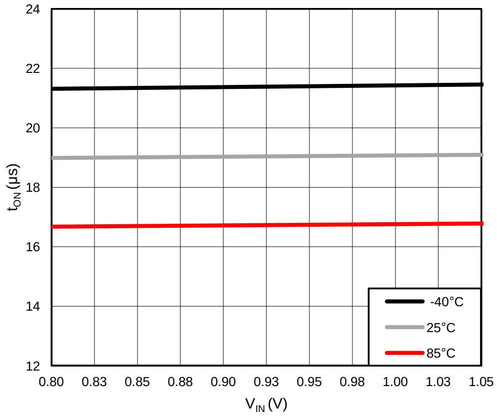
Figure 18. t_{OFF} vs V_{IN}



V_{BIAS} = 5 V R_L = 10 Ω C_L = 0.1 µF

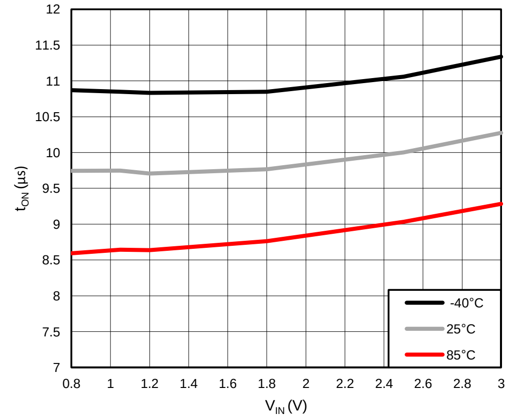
Figure 19. t_{OFF} vs V_{IN}

Typical Characteristics (continued)



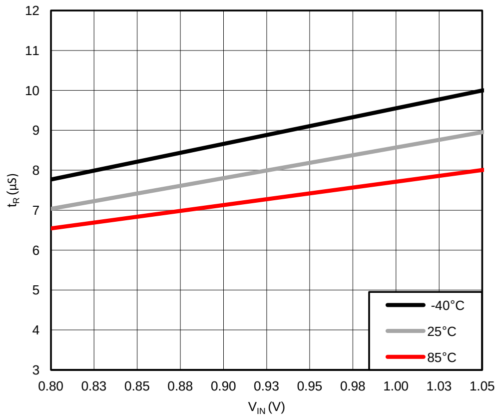
V_{BIAS} = 3 V R_L = 10 Ω C_L = 0.1 µF

Figure 20. t_{ON} vs V_{IN}



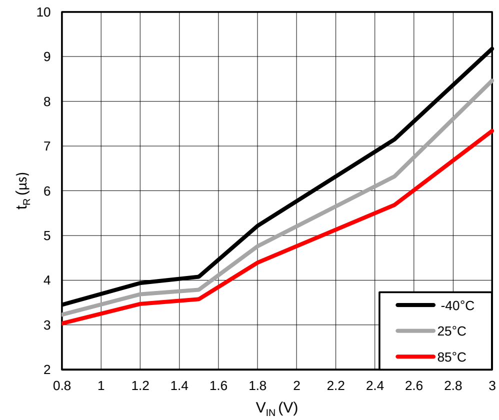
V_{BIAS} = 5 V R_L = 10 Ω C_L = 0.1 µF

Figure 21. t_{ON} vs V_{IN}



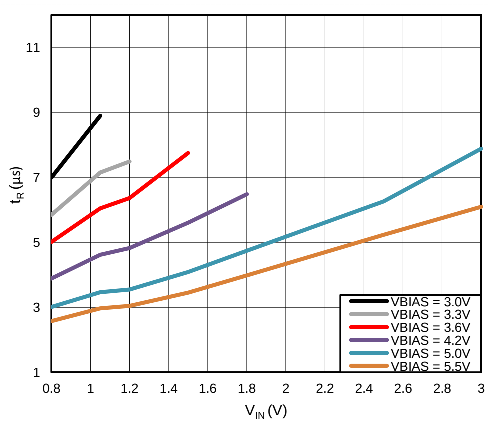
V_{BIAS} = 3 V R_L = 10 Ω C_L = 0.1 µF

Figure 22. t_R vs V_{IN}



V_{BIAS} = 5 V R_L = 10 Ω C_L = 0.1 µF

Figure 23. t_R vs V_{IN}



T_A = 25°C R_L = 10 Ω C_L = 0.1 µF

Figure 24. t_R vs V_{IN} for Various V_{BIAS}

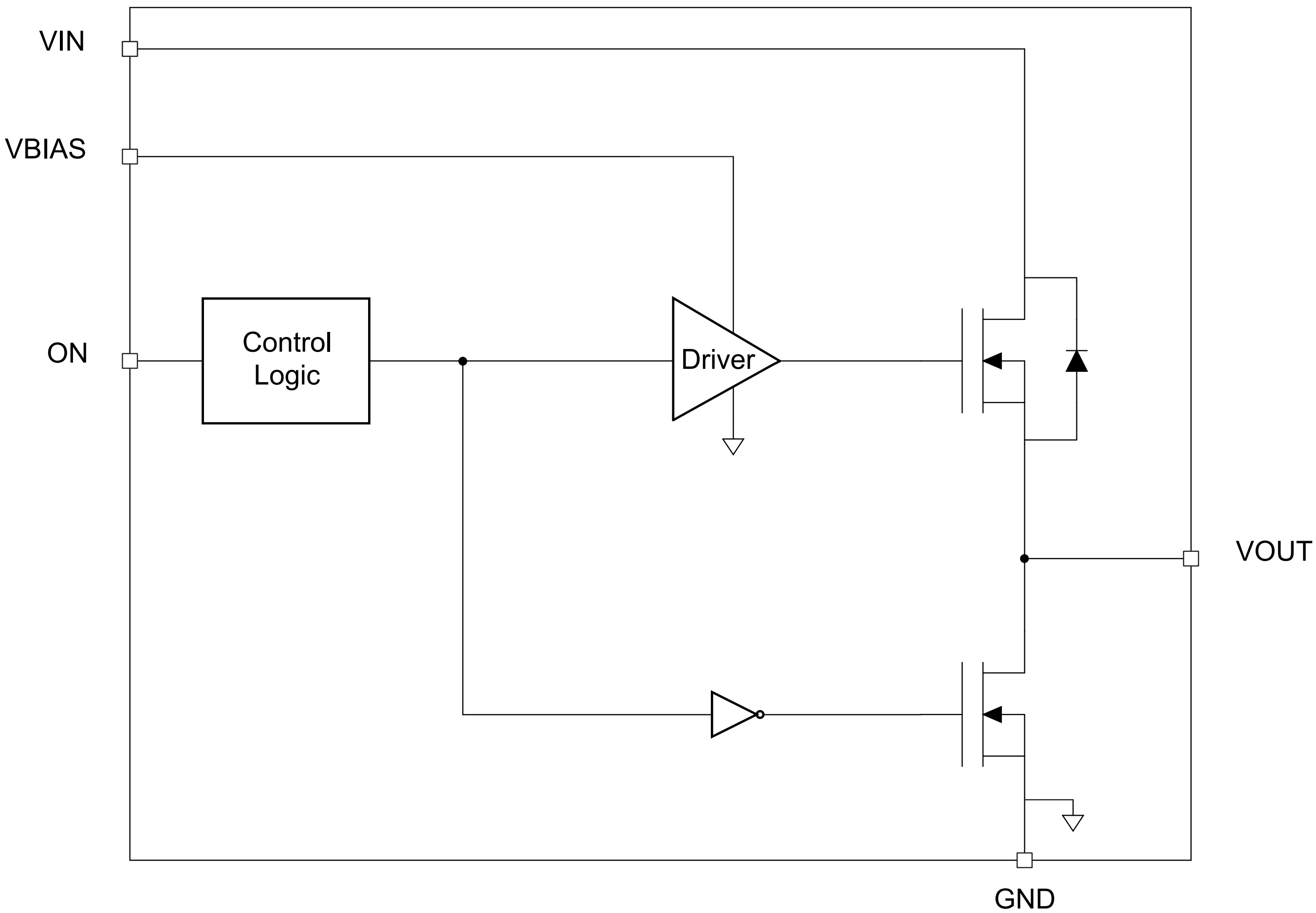
8 Detailed Description

8.1 Overview

The device is a 3.5 V, 6 A load switch in a 8-terminal SON package. To reduce voltage drop for low voltage and high current rails, the device implements an ultra-low resistance N-channel MOSFET which reduces the drop out voltage through the device at very high currents.

The device has a controlled, yet quick, fixed slew rate for applications that require quick turn-on response. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On/off Control

The ON terminal controls the state of the load switch, and asserting the terminal high (active high) enables the switch. The ON terminal is compatible with standard GPIO logic threshold and can be used with any microcontroller or discrete logic with 1.2 V or higher GPIO voltage. This terminal cannot be left floating and must be tied either high or low for proper functionality.

8.3.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1 µF ceramic capacitor, C_{IN}, placed close to the terminals, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop in high-current application. When switching heavy loads, it is recommended to have an input capacitor 10 times higher than the output capacitor to avoid excessive voltage drop.

8.3.3 Output Capacitor (C_L)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUTT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause a V_{IN} dip upon turn-on due to inrush currents.

8.3.4 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq (V_{BIAS} – 1.95\ V)$. For example, in order to have V_{IN} = 3.5V, VBIAS must be 5.5 V. The device will still be functional if $V_{IN} > (V_{BIAS} – 1.95\ V)$ but it will exhibit R_{ON} greater than what is listed in the *Electrical Characteristics, V_{BIAS} = 5.0 V* table. See Figure 25 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} increases. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.

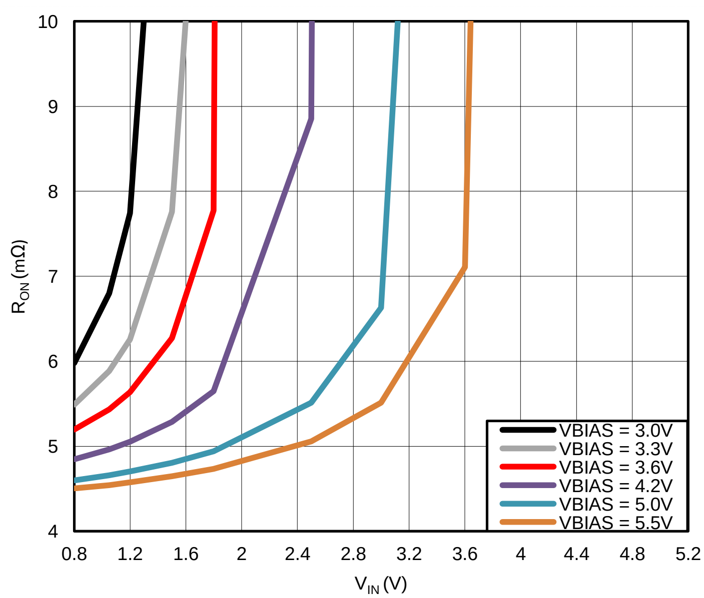


Figure 25. R_{ON} vs V_{IN} ($V_{IN} > V_{BIAS}$)

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com for further aid.

9.2 Typical Application

9.2.1 Typical Application Powering a Downstream Module

This application demonstrates how the TPS22961 can be used to power downstream modules.

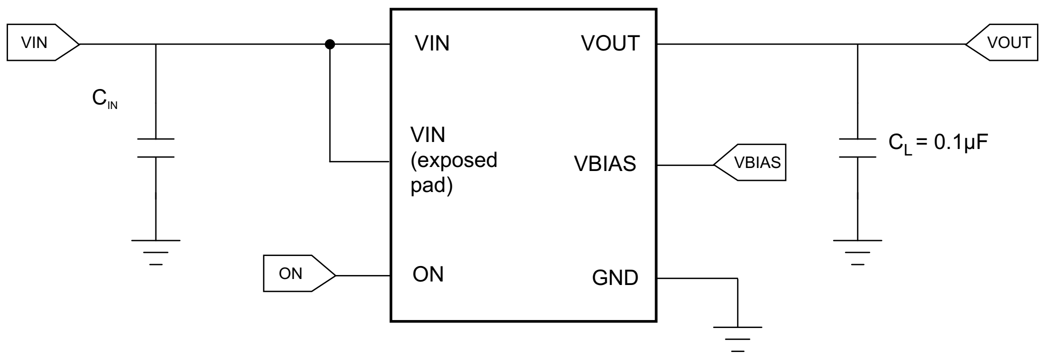


Figure 26. Typical Application Schematic for Powering a Downstream Module

9.2.1.1 Design Requirements

For this design example, use the following as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.05 V
V_{BIAS}	5.0 V
Load current	6 A

9.2.1.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- VIN voltage
- VBIAS voltage
- Load current

9.2.1.2.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use Equation 1 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \tag{1}$$

where

- ΔV = voltage drop from VIN to VOUT
- I_{LOAD} = load current
- R_{ON} = On-resistance of the device for a specific V_{IN} and V_{BIAS} combination

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

9.2.1.2.2 Inrush Current

To determine how much inrush current will be caused by the C_L capacitor, use Equation 2:

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \tag{2}$$

where

- I_{INRUSH} = amount of inrush caused by C_L
- C_L = capacitance on VOUT
- dt = time it takes for change in V_{OUT} during the ramp up of VOUT when the device is enabled
- dV_{OUT} = change in V_{OUT} during the ramp up of VOUT when the device is enabled

An appropriate C_L value should be placed on VOUT such that the I_{MAX} and I_{PLS} specficiations of the device are not violated.

9.2.1.2.3 Thermal Considerations

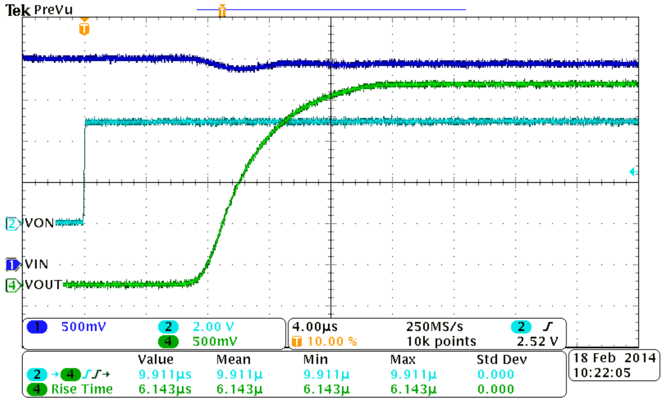
The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 3.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \tag{3}$$

where

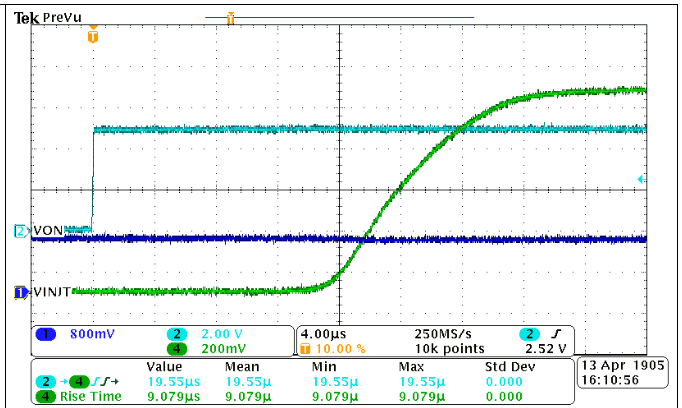
- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22961)
- T_A = ambient temperature of the device
- Θ_{JA} = junction to air thermal impedance. See *Thermal Information* section. This parameter is highly dependent upon board layout.

9.2.1.3 Application Curves



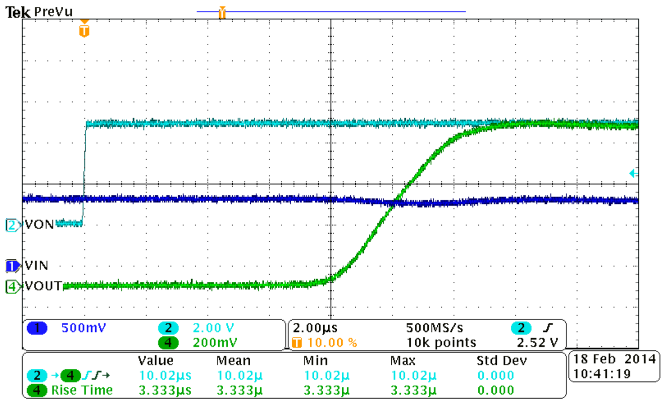
V_{BIAS} = 5 V V_{IN} = 2.5 V CIN = 1 µF C_L = 0.1 µF

Figure 27. t_R at V_{BIAS} = 5 V



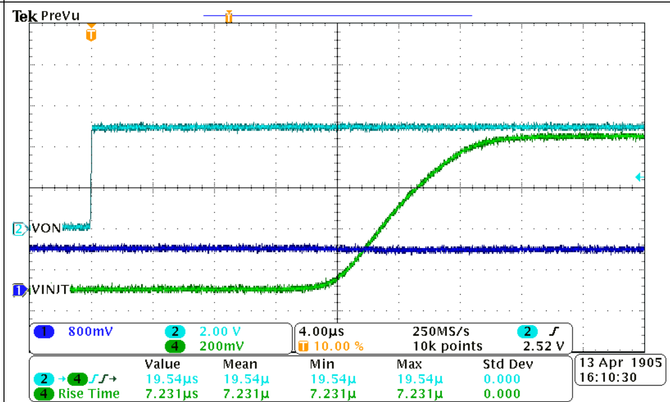
V_{BIAS} = 5 V V_{IN} = 0.8 V CIN = 1 µF C_L = 0.1 µF

Figure 28. t_R at V_{BIAS} = 5 V



V_{BIAS} = 5 V V_{IN} = 1.05 V CIN = 1 µF C_L = 0.1 µF

Figure 29. t_R at V_{BIAS} = 3 V



V_{BIAS} = 5 V V_{IN} = 0.8 V CIN = 1 µF C_L = 0.1 µF

Figure 30. t_R at V_{BIAS} = 3 V

9.2.2 Typical Application Powering Rails Sensitive to Ringing and Overvoltage due to Fast Rise Time

This application demonstrates how the TPS22961 can be used to power rails senstive to ringing and overvoltage that can often happen due to fast rise times.

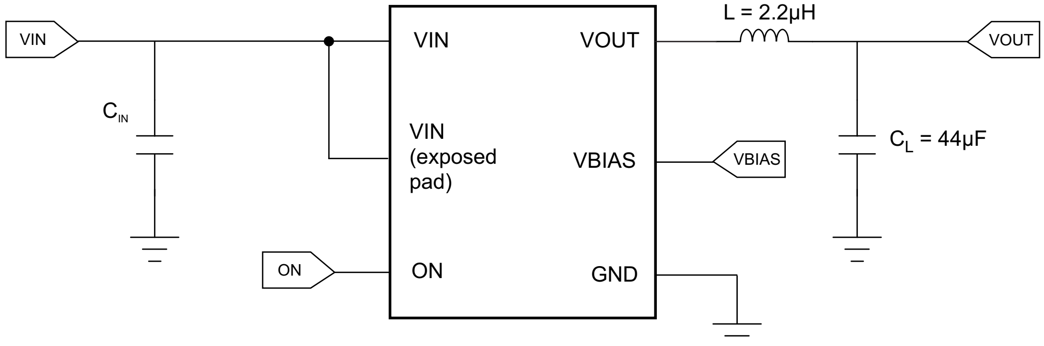


Figure 31. Typical Application Schematic for Powering Rails Sensitive to Ringing

9.2.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.05 V
V_{BIAS}	5.0 V
Acceptable percent overshoot (ρ)	3.2%
Maximum settling time (t_{SETTLE})	40 µs

9.2.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- VIN voltage
- VBIAS voltage
- Acceptable percent overshoot
- Maximum allowed settling time for the power rail

9.2.2.2.1 Picking Proper Inductor and Capacitor to Meet Voltage Overshoot Requirements

To determine the value of L and C_L in the circuit, the damping factor associated with the acceptable percent overshoot must be calculated. To calculate the damping factor (ε), use Equation 4.

$$\varepsilon = \frac{-\ln \rho}{\sqrt{\pi^2 + (\ln \rho)^2}} \tag{4}$$

where

- ε = damping factor of the LC filter
- ρ = allowable percent overshoot for the power rail

Use the damping factor calculated in Equation 4 to determine the inductance (L), the DCR of the inductor (R_{DCR}), and capacitance (C_L) to achieve the percent overshoot. This will be an iterative process to determine the optimal combination of L and C_L with standard value components available. Use Equation 5 to determine the combination of L, R_{DCR}, and C_L that is needed to satisfy damping factor calculated from Equation 4.

$$\varepsilon = \frac{R_{DCR}}{2} x \sqrt{\frac{C_L}{L}} \tag{5}$$

where
- ε = damping factor of the LC filter
- R_{DCR} = DCR of the inductor
- C_L = the capacitance of the filter
- L = the inductor of the filter

To determine the setting time (within 5% of steady state value) of the filter, use Equation 6.

$$t_{SETTLE} \approx \frac{3 \times \sqrt{L \times C_L}}{\varepsilon} \tag{6}$$

where
- t_{SETTLE} = settling time of filter to within 5% of steady state value
- ε = damping factor of the LC filter
- C_L = the capacitance of the filter
- L = the inductor of the filter

The combination of damping factor (ε) and filter settling time (t_{SETTLE}) will bound the values for L, R_{DCR}, and C_L that can be used to meet the design constraints in Table 2.

9.2.2.3 Application Curves

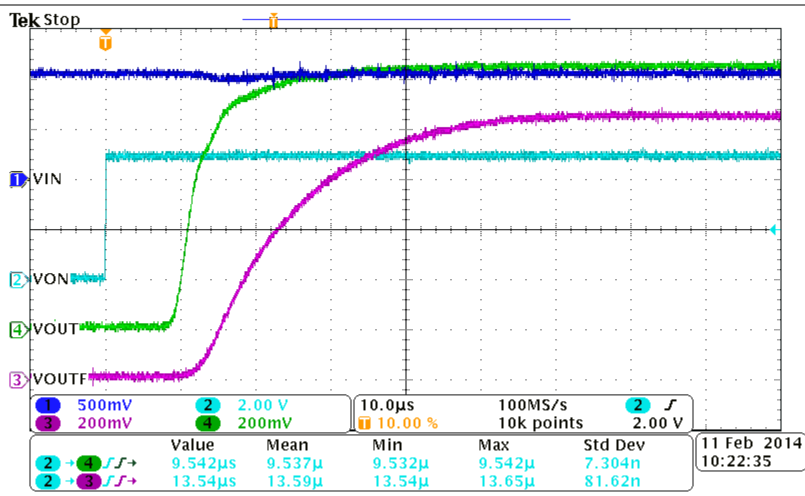


Figure 32. Filtered Output (CH1 = VIN, CH2 = ON, CH3 = Output of LC filter, CH4 = VOUT of TPS22961)

10 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 3 V to 5.5 V and VIN range of 0.8 V to 3.5 V. This supply must be well regulated and placed as close to the TPS22961 as possible. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

11 Layout

11.1 Layout Guidelines

- VIN and VOUT traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The VIN terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1-µF ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device terminals as possible.
- The VOUT terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor should be placed as close to the device terminals as possible.
- The VBIAS terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1-µF ceramic with X5R or X7R dielectric.

11.2 Layout Example

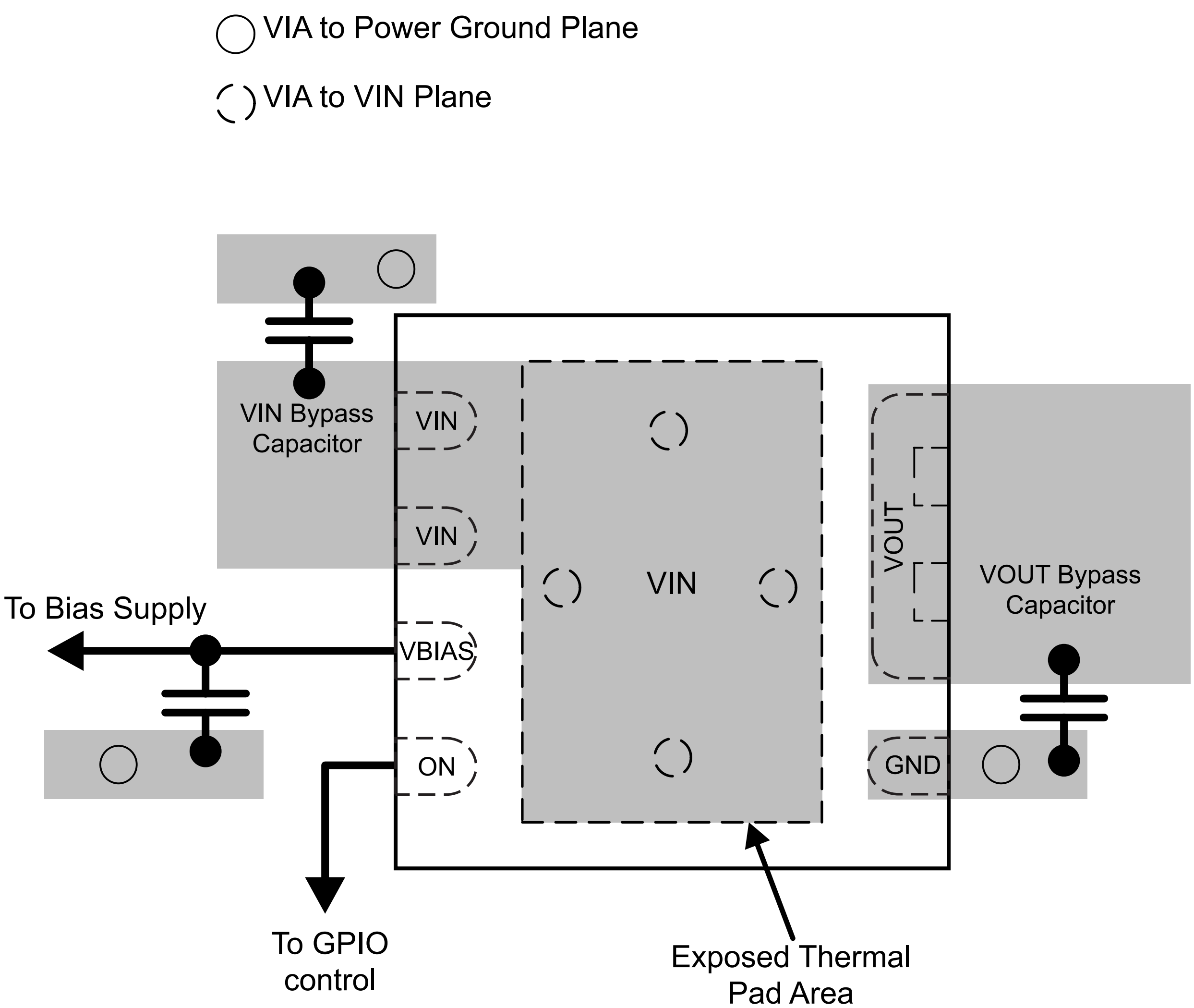


Figure 33. Recommended Board Layout

12 Device and Documentation Support

12.1 Trademarks

Ultrabook is a trademark of Intel.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22961DNYR	ACTIVE	WSON	DNY	8	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	961A1	Samples
TPS22961DNYT	ACTIVE	WSON	DNY	8	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	961A1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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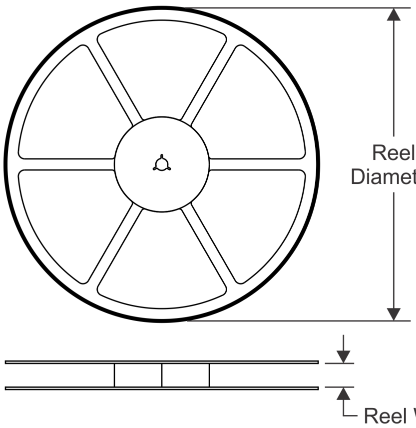
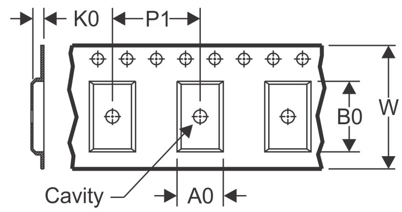
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

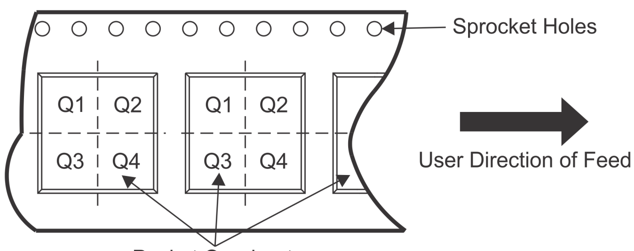


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

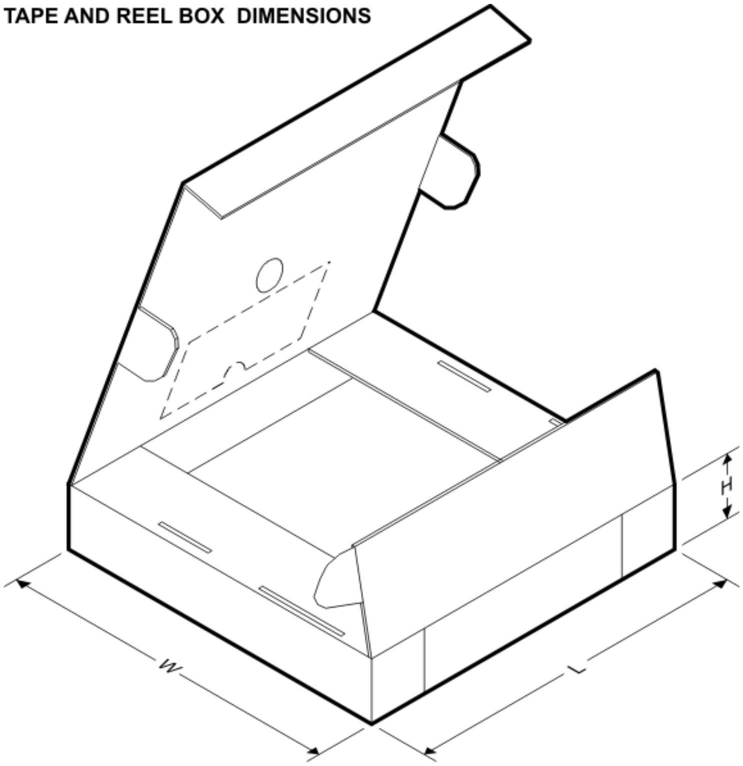
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

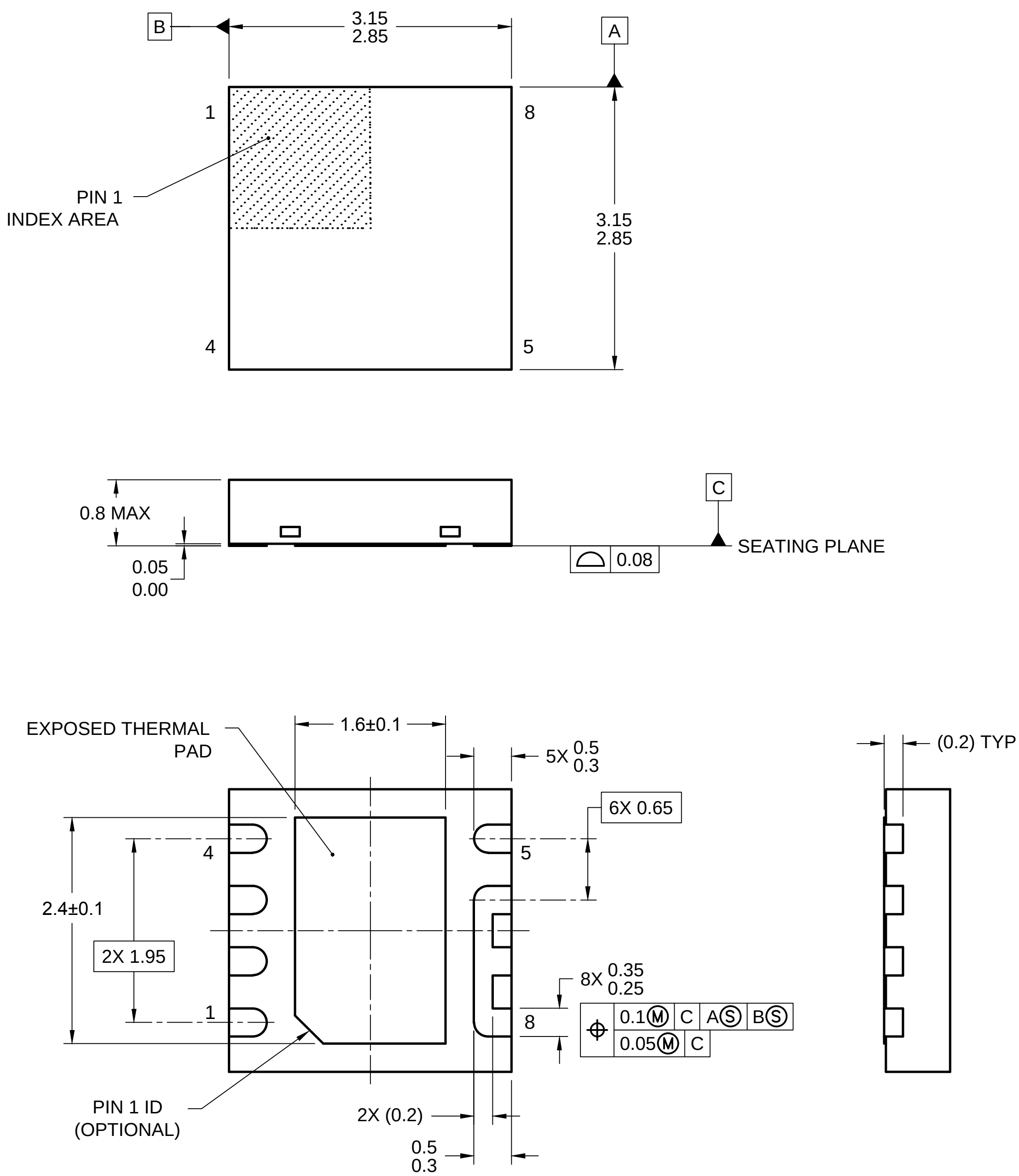
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22961DNYR	WSON	DNY	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS22961DNYT	WSON	DNY	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22961DNYR	WSON	DNY	8	3000	370.0	355.0	55.0
TPS22961DNYT	WSON	DNY	8	250	195.0	200.0	45.0



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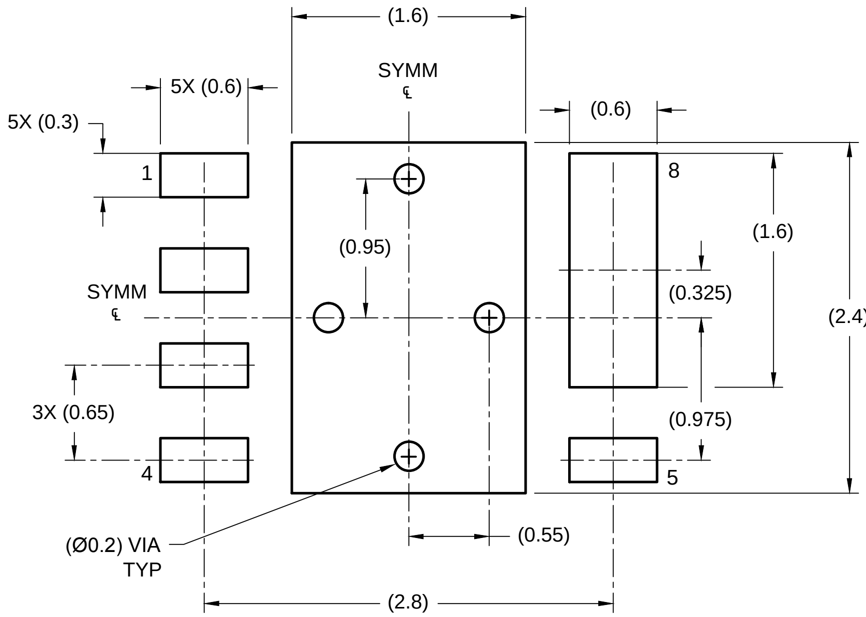
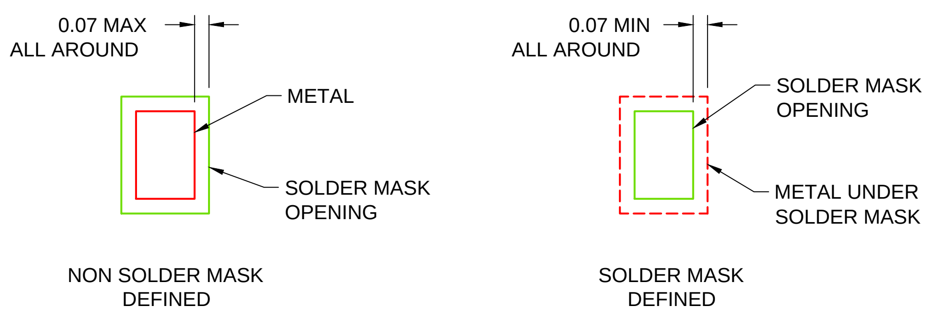
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

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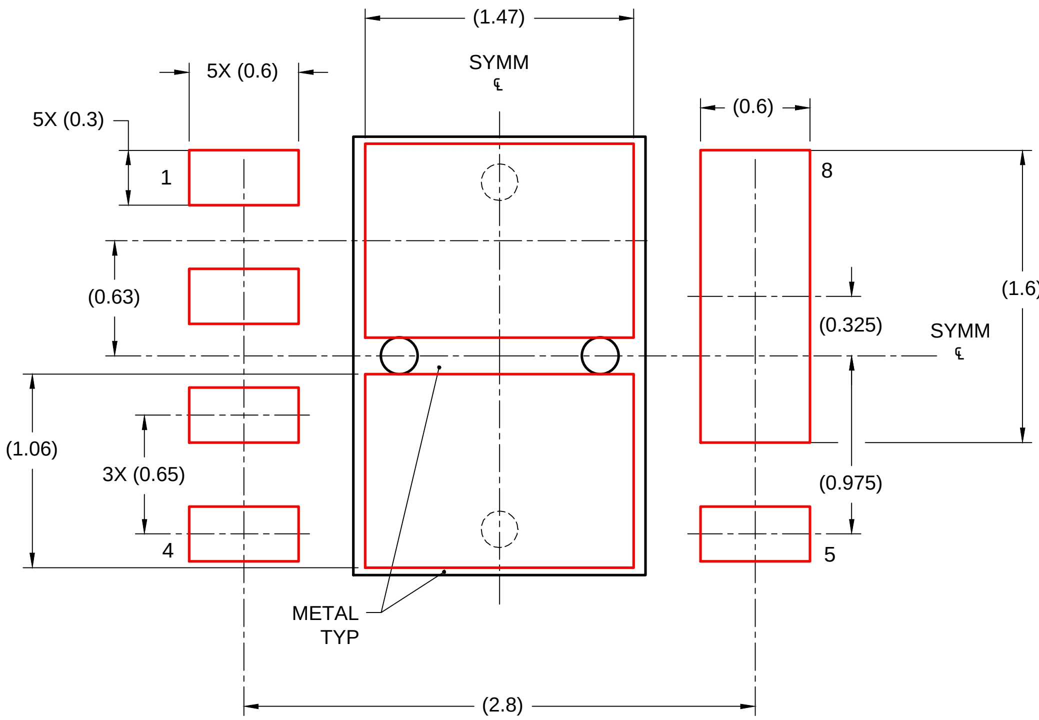
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE: 25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.