

Three-PLL General-Purpose EPROM-Programmable Clock Generator

Features

- Three integrated phase locked loops (PLLs)
- Erasable programmable read only memory (EPROM) programmability
- Factory programmable (CY2292) or field programmable (CY2292F) device options
- Low-skew, low-jitter, high accuracy outputs
- Power management options (shutdown, OE, suspend)
- Frequency select option
- Smooth slewing on CPUCLK
- Configurable 3.3 V or 5 V operation
- 16-pin small-outline integrated circuit (SOIC) package (CY2292F also in TSSOP)

Benefits

- Generates up to three custom frequencies from one external source
- Easy customization and fast turnaround
- Programming support available for all opportunities
- Supports low power applications
- Eight user selectable frequencies on CPUPLL
- Allows downstream PLLs to stay locked on CPUCLK output
- Industry standard packaging saves on board space

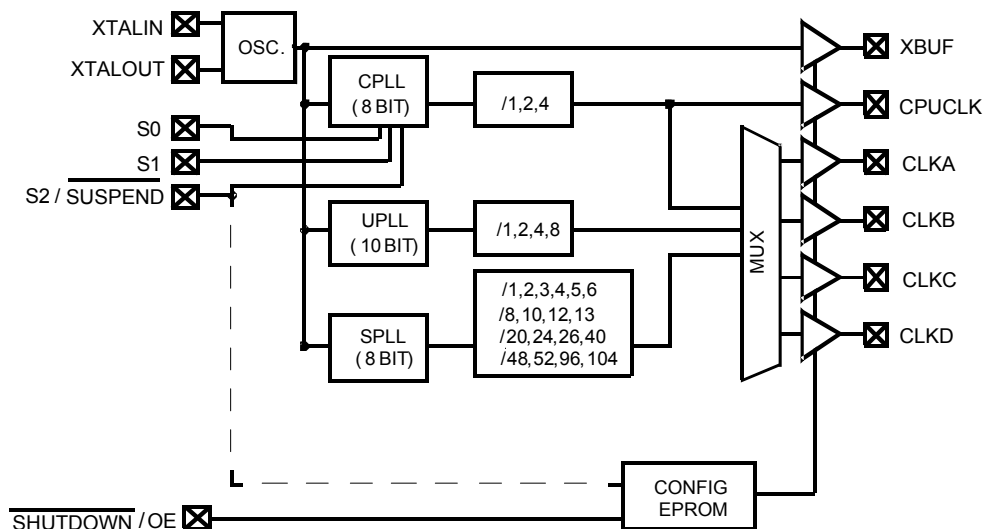
Functional Description

For a complete list of related documentation, click [here](#).

Selector Guide

| Part Number | Input Frequency Range | Output Frequency Range | Specifics |
|------------------------|--|--|--|
| CY2292SC, SL, SXC, SXL | 10 MHz to 25 MHz (external crystal) 1 MHz to 30 MHz (reference clock) | 76.923 kHz to 100 MHz (5 V) 76.923 kHz to 80 MHz (3.3 V) | Factory programmable Commercial temperature |
| CY2292SI, SXI | 10 MHz to 25 MHz (external crystal) 1 MHz to 30 MHz (reference clock) | 76.923 kHz to 90 MHz (5 V) 76.923 kHz to 66.6 MHz (3.3 V) | Factory programmable Industrial temperature |
| CY2292F, FXC, FZX | 10 MHz to 25 MHz (external crystal) 1 MHz to 30 MHz (reference clock) | 76.923 kHz to 90 MHz (5 V) 76.923 kHz to 66.6 MHz (3.3 V) | Field programmable Commercial temperature |
| CY2292FXI, FZXI | 10 MHz to 25 MHz (external crystal) 1 MHz to 30 MHz (reference clock) | 76.923 kHz to 80 MHz (5 V) 76.923 kHz to 60.0 MHz (3.3 V) | Field programmable Industrial temperature |

Logic Block Diagram

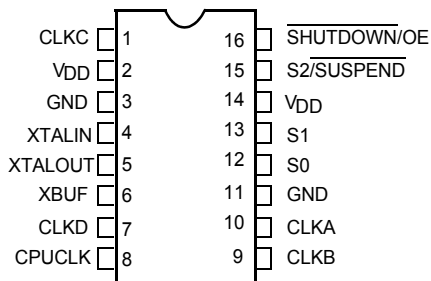


Contents

| | | | |
|---|-----------|--|-----------|
| Pinouts | 3 | Switching Characteristics | 12 |
| Pin Definitions | 3 | Switching Waveforms | 13 |
| Operation | 4 | Ordering Information | 14 |
| Output Configuration | 4 | Possible Configurations | 14 |
| Power Saving Features | 4 | Ordering Code Definitions | 14 |
| CyClocks Software | 4 | Package Characteristics | 15 |
| Cypress FTG Programmer | 4 | Package Diagrams | 15 |
| Custom Configuration Request Procedure | 4 | Acronyms | 16 |
| Maximum Ratings | 5 | Document Conventions | 16 |
| Operating Conditions | 5 | Units of Measure | 16 |
| Electrical Characteristics | 6 | Document History Page | 17 |
| Electrical Characteristics | 6 | Sales, Solutions, and Legal Information | 19 |
| Electrical Characteristics | 7 | Worldwide Sales and Design Support | 19 |
| Electrical Characteristics | 7 | Products | 19 |
| Test Circuit | 8 | PSoC® Solutions | 19 |
| Switching Characteristics | 9 | Cypress Developer Community | 19 |
| Switching Characteristics | 10 | Technical Support | 19 |
| Switching Characteristics | 11 | | |

Pinouts

Figure 1. 16-pin SOIC / TSSOP pinout



Pin Definitions

| Name | Pin Number | Description |
|---------------------------|------------|--|
| CLKC | 1 | Configurable clock output C. |
| V _{DD} | 2, 14 | Voltage supply. |
| GND | 3, 11 | Ground. |
| XTALIN ^[1] | 4 | Reference crystal input or external reference clock input. |
| XTALOUT ^[1, 2] | 5 | Reference crystal feedback. |
| XBUF | 6 | Buffered reference clock output. |
| CLKD | 7 | Configurable clock output D. |
| CPUCLK | 8 | CPU frequency clock output. |
| CLKB | 9 | Configurable clock output B. |
| CLKA | 10 | Configurable clock output A. |
| S0 | 12 | CPU clock select input, bit 0. |
| S1 | 13 | CPU clock select input, bit 1. |
| S2/SUSPEND | 15 | CPU clock select input, bit 2. Optionally enables suspend feature when LOW. |
| SHUTDOWN/OE | 16 | Places outputs in tristate ^[3] condition and shuts down chip when LOW. Optionally, only places outputs in tristate ^[3] condition and does not shut down chip when LOW. |

Notes

- For best accuracy, use a parallel-resonant crystal, C_{LOAD} ≈ 17 pF or 18 pF.
- Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).
- The CY2292 has weak pull downs on all outputs. Hence, when a tristate condition is forced on the outputs, the output pins are pulled low.

Operation

The CY2292 is a third-generation family of clock generators. The CY2292 is upwardly compatible with the industry standard ICD2023 and ICD2028 and continues their tradition by providing a high level of customizable features to meet the diverse clock generation needs of modern motherboards and other synchronous systems.

All parts provide a highly configurable set of clocks for PC motherboard applications. Each of the four configurable clock outputs (CLKA–CLKD) can be assigned 1 of 30 frequencies in any combination. Multiple outputs configured for the same or related frequencies have low (less than 500 ps) skew, in effect providing on-chip buffering for heavily loaded signals.

The CY2292 can be configured for either 5 V or 3.3 V operation. The internal ROM tables use EPROM technology, allowing full customization of output frequencies. The reference oscillator is designed for 10 MHz to 25 MHz crystals, providing additional flexibility. No external components are required with this crystal. Alternatively, an external reference clock of frequency between 1 MHz and 30 MHz can be used.

Output Configuration

The CY2292 has four independent frequency sources on-chip. These are the reference oscillator and three PLLs. Each PLL has a specific function. The system PLL (SPLL) provides fixed output frequencies on the configurable outputs. The SPLL offers the most output frequency divider options. The CPU PLL (CPLL) is controlled by the select inputs (S0–S2) to provide eight user-selectable frequencies with smooth slewing between frequencies. The utility PLL (UPLL) provides the most accurate clock. It is often used for miscellaneous frequencies not provided by the other frequency sources.

All configurations are EPROM programmable, providing short sample and production lead times.

Power Saving Features

The SHUTDOWN/OE input tristates the outputs when pulled LOW. If system shutdown is enabled, a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins is less than 50 μA (for commercial temperature or 100 μA for industrial temperature). After leaving shutdown mode, the PLLs have to relock. All outputs have a weak pull down so that the outputs do not float when tristated.^[4]

The S2/SUSPEND input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a tristate condition.

Note

4. The CY2292 has weak pull downs on all outputs. Hence, when a tristate condition is forced on the outputs, the output pins are pulled low.

The CPUCLK can slew (transition) smoothly between 20 MHz and the maximum output frequency (100 MHz at 5 V / 80 MHz at 3.3 V for commercial temperature parts or 90 MHz at 5 V / 66.6 MHz at 3.3 V for industrial temperature and for field-programmed parts). This feature is extremely useful in green applications, where reducing the frequency of operation can result in considerable power savings.

CyClocks Software

CyClocks™ is an easy-to-use application that allows you to configure any one of the EPROM-programmable clocks offered by Cypress. Specify the input frequency, PLL and output frequencies, and different functional options. Note the output frequency ranges in this datasheet when specifying them in CyClocks to ensure that you stay within the limits. CyClocks also has a power calculation feature that allows you to see the power consumption of your specific configuration. CyClocks is a sub application located within the CyberClocks™ software. You can download a copy of CyberClocks for free on the Cypress web site at <http://www.cypress.com>.

Cypress FTG Programmer

The Cypress frequency timing generator (FTG) programmer is a portable programmer designed to custom program our family of EPROM field programmable clock devices. The FTG programmer connects to a PC serial port and allow users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F and CY2907F devices. The ordering code for the Cypress FTG Programmer is CY3670. An adapter, the CY3095, connects to the CY3670 and is required for programming the CY2292F.

Custom Configuration Request Procedure

The CY229x are EPROM-programmable devices that may be configured in the factory or in the field by a Cypress field application engineer (FAE). The output frequencies requested is matched as closely as the internal PLL divider and multiplier options allow. All custom requests must be submitted to your local Cypress FAE or sales representative. The method to use to request custom configurations is:

Use CyClocks software. This software automatically calculates the output frequencies that can be generated by the CY229x devices and provides a print-out of final pinout which can be submitted (in electronic or print format) to your local FAE or sales representative.

When the custom request is processed, you receive a part number with a 3-digit extension (for example, CY2292SC-128) specific to the frequencies and pinout of your device. This is the part number used for samples requests and production orders.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply voltage -0.5 V to +7.0 V
 DC input voltage -0.5 V to +7.0 V

Storage temperature -65 °C to +150 °C
 Maximum soldering temperature (10 sec) 260 °C
 Junction temperature 150 °C
 Package power dissipation 750 mW
 Static discharge voltage
 (per MIL-STD-883, method 3015) ≤ 2000 V

Operating Conditions

| Parameter ^[5] | Description | Part Numbers | Min | Max | Unit |
|--------------------------|---|--------------------|------|------|------|
| V _{DD} | Supply voltage, 5.0 V operation | All | 4.5 | 5.5 | V |
| V _{DD} | Supply voltage, 3.3 V operation | All | 3.0 | 3.6 | V |
| T _A | Commercial operating temperature, ambient | CY2292 / CY2292F | 0 | 70 | °C |
| | Industrial operating temperature, ambient | CY2292I / CY2292FI | -40 | 85 | °C |
| C _{LOAD} | Maximum load capacitance 5.0 V operation | All | – | 25 | pF |
| C _{LOAD} | Maximum load capacitance 3.3 V operation | All | – | 15 | pF |
| f _{REF} | External reference crystal | All | 10.0 | 25.0 | MHz |
| | External reference clock ^[6, 7, 8] | All | 1 | 30 | MHz |

Notes

5. Electrical parameters are guaranteed by design with these operating conditions, unless otherwise noted.
6. External input reference clock must have a duty cycle between 40% and 60%, measured at V_{DD} / 2.
7. Refer to white paper "Crystal Oscillator Topics" for information on AC-coupling the external input reference clock.
8. The oscillator circuit is optimized for a crystal reference and for external reference clocks up to 20 MHz. For external reference clocks above 20 MHz, it is recommended that a 150 Ω pull up resistor to V_{DD} be connected to the Xout pin.

Electrical Characteristics

Commercial, 5.0 V

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|--|--|-----|-----|-----|------|
| V _{OH} | High level output voltage | I _{OH} = 4.0 mA | 2.4 | – | – | V |
| V _{OL} | Low level output voltage | I _{OL} = 4.0 mA | – | – | 0.4 | V |
| V _{IH} | High level input voltage ^[9] | Except crystal pins | 2.0 | – | – | V |
| V _{IL} | Low level input voltage ^[9] | Except crystal pins | – | – | 0.8 | V |
| I _{IH} | Input high current | V _{IN} = V _{DD} – 0.5 V | – | < 1 | 10 | μA |
| I _{IL} | Input low current | V _{IN} = +0.5 V | – | < 1 | 10 | μA |
| I _{OZ} | Output leakage current | Tristate outputs | – | – | 250 | μA |
| I _{DD} | V _{DD} supply current ^[10] commercial | V _{DD} = V _{DD} max, 5 V operation | – | 75 | 100 | mA |
| I _{DDS} | V _{DD} power supply current in shutdown mode ^[10] | Shutdown active | – | 10 | 50 | μA |

Electrical Characteristics

Commercial, 3.3 V

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|--|--|-----|-----|-----|------|
| V _{OH} | High level output voltage | I _{OH} = 4.0 mA | 2.4 | – | – | V |
| V _{OL} | Low level output voltage | I _{OL} = 4.0 mA | – | – | 0.4 | V |
| V _{IH} | High level input voltage ^[9] | Except crystal pins | 2.0 | – | – | V |
| V _{IL} | Low level input voltage ^[9] | Except crystal pins | – | – | 0.8 | V |
| I _{IH} | Input high current | V _{IN} = V _{DD} – 0.5 V | – | < 1 | 10 | μA |
| I _{IL} | Input low current | V _{IN} = +0.5 V | – | < 1 | 10 | μA |
| I _{OZ} | Output leakage current | Tristate outputs | – | – | 250 | μA |
| I _{DD} | V _{DD} supply current ^[10] commercial | V _{DD} = V _{DD} max, 3.3 V operation | – | 50 | 65 | mA |
| I _{DDS} | V _{DD} power supply current in shutdown mode ^[10] | Shutdown active | – | 10 | 50 | μA |

Notes

9. Xtal inputs have CMOS thresholds.

 10. Load = Max, V_{IN} = 0 V or V_{DD}. Typical (–104) configuration, CPUCLK = 66 MHz. Other configurations vary. Power can be approximated by the following formula (multiply by 0.65 for 3 V operation): I_{DD} = 10 + 0.06•(F_{CPLL} + F_{UPLL} + 2•F_{SPLL}) + 0.27•(F_{CLKA} + F_{CLKB} + F_{CLKC} + F_{CLKD} + F_{CPUCLK} + F_{XBUF}).

Electrical Characteristics

Industrial, 5.0 V

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|---|--|-----|-----|-----|------|
| V _{OH} | High level output voltage | I _{OH} = 4.0 mA | 2.4 | – | – | V |
| V _{OL} | Low level output voltage | I _{OL} = 4.0 mA | – | – | 0.4 | V |
| V _{IH} | High level input voltage ^[11] | Except crystal pins | 2.0 | – | – | V |
| V _{IL} | Low level input voltage ^[11] | Except crystal pins | – | – | 0.8 | V |
| I _{IH} | Input high current | V _{IN} = V _{DD} – 0.5 V | – | < 1 | 10 | μA |
| I _{IL} | Input low current | V _{IN} = +0.5 V | – | < 1 | 10 | μA |
| I _{OZ} | Output leakage current | Tristate outputs | – | – | 250 | μA |
| I _{DD} | V _{DD} supply current ^[12] industrial | V _{DD} = V _{DD} max, 5 V operation | – | 75 | 110 | mA |
| I _{DDS} | V _{DD} power supply current in shutdown mode ^[12] | Shutdown active | – | 10 | 100 | μA |

Electrical Characteristics

Industrial, 3.3 V

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|---|--|-----|-----|-----|------|
| V _{OH} | High level output voltage | I _{OH} = 4.0 mA | 2.4 | – | – | V |
| V _{OL} | Low level output voltage | I _{OL} = 4.0 mA | – | – | 0.4 | V |
| V _{IH} | High level input voltage ^[11] | Except crystal pins | 2.0 | – | – | V |
| V _{IL} | Low level input voltage ^[11] | Except crystal pins | – | – | 0.8 | V |
| I _{IH} | Input high current | V _{IN} = V _{DD} – 0.5 V | – | < 1 | 10 | μA |
| I _{IL} | Input low current | V _{IN} = +0.5 V | – | < 1 | 10 | μA |
| I _{OZ} | Output leakage current | Tristate outputs | – | – | 250 | μA |
| I _{DD} | V _{DD} supply current ^[12] industrial | V _{DD} = V _{DD} max, 3.3 V operation | – | 50 | 70 | mA |
| I _{DDS} | V _{DD} power supply current in shutdown mode ^[12] | Shutdown active | – | 10 | 100 | μA |

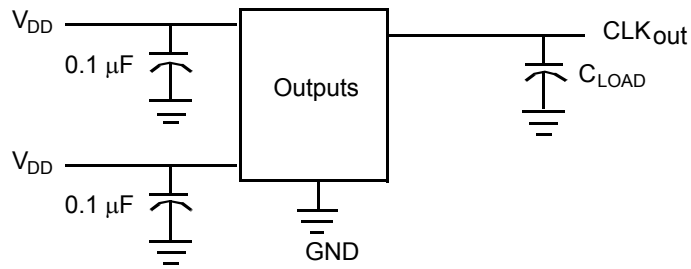
Notes

11. Xtal inputs have CMOS thresholds.

 12. Load = Max, V_{IN} = 0 V or V_{DD}, Typical (–104) configuration, CPUCLK = 66 MHz. Other configurations vary. Power can be approximated by the following formula (multiply by 0.65 for 3 V operation): I_{DD} = 10 + 0.06*(F_{CPLL} + F_{UPLL} + 2*F_{SPLL}) + 0.27*(F_{CLKA} + F_{CLKB} + F_{CLKC} + F_{CLKD} + F_{CPCLK} + F_{XBUF}).

Test Circuit

Figure 2. Test Circuit



Switching Characteristics

Commercial, 5.0 V

| Parameter | Name | Description | Min | Typ | Max | Unit |
|------------------|-----------------------------------|---|------------------|--------|-----------------------|------------|
| t ₁ | Output period | Clock output range, 5 V operation | 10 (100 MHz) | – | 13000 (76.923 kHz) | ns |
| | | | CY2292SC, SXC | – | – | – |
| | | | 11.1 (90 MHz) | – | 13000 (76.923 kHz) | ns |
| | Output duty cycle ^[13] | Duty cycle for outputs, defined as $t_2 \div t_1$ ^[14] f _{OUT} ≥ 66 MHz | 40 | 50 | 60 | % |
| | | Duty cycle for outputs, defined as $t_2 \div t_1$ ^[14] f _{OUT} < 66 MHz | 45 | 50 | 55 | % |
| t ₃ | Rise time | Output clock rise time ^[15] | – | 3 | 5 | ns |
| t ₄ | Fall time | Output clock fall time ^[15] | – | 2.5 | 4 | ns |
| t ₅ | Output disable time | Time for output to enter tristate mode after SHUTDOWN/OE goes LOW | – | 10 | 15 | ns |
| t ₆ | Output enable time | Time for output to leave tristate mode after SHUTDOWN/OE goes HIGH | – | 10 | 15 | ns |
| t ₇ | Skew | Skew delay between any identical or related outputs ^[14, 16] | – | < 0.25 | 0.5 | ns |
| t ₈ | CPUCLK slew | Frequency transition rate | 1.0 | – | 20.0 | MHz/ ms |
| t _{9A} | Clock jitter ^[16] | Peak-to-peak period jitter (t _{9A} max – t _{9A} min), percentage of clock period (f _{OUT} ≤ 4 MHz) | – | < 0.5 | 1 | % |
| t _{9B} | Clock jitter ^[16] | Peak-to-peak period jitter (t _{9B} max – t _{9B} min) (4 MHz ≤ f _{OUT} ≤ 16 MHz) | – | < 0.7 | 1 | ns |
| t _{9C} | Clock jitter ^[16] | Peak-to-peak period jitter (16 MHz < f _{OUT} ≤ 50 MHz) | – | < 400 | 500 | ps |
| t _{9D} | Clock jitter ^[16] | Peak-to-peak period jitter (f _{OUT} > 50 MHz) | – | < 250 | 350 | ps |
| t _{10A} | Lock time for CPLL | Lock time from power-up | – | < 25 | 50 | ms |
| t _{10B} | Lock time for UPLL and SPLL | Lock time from power-up | – | < 0.25 | 1 | ms |
| | Slew limits | CPU PLL slew limits | 20 | – | 100 | MHz |
| | | | CY2292SC, SXC | – | – | – |
| | | | 20 | – | 90 | MHz |
| | | | | – | – | – |

Notes

13. XBUF duty cycle depends on XTALIN duty cycle.

14. Measured at 1.4 V.

15. Measured between 0.4 V and 2.4 V.

16. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit.

Switching Characteristics

Commercial, 3.3 V

| Parameter | Name | Description | Min | Typ | Max | Unit | |
|------------------|-----------------------------------|---|-------------------|------------------|------|-----------------------|-----|
| t ₁ | Output period | Clock output range, 3.3 V operation | CY2292SL, SXL | 12.5 (80 MHz) | – | 13000 (76.923 kHz) | ns |
| | | | CY2292F, FXC, FZX | 15 (66.6 MHz) | – | 13000 (76.923 kHz) | ns |
| | Output duty cycle ^[17] | Duty cycle for outputs, defined as $t_2 \div t_1$ ^[18] f _{OUT} ≥ 66 MHz | 40 | 50 | 60 | % | |
| | | Duty cycle for outputs, defined as $t_2 \div t_1$ ^[18] f _{OUT} < 66 MHz | 45 | 50 | 55 | % | |
| t ₃ | Rise time | Output clock rise time ^[19] | – | 3 | 5 | ns | |
| t ₄ | Fall time | Output clock fall time ^[19] | – | 2.5 | 4 | ns | |
| t ₅ | Output disable time | Time for output to enter tristate mode after SHUTDOWN/OE goes LOW | – | 10 | 15 | ns | |
| t ₆ | Output enable time | Time for output to leave tristate mode after SHUTDOWN/OE goes HIGH | – | 10 | 15 | ns | |
| t ₇ | Skew | Skew delay between any identical or related outputs ^[18, 20] | – | < 0.25 | 0.5 | ns | |
| t ₈ | CPUCLK slew | Frequency transition rate | 1.0 | – | 20.0 | MHz/ ms | |
| t _{9A} | Clock jitter ^[20] | Peak-to-peak period jitter (t _{9A} max – t _{9A} min), percentage of clock period (f _{OUT} ≤ 4 MHz) | – | < 0.5 | 1 | % | |
| t _{9B} | Clock jitter ^[20] | Peak-to-peak period jitter (t _{9B} max – t _{9B} min) (4 MHz ≤ f _{OUT} ≤ 16 MHz) | – | < 0.7 | 1 | ns | |
| t _{9C} | Clock jitter ^[20] | Peak-to-peak period jitter (16 MHz < f _{OUT} ≤ 50 MHz) | – | < 400 | 500 | ps | |
| t _{9D} | Clock jitter ^[20] | Peak-to-peak period jitter (f _{OUT} > 50 MHz) | – | < 250 | 350 | ps | |
| t _{10A} | Lock time for CPLL | Lock time from power-up | – | < 25 | 50 | ms | |
| t _{10B} | Lock time for UPLL and SPLL | Lock time from power-up | – | < 0.25 | 1 | ms | |
| | Slew limits | CPU PLL slew limits | CY2292SL, SXL | 20 | – | 80 | MHz |
| | | | CY2292F, FXC, FZX | 20 | – | 66.6 | MHz |

Notes

17. XBUF duty cycle depends on XTALIN duty cycle.

18. Measured at 1.4 V.

19. Measured between 0.4 V and 2.4 V.

20. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit.

Switching Characteristics

Industrial, 5.0 V

| Parameter | Name | Description | Min | Typ | Max | Unit | |
|------------------|-----------------------------------|---|------------------|------------------|-----------------------|-----------------------|-----|
| t ₁ | Output period | Clock output range, 5 V operation | 11.1 (90 MHz) | – | 13000 (76.923 kHz) | ns | |
| | | | CY2292FXI, FZXI | 12.5 (80 MHz) | – | 13000 (76.923 kHz) | ns |
| | Output duty cycle ^[21] | Duty cycle for outputs, defined as $t_2 \div t_1$ ^[22] f _{OUT} ≥ 66 MHz | 40 | 50 | 60 | % | |
| | | Duty cycle for outputs, defined as $t_2 \div t_1$ ^[22] f _{OUT} < 66 MHz | 45 | 50 | 55 | % | |
| t ₃ | Rise time | Output clock rise time ^[23] | – | 3 | 5 | ns | |
| t ₄ | Fall time | Output clock fall time ^[23] | – | 2.5 | 4 | ns | |
| t ₅ | Output disable time | Time for output to enter tristate mode after SHUTDOWN/OE goes LOW | – | 10 | 15 | ns | |
| t ₆ | Output enable time | Time for output to leave tristate mode after SHUTDOWN/OE goes HIGH | – | 10 | 15 | ns | |
| t ₇ | Skew | Skew delay between any identical or related outputs ^[22, 24] | – | < 0.25 | 0.5 | ns | |
| t ₈ | CPUCLK slew | Frequency transition rate | 1.0 | – | 20.0 | MHz/ ms | |
| t _{9A} | Clock jitter ^[24] | Peak-to-peak period jitter (t _{9A} max – t _{9A} min), percentage of clock period (f _{OUT} ≤ 4 MHz) | – | < 0.5 | 1 | % | |
| t _{9B} | Clock jitter ^[24] | Peak-to-peak period jitter (t _{9B} max – t _{9B} min) (4 MHz ≤ f _{OUT} ≤ 16 MHz) | – | < 0.7 | 1 | ns | |
| t _{9C} | Clock jitter ^[28] | Peak-to-peak period jitter (16 MHz < f _{OUT} ≤ 50 MHz) | – | < 400 | 500 | ps | |
| t _{9D} | Clock jitter ^[28] | Peak-to-peak period jitter (f _{OUT} > 50 MHz) | – | < 250 | 350 | ps | |
| t _{10A} | Lock time for CPLL | Lock time from power-up | – | < 25 | 50 | ms | |
| t _{10B} | Lock time for UPLL and SPLL | Lock time from power-up | – | < 0.25 | 1 | ms | |
| | Slew limits | CPU PLL slew limits | CY2292SI, SXI | 20 | – | 90 | MHz |
| | | | CY2292FXI, FZXI | 20 | – | 80 | MHz |

Notes

21. XBUF duty cycle depends on XTALIN duty cycle.

22. Measured at 1.4 V.

23. Measured between 0.4 V and 2.4 V.

24. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit.

Switching Characteristics

Industrial, 3.3 V

| Parameter | Name | Description | Min | Typ | Max | Unit | |
|------------------|-----------------------------------|---|-----------------|-------------------|------|-----------------------|-----|
| t ₁ | Output period | Clock output range, 3.3 V operation | CY2292SI, SXI | 15 (66.6 MHz) | – | 13000 (76.923 kHz) | ns |
| | | | CY2292FXI, FZXI | 16.66 (60 MHz) | – | 13000 (76.923 kHz) | ns |
| | Output duty cycle ^[25] | Duty cycle for outputs, defined as $t_2 \div t_1$ ^[26] f _{OUT} ≥ 66 MHz | 40 | 50 | 60 | % | |
| | | Duty cycle for outputs, defined as $t_2 \div t_1$ ^[26] f _{OUT} < 66 MHz | 45 | 50 | 55 | % | |
| t ₃ | Rise time | Output clock rise time ^[27] | – | 3 | 5 | ns | |
| t ₄ | Fall time | Output clock fall time ^[27] | – | 2.5 | 4 | ns | |
| t ₅ | Output disable time | Time for output to enter tristate mode after SHUTDOWN/OE goes LOW | – | 10 | 15 | ns | |
| t ₆ | Output enable time | Time for output to leave tristate mode after SHUTDOWN/OE goes HIGH | – | 10 | 15 | ns | |
| t ₇ | Skew | Skew delay between any identical or related outputs ^[26, 28] | – | < 0.25 | 0.5 | ns | |
| t ₈ | CPUCLK slew | Frequency transition rate | 1.0 | – | 20.0 | MHz/ ms | |
| t _{9A} | Clock jitter ^[28] | Peak-to-peak period jitter (t _{9A} max – t _{9A} min), percentage of clock period (f _{OUT} ≤ 4 MHz) | – | < 0.5 | 1 | % | |
| t _{9B} | Clock jitter ^[28] | Peak-to-peak period jitter (t _{9B} max – t _{9B} min) (4 MHz ≤ f _{OUT} ≤ 16 MHz) | – | < 0.7 | 1 | ns | |
| t _{9C} | Clock jitter ^[28] | Peak-to-peak period jitter (16 MHz < f _{OUT} ≤ 50 MHz) | – | < 400 | 500 | ps | |
| t _{9D} | Clock jitter ^[28] | Peak-to-peak period jitter (f _{OUT} > 50 MHz) | – | < 250 | 350 | ps | |
| t _{10A} | Lock time for CPLL | Lock time from power-up | – | < 25 | 50 | ms | |
| t _{10B} | Lock time for UPLL and SPLL | Lock time from power-up | – | < 0.25 | 1 | ms | |
| | Slew limits | CPU PLL slew limits | CY2292SI, SXI | 20 | – | 66.6 | MHz |
| | | | CY2292FXI, FZXI | 20 | – | 60 | MHz |

Notes

25. XBUF duty cycle depends on XTALIN duty cycle.

26. Measured at 1.4 V.

27. Measured between 0.4 V and 2.4 V.

28. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit.

Switching Waveforms

Figure 3. All Outputs, Duty Cycle and Rise / Fall Time

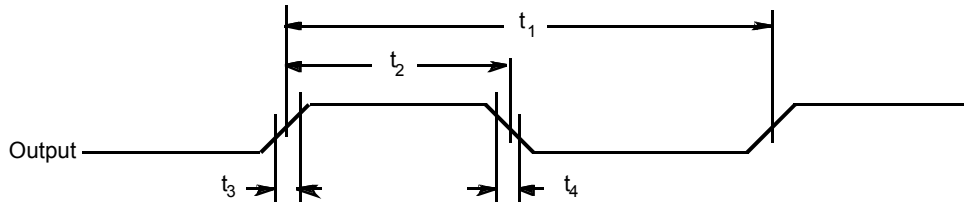


Figure 4. Output Tristate Timing [29]

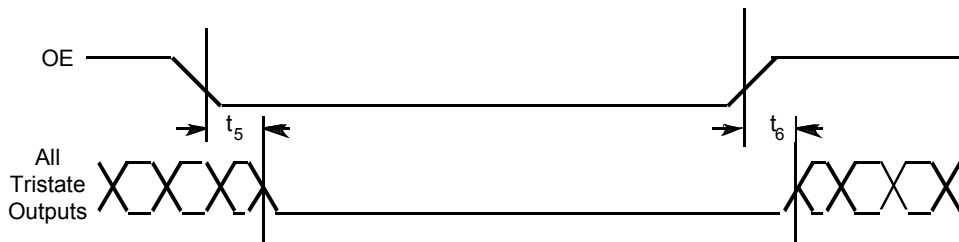


Figure 5. CLK Outputs Jitter and Skew

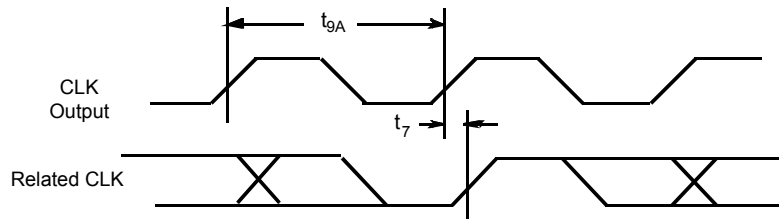
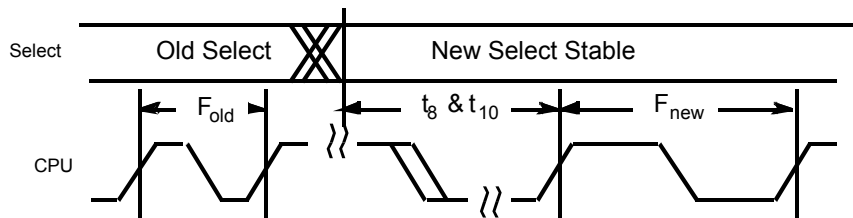


Figure 6. CPU Frequency Change



Note

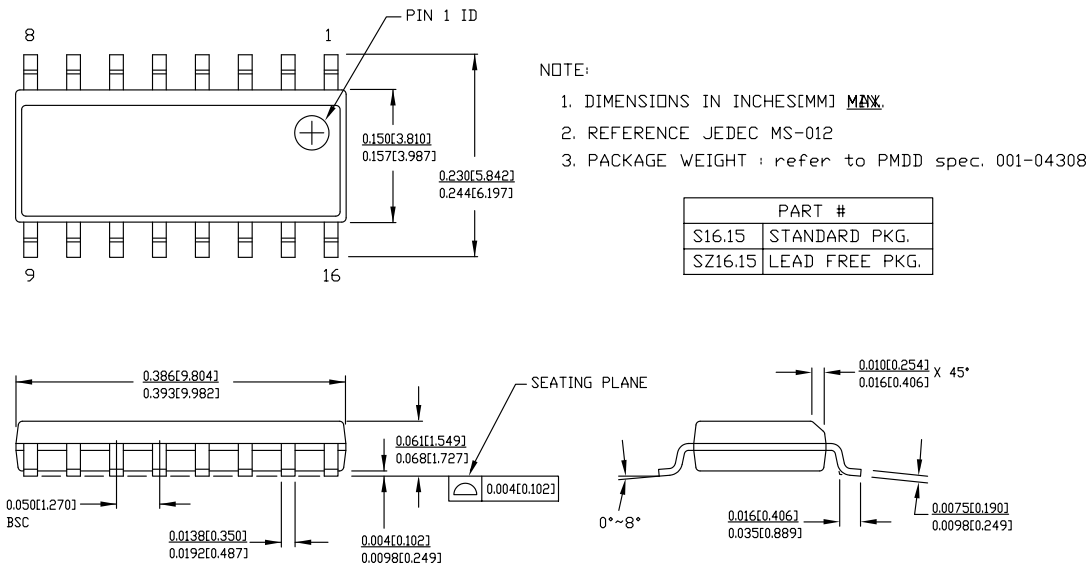
29. The CY2292 has weak pull downs on all outputs. Hence, when a tristate condition is forced on the outputs, the output pins are pulled low.

Package Characteristics

| Package | θ_{JA} (°C/W) | θ_{JC} (°C/W) | Transistor Count |
|--------------|----------------------|----------------------|------------------|
| 16-pin SOIC | 83 | 19 | 9271 |
| 16-pin TSSOP | 103 | 32 | |

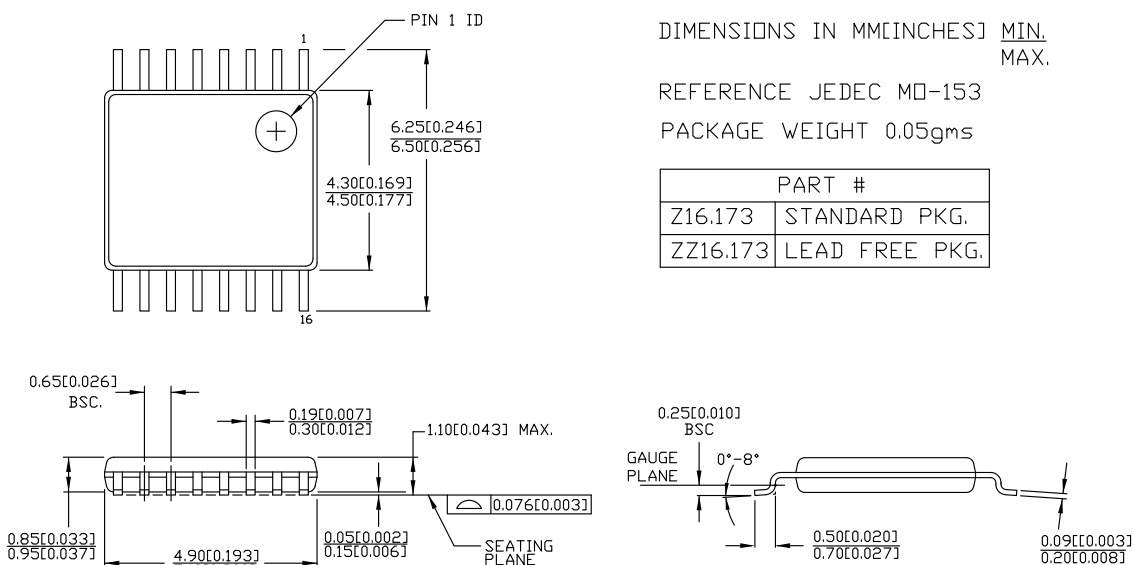
Package Diagrams

Figure 7. 16-pin SOIC (150 Mils) S16.15/SZ16.15 Package Outline, 51-85068



51-85068 *E

Figure 8. 16-pin TSSOP 4.40 mm Body Z16.173/ZZ16.173 Package Outline, 51-85091



51-85091 *E

Acronyms

| Acronym | Description |
|---------|---|
| CPU | Central Processing Unit |
| CMOS | Complementary Metal Oxide Semiconductor |
| DC | Direct Current |
| EPROM | Erasable Programmable Read Only Memory |
| FAE | Field Application Engineer |
| FTG | Frequency Timing Group |
| OE | Output Enable |
| OSC | Oscillator |
| PD | Power Down |
| PLL | Phase Locked Loop |
| ROM | Read Only Memory |
| SOIC | Small Outline Integrated Circuit |
| TSSOP | Thin Shrunk Small Outline Package |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-------------------|
| °C | degree Celsius |
| kΩ | kilohm |
| MHz | megahertz |
| μA | microampere |
| mA | milliampere |
| ms | millisecond |
| mW | milliwatt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| V | volt |

Document History Page

| Document Title: CY2292, Three-PLL General-Purpose EPROM-Programmable Clock Generator | | | | |
|--|---------|-----------------|-----------------|---|
| Document Number: 38-07449 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 116993 | DSG | 07/01/02 | Changed from Spec number: 38-00946 to 38-07449 |
| *A | 119639 | CKN | 12/05/02 | Updated Operation : Updated Power Saving Features : Replaced 8 MHz with 20 MHz. |
| *B | 277130 | RGL | 10/26/04 | Updated Ordering Information : Updated part numbers. |
| *C | 395808 | RGL | 09/07/05 | Updated Ordering Information : No change in part numbers. Minor Change: Fixed typo in the "Package Type" column. |
| *D | 2565316 | AESA / KVM | 09/16/08 | Updated CyClocks Software : Updated description. Updated Ordering Information : Updated part numbers. Replaced "Lead-Free" with "Pb-Free". Added Note "Not recommended for new designs." and referred in non Pb-free part numbers. Updated to new template. |
| *E | 2761988 | KVM | 09/10/09 | Updated Selector Guide : Updated details in "Part Number" column. Removed the column "Outputs". Consolidated two rows. Updated Switching Characteristics : Updated details in "Description" column (Updated part number suffixes). Updated Switching Characteristics : Updated details in "Description" column (Updated part number suffixes). Updated Switching Characteristics : Updated details in "Description" column (Updated part number suffixes). Updated Switching Characteristics : Updated details in "Description" column (Updated part number suffixes). Updated Ordering Information : No change in part numbers. Included Temperature Range values in "Operating Range" column. Minor Change: Fixed typo in the "Operating Range" column corresponding to part numbers CY2292FZXI and CY2292FZXIT. |
| *F | 2897775 | KVM | 03/23/10 | Updated Ordering Information : Updated part numbers. Added Possible Configurations . Moved xxx parts from ordering information table to possible configurations table. Updated Package Diagrams . |
| *G | 2948137 | KVM | 06/09/10 | Updated Pinouts : Updated Figure 1 (Updated title only (to include both SOIC and TSSOP)). Added Acronyms . |
| *H | 3010397 | KVM | 08/18/2010 | Removed CY2071F related information in all instances across the document as CY2071F is obsolete. Updated Cypress FTG Programmer : Updated description. Updated Ordering Information : Updated part numbers. Added Ordering Code Definitions . |

Document History Page *(continued)*

| Document Title: CY2292, Three-PLL General-Purpose EPROM-Programmable Clock Generator | | | | |
|--|---------|-----------------|-----------------|--|
| Document Number: 38-07449 | | | | |
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *I | 3849272 | PURU | 12/21/2012 | Removed "Understanding the CY2291 and CY2292" application note related information in all instances across the document. Updated Package Diagrams : spec 51-85068 – Changed revision from *C to *E. spec 51-85091 – Changed revision from *C to *D. |
| *J | 4161799 | CINM | 10/18/2013 | Updated Package Characteristics : Added θ_{JA} and θ_{JC} values for 16-pin TSSOP package. Updated to new template. Completing Sunset Review. |
| *K | 4576237 | AJU | 11/21/2014 | Updated Functional Description : Added "For a complete list of related documentation, click here ." at the end. Updated Package Diagrams . |
| *L | 5495659 | XHT | 10/26/2016 | Updated to new template. Completing Sunset Review. |
| *M | 5986795 | AESATP12 | 12/07/2017 | Updated logo and copyright. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|-------------------------------|--|
| ARM® Cortex® Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Internet of Things | cypress.com/iot |
| Memory | cypress.com/memory |
| Microcontrollers | cypress.com/mcu |
| PSoC | cypress.com/psoc |
| Power Management ICs | cypress.com/pmic |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless Connectivity | cypress.com/wireless |

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2002-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Cypress Semiconductor:

[CY2292FXC](#) [CY2292FXCT](#) [CY2292FXI](#) [CY2292FXIT](#) [CY2292FZX](#) [CY2292FZXT](#) [CY2292FZXI](#) [CY2292FZXIT](#)
[CY2292SXC-492](#) [CY2292SXC-492T](#) [CY2292SXL-1X6](#) [CY2292SXL-1X6T](#) [CY2292SXL-1J4T](#) [CY2292SXC-984](#)
[CY2292SXC-984T](#) [CY2292SXL-1K2](#) [CY2292SXL-1K2T](#) [CY2292SXL-1T3](#) [CY2292SXL-1T3T](#) [CY2292SXL-1V1](#)
[CY2292SXL-1V1T](#) [CY2292SXL-808](#) [CY2292SXL-808T](#) [CY2292ASXI-026](#) [CY2292ASXI-026T](#) [CY2292SC-984](#)
[CY2292SL-1V1](#) [CY2292SL-1J5](#)