TPIC7218-Q1 Power Controller and Sensor ASIC For Braking Applications

1 Device Overview

1.1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4
- PWM Low-Side Drivers
  - 4 PWM Low-Side Driver Outputs
  - Current Limitation
  - Thermal Protection: T_J = 185°C (Minimum)
  - Open-Load Detection
  - Energy Capability: 30 mJ at T_J = 150°C
  - Clamp Voltage: 40 V
  - Low R_{DSon}: 0.3 Ω (Maximum) at T_J = 150°C
- Digital Low-Side Drivers
  - 4 Digital Low-Side Driver Outputs
  - Current Limitation
  - Thermal Protection: T_J = 185°C (Minimum)
  - Open-Load Detection
  - Energy Capability: 50 mJ at T_J = 150°C
  - Clamp Voltage: 40 V
  - Low R_{DSon}: 0.2 Ω (Maximum) at T_J = 150°C
- Dual High-Side Power Drivers
  - Direct Input Control
  - PWM Capability
  - Load Dump (overvoltage) Detection
  - Programmable overcurrent detection
  - Load Leakage Detection
  - Programmable short-circuit Protection
  - Fault detection over SPI
- Wheel-Speed Sensor Interface
  - Compatible with Intelligent and Active Wheel-Speed Sensors
  - 4 High-Side Switches With Short-Circuit Protection
  - 4 Low-Side Switches With Short-Circuit Protection
  - 2 High Voltage Low-Side Output Drivers
  - 4 Digital Outputs to Indicate the Speed
  - Integrated Data Decoder for Intelligent Wheel-Speed Sensors
- Open-Drain Warning Lamp Drivers
  - 2 High Voltage Drivers
  - Thermal Protection With Hysteresis
  - Current Limitation
  - T_J = 185°C (Minimum)
  - R_{DSon}: 4 Ω at T_J = 150°C
  - Clamp Voltage: 40 V
- Other Features
  - K-LINE Transceiver
  - 3.3-V or 5-V Compatible Digital IO
  - Internal 3.3-V Regulator
  - Internal Charge Pump
  - 1 Low-Voltage Open-Drain Warning Lamp Driver
  - Full Duplex SPI Interface
  - Watchdog Input With Open-Drain Fault Reporting for Safety
  - Pb-Free ASIC
  - Compliant With CISPR 25 NB Class 5 for Conducted and Radiated Emissions

1.2 Applications

- Anti-lock Braking Systems (ABS)
- Electronic Stability Control Systems (ESC)

1.3 Description

The TPIC7218-Q1 device integrates in single package several functions needed in ABS and ESC electronic control units (ECU). This integration coupled with the minimization of the external components saves valuable ECU board space.

The TPIC7218-Q1 device is an antilock braking controller capable of directly driving eight solenoid valves with internal high-current low-side drivers. Low-side drivers configured for digital control do not require external voltage clamps. The TPIC7218-Q1 device has gate drive capability for two high-side N-Channel MOSFETs that can be used to drive a pump motor and power to all solenoids. The TPIC7218-Q1 device provides a fault-tolerant interface for both Intelligent and Active wheel-speed sensors to an external microprocessor. The TPIC7218-Q1 device can be used with either 3.3- or 5-V microprocessors and uses a standard SPI (Serial-Peripheral Interface).

The TPIC7218-Q1 device has two internal open-drain warning lamp drivers that can be pulled up to battery voltage, as well as one low-voltage driver. An internal state machine monitors a watchdog input and reports faults on a warning-lamp pin and SPI register. A K-Line transceiver is also included. A multitude of safety and fault monitoring functionality supervise both system and TPIC7218-Q1 circuits. Faults must be polled and reset over SPI. The TPIC7218-Q1 device is designed for use in harsh automotive environments, capable of withstanding high operating temperatures and electrically noisy signals and power. Short-to-ground, short-to-battery, and open-load conditions are tolerated and monitored. The TPIC7218-Q1 device also exhibits outstanding Electro-Magnetic Compatibility (EMC) performance.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPIC7218-Q1	HTQFP (80)	12.00 mm × 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

1.4 Functional Block Diagram

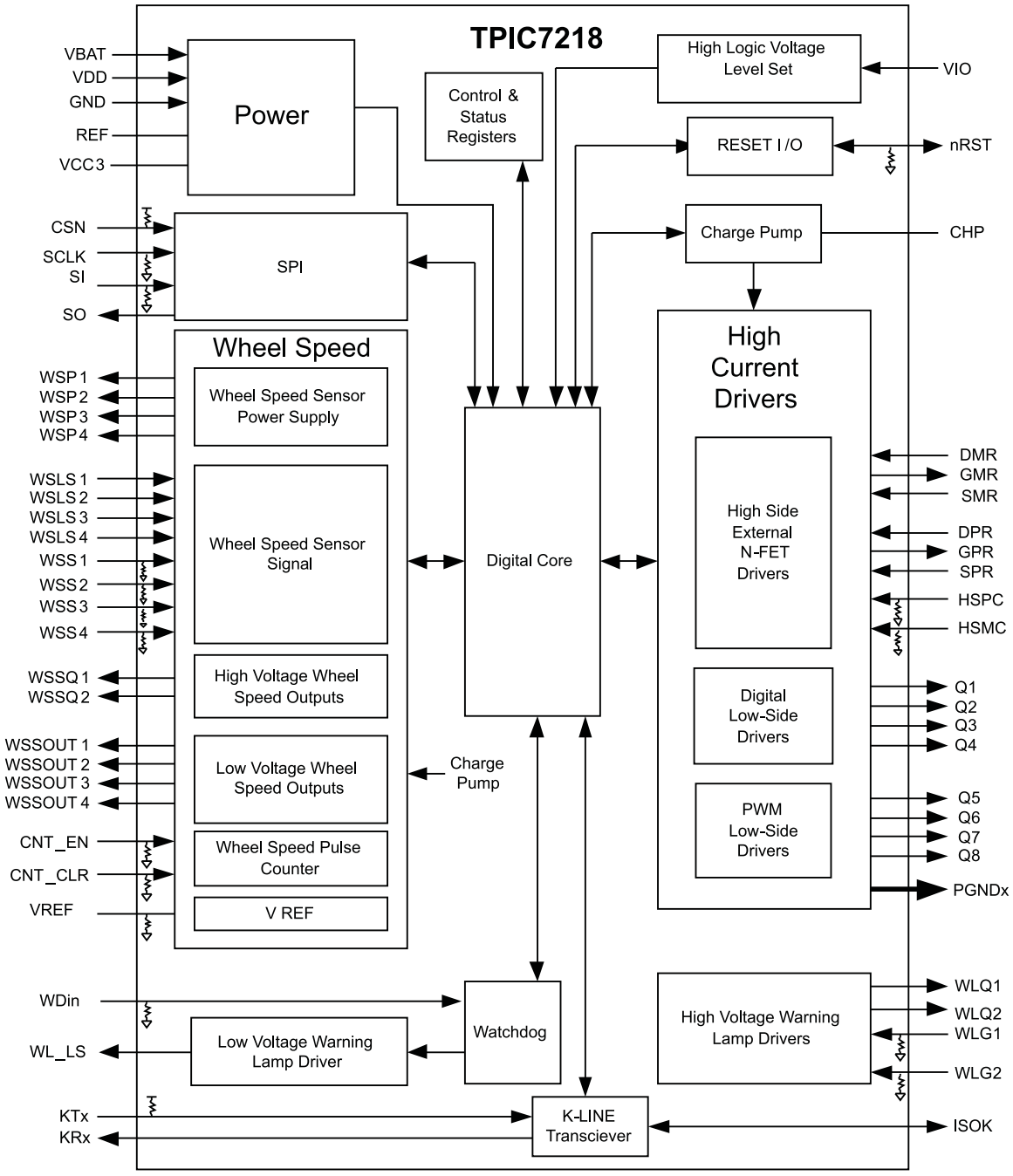


Figure 1-1. Functional Block Diagram

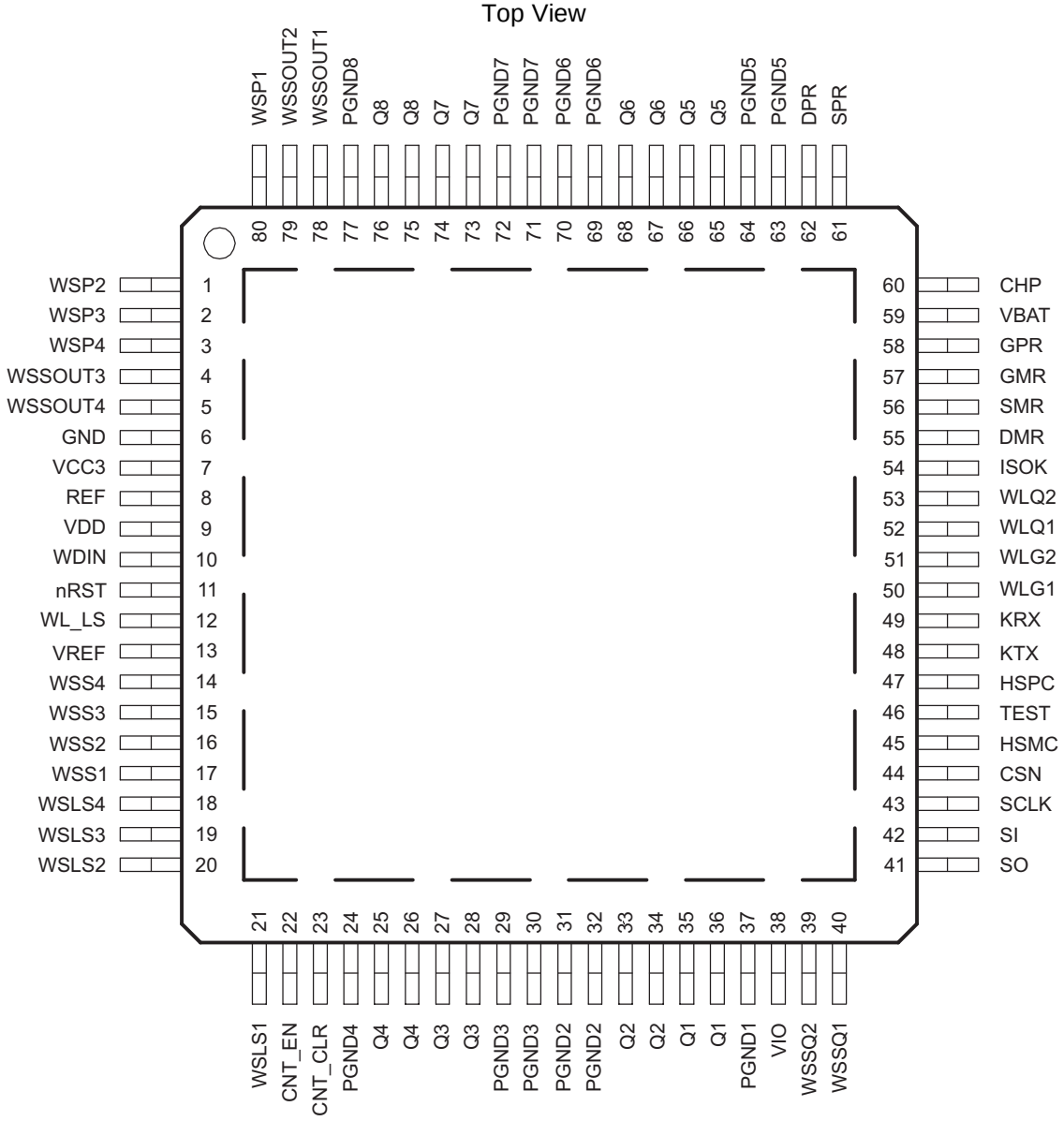
Table of Contents

2 Revision History

Changes from Original (August 2010) to Revision A	Page
• Released full version of the data sheet	1

3 Pin Configuration and Functions

PFP Package
80-Pin HTQFP With PowerPAD™
Top View



Pin Functions

PIN		I/O	FUNCTION DESCRIPTION	INPUT PIN PULLUP OR PULLDOWN	PIN DURING RESET CONDITION
NAME	NO.				
CHP	60	O	External 100-nF capacitor to VBAT for an internal charge pump	Pullup	VCHP = VBAT + 12 V (typical)
CNT_CLR	23	I	Clear bit for the 8-bit digital counter that counts the wheel-speed sensor pulse edges seen in WSSOUTx	Pulldown	
CNT_EN	22	I	Enable bit for the 8-bit digital counter that counts the wheel-speed sensor pulse edges seen in WSSOUTx	Pulldown	
CSN	44	I	SPI chip select active low pin	Pullup	

Pin Functions (continued)

PIN		I/O	FUNCTION DESCRIPTION	INPUT PIN PULLUP OR PULLDOWN	PIN DURING RESET CONDITION
NAME	NO.				
DMR	55	I	Drain pin for master relay (MR) FET	Pulldown	Externally supplied voltage (VBAT)
DPR	62	I	Drain pin for PR (pump motor relay) FET	Pulldown	Externally supplied voltage (VBAT)
GMR	57	O	Gate pin for master relay (MR) FET		Low
GND	6	Ground	Ground		
GPR	58	O	Gate pin for PR (pump motor relay) FET		Low
HSMC	45	I	Logic input for MR (master relay) FET	Pulldown	
HSPC	47	In	Logic input for PR (pump motor relay) FET	Pulldown	
ISOK	54	I/O	K-line serial data transmit output to diagnosis tester and K-line serial data receive input from diagnosis tester	High-Z	High-Z
KRx	49	O	K-line serial data input to the microcontroller		High
KTx	48	I	K-line serial data output from the microcontroller	Pullup	
nRST	11	I/O	Reset signal that is used to either indicate an internal reset event or to induce an external reset	Pulldown	See Table 5-1
PGND1	37	Ground	Power ground pin for low-side valve driver 1		
PGND2	31	Ground	Power ground pin for low-side valve driver 2		
	32				
PGND3	29	Ground	Power ground pin for low-side valve driver 3		
	30				
PGND4	24	Ground	Power ground pin for low-side valve driver 4		
PGND5	63	Ground	Power ground pin for low-side valve driver 5		
	64				
PGND6	69	Ground	Power ground pin for low-side valve driver 6		
	70				
PGND7	71	Ground	Power ground pin for low-side valve driver 7		
	72				
PGND8	77	Ground	Power ground pin for low-side valve driver 8		
Q1	35	O	Drain pin of the low-side valve driver 1		High-Z
	36				
Q2	33	O	Drain pin of the low-side valve driver 2		High-Z
	34				
Q3	27	O	Drain pin of the low-side valve driver 3		High-Z
	28				
Q4	25	O	Drain pin of the low-side valve driver 4		High-Z
	26				
Q5	65	O	Drain pin of the low-side valve driver 5		High-Z
	66				
Q6	67	O	Drain pin of the low-side valve driver 6		High-Z
	68				
Q7	73	O	Drain pin of the low-side valve driver 7		High-Z
	74				
Q8	75	O	Drain pin of the low-side valve driver 8		High-Z
	76				
REF	8	I	Reference pin used to generate the internal bias currents. An external load of 10 kΩ is needed.	Pulldown	REF = 1.25 V
SCLK	43	I	SPI clock pin	Pulldown	

Pin Functions (continued)

PIN		I/O	FUNCTION DESCRIPTION	INPUT PIN PULLUP OR PULLDOWN	PIN DURING RESET CONDITION
NAME	NO.				
SI	42	I	SPI input pin	Pulldown	
SMR	56	O	Source pin for master relay (MR) FET		Low
SO	41	O	SPI output pin		High-Z
SPR	61	I/O	Source pin for PR (pump motor relay) FET		Low
TEST	46	I	Internal test pin. For any application, this is externally pulled to ground with a 1-kΩ resistor.	Pulldown	
VBAT	59	Power	Battery power supply (after reverse battery)		
VCC3	7	Power	Internal regulator for digital logic. Connect this pin only to a capacitor for regulator stability.		VCC3 = 3.3 V
VDD	9	Power	5-V external power supply		
VIO	38	Power	3.3-V or 5-V external supply for the I/O buffers		
VREF	13	I	Externally supplied voltage reference used to set the current detection thresholds for the wheel-speed sensor interface	Pulldown	
WDIN	10	I	Watchdog timer signal	Pulldown	
WLG1	50	I	Logic input for warning lamp driver 1	Pulldown	
WLG2	51	I	Logic input for warning lamp driver 2	Pulldown	
WLQ1	52	O	Drain pin of low-side warning lamp driver 1		See Table 5-1
WLQ2	53	O	Drain pin of low-side warning lamp driver 2		See Table 5-1
WL_LS	12	O	Low side switch for warning-lamp driver control that indicates the watchdog status	High-Z	See Table 5-1
WSLS1	21	I	Wheel-speed sensor channel 1 low-side switch	High-Z	
WSLS2	20	I	Wheel-speed sensor channel 2 low-side switch	High-Z	
WSLS3	19	I	Wheel-speed sensor channel 3 low-side switch	High-Z	
WSLS4	18	I	Wheel-speed sensor channel 4 low-side switch	High-Z	
WSP1	80	O	Supplies VBAT power to wheel-speed sensor channel 2		Low
WSP2	1	O	Supplies VBAT power to wheel-speed sensor channel 2		Low
WSP3	2	O	Supplies VBAT power to wheel-speed sensor channel 3		Low
WSP4	3	O	Supplies VBAT power to wheel-speed sensorchannel 4		Low
WSS1	17	I	Wheel-speed sensor channel 1 signal pin	Pulldown	
WSS2	16	I	Wheel-speed sensor channel 2 signal pin	Pulldown	
WSS3	15	I	Wheel-speed sensor channel 3 signal pin	Pulldown	
WSS4	14	I	Wheel-speed sensor channel 4 signal pin	Pulldown	
WSSOUT1	78	O	Supplies processed wheel-speed pulse signal output to the microcontroller of channel 1 in a digital voltage form		Low
WSSOUT2	79	O	Supplies to the microcontroller the processed wheel-speed pulse signal of channel 2 in a digital voltage form		Low
WSSOUT3	4	O	Supplies to the microcontroller the processed wheel-speed pulse signal of channel 3 in a digital voltage form		Low
WSSOUT4	5	O	Supplies to the microcontroller the processed wheel-speed pulse signal of channel 4 in a digital voltage form		Low
WSSQ1	40	O	Drain pin for wheel-speed channel 1 output driver. Used to pass WSSOUT1 information to a high-voltage capable node		High-Z
WSSQ2	39	O	Drain pin for wheel-speed channel 2 output driver. Used to pass WSSOUT2 information to a high-voltage capable node		High-Z
PAD		Ground	Thermal power ground pin for low-side drivers. Connect to PGNDx plane.		

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_{CC}		VDD, VIO	–0.3	6.5	V
Input voltage, V_{IN}		WDin, CNT_EN, CNT_CLR, SI, SCLK, CSN, KRX, KTX, WL_LS, WLGx, VIO, HSMC, HSPC	–0.3	6.5	V
		WSSQx, WSSx, WSLSx	–0.3	40	V
		CHP	–0.3	55	V
		DMR,DPR	–1	40	V
		SMR,SPR, TEST	–0.3	40	V
Supply voltage range, V_{BAT}	Load dump	VBAT	–1	40	V
	Transient (2 ms)		–1	40	V
Load dump voltage, V_{ISOK}(2)		ISOK	–0.3	40	V
Output voltage, V_{OUT}		Qx, WLQx, WSSQx	–0.3	40	V
		SO	–0.3	(V_{CC} + 0.3)	V
		nRST , WL_LS	–0.3	6.5	V
		GMR, GPR	–1	55	V
REF voltage, V_{REF}		REF, VREF	–0.3	6.5	V
Ground voltage, V_{GND}		PGNDx, GND	–0.3	0.3	V
Drain current, I_{IN}	Continuous	Q1, 2, 3, 4	0	5	A
		Q5, 6, 7, 8,	0	3.5	A
		WLQx	0	100	mA
		nRST		±20	mA
	Negative Transients	Q1, 2, 3, 4 (10 ms)	–5	0	A
		Q5, 6, 7, 8, (10 ms)	–5	0	A
		WLQx (2 ms)	–5	0	A
Input current, I_{IN}		WDIN, WLGx, CNT_EN, CNT_CLR, SI, SCLK, CSN, KRX, KTX, HSMC, HSPC		±20	mA
		SPR, SMR	–10	10	
Output current, I_{OUT}		SO		±20	mA
REF current, I_{REF}		REF		±20	mA
Short-circuit current limit, I_{SC}		ISOK		1000	mA
Current with 510-Ω sense, I_{ISOK}		ISOK	–100	113.5	mA
Supply current, I_{CC}		VDD	–20	50	mA
		VBAT (including WSSPx current limit thresholds)	–20	620	mA
Repetitive avalanche energy, E_{AR_DQ150} (T_J = 150°C)		Q1, 2, 3, 4		50	mJ
Repetitive avalanche energy, E_{AR_PQ150} (T_J = 150°C)		Q5, 6, 7, 8		30	mJ
ISOK clamp energy, E_{Clamp}		ISOK		20	mJ
Operating virtual-junction temperature, T_J			–40	175	°C
T_{stg}		Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This module survives double-battery jump-start conditions in typical application for 10 minutes duration.

4.2 ESD Ratings

				VALUES	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	WLQx, Qx, VBAT, ISOK, DMR, SMR, WSSx, WSLSx, WSPx, WSSQx, DPR, SPR (to GND)	±4000	V
			Other pins	±2000	
		Charged device model (CDM), per AEC Q100-011	Corner pins (WSP2, WSP1, SPR, CHP SO, WSSQ1, WSLS1, and WSLS2)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BAT}	Supply voltage, battery	VBAT	6	20	V
V_{DD}	Supply voltage	VDD	4.5	5.5	V
$V_{IO\_3.3V}$	Supply voltage I/O 3.3V	VIO is a 3.3-V externally supplied power	2.8	3.6	V
V_{IO_5V}	Supply voltage I/O 5V	VIO is a 5-V externally supplied power	4.5	5.5	V
V_{IN}	Input voltage	WDIN, CNT_EN, CNT_CLR, SI, SCLK, CSN, nRST, HSMC, HSPC, KTX, WLGx	0	V_{IO} + 0.5	V
V_{OUT}	Output voltage	Qx, WLQx	0	V_{BAT}	V
T_A	Operating ambient temperature		–40	125	°C

4.4 Thermal Information

THERMAL METRIC (1)		TPIC7218-Q1 PFP (HTQFP) 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

4.5 Input Port Electrical Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
$V_{IH\_3.3V}$	Input high voltage (3.3-V compatible)	WDIN, CNT_CLR, CNT_EN, HSMC, HSPC, WLGx, CSN, SI, SCLK, nRST			2.2	V
$V_{IL\_3.3V}$	Input low voltage (3.3-V compatible)	WDIN, CNT_CLR, CNT_EN, HSMC, HSPC, WLGx, CSN, SI, SCLK, nRST	0.8			V
$V_{hys\_3.3V}$	Input voltage threshold hysteresis (5-V compatible)	WDIN, CNT_CLR, CNT_EN, HSMC, HSPC, WLGx, CSN, SI, SCLK, nRST	300			mV
V_{IH_5V}	Input high voltage (5-V compatible)	WDIN, CNT_CLR, CNT_EN, HSMC, HSPC, WLGx, CSN, SI, SCLK, nRST			3.5	V
V_{IL_5V}	Input low voltage (5-V compatible)	WDIN, CNT_CLR, CNT_EN, HSMC, HSPC, WLGx, CSN, SI, SCLK, nRST	1			V
V_{hys_5V}	Input voltage threshold hysteresis (5-V compatible)	WDIN, CNT_CLR, CNT_EN, HSMC, HSPC, WLGx, CSN, SI, SCLK, nRST	300			mV
I_{PD}	Pin pulldown current, with V_{IN} = V_{DD} (max)(5.5 V) to V_{IL} (min)	WDIN, CNT_CLR, CNT_EN, HSMC, HSPC, WLGx, SI, SCLK, nRST	5		20	µA
I_{pu_csn}	CSN pullup current		–20		–5	µA
I_{PD_SMR}	SMR pin input current		–1	0	1	mA

4.6 PWM Low-Side Driver Electrical Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{on_PWMx}	On resistance	150°C junction temperature, 6 V ≤ V_{BAT} ≤ 20 V			0.3	Ω
I_{lim_PWMx}	Current limit		5			A
		T_A = –40°C	5.5			A
I_{sink_PWMx}	Sink current	Qx between 1 V and 20 V	10		60	µA
I_{leak_PWMx}	Drain leakage current	V_{BAT} = 0, V_{DD} = 0			1	µA
T_{sd_PWMx}	Thermal shutdown junction temperature		185		215	°C
$V_{olvtDlPWMx}$	Open load comparator threshold voltage		1.84		2.16	V
V_{cl_PWMx}	Active clamp voltage		40		50	V
V_{bvdss_PWMx}	Max BVDSS voltage without active clamp		50			V
I_{neg_PWMx}	Maximum negative current for 10 ms		–5			A

4.7 Digital Low-Side Driver Electrical Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{on_DLSx}	On resistance	150°C junction temperature, 6 V ≤ V_{BAT} ≤ 20 V			0.2	Ω
I_{lim_DLSx}	Current limit		6			A
I_{sink_DLSx}	Sink current	Qx output between 1 V and 20 V	10		60	µA
I_{leak_DLSx}	Drain leakage current	V_{BAT} = 0, VDD = 0			1	µA
T_{sd_DLSx}	Thermal shutdown junction temperature		185		215	°C
V_{olvt_DLSx}	Open load comparator threshold		1.84		2.16	V
V_{cl_DLSx}	Active clamp voltage		40		50	V
V_{bvdss_DLSx}	Max BVDSS voltage without active clamp		50			V
I_{neg_DLSx}	Maximum negative current for 10 ms		–5			A

4.8 High-Side Driver Electrical Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DMR}/I_{DPR}	Overcurrent threshold current		60	75	90	µA
V_{STG}	On-state short-to-ground detection voltage		1.6	2	2.4	V
I_{LCdet}	Leakage current in SMR pin		3	5	7	mA
I_{leak_SMR}	Leakage current on SMR	0 ≤ SMR ≤ 20 V, 6 V ≤ V_{BAT} ≤ 20 V			135	µA
I_{Dark_DMR}	Dark current	0 ≤ DMR ≤ 20 V, V_{BAT} = 0, V_{DD} ≤ 0			2.5	µA
V_{FGMR}/V_{FGPR}	Voltage threshold FGMR in GMR pin and FGPR in GPR pin		1.6	2	2.4	V
V_{gs_clamp}	Voltage clamp between GMR-SMR and GPR-SPR pins		16		20	V
V_{ON}	Output on voltage for GMR and GMR (each are turned on individually)	6 V < V_{BAT} < 7 V	V_{BAT} + 5		V_{BAT} + 15	V
		7 V ≤ V_{BAT} < 10 V	V_{BAT} + 7		V_{BAT} + 15	
		10 V ≤ V_{BAT} < 20 V	V_{BAT} + 10		V_{BAT} + 15	
		7 V ≤ V_{BAT} < 10 V	V_{BAT} + 7		V_{BAT} + 15	
		10 V ≤ V_{BAT} < 20 V	V_{BAT} + 10		V_{BAT} + 15	

4.9 K-Line Electrical Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL_tx}	KTX input low voltage threshold		0.3 × V_{DD}			V
V_{IH_tx}	KTX input high voltage threshold				0.7 × V_{DD}	V
I_{pu_tx}	KTX pullup current		–40		–2	µA
V_{OL_rx}	KRX output low voltage threshold				0.2* × V_{DD}	V
V_{OH_rx}	KRX output high voltage threshold		0.8 × V_{DD}			V
T_{lim}	Thermal shutdown temperature		185		215	C
V_{hys_kln}	Thermal shutdown hysteresis		20		30	C
V_{IL_iso}	ISOK input low voltage threshold		0.4 × V_{BAT}			V
V_{IH_iso}	ISOK input high voltage threshold				0.7 × V_{BAT}	V
V_{hys_iso}	Input hysteresis	$V_{hys\_iso} = V_{IH\_iso} – V_{IL\_iso}$	0.05 × V_{BAT}		0.1 × V_{BAT}	V
I_{SC_iso}	Short-circuit current limit		50		1000	mA
V_{OL_iso}	Output low voltage				0.1 × V_{BAT}	V
V_{OH_iso}	Output high voltage		0.95 × V_{BAT}			V
I_{leak_isok}	Drain leakage current	V_{BAT} = 0, V_{DD} = 0, I_{SOK} = 12 V			6	µA

4.10 Warning Lamp Electrical Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{on_WLQx}	On resistance	150°C junction temperature			4	Ω
I_{lim_WLQx}	Current limitation		250			mA
T_{sd_WLQx}	Thermal shutdown temperature		185		215	C

Warning Lamp Electrical Characteristics *(continued)*

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{hys_WLQx}	Thermal shutdown hysteresis		20		30	C
I_{sink_WLQx}	Sink current	WLQx output between 1 V and 20 V	10		60	µA
I_{leak_WLQx}	Drain leakage current	VBAT = 0, VDD = 0			1	µA
V_{olvt_WLQx}	Open load comparator threshold voltage		2.3		2.7	V
V_{cl_WLQx}	Active clamp voltage		40		50	V
V_{bvdss_WLQx}	Max BVDSS voltage without active clamp		50			V
I_{neg_WLQx}	Maximum negative current for 2 ms		5			A

4.11 Power Supply Electrical Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD}	Current consumption on VDD				20	mA
I_{VBAT}	Current consumption on VBAT				10	mA
$V_{urvlVDD}$	Undervoltage shutdown voltage		4.5	4.625	4.75	V
$V_{uvrhVDD}$	Undervoltage reset threshold for microcontroller		4.6	4.725	4.85	V
$V_{VDD\_uvr\_hys}$	Undervoltage recovery hysteresis		50			mV
V_{rstVDD}	Undervoltage reset voltage				3	V
V_{uvVBAT}	Undervoltage shutdown		5.2	5.6	6	V
V_{ovVBAT}	Overvoltage shutdown		27	29	31	V
V_{REF}	Band-gap reference voltage			1.25		V
	External reference resistor accuracy (chip resistor)	R_{REF} = 10 kΩ			1%	
	External predriver capacitor tolerance	C_{CHP} = 100 nF			20%	
	External load capacitor for internally used VCC3 regulator	100 pF < C_{VCC3} < 10 nF			20%	

4.12 SPI Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	SO output threshold high voltage		V_{DD} –1			V
V_{OL}	SO output threshold low voltage				0.4	V

4.13 WL_LS Low-Side Switch Output Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	WL_LS output low voltage	I_{OL} = 20 mA , WDSTAT = '0'			0.4	V

4.14 Wheel-Speed High-Side Driver Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{on_WSPx}	On resistance	150°C junction temperature	10		30	Ω
I_{leak_WSPx}	Leakage current	Switch disabled, V_{BAT} = 18 V,			10	µA
I_{rvleak_WSPx}	Reverse polarity leakage current	Switch disabled, V_{BAT} open, V_{WSPx}=18 V		100		µA
I_{oc_WSPx}	Short to ground current limitation		50		150	mA
V_{clamp_WSPx}	Maximum output voltage		8	12	15	V
C_{LOAD_WSPx}	Maximum capacitive load				10	nF

4.15 Wheel-Speed Low-Side Driver Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.85 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{on_WSLSx}	On resistance	150°C junction temperature	2		10	Ω
I_{leak_WSLSx}	Leakage current	Switch disabled, V_{BAT} = 18 V,V_{WSLSx} = 18V			200	µA
I_{leak_WSSx}	Leakage current	Switch disabled, V_{BAT} = 18 V,V_{WSLSx} = 18V			200	µA
V_{REF}	Reference voltage used to set WSS threshold detection		1		3.3	V
$V_{THRESH4}$	100% threshold detection V_{REF} / R_{LOAD} (Intelligent Sensor)	V_{WSSX} – V_{WSLSX}	–10%	1 × V_{REF}	10%	V
$V_{THRESH3}$	50% threshold detection V_{REF} / R_{LOAD} (Intelligent Sensor)	V_{WSSX} – V_{WSLSX}	–10%	1 × V_{REF}	10%	V
	100% threshold detection V_{REF} / R_{LOAD} (Active Sensor)		–10%	0.5 × V_{REF}	10%	
$V_{THRESH2}$	25% threshold detection V_{REF} / R_{LOAD} (Intelligent Sensor)V_{WSSX} – V_{WSLSX}	V_{WSSX} – V_{WSLSX}	–10%	0.25 × V_{REF}	10%	V
	50% threshold detection V_{REF} / R_{LOAD}(Active Sensor)		–10%	0.5 × V_{REF}	10%	
$V_{THRESH1}$	11.25% threshold detection V_{REF} / R_{LOAD} (Intelligent Sensor)	V_{WSSX} – V_{WSLSX}	–20%	0.1125 × V_{REF}	20%	V
	22.5% threshold detection V_{REF} / R_{LOAD} (Active Sensor)		–20%	0.225 × V_{REF}	20%	
$V_{WSSthresh}$	$V_{THRESH2}$ = $V_{THRESH3}$ = $V_{THRESH4}$ = 5 kHz, $V_{THRESH1}$= Measured	3 WSS channels switching at 5 kHz			40	dB

4.16 Wheel-Speed Output Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{on_WSSQx}	On resistance	150°C junction temperature	5		15	Ω
I_{lim_WSSQx}	Current limitation		50			mA
I_{leak_WSSQx}	Drain leakage current	V_{WSSQx} = 13.5 V			20	µA
V_{olvt_WSSQx}	Open load/Short to ground comparator threshold voltage		1.84	2	2.16	V
C_{load_WSSQx}	Capacitive Load (Inductive load is not supported)				22	nF

4.17 RST Output Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	RST output low voltage	I_{OL} = 1.6 mA			0.4	V
		1 V < VDD < $V_{urvlVDD}$, I_{OL} = V_{DD}/10 kΩ			0.4	V

4.18 SPI Timing Electrical Characteristics

V_{BAT} = 6 V to 20 V, VDD = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted) (see Figure 4-1)

		MIN	NOM	MAX	UNIT
f_{SPI}	SPI operation frequency	4		8	MHz
t_{SCLK}	SCLK clock period	125			ns
$T_{(WH)}$	SCLK clock high time	62.5			ns
$T_{(WL)}$	SCLK clock low time	62.5			ns
$t_{SU(lead)}$	Setup time from falling edge of CSN to rising edge of SCLK	62.5			ns
$t_{SU(lag)}$	Setup time from falling edge of SCLK to rising edge of CSN	62.5			ns
$t_{pd(SDOEN)}$	Propagation delay from falling edge of CSN to SO valid			50	ns

SPI Timing Electrical Characteristics *(continued)*

V_{BAT} = 6 V to 20 V, VDD = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted) (see Figure 4-1)

			MIN	NOM	MAX	UNIT
$t_{pd(SDODIS)}$	Propagation delay from rising edge of CSN to SO Hi-Z state				50	ns
$t_{pd(valid)}$	Propagation delay from rising edge SCLK to SO	0.2 V1 < SO < 0.8 V1, CL = 200 pF			50	ns

4.19 Power Supply Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RST}	Reset response time				5	µs
t_{rst_delay}	Delay time for reset from low to high (minimum reset hight)		53	76.5	100	ms
$t_{VovVBAT}$	Overvoltage blanking time		280	400	520	µs
$t_{VuvVBAT}$	Undervoltage blanking time		280	400	520	µs

4.20 Wheel-Speed Counter Switching Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{cnt_clr}	CNT_CLR deglitcher duration		4.2		7.8	µs
t_{cnt_en}	CNT_EN deglitcher duration		4.2		7.8	µs

4.21 HS Driver Switching Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{Fovdet}	Overvoltage detection time			280	400	520	µs
t_{GPRact}	Overvoltage activation time			320	460	600	ms
t_{OCdet}	Overcurrent detection time			560	800	1040	µs
t_{STG}	Short to ground detection time			70	100	130	µs
$t_{HSDUVBAT}$	HSD deglitcher time for VBAT undervoltage			1.3		2.5	µs
t_{C1deg} / t_{C2deg}	Comparator deglitcher time			4.2		7.8	µs
t_{LCdet}	Leakage current detection time in SMR pin			140	200	260	µs
t_{Dark_DMR}	Time to reach dark current	After V_{BAT} = 0 V and V_{DD} = 0				300	µs
t_{STGMR}/ t_{STGPR}	Turnon masking time(1)			5		8	ms
t_{ON1}	Turnon time	GMR = 8 nF	–6 V < V_{BAT} < 7 V, GPR > V_{BAT} + 4			0.8	ms
			–7 V ≤ V_{BAT} < 10 V, GPR > V_{BAT} + 6			1.3	
			–10 V ≤ V_{BAT} < 20 V, GPR > V_{BAT} + 9			1.5	
t_{ON2_P}	Turnon time	GPR = 16 nF, GMR, GPR turn ON together	–6 V < VBAT < 7 V, GPR > VBAT + 4			2	ms
			–7 V ≤ V_{BAT} < 10 V, GPR > V_{BAT} + 6			2.8	
			–10 V ≤ V_{BAT} < 20 V, GPR > V_{BAT} + 9			3.3	
t_{ON2_S}	Turnon time	GPR = 16 nF, GPR turnon only	–6 V < VBAT < 7 V, GPR > VBAT + 4			1.1	ms
			–7 V ≤ V_{BAT} < 10 V, GPR > V_{BAT} + 6			1.5	
			–10 V ≤ V_{BAT} < 20 V, GPR > V_{BAT} + 9			1.8	

(1) This deglitcher applies only during the turnon time of GMR/GPR pins. During this masking time, no overcurrent conditions are reported.

4.22 Digital Low-Side Driver Switching Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{osoff_DLSx}	Open load comparator deglitcher		140	200	260	µs
t_r/t_{f_DLSx}	Rise time/fall time	From 10% to 90%	10		50	µs
$t_{d\_on\_DLSx}$	Turnon/turnoff delay time	From CSN going high to digital LSD turning off or turning on			70	µs
$t_{d\_off\_DLSx}$						
$t_{off\_blank\_DLSx}$	Blank time before output shutdown in current limitation		140	200	260	µs
$t_{off\_tmp\_DLSx}$	Blank time before output shutdown in overtemperature		140	200	260	µs

4.23 PWM Low-Side Driver Switching Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{osoff_PWMx}	Open load comparator deglitcher time		140	200	260	µs
t_r/t_{f_PWMx}	Rise time/fall time	From 10% to 90%	30		500	ns
$t_{d\_on\_PWMx}$	Turnon delay time	From CSN going high to PWM LSD turning off			10	µs
$t_{d\_off\_PWMx}$	Turnoff delay time	From CSN going high to PWM LSD turning off			2.25	µs
$t_{off\_blank\_PWMx}$	Blank time before output shutdown in case of current limitation		5	6	7	µs
$t_{off\_tmp\_PWMx}$	Blank time before output shutdown during overtemperature		140	200	260	µs

4.24 K-Line Switching Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{t\_rx\ ft\_tx\ ft\_iso}$	Transmission frequency	KRX, KTX, ISOK, R_{ISO} = 510 Ω, C_{ISO} = 1.3 nF	50		100	kHz
$t_{fall\_tx\_iso}$	Fall time (20% to 80% of ISOK)	R_{ISO} = 510 Ω to VBAT, C_{ISO} = 10 nF to GND			2	µs
$t_{rise\_tx\_iso}$	Rise time (80% to 20% of ISOK)	R_{ISO} = 510 Ω to VBAT, C_{ISO} = 10 nF to GND			15	µs
$t_{pd\_tx\_iso}$	ISOK propagation delay	High to low, R_{ISO} = 510 Ω, C_{ISO} = 10 nF			6	µs
		Low to high, R_{ISO} = 510 Ω, C_{ISO} = 10 nF			6	
$t_{off\_iso\_rx}$	Turnoff propagation delay time	R_{ISO} = 510 Ω, C_{ISO} = 10 nF			17	µs
$t_{off\_tx\_iso}$						
$t_{on\_iso\_rx}$	Turnon propagation delay time	R_{ISO} = 510 Ω, C_{ISO} = 10 nF			4	µs
$t_{on\_tx\_iso}$						
t_{off_kln}	Blank time for overtemperature (1)		140	200	260	µs
t_{on_kln}						
t_{off_isok}	Cumulative blank time before shutdown for overcurrent		15	20	25	µs

(1) t_{off_kln} is the deglitcher time for K-Line to turnoff, and t_{on_kln} is the deglitcher time for K-Line to turn on from shutdown.

4.25 Warning Lamp Switching Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{osoff_WLQx}	Open-load comparator deglitcher time		140	200	260	µs

Warning Lamp Switching Characteristics *(continued)*

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r_WLQx} t_{f_WLQx}	Rise time/fall time	From 10% to 90%			60	µs
$t_{d\_on\_WLQx}$ $t_{d\_off\_WLQx}$	Turnon/turnoff delay time				25	µs
$t_{off\_blank\_WLQx}$ $t_{off\_tmp\_WLQx}$	Blank time for overcurrent /short battery sensing		8	10	12	µs
$t_{on\_tmp\_WLQx}$	Blank time in case of overtemperature		140	200	260	µs

4.26 Watchdog Switching Characteristics

V_{BAT} = 6 V to 20 V, V_{DD} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{WD}	Watchdog window	Upper window (WDH<1:0>)	–10%	programmable	10%	ms
		Lower window (WDL<1:0>)	10%	programmable	10%	
		Out-of-range window (2 × WDH<1:0>)	10%	programmable	10%	
T_{WD_PULSE}	Watchdog induced reset pulse	Watchdog out-of-range (counter stays at 000)	1	1.5	2	ms

4.27 Wheel Speed Interface Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rise_WSPx} t_{fall_WSP}	Propagation delay from rising edge of CSN to the rising and falling edge of WSPx.	20 mA load, C_{load} = 10 nF			100	µs
t_{rise_WSLSx} t_{fall_WSLSx}	Propagation delay from rising edge of CSN to rising and falling edge of WSLSx	50-mA load			50	µs
t_{rise_WSSQx} t_{fall_WSSQx}	Propagation delay from rising edge of CSN to rising and falling edge of WSSQx	50 mA load, C = 200 pF			50	µs

4.28 Wheel-Speed High-Side Driver Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{delay_WSPx}	Delay time for fault reporting		80	100	120	µs

4.29 Wheel-Speed Output Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{delay_WSSQx}	Delay time for overcurrent fault reporting		15	20	25	µs
	Delay time for open load fault reporting		140	200	260	µs

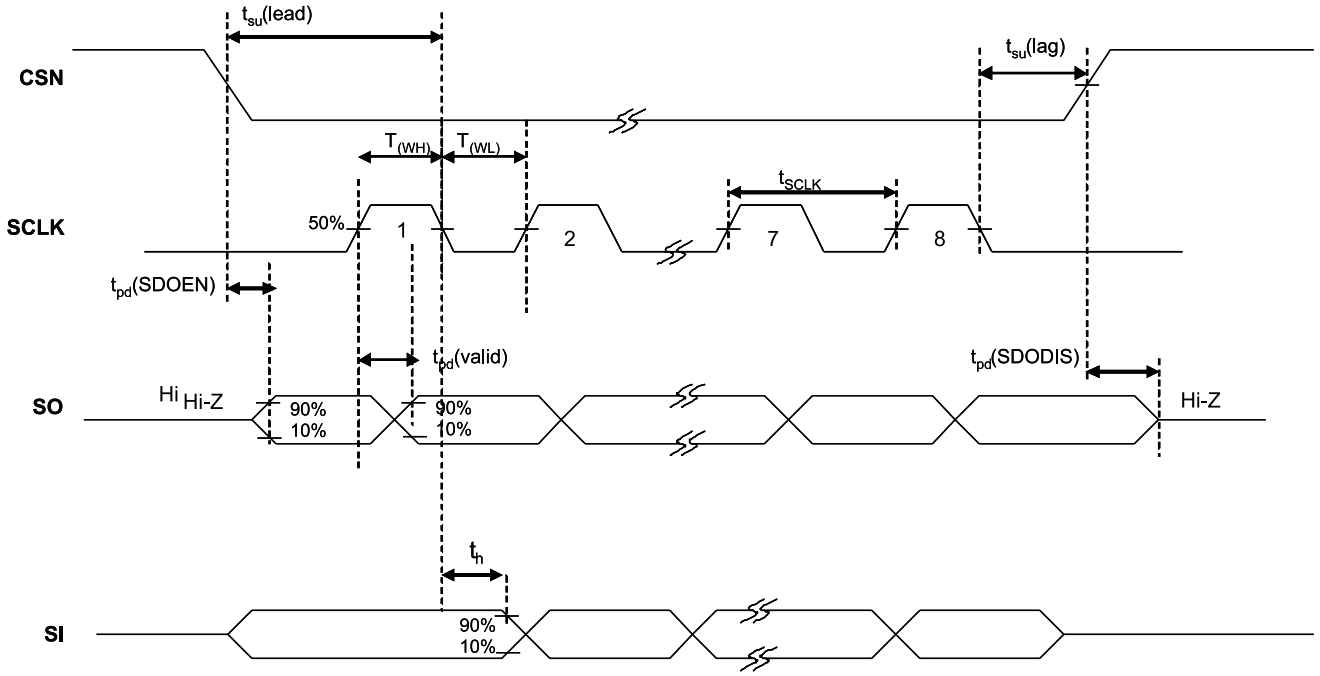


Figure 4-1. SPI Interface Input Timing

4.30 Typical Characteristics

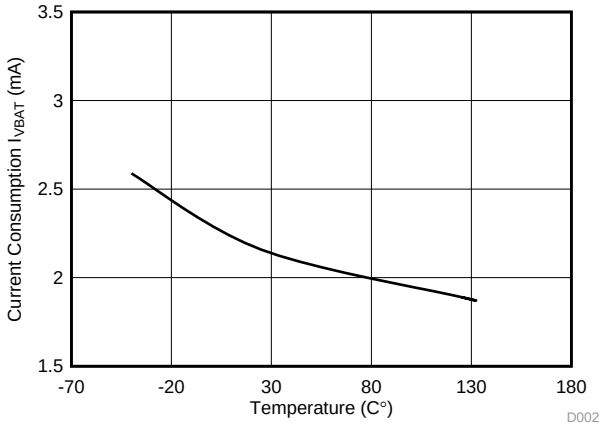


Figure 4-2. Current Consumption from VBAT vs Temperature

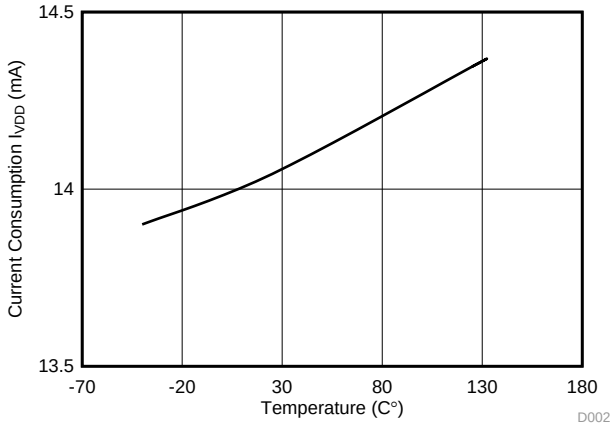


Figure 4-3. Current Consumption from VDD vs Temperature

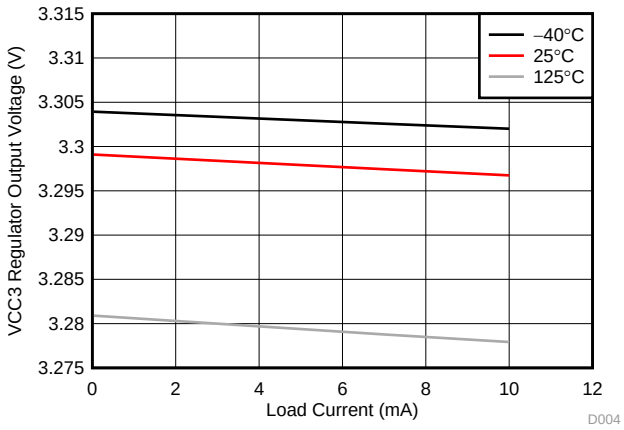


Figure 4-4. VCC3 Regulator Load Regulation Across Temperature (VDD = 4.5 V)

5 Detailed Description

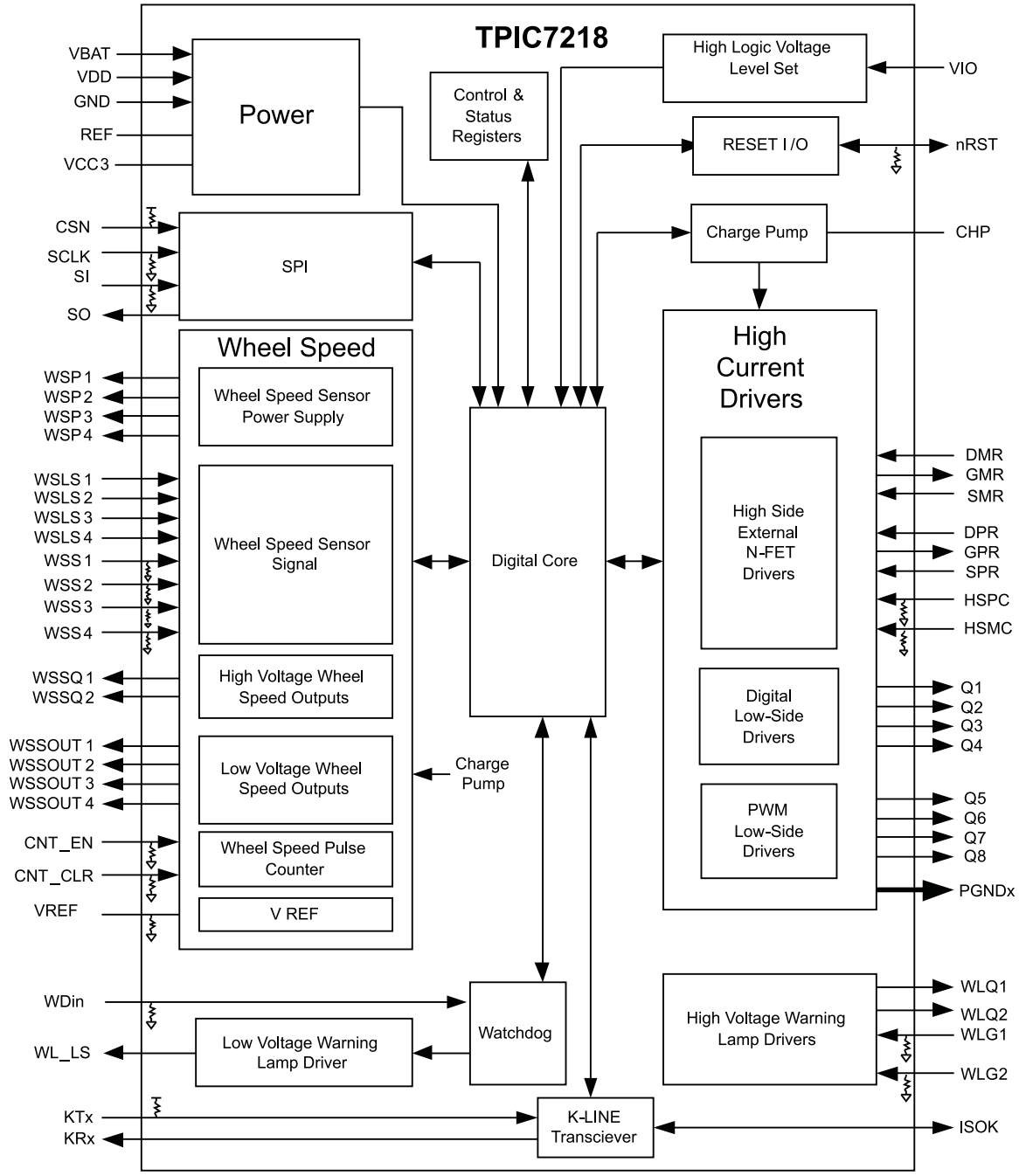
5.1 Overview

The TPIC7218-Q1 device is an anti-lock braking controller capable of directly driving eight solenoid valves with internal high-current low-side drivers. Low-side drivers configured for digital control do not require external voltage clamps. The TPIC7218-Q1 device has gate drive capability for two high-side N-Channel MOSFETs that can be used to drive a pump motor and power to all solenoids. The TPIC7218-Q1 device provides a fault-tolerant interface for both Intelligent and Active wheel-speed sensors to an external microprocessor.

The TPIC7218-Q1 device can be used with either 3.3- or 5-V microprocessors and uses a standard SPI (Serial-Peripheral Interface). The TPIC7218-Q1 device has two internal open-drain warning lamp drivers that can be pulled up to battery voltage, as well as one low-voltage driver. An internal state machine monitors a watchdog input and reports faults on a warning-lamp pin and SPI register. A K-Line transceiver is also included. A multitude of safety and fault monitoring functionality supervise both system and TPIC7218-Q1 circuits. Faults must be polled and reset over SPI.

The TPIC7218-Q1 device is designed for use in harsh automotive environments, capable of withstanding high operating temperatures and electrically noisy signals and power. Short-to-ground, short-to-battery, and open-load conditions are tolerated and monitored. The TPIC7218-Q1 device also exhibits outstanding electromagnetic compatibility (EMC) performance.

5.2 Functional Block Diagram



5.3 Feature Description

5.3.1 Ground Connections

The TPIC7218-Q1 device has two types of grounds: Power-grounds (PGND), which are used to provide a path for internal high-current open-drain FETs, and ground (GND), which are used to provide ground to all analog and digital circuitry. All the PGND pins and the thermal pad are internally shorted together. A very-low impedance connection exists internal to the TPIC7218-Q1 device between all power grounds and the ground pin (pin 6). TI recommends that all PGND, GND, and PowerPad pins be connected together at the pins of the TPIC7218-Q1 device to a solid ground plane. Failure to implement the grounding in this way is likely to result in poor EMC performance.

5.3.2 Charge Pump

An internal charge pump generates the charge necessary for proper operation of all drivers. A capacitor with a value of 100 nF connected between the CHP pin and VBAT pin is required for proper operation. The voltage on the CHP pin is typically 12 V greater than the voltage on the VBAT pin. When selecting a charge pump capacitor, care must be taken to ensure that the capacitors specifications are not violated.

5.3.3 Reference Current Generator

The TPIC7218-Q1 device generates an internal reference current that is output on the REF pin. This pin requires a 10-kΩ, ±1% resistor connected to GND.

5.3.4 Wheel-Speed Reference, V_{REF}

The voltage set on the V_{REF} pin must be stable at all times. If this voltage deviates from the desired setting, then all the wheel-speed thresholds will change. TI recommends externally monitoring the V_{REF} voltage to ensure proper operation of the wheel-speed functional block.

5.3.5 Faults Common To Most Functional Blocks

Table 5-1. Summary Fault State Table

EVENT	GMR	GPR	WLQ1	WLQ2	WL_LS	nRST	Q1-Q4	Q5-Q8	WSPx	WSLSx	SPI
VDD undervoltage shutdown	OFF	OFF	High Z	High Z	Low	Low	High Z	High Z	OFF	High Z	YES(1)
VDD undervoltage reset	OFF	OFF	High Z	High Z	High Z	High Z	High Z	High Z	OFF	High Z	NO
Recovery after VDD undervoltage reset (VDD>4.85V)	OFF	OFF	High Z	High Z	Low	High Z	High Z	High Z	OFF	High Z	YES
Recovery after VDD undervoltage reset (VDD<4.75V)	OFF	OFF	High Z	High Z	Low	Low	High Z	high Z	OFF	High Z	YES
VBAT overvoltage	Not affected(2)	ON	Not affected	Not affected	Not affected	Not affected	High Z	High Z	OFF	High Z	YES
VBAT undervoltage	OFF	OFF	Not affected	Not affected	Not affected	Not affected	High Z	High Z	Not affected	Not affected	YES
Thermal fault (OTSD = '1')	Not affected	Not affected	High Z(3)	High Z	Not affected	Not affected	High Z	High Z	Not affected	Not affected	YES
Watchdog bad (WDSTAT ='0')	OFF	OFF	High Z	High Z	Low	High Z	High Z	High Z	Not affected	Not affected	YES
While in Reset because of Watchdog going to state '000'	OFF	OFF	High Z	High Z	Low	Low	High Z	High Z	OFF	High Z	YES(4)
external reset by pulling nRST pin low	OFF	OFF	High Z	High Z	Low(5)	Low	High Z	High Z	OFF	High Z	YES(1)

(1) The SPI is available if the ASIC is tested standalone. In a system level it would not be available because the VDD supplied microcontroller would be in reset condition.
(2) This state depends on the setting of register map bit, OV_GMR.
(3) There are 8 thermal sensors in the ASIC. 3 implemented for the PWM drivers, 3 for the digital drivers one for the warning lamps and 1 for K-LINE. Only the drivers affected will turn off. There is no master thermal shutdown implemented for the ASIC.
(4) While the watchdog is in reset, the only SPI settings that are not reset are the ones pertaining to the watchdog such as WD_EN and WDH, WDL bits.
(5) WL_LS pin will be pulled low every time that WDSTAT = 0. This can result because of a bad watchdog event or because WD_EN = 0. WL_LS pin will be High Z when WDSTAT = 1.

5.3.6 PWM Low-Side Drivers

The TPIC7218-Q1 device features eight low-side drivers, four of which can be used for pulse width modulation (PWM) of solenoids. The low-side driver pins: Q5, Q6, Q7, and Q8 are open-drain MOSFETs that are capable of sinking large amounts of current. Each driver is monitored for three fault conditions: overcurrent, open-load, and over-temperature. In addition, driver operation is dependent on other fault conditions: VBAT undervoltage, VBAT overvoltage, VDD undervoltage, watchdog fault. See the application circuit and register diagram in Figure 5-1.

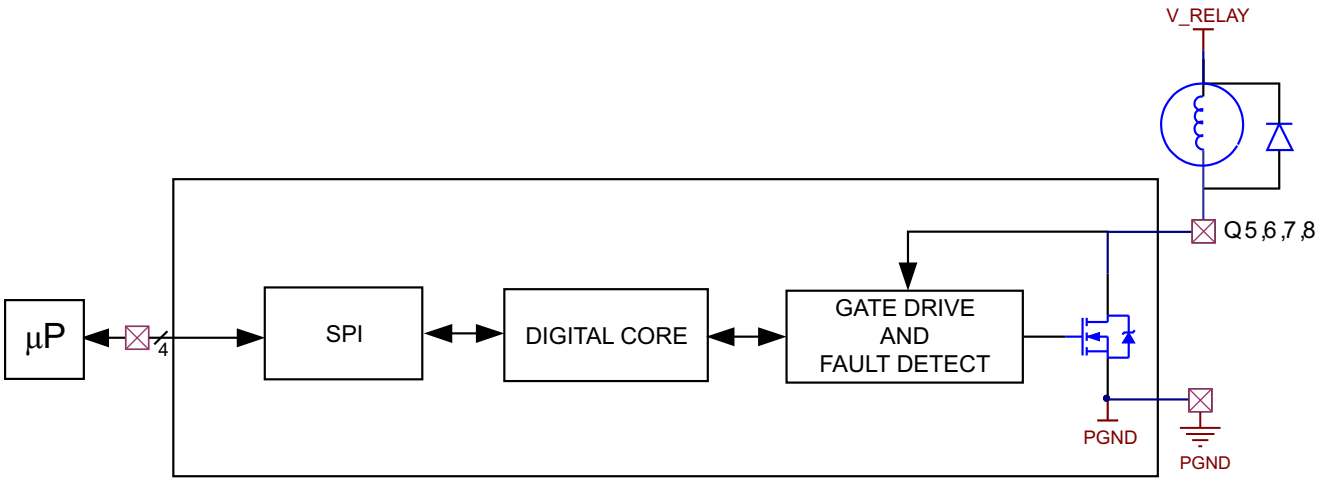


Figure 5-1. PWM Driver Register and Application Circuit Diagram

Each PWM driver features a 10-bit configurable duty-cycle setting, and options for independent phase control. Available phases of 0°, 90°, 180°, and 270° can be set for each driver in registers 0x14, 0x16, 0x18, and 0x1A. Changes in the dedicated 2-bits result in a phase change in the following complete period to prevent glitches. Table 5-2 lists the available phase options based on the settings of the dedicated 2-bit selection

Table 5-2. PWM Phase Selection

$PWMQX_{Phase}$<1>	$PWMQX_{Phase}$<0>	SELECTED PHASE
0	0	0°
1	0	90°
0	1	180°
1	1	270°

Each duty cycle of the PWM driver can be selected by setting the appropriate bits using Equation 1.

$$DutyCycle = \frac{PWMQx<9:0>}{1024} * 100\% \quad (1)$$

For example, a setting of 0x3FF causes a 100% duty cycle and a setting of 0x000 causes a 0% duty cycle.

All 10 bits must be written for the new duty cycle code to be latched into the state machine. Changes in the 10-bit result in a duty-cycle change in the following complete period to prevent glitches. PWM drivers can be used as digital drivers by fully turning them on (100% duty cycle) and off (0% duty cycle). However, care must be taken not to violate electrical specifications when using PWM drivers in this way (such as energy handling capability).

The frequency is also configurable (see Table 5-3), but is not independent for each enabled driver; all PWM drivers are set by selecting a 2-bit value in register 0x12. Frequency selection changes take place only when the PWM drivers are disabled and then re-enabled.

Table 5-3. PWM Frequency Selection

PWM_{Freq}<1>	PWM_{Freq}<0>	SELECTED FREQUENCY
0	0	2 kHz
1	0	4 kHz
0	1	8 kHz
1	1	16 kHz

For example, if Q5 is enabled while the frequency setting is <00> but Q6 is enabled after the frequency setting was changed to <11>, then Q5 is switching at 2 kHz and Q6 is switching at 16 kHz.

Each PWM driver monitors, reports, and has integrated protection for many electrical fault conditions. Overcurrent faults are reported as a 1 in register 0x02, (bits 0, 2, 4, and 6 are referenced by bits F5, F6, F7, and F8) and cause the affected driver to disable after a deglitch time of toff_blank_PWMx. Over-temperature (junction) faults are reported in register 0x03, (bit-6 OTSD) and cause not only the affected driver, but also the adjacent driver to disable after a deglitch time of toff_tmp_PWMx. The PWM drivers also check for an open-load or short to ground condition whenever they are not disabled. This type of fault is reported as 1 in register 0x02, (bits 1, 3, 5, 7 are referenced by bits S5, S6, S7, and S8). A master low-side fault bit in register 0x00, (bit-0) becomes high whenever any of the previously mentioned overcurrent or open-load faults occur. Fault flags can be cleared after the removal of the fault condition by reading the appropriate fault reporting register. When the fault flags are cleared, the low-side master fault bit (FAIL) can be cleared by reading it.

The PWM drivers also respond to fault conditions within other functional blocks. The drivers are disabled whenever VBAT undervoltage, VBAT overvoltage, or VDD undervoltage fault bits in register 0x00 are set. Also watchdog fault can cause PWM drivers to disable, if register 0x11, bit-4 (WD_EN) is set. This bit defaults to 0 upon power up. Any of these faults do not cause the FAIL bit to be set.

Faults can be cleared by reading the appropriate fault reporting register. When the faults are cleared, the drivers can be re-enabled. To enable or re-enable a driver, simply toggle the driver bits (GE5, GE6, GE7, GE8) by writing a 0, then 1. Fault reporting bits do not have any affect on PWM drivers; only the actual fault condition causes a driver to disable. Nevertheless, TI recommends clearing the fault bits by reading these bits before enabling the drivers.

Besides monitoring and reporting faults, PWM drivers have overvoltage-protection circuitry built in. An active-clamp monitors the voltage on PWM driver pins and limits it to V_{cl_PWMx}. At the system level, PWM drivers use an external recirculation diode in parallel with the inductive load.

5.3.7 Digital Low-Side Drivers

The TPIC7218-Q1 device features eight low-side drivers, four of which can be used digital control of solenoids. The low-side driver pins: Q1, Q2, Q3, and Q4 are open-drain MOSFETs that are capable of sinking large amounts of current. Each driver is monitored for three fault conditions: overcurrent, open-load, and over-temperature. However, driver operation also is dependant on other fault conditions: VBAT undervoltage, VBAT overvoltage, VDD undervoltage, watchdog fault. See the application circuit and register diagram in Figure 5-2.

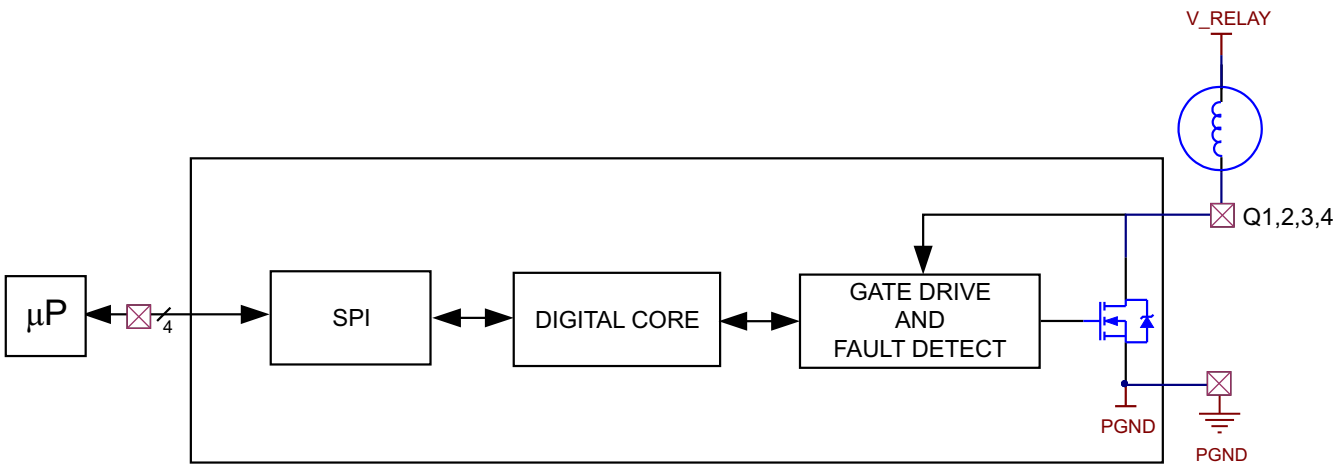


Figure 5-2. Digital Driver Register and Application Circuit Diagram

Each digital driver monitors, reports, and has integrated protection for many electrical fault conditions. Overcurrent faults are reported as a 1 in register 0x01, (bits 0, 2, 4, and 6 are referenced by bits F1, F2, F3, and F4) and cause the affected driver to disable after a deglitch time of toff_blank_DLSx. Over-temperature (junction) faults are reported in register 0x03, (bit-6 OTSD) and cause not only the affected driver, but also the adjacent driver to disable after a deglitch time of toff_tmp_DLSLx. Digital drivers also check for an open-load or short to ground condition whenever they are not enabled. This type of fault is reported as a 1 in register 0x01, (bits 1, 3, 5, 7 are referenced by S1, S2, S3, and S4). The master low-side fault bit in register 0x00, (bit-0) becomes high whenever an overcurrent or open-load fault occurs. Fault flags can be cleared after the removal of the fault condition by reading the appropriate fault reporting register. When this occurs the low-side master fault bit (FAIL) can be cleared by reading it.

The digital drivers also respond to fault conditions within other functional blocks. These drvers are disabled whenever the VBAT undervoltage, VBAT overvoltage, or VDD undervoltage fault bits in register 0x00 are set. Also, a watchdog fault can cause the digital drivers to disable if register 0x11, bit-4 (WD_EN) is set. This bit defaults to 0 upon power up. Any of these faults do not cause the FAIL bit to be set.

Faults can be cleared by reading the appropriate fault reporting register. When this is complete the digital drivers can be re-enabled. To enable or re-enable a driver, simply toggle the driver bits (GE1, GE2, GE3, GE4) by writing a 0, then 1. Fault reporting bits do not have any affect on the digital drivers; only the actual fault condition will cause a driver to disable. Nevertheless, TI recommends clearing the fault bits by reading them before enabling the drivers.

Besides monitoring and reporting faults, digital drivers have overvoltage protection circuitry built in. An active-clamp monitors voltage on the pins of these drivers and limits the voltage to V_{cl_DLSx}.

5.3.8 High-Side Drivers

The TPIC7218-Q1 device features two independent high-side gate drivers to control and monitor external N-Channel FETs. The pins, GPR, SPR, and DPR, are typically used to control an external N-MOSFET for the purpose of providing power to a motor pump. The pins, GMR, SMR, and DMR are typically used to control an external N-MOSFET for the purpose of providing power to the solenoid coils. When activated, the gate voltage drive on the GPR and GMR pins is sufficient to provide a strong V_{GS} because of a built-in charge pump. High-side drivers are electrically protected and monitored for fault conditions.

5.3.8.1 High-Side Terminals: GPR, SPR, DPR, and HSPC

The GPR, SPR, and DPR (gate, source, and drain-pump relay) pins connect to an external N-MOSFET as shown in Figure 5-3. The purpose of this MOSFET is to relay the VBAT power to a pump motor. The N-MOSFET is turned on when the GPR pin is enabled. The GPR pin is controlled by either the HSPC pin or the GE_PR bit, bit-3 of address 0x11 as listed in Table 5-4.

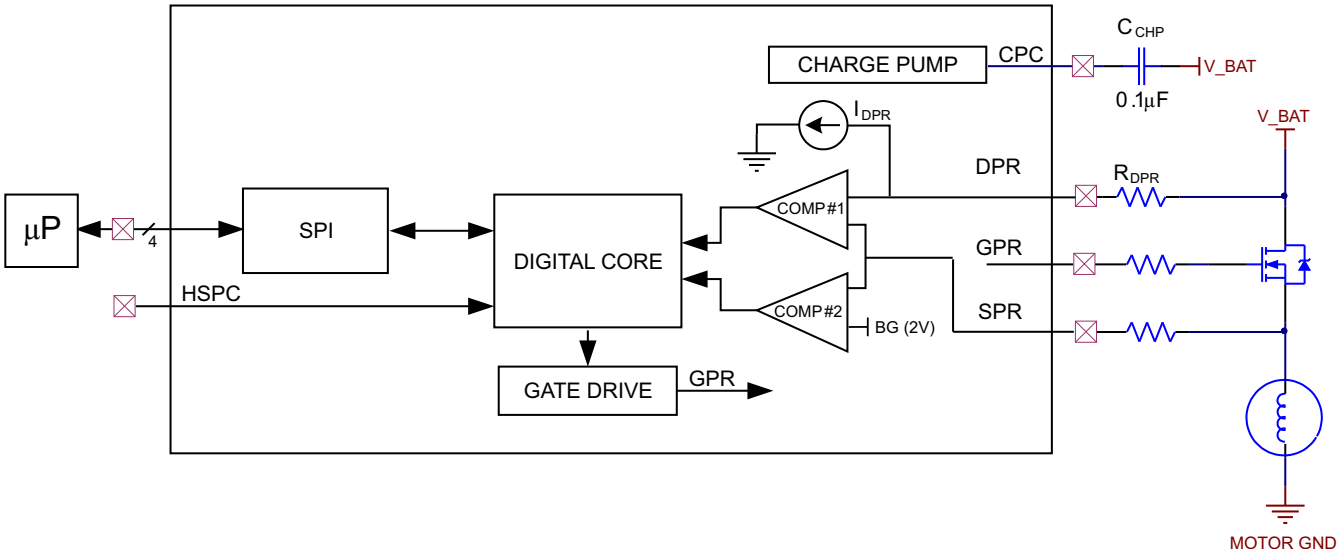


Figure 5-3. GPR, SPR, DPR, and HSPC Register and Application Circuit Diagram

Table 5-4. High-Side Operation Logic

HSPC PIN	GE_PR BIT	GPR GATE PIN
LOW	0	OFF
LOW	1	ON
HIGH	0	ON
HIGH	1	ON
OPEN	1	ON
OPEN	0	OFF

The overcurrent detection of the external N-MOSFET is triggered by a voltage difference between the DPR and SPR pins in comparator COMP #1. To set the overcurrent threshold the external series resistor, R_{DPR}, must be sized to generate a particular input voltage (in conjunction with I_{DPR}) on one input of the comparator. The other input voltage of the comparator changes as a function of the $RDS_{ON(MAX)}$ and I_{DS} values of the N-MOSFET. By comparing these voltages, the N-MOSFET overcurrent condition is reported. Given the $RDS_{ON(MAX)}$ value of the N-MOSFET and the desired overcurrent threshold, R_{DPR} can be calculated using Equation 2.

$$VBAT - (I_{DS} * RDS_{ON(MAX)}) > VBAT - (I_{DPR} * R_{DPR}) \quad (2)$$

If the V_{DS} value of the N-MOSFET exceeds the threshold set by the comparator for more than the deglitcher time, t_{OCdet}, the GPR pin switches off and the appropriate fault flag (OCPR) is set high. When the overcurrent condition ends, the GPR pin can be switched on again with the SPI enable bit or the external enable pin.

Faults detected on VDD, VBAT, Watchdog (if WD_EN bit is high) prevent the high-side driver from enabling; GPR remains low or turns off. At the time the high-side driver is enabled, voltage on GPR pin is tested for a short-to-ground condition only after a certain delay time defined as t_{STGPR}. If a short is detected the GPR pin remains low. Any time the high-side driver is enabled overcurrent in the external MOSFET, short-to-ground on GPR, and short-to-ground on SMR can cause a fault condition and disable the high-side driver.

An overvoltage condition (such as load-dump) on VBAT turns the GPR pin on (clamping any energy from the alternator). If VBAT returns to normal operating voltage from an overvoltage fault condition, the GPR pin remains on for a minimum time, t_{GPRact}.

If an overvoltage condition occurs on VBAT, the fault flag, FOV, is set after a deglitch time, t_{Fovdet}. With the overvoltage removed, the FOV flag can be cleared by reading address 0x00. After the fault bit is cleared, the GPR pin can be re-enabled. The GPR pin does not respond to successive overvoltage conditions until after a blanking time. See Table 5-5 and Figure 5-4 for more details.

Table 5-5. Pump Relay Fault and Operation

SYSTEM EVENT	FAULT BITS AFFECTED	TPIC7218-Q1 STATE		NOTES
		BEFORE EVENT	AFTER EVENT	
VDD Undervoltage	PORn = 1	GPR ON	GPR OFF	nRST is internally driven low
VBAT Overvoltage (>V_{ovVBAT})	FOV = 1	GPR OFF	GPR ON	
VBAT Undervoltage (<V_{uvVBAT})	FUV = 1	GPR ON	GPR OFF	
Watchdog fault (must be enabled)	WDSTAT = 0, WD_FAULT = 1	GPR ON	GPR OFF	WD_EN = 1 (enabled)
nRST pin externally driven low	Erst = 1	GPR ON	GPR OFF	
Overcurrent in motor	OCPR=1,FHSD = 1	GPR ON	GPR OFF	$OCPR_{DIS}$ = 0 (disabled)
Overcurrent in motor	OCPR=1,FHSD = 1	GPR ON	GPR ON	$OCPR_{DIS}$ = 1 (enabled)
Short to GND on GPR, while GPR is OFF (time > t_{STGPR})	FGPR = 1,FHSD = 1	GPR OFF	GPR OFF	$FGPR_{DIS}$ = 0 (disabled), turn ON GPR
Short to GND on GPR, while GPR is ON	FGPR = 1,FHSD = 1	GPR ON	GPR OFF	$FGPR_{DIS}$ = 0 (enabled)
Short to GND on GPR, while GPR is OFF (time > t_{STGPR})	FGPR = 1,FHSD = 1	GPR OFF	GPR ON	$FGPR_{DIS}$ = 1 (enabled), turn ON GPR
Short to GND on GPR, while GPR is ON	FGPR = 1,FHSD = 1	GPR ON	GPR ON	$FGPR_{DIS}$ = 1 (enabled)
Short to GND on SPR	STGPR = 1,FHSD = 1	GPR ON	GPR ON	$STGPR_{DIS}$ = 1 (enabled)
Short to GND on SPR	STGPR = 1,FHSD = 1	GPR ON	GPR OFF	$STGPR_{DIS}$ = 0 (disabled)

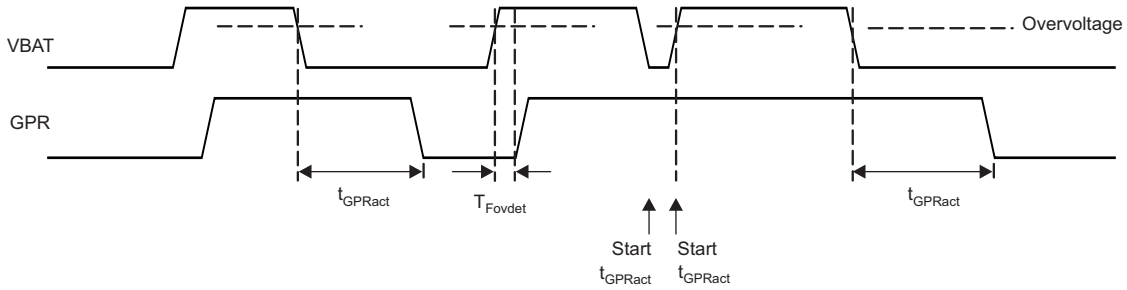


Figure 5-4. Pump Relay High-Side Driver Overvoltage Behavior

The pump relay external MOSFET is electrically protected from voltage spikes by an active voltage clamp that limits any voltage levels between the GPR and SPR pins that are larger than V_{gs_clamp}.

The GPR function supports PWM output. The charge on the charge-pump capacitor, C_{CHP}, which is lost when GPR is switched on, is refreshed before the start of the next PWM cycle to a value that sufficiently ensures proper turnon behavior. The PWM capability consists of a period of T = 5 ms with a duty cycle 10% to 90%. When selecting a duty cycle the rise and fall times of GPR must be taken into account.

5.3.8.2 High-Side Terminals: GMR, SMR, DMR, and HSMC

The GMR, SMR, and DMR (gate, source, and drain master relay) pins connect to an external N-MOSFET as shown in Figure 5-5. The purpose of this MOSFET is to relay VBAT power to a master power supply for solenoid coils. The N-MOSFET turns on when the GMR pin is enabled. The GMR pin function is controlled by either the HSMC pin or the GE_MR bit, bit-2 of address 0x11 as shown in Table 5-6.

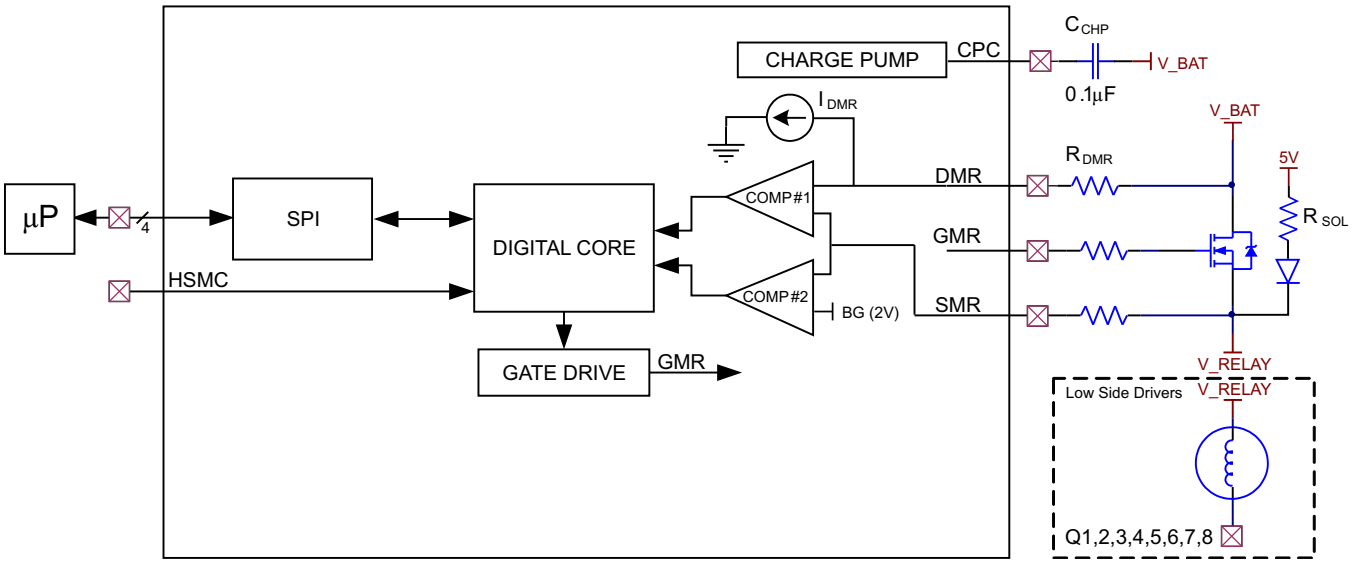


Figure 5-5. GMR, SMR, DMR, and HSMC Register and Application Circuit Diagram

Table 5-6. High-Side Operation Logic

HSMC PIN	GE_MR BIT	GMR GATE PIN
LOW	0	OFF
LOW	1	ON
HIGH	0	ON
HIGH	1	ON
OPEN	1	ON
OPEN	0	OFF

The overcurrent detection of the external N-MOSFET is triggered by a voltage difference between the DMR and SMR pins in comparator COMP #1. To set the overcurrent threshold, the external series resistor, R_{DMR}, must be sized to generate a particular input voltage (in conjunction with I_{DMR}) on one input of the comparator. The other input voltage of the comparator changes as a function of the $RDS_{ON(MAX)}$ and I_{DS} values of the N-MOSFET. By comparing these voltages, the N-MOSFET overcurrent condition is reported. Given the $RDS_{ON(MAX)}$ value of the N-MOSFET and the desired overcurrent threshold, R_{DMR} can be calculated using Equation 3.

$$VBAT - (I_{DS} * RDS_{ON(MAX)}) > VBAT - (I_{DMR} * R_{DMR}) \quad (3)$$

If the V_{DS} of the N-MOSFET exceeds the threshold set by the comparator for more than the deglitcher time, t_{OCdet}, the GMR pin switches off and the appropriate fault flag (OCMR) is set high. When the overcurrent condition ends, the GMR pin can be switched on again with the SPI enable bit or the external enable pin.

Faults detected on VDD, VBAT, Watchdog (if WD_EN bit is high) prevent the high-side driver from enabling; the GMR pin remains low or turns off. At the time the high-side driver is enabled, the voltage on the GMR pin is tested for a short-to-ground condition only after a certain delay time defined as t_{STGPR}. If a short is detected the GMR pin remains low. Any time the high-side driver is enabled overcurrent in MOSFET, short-to-ground on the GMR pin, and short-to-ground on the SMR pin can cause a fault condition and disable the high-side driver.

An overvoltage condition (such as a load-dump) on VBAT either turns the GMR pin off or allows it to remain in the previous state depending on the setting of bit 5 (OV_GMR) in register 0x11. With the overvoltage removed, the fault flag FOV can be cleared by reading address 0x00.

The main relay external MOSFET is electrically protected from voltage spikes by an active voltage clamp that limits any voltage levels between GMR and SMR larger than V_{gs_clamp}.

Load-leakage faults are tested by sourcing a current, I_{LCdet}, out of the SMR pin into the source of the external N-MOSFET. After a time, t_{LCdet}, the SMR voltage is checked to see if it is above VDD. If no leakage is present, the source is above VDD and the GMR pin is turned on. If leakage is present, the source is below VDD and the GMR pin does not turn on. A high on the LMR bit indicates a load-leakage fault. During a load-leakage fault, the SMR pin is biased to the voltage set by the external resistor (R_{SOL}) and a series diode to VDD. Without this path, the SMR pin is floating and may not display faults properly.

Table 5-7 lists a summary of the faults that affect the GMR pin behavior.

Table 5-7. Master Relay Fault and Operation

SYSTEM EVENT	FAULT BITS AFFECTED	TPIC7218-Q1 STATE		NOTES
		BEFORE EVENT	AFTER EVENT	
VDD Undervoltage	PORn = 1	GMR ON	GMR OFF	nRST pin is internally driven low
VBAT Overvoltage (>V_{ovVBAT})	FOV = 1	GMR ON	GMR OFF	OV_GMR = 1
VBAT Overvoltage (>V_{ovVBAT})	FOV = 1	GMR ON	GMR ON	OV_GMR = 0
VBAT Undervoltage (<V_{uvVBAT})	FUV = 1	GMR ON	GMR OFF	
Watchdog fault (must be enabled)	WDSTAT = 0, WD_FAULT = 1	GMR ON	GMR OFF	WD_EN = 1 (enabled)
nRST pin externally driven low	Erst = 1	GMR ON	GMR OFF	
Overcurrent in master relay	OCMR=1,FHSD = 1	GMR ON	GMR OFF	$OCMR_{DIS}$ = 0 (disabled)
Overcurrent in master relay	OCMR=1,FHSD = 1	GMR ON	GMR ON	$OCMR_{DIS}$ = 1 (enabled)
Short to GND on GMR, while GMR is OFF (time > t_{STGMR})	FGMR = 1,FHSD = 1	GMR OFF	GMR OFF	$FGMR_{DIS}$ = 0 (disabled), turn ON GMR
Short to GND on GMR, while GMR is ON	FGMR = 1,FHSD = 1	GMR ON	GMR OFF	$FGMR_{DIS}$ = 0 (disabled)
Short to GND on GMR, while GMR is OFF (time > t_{STGMR})	FGMR = 1,FHSD = 1	GMR OFF	GMR ON	$FGMR_{DIS}$ = 1 (enabled), turn ON GMR
Short to GND on GMR, while GMR is ON	FGMR = 1,FHSD = 1	GMR ON	GMR ON	$FGMR_{DIS}$ = 1 (enabled)
Short to GND on SMR	STGMR = 1,FHSD = 1	GMR ON	GMR OFF	$STGMR_{DIS}$ = 0 (disabled)
Short to GND on SMR	STGMR = 1,FHSD = 1	GMR ON	GMR ON	$STGMR_{DIS}$ = 1 (enabled)
GMR is turned on while Q1-Q8 on	LGMR = 1,FHSD = 1	GMR OFF	GMR OFF	$LGMR_{DIS}$ = 0 (disabled), turn ON GMR
GMR is turned on while Q1-Q8 on	LGMR = 1,FHSD = 1	GMR OFF	GMR ON	$LGMR_{DIS}$ = 1 (enabled), turn ON GMR

The high-side GMR, SMR, and DMR functionality also includes logic that facilitates system diagnostic testing. The operational status, as well as some fault conditions can be determined for both high-side drivers (HSD) and low-side drivers (LSD). Table 5-8 lists the details.

Table 5-8. High-Side Driver Logic (GMR Only)

HSD FET	LSD FETx	COMP #1 (HSDC1)	COMP #2 (HSDC2)	RESULT
ON	OFF	L	L	Normal operating condition for HSD FET
ON	OFF	H	L	HSD FET open
ON	ON	L	L	Normal operating condition for HSD and LSD FETs
ON	ON	H	L	HSD (GMR) FET in overcurrent condition
ON	ON	H	H	HSD (GMR) FET in short to ground condition
OFF	ON	H	H	Normal operating condition for LSD
OFF	ON	H	L	Open load or open LSD FETx
OFF	OFF	H	L	Normal operating condition for HSD FET
OFF	OFF	H	H	Load short to ground/LSD FETx short to ground

5.3.9 Wheel-Speed Sensing

The TPIC7218-Q1 device is capable of interfacing with industry standard Active and Intelligent wheel-speed sensors. The TPIC7218-Q1 device features an analog front end that provides power, ground, and interprets current-encoded speed and diagnostic information (Intelligent VDA sensors only) for sensors. Current thresholds can be adjusted to easily interface with most sensors. By setting a voltage on the V_{REF} pin in conjunction with an appropriate current sense resistor, R_{LOAD}, current levels through the wheel-speed sensors are evaluated according to the threshold states. Active wheel-speed sensor current pulse levels can be: undercurrent, overcurrent, wheel-speed-pulse-low (for example 7 mA), and wheel-speed-pulse-high (for example 14 mA). Intelligent wheel-speed sensor current pulse levels can be: undercurrent, overcurrent, wheel-speed-pulse-low (for example 7 mA), wheel-speed-pulse-high (for example 28 mA), and diagnostic-data-bit (for example 14 mA). Wheel-speed-pulse-low and wheel-speed-pulse-high logic state is directly interpreted to a digital voltage output for each sensor (rotational speed). Diagnostic information, diagnostic-data-bit, is directly decoded and placed in four 9-bit registers. Rotational speed information (for two sensors) is also available on high-voltage open-drain outputs. Rotational wheel-speed pulse information for any of the sensors can be MUX-ed into a digital pulse counter. This counter increments on both rising and falling edges. The 8-bit counter, along with other wheel-speed bits are available over SPI. Wheel-speed pins are also electrically protected from typical fault conditions. See Figure 5-6 for register and applications information.

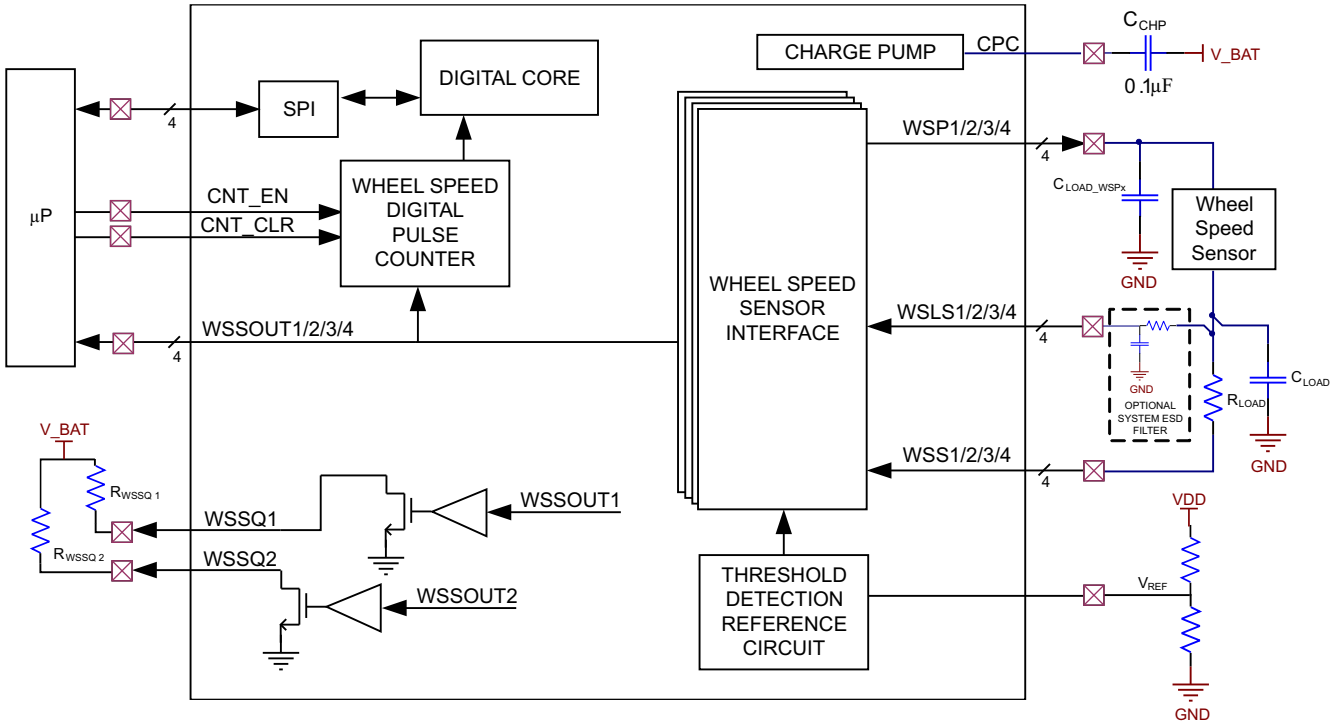


Figure 5-6. Wheel-Speed Register and Application Circuit Diagram

The TPIC7218-Q1 device has three pins for each of the four wheel-speed sensors. The WSPx pins provide a path for current from VBAT to the wheel-speed sensor. The WSLSx pins provide a path for current from the wheel-speed sensor to GND. The WSSx pins monitor current through the sensor by measuring a voltage across the R_{LOAD} resistance, shown in Figure 5-6.

Current is provided to the sensor from the WSP1, WSP2, WSP3, and WSP4 pins. When enabled (by setting the WSPx bits in register 0x1B), the WSPx pins output current and are voltage clamped to V_{clamp_WSPx}. WSPx pins are electrically protected from short-to-battery, short-to-ground, and overcurrent. Short-to-battery fault bits, WSPx_STB, are located in registers 0x08, 0x0A, 0x0C, 0x0E and overcurrent fault bits, WSPxILIMIT, are located in register 0x1D. If a fault is detected, then the WSPx pins disable. Reading these registers clears the fault bits after the fault condition has been removed.

Current from the sensors is returned to the WSP1, WSP2, WSP3, and WSP4 pins of the TPIC7218-Q1 device, thus providing a path to ground. Current out of the sensor passes through a series resistor, R_{LOAD}, into internal open-drain MOSFETs. These open-drain MOSFETs are controlled by setting the WSLSx bits in register 0x1C. The WSLSx pins are electrically protected from overcurrent by detecting an excessive voltage between WSLSx and WSSx pins. Overcurrent fault bits, $WSSx_{OC}$, are located in register 0x0F. If a fault is detected then the WSLSx pins stop sinking current. Reading these registers clears the fault bits after the fault is removed.

The sensed voltage difference between the WSSx and WSLSx pins provides the current encoded sensor information to the wheel-speed logic. The WSSx pins are electrically protected from short-to-battery and short-to-ground. These conditions are reported by reading the $WSSx_{OC}$ and $WSSx_{FAULT}$ bits in register 0x0F.

If a fault occurs on WSLSx, the path of the sensor to ground is removed. This type of fault must be cleared by following a specific procedure to prevent an overcurrent fault from being erroneously reported. To clear this fault, first disable the WSPx pins, re-enable the WSLSx pins, and finally re-enable the WSPx pins. The main purpose for this procedure is to first provide a ground path for the sensor before providing power. Other types of faults can be cleared in the normal way, as long as the WSLSx pins are enabled. Table 5-9 lists more information about wheel-speed faults.

Table 5-9. Wheel-Speed Sense Fault and Operation

SYSTEM EVENT	FAULT BITS AFFECTED	TPIC7218-Q1		NOTES
		PRIOR TO EVENT	POST EVENT	
VDD Undervoltage	PORn = 1	WSPx ON WSLSx ON WSSQx ON	WSPx OFF WSLSx OFF WSSQx OFF	All of the enable bits for these functions are cleared. nRST is driven low.
VBAT Overvoltage ($>V_{ovVBAT}$)	FOV = 1	WSPx ON WSLSx ON WSSQx ON	WSPx OFF WSLSx OFF WSSQx OFF	All of the enable bits for these functions are cleared
nRST pin externally driven low	Erst = 1	WSPx ON WSLSx ON WSSQx ON	WSPx OFF WSLSx OFF WSSQx OFF	All of the enable bits for these functions are cleared
Overcurrent in WSPx	$WSPx_{ILIMIT}$ = 1	WSPx ON WSLSx ON WSSQx ON	WSPx OFF WSLSx ON WSSQx ON	WSSQx and WSLSx remain on but no wheel-speed output is produced because the sensor has no power. The enable bits for WSPx remain 1
Overcurrent in WSSx-WSLSx	$WSSx_{OC}$ = 1	WSPx ON WSLSx ON WSSQx ON	WSPx ON WSLSx OFF WSSQx ON	WSPx and WSSQx remain on but no wheel-speed output is produced because the sensor has no ground. The enable bits for WSLSx remain 1
Overcurrent in WSSQx	$WSSQx_{ILIMIT}$ = 1	WSPx ON WSLSx ON WSSQx ON	WSPx ON WSLSx ON WSSQx OFF	WSLSx and WSPx remain on. The enable bits for WSSQx remain 1
Short to VBAT on WSPx	WSPx_VBAT = 1	WSPx OFF WSLSx ON WSSQx ON	WSPx OFF WSLSx ON WSSQx ON	This fault is detected only while WSPx are OFF. WSLSx and WSSQx remain unaffected while WSPx is on and shorted to VBAT.
Short to GND on WSLSx	$WSSx_{FAULT}$ = 1	WSPx ON WSLSx ON WSSQx ON	WSPx ON WSLSx ON WSSQx ON	WSSQx and WSPx remain on; wheel-speed outputs may be produced but the wheel-speed ground path is not through TPIC7218-Q1 anymore
Short to GND on WSSQx	$WSSQx_{FAULT}$ = 1	WSPx ON WSLSx ON WSSQx OFF	WSPx ON WSLSx ON WSSQx OFF	This fault is detected only while WSSQx are off. WSPx and WSLSx remain on and wheel-speed outputs can still be observed.

The wheel-speed internal equivalent model, shown in Figure 5-7 and Figure 5-8, describe how this functional block works. Users need only select a wheel-speed sensor, current sense resistor, R_{LOAD}, and V_{REF} voltage for basic operation. The wheel-speed functionality is designed to accommodate both Active and Intelligent sensors; the WSS_{TYPE} bit in register 0x1D must be set appropriately.

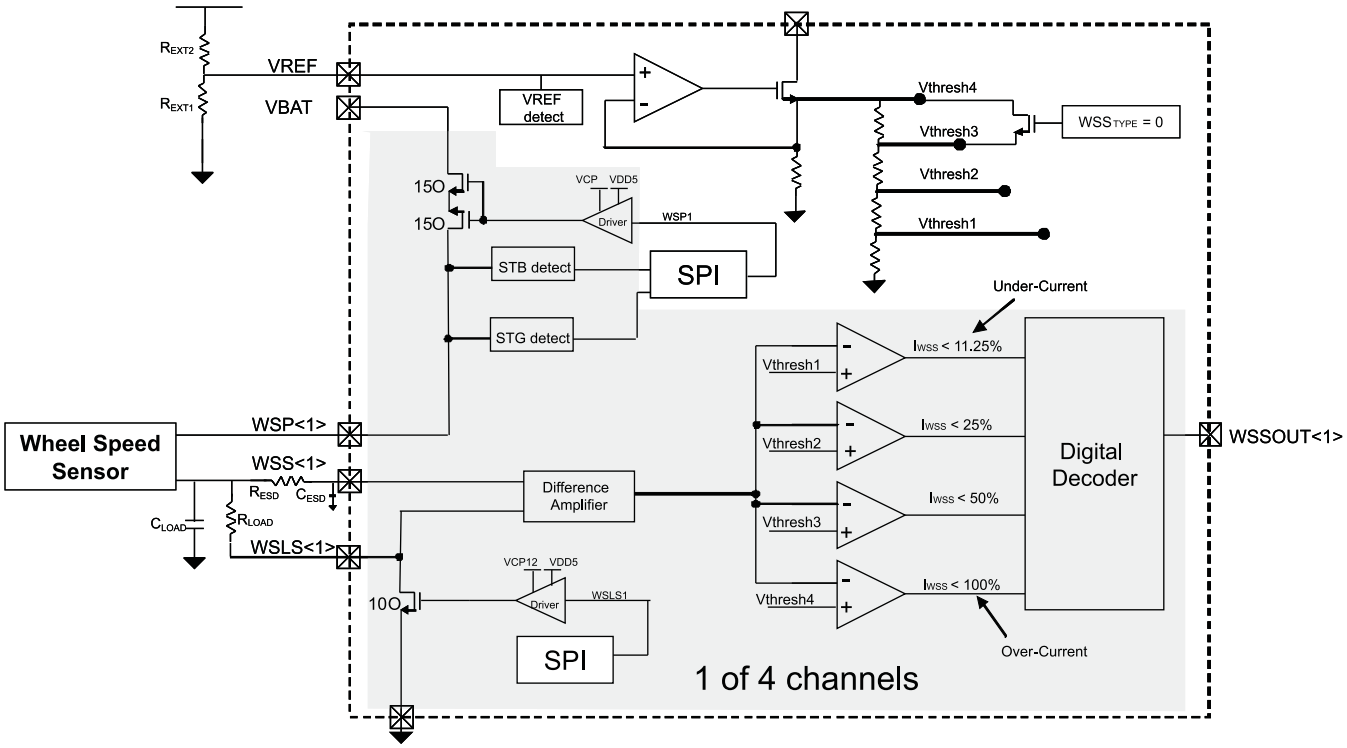


Figure 5-7. Internal Diagram Using Intelligent Type Sensor (Wss_{TYPE} = 0)

Table 5-10. Intelligent Sensor Wheel-Speed Thresholds

THRESHOLD	SIGNIFICANCE	PERCENTAGE OF MAXIMUM THRESHOLD(1)
$V_{THRESH4}$	$I_{SENSOR} > I_{THRESH4}$ Overcurrent (possible short to battery)	100% (40 mA)
$V_{THRESH3}$	$I_{THRESH4} > I_{SENSOR} > I_{THRESH3}$ Rotational Wheel-Speed Logic- High	50% (20 mA)
$V_{THRESH2}$	$I_{THRESH3} > I_{SENSOR} > I_{THRESH2}$ Diagnostic sensor Information (9-bit)	25% (10 mA)
$V_{THRESH1}$	$I_{SENSOR} < I_{THRESH1}$ Undercurrent (possible short to ground)	11.25% (4.5 mA)

(1) The current is based on maximum of 40 mA, R_{LOAD} OF 50 Ω, and V_{REF} of 2 V

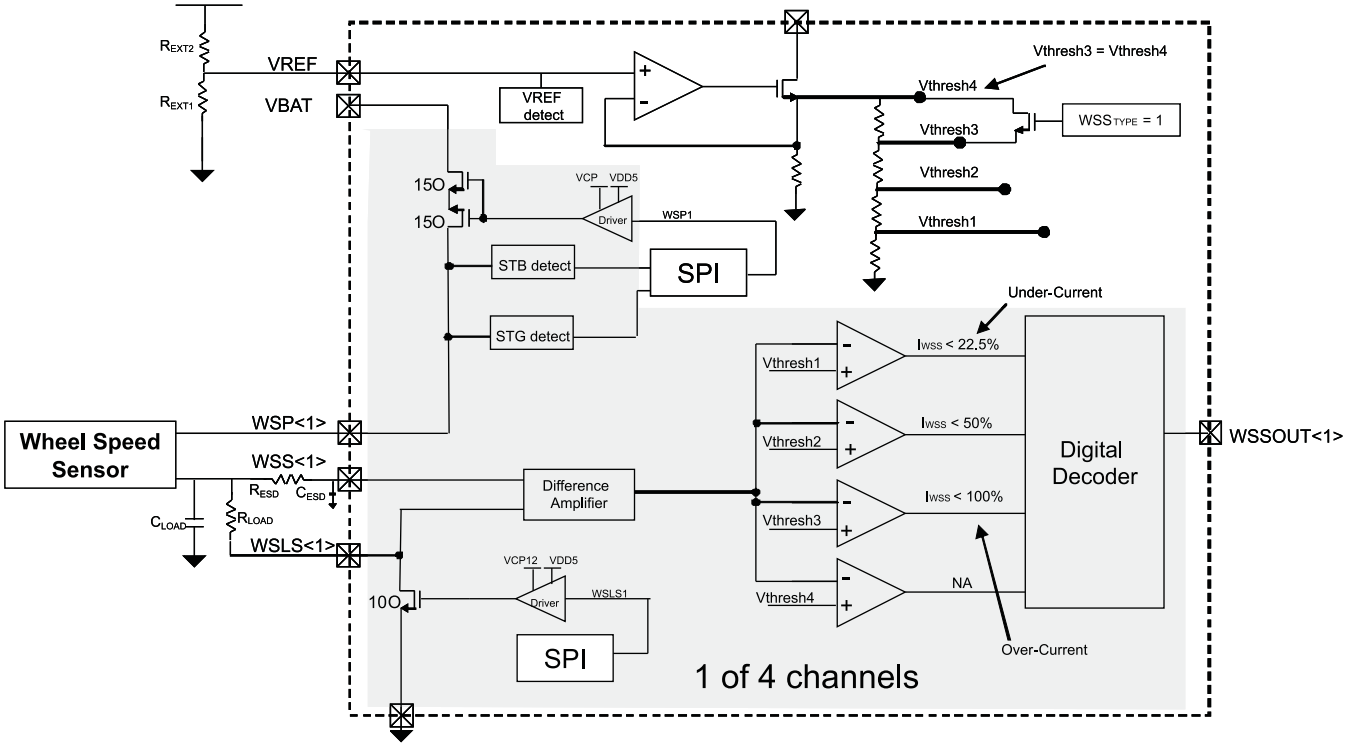


Figure 5-8. Internal Diagram Using Active Type Sensor (Wss_{TYPE} = 1)

Table 5-11. Active Sensor Wheel-Speed Thresholds

THRESHOLD	SIGNIFICANCE	PERCENTAGE OF MAXIMUM THRESHOLD(1)
$V_{THRESH4}$	$I_{SENSOR} > I_{THRESH4}$ *Not used	100% (20 mA) *Not used
$V_{THRESH3}$	$I_{SENSOR} > I_{THRESH3}$ Overcurrent (possible short to battery)	100% (20 mA)
$V_{THRESH2}$	$I_{THRESH3} > I_{SENSOR} > I_{THRESH2}$ Rotational wheel-speed logic- high	50% (10 mA)
$V_{THRESH1}$	$I_{SENSOR} < I_{THRESH1}$ Undercurrent (possible short to ground)	22.5% (4.5 mA)

(1) The current is based on maximum of 40 mA, R_{LOAD} OF 50 Ω, and V_{REF} of 2 V.

Both types of sensors provide information based on varying current levels. The TPIC7218-Q1 device provides a way to select different current thresholds by adjusting a voltage on the V_{REF} pin. Internally, the voltage on V_{REF} governs all four thresholds in a ratio metric manner. V_{REF} voltage actually sets the maximum threshold (100%), then, all the other thresholds are automatically set. Intelligent sensors require $I_{THRESH4}$ to be set to the maximum threshold, $I_{WSS(overcurrent)}$, and Active sensors require $I_{THRESH3}$ to be set to the maximum threshold. For both Intelligent sensors (requiring four thresholds) and Active sensors (requiring three thresholds) use Equation 4 to select a value for V_{REF}.

$$V_{REF} = R_{LOAD} * I_{WSS(over-current)} \quad (4)$$

For example, a typical Intelligent wheel-speed sensor may have a maximum typical current less than 40 mA. This 40-mA current must be set to correspond to $V_{THRESH4}$ (100%). If the value of R_{LOAD} is selected as 50 Ω, then the resulting V_{REF} voltage is calculated to be 2 V. Similarly, a typical Active wheel-speed sensor may have a maximum typical current less than 20 mA. This 20-mA current must be set to correspond to $V_{THRESH3}$ (100%). However, by setting the WSS_{TYPE} bit, the digital decoder uses $V_{THRESH3}$ threshold to actually determine if an overcurrent condition is occurring. By effectively removing the $V_{THRESH4}$ resistor in the comparator resistor chain, shown in Figure 5-9, a V_{REF} voltage of 2.4 V and an R_{LOAD} of 120 Ω, are needed to properly set the current thresholds. The ratio of the resistor chain did not change, however the current threshold detection levels did. See Figure 5-9 for more detail.

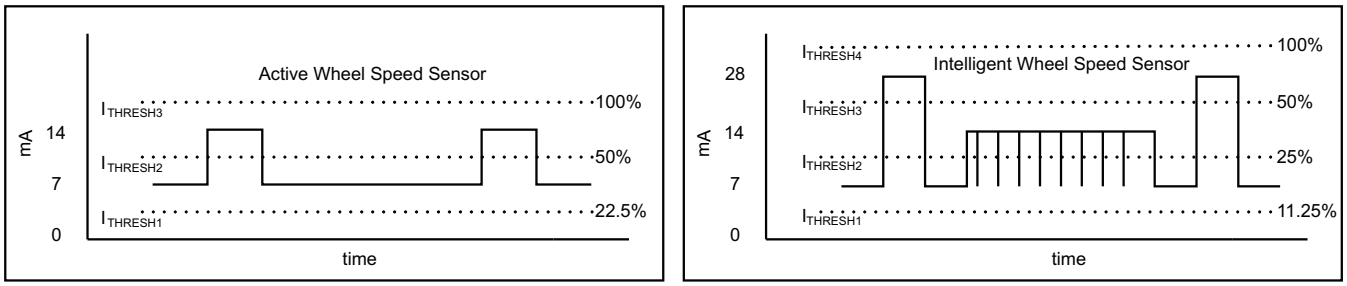


Figure 5-9. Example Wheel-Speed Current Pulse Diagram

While selecting R_{LOAD} and V_{REF}, care must be taken so that all electrical specification values are not violated. When the maximum current threshold is selected, the other three thresholds are automatically set.

During normal operation, the WSSOUTx pins provide a digital signal that is high whenever sensor current creates a voltage drop across R_{Load} that is above the $V_{THRESH3}$ level for intelligent sensors and $V_{THRESH2}$ level for Active sensors. If the current is less than these respective thresholds, the WSSOUTx pins return to ground. The WSSQ1 and WSSQ2 pins are open-drain outputs that reproduce signals on the WSSOUT1 and WSSOUT2 pins after a propagation delay time of t_{wss_delay}. A high level on WSSOUT1 or WSSOUT2 results in low level on WSSQ1 or WSSQ2 pin. These two pins are useful for providing wheel-speed information in a high voltage signal form. The WSSQ1 and WSSQ2 pins also have short-to-ground and open-load detection functionality. The $WSSQx_{FAULT}$ and $WSSQx_{ILIMIT}$ bits in register 0x05 report these faults and are cleared by reading them after the removal of the fault condition. During an overcurrent fault the WSSQ1 and WSSQ2 pins remain enabled for a time of t_{delay_WSSQx}. After this time these pins are disabled.

The TPIC7218-Q1 device also features an 8-bit wheel-speed pulse counter. This counter increments on every rising and falling edge of a selected WSSOUTx. A MUX selects which the WSSOUTx signal is input to the counter; bits WS_Cnt_MUX[1] and WS_Cnt_MUX[0] program the MUX as listed in Table 5-12. Count data is reported in register 0x04. A high on the CNT_EN pin allows the counter to increment. A high on the CNT_CLR pin forces the counter to reset to 0. The count value is available for read through SPI at any point. If the counter is allowed to reach maximum value, the count value remains at maximum but an overflow bit, WSS_OV_Cnt is set. If both CNT_CLR and CNT_EN pins are in a high logic state then the WS_Fail_Cnt bit is set. These bits clear on read after the fault conditions have been removed.

Table 5-12. Wheel-Speed Counter Input

WS_Cnt_MUX[1]	WS_Cnt_MUX[0]	SELECTED INPUT
0	0	WSSOUT1
1	0	WSSOUT2
0	1	WSSOUT3
1	1	WSSOUT4

When the TPIC7218-Q1 device is paired with VDA protocol compatible Intelligent wheel-speed sensors, additional functionality for processing and reporting diagnostic information can be enabled. Diagnostic encoded data (Manchester encoded) in the form of current pulses reaching the $I_{THRESH2}$ (10 mA) threshold are decoded and placed in the WSSxDx bits. All nine bits are available for reading. If any of the (nine) bit pulse widths were outside the allowed pulse width range (36 µs to 64 µs including variations) then the pulse widths are not counted as valid. As each of the nine bits are input, only valid bits cause the WSSx_Valid counter to increment. In this way information about bit errors, or fewer than nine bits being sent from the sensor is recorded and available for each wheel-speed channel. The TPIC7218-Q1 device also contains logic to determine when a new 9-bit frame has started to be input. When detected, the WSSx_New bit is set. If the wheel-speed sensor is in *stand still mode* then the TPIC7218-Q1 device detects this current pulse activity, resulting in the WSS_MODE bit being set. Both of these bits can be cleared upon read.

5.3.10 K-Line

The TPIC7218-Q1 device includes a serial communication transceiver for K-Line. K-Line provides a bi-directional half-duplex interface for automotive diagnostic communication with data transfer rates of up to 10.4 kbps. The integrated transceiver conforms to the ISO-9141 standard and meets the on-board diagnostic (OBD) requirements of the California Air Resources Board (CARB). For more information on the K-Line protocol see the compete K-Line standard.

Features of the K-Line module include the following:

- ISO-K operates over a wide signal voltage range and is capable of driving high currents.
- ISO-K pin can tolerate a parasitic capacitance of up to 10 nF.
- ISO-K pin is electrically protected to withstand short-to-ground and overcurrent faults.
- The driver stage of the ISO-K pin is thermally protected. A temperature fault disables the bus. Thermal protection also includes hysteresis and blank time before restarting.
- KRx and KTx directly interface to both 5-V and 3.3-V microprocessors without the need for pullup resistors.
- K-Line continues to function regardless of any TPIC7218-Q1 fault conditions with the exception of VDD undervoltage reset condition which powers down the entire TPIC7218-Q1 device.

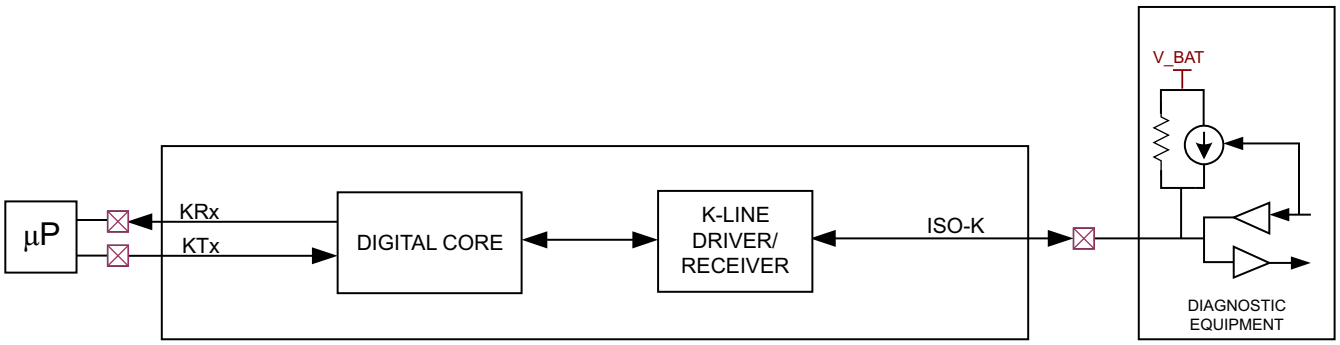


Figure 5-10. K-Line Application Schematic

5.3.11 Warning Lamp Drivers

The TPIC7218-Q1 device features three output pins for warning lamps. The WLQ1 and WLQ2 pins are high voltage low-side drivers. The WL_LS pin is a low voltage low-side driver.

The WL_LS driver enables whenever the watchdog controlled bit, WD_STAT, is high. This low-side driver is an open-drain MOSFET; to realize a high logic level and external pullup resistor must be used. Driver operation is only dependent on a watchdog fault.

The WLQ1 driver enables whenever the WLG1 pin and the GE_9 bit is set. The WLQ2 driver works in the same way utilizing the WLG2 pin and the GE_10 bit. Each driver is monitored for three fault conditions: overcurrent, open-load, and over-temperature. However, driver operation also depends on other fault conditions: VDD undervoltage, and watchdog fault. See the application circuit and register diagram in Figure 5-11.

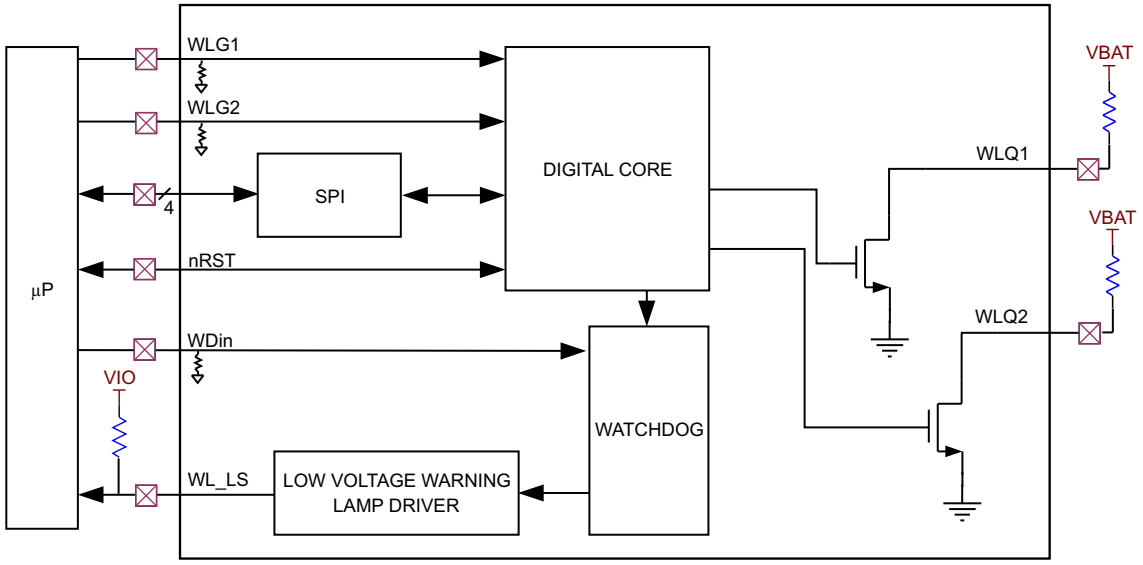


Figure 5-11. Warning Lamp Driver Register and Application Circuit Diagram

Each digital driver monitors, reports, and has integrated protection for many electrical fault conditions. Overcurrents are reported as a 1 in register 0x03, (bits 0 and 2 are referenced by bits F9, F10) and do not cause the affected driver to disable. Overcurrents are merely reported after a deglitch time of $t_{off\_blank\_WLQx}$. Over-temperature (junction) faults are reported in register 0x03, (bit-6 OTSD) and cause both drivers to disable after a deglitch time of $t_{off\_tmp\_WLQx.}$. The high-voltage warning-lamp drivers are also checked for an open-load or short to ground condition whenever they are not enabled. This type of fault causes register 0x03, (bits 1 and 3 are referenced by bits S9 and S10) to be reported as a 1. A master low-side fault bit in register 0x00, (bit-0) becomes high whenever an overcurrent or open-load fault occurs. Faults can be cleared by reading the appropriate fault reporting register. When this occurs, the low-side master fault bit (FAIL) can be cleared by reading it.

The high-voltage warning-lamp drivers also respond to fault conditions within other functional blocks. These drivers are disabled whenever the VDD undervoltage fault bit in register 0x00 is set. Also, a watchdog fault can cause these drivers to disable, if register 0x11, bit-4 (WD_EN) is set. This bit defaults to 0 upon power up. Any of these faults do not cause the FAIL bit to be set.

Faults can be cleared by reading the appropriate fault reporting register. When this occurs the digital drivers can be re-enabled. Fault reporting bits do not have any affect on these warning lamp drivers; only the actual fault condition causes a driver to disable. Nevertheless, TI recommends clearing the fault bits by reading them before enabling the drivers.

Aside from monitoring and reporting faults, the high-voltage warning-lamp drivers have overvoltage protection circuitry built in. An active-clamp monitors voltage on the pins of these drivers. Voltages larger than V_{cl_WLQx} are clamped.

5.3.12 Watchdog Operation

The TPIC7218-Q1 device also features watchdog functionality. Watchdog functionality is programmable and can be disabled. This functional block receives clock pulses from an external microprocessor through WDIN pin to verify proper system operation. Whenever a watchdog fault occurs, the low-voltage warning-lamp pin (WL_LS), the reset pin (nRST), and many of the other functional blocks within the TPIC7218-Q1 device are affected. The TPIC7218-Q1 device can be set to accept a range of different pulse widths for easy connection to most microprocessors.

If watchdog functionality is enabled (WD_EN = 1), the TPIC7218-Q1 logic monitors WDIN pulse widths by counting the number of internal clocks that occur between WDIN rising and falling edges. Two, 2-bit values (WDH<1:0>, WDL<1:0>) can be adjusted to select the length of a valid window range for a WDIN pulse. Pulse widths inside of this window range are counted as a *good pulse*. A good pulse increments a 3-bit state machine counter by one (WDCNTx bits, in register 0x05). When a counter value of 7 is reached, the status bit, WDSTAT , becomes a 1 and all TPIC7218-Q1 watchdog inhibited functionality is enabled. If a *bad pulse* occurs then the state machine counter is decremented by three. The WD_FAULT bit is set whenever the counter value is 0, causing the WD_STAT bit to become low. A fault turns off high-side drivers, low-side drivers, wheel-speed functionality, and high-voltage warning-lamp drivers. Both the low-voltage warning-lamp driver (WL_LS) and the reset pin (nRST) enables. The SPI continues to function and the WD_FAULT and WDSTAT bits indicate a watchdog fault. When a full watchdog count is reached, register bits and functionality would return to normal state. Refer to Figure 5-12 through Figure 5-14 for more details on the state transitions and timing.

If the WDIN pin does not realize a transition after twice the length of time selected in the upper window, which is set by bits WDH<1:0>, then an out-of-range condition occurs. The watchdog fault becomes high and the watchdog status bit becomes low (WD_FAULT = 1, and WDSTAT = 0).

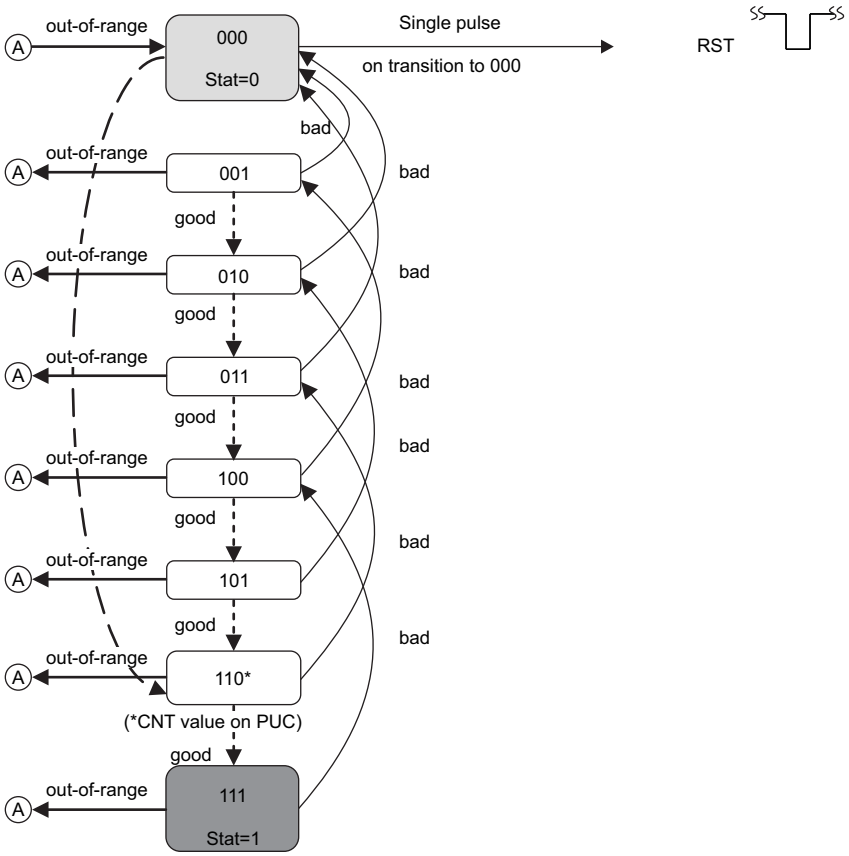


Figure 5-12. Watchdog State Transition Diagram

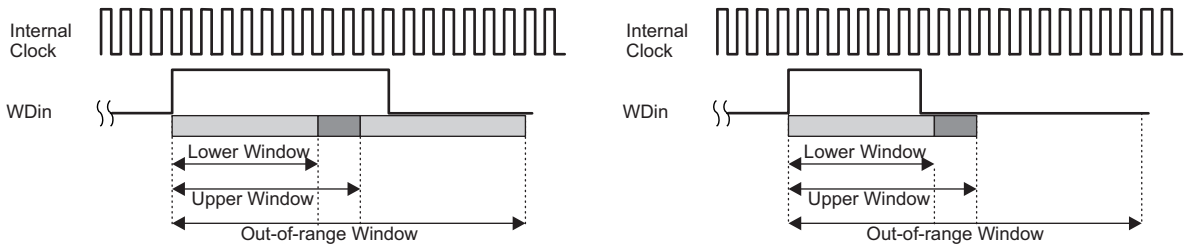


Figure 5-13. Timing Diagram Showing A Bad Pulse

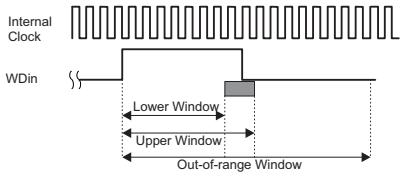


Figure 5-14. Timing Diagram Showing A Good Pulse

5.4 Device Functional Modes

The device operates in normal mode as described in **Section 5.3** unless it is in the reset state.

5.4.1 Device Reset

Several events cause the TPIC7218-Q1 device to reset. For a compete view of TPIC7218-Q1 behavior during reset, refer to Table 5-1.

Power-On Reset A power-on reset, POR, is caused when the VDD supply voltage falls below the reset threshold. On POR the nRST pin is pulled low by the TPIC7218-Q1 device.

Watchdog Reset A watchdog reset is initiated whenever the Watchdog counter decrements to 000. Upon Watchdog Reset, the nRST pin is pulsed low, and the WDSTAT flag is cleared. As the nRST pin is released, the Watchdog state machine is restarted. The watchdog will re-enable after a delay time T_{WD_PULSE} to allow sufficient time for the microcontroller to reset.

External Reset An external reset is realized whenever the nRST pin is driven low by an external signal (usually from a microprocessor). When nRST is released the Erst bit is set, indicating that an external reset occurred.

5.5 Programming

5.5.1 Serial Peripheral Interface (SPI) Interface To Microcontroller

The TPIC7218-Q1 device uses a SPI communication interface. The TPIC7218-Q1 device operates as a slave with full-duplex, synchronous, 8-bit transfer frames. The device can be controlled and monitored in one of three modes: Read, Write, and Dummy. Read command returns data to the master. If a fault register is read, then any faults will be cleared. However, if the fault still exists then the fault reporting bit(s) will remain high. A write command sends data to the slave. Data is latched in on the rising edge of the second chip select. A dummy command is used whenever the master and slave loose synchronization. This happens whenever the master does not issue a normal 16 bit transfer using two eight bit frames. Dummy commands essentially reset the SPI logic to the default state.

A typical SPI operation contains two full chip select frames; each containing eight clock pulses. All SPI transaction starts when CSN transitions to a logic low. During this time 8-bits of mode, R/W, and address data are clocked into SI. Finally, the CSN returns high, concluding the first half of the normal transaction. The second half of the normal transaction starts when CSN again transitions to a logic low. During this time 8-bits of data are clocked into SI. Finally, the CSN returns high, and a normal SPI transaction is concluded. If one chip-select frame does not have exactly eight clocks, then the whole 16-bit transaction is considered invalid and is ignored. The CSN must go high for a window of 2 µs to 28 µs ($CSN_{timeout}$) between two 8-bit commands for the 16-bit command to be considered valid. A 16-bit read command consists of an 8-bit read command of the intended address and an 8-bit dummy command. The SPI can also operate in burst mode, whereby consecutive 8-bit read commands result in a consecutive 8-bit data being returned to the master.

Table 5-13. SPI Instruction Encoding

MODE	R/W_n	STAT.	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
Unused	0	1	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
Read	1	0	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
Write	0	0	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
Dummy	1	1	X	X	X	X	X	X

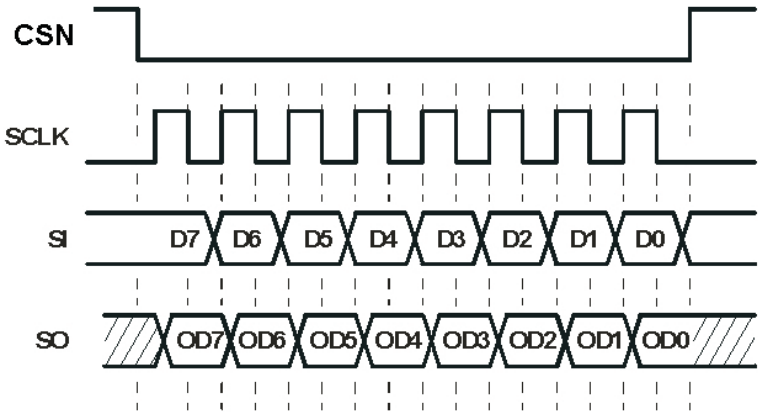


Figure 5-15. One Chip-Select Frame

The SO pin contains the register data in response to the previous eight bit frame. Data out is always delayed by one SPI transfer (for example, response to the command N is shifted out at the same time command N+1 is shifted in). Valid data is shifted out from the SO pin on the rising edge of SCLK. The response to the SPI frame depends on which type of transaction mode is requested by the Master (read, write, or dummy).

If the SPI transaction is valid, the Slave determines what type of operation is being requested. If a Read transaction is requested, the Slave responds with the Read byte during the next SPI transaction. Figure 5-16 shows the SPI Read operation.

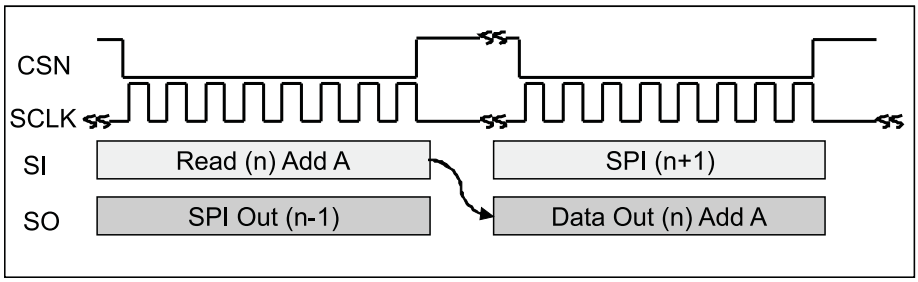


Figure 5-16. One Chip-Select Frame

A Write operation places the data byte into the address specified in the previous chip select frame.

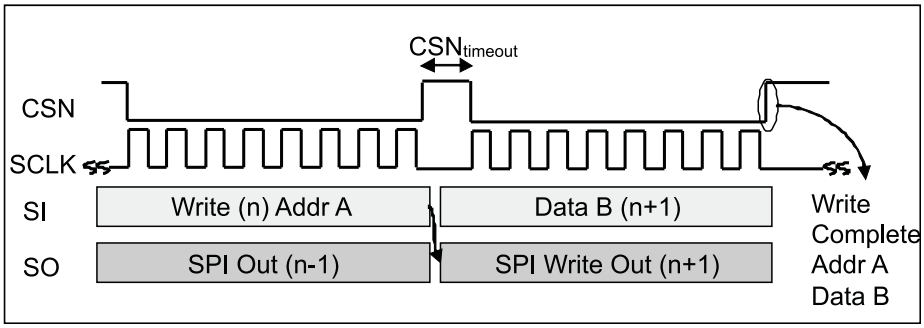


Figure 5-17. One Chip-Select Frame

5.5.1.1 Summary and Description Of Control and Reporting Registers

The TPIC7218-Q1 device contains 30 registers that contain both fault reporting and control bits. Refer to the following tables for register map and functional description of each bit.

5.6 Register Maps

5.6.1 SPI Registers

Table 5-14. SPI Registers Map

ADDRESS	R/W	b7	b6	b5	b4	b3	b2	b1	b0
0x00	R	HSDC2	FHSD	FOV	FUV	Erst	HSDC1	PORn	FAIL
0x01	R	S4	F4	S3	F3	S2	F2	S1	F1
0x02	R	S8	F8	S7	F7	S6	F6	S5	F5
0x03	R	WS_OV_Cnt	OTSD	WS_Fail_Cnt	KI	S10	F10	S9	F9
0x04	R	WS_Cnt_OUT7	WS_Cnt_OUT6	WS_Cnt_OUT5	WS_Cnt_OUT4	WS_Cnt_OUT3	WS_Cnt_OUT2	WS_Cnt_OUT1	WS_Cnt_OUT0
0x05	R	$WSSQ2_{ILIMIT}$	$WSSQ1_{ILIMIT}$	$WSSQ2_{FAULT}$	$WSSQ1_{FAULT}$	WDSTAT	WDCNT2	WDCNT1	WDCNT0
0x06	R	VLD_{DEG}	OCPR	STGPR	FGPR	LMR	FGMR	STGMR	OCMR
0x07	R	WSS1D7	WSS1D6	WSS1D5	WSS1D4	WSS1D3	WSS1D2	WSS1D1	WSS1D0
0x08	R	WSS1_Valid3	WSS1_Valid2	WSS1_Valid1	WSS1_Valid0	WSP1_STB	WSS1_Mode	WSS1_New	WSS1D8
0x09	R	WSS2D7	WSS2D6	WSS2D5	WSS2D4	WSS2D3	WSS2D2	WSS2D1	WSS2D0
0x0A	R	WSS2_Valid3	WSS2_Valid2	WSS2_Valid1	WSS2_Valid0	WSP2_STB	WSS2_Mode	WSS2_New	WSS2D8
0x0B	R	WSS3D7	WSS3D6	WSS3D5	WSS3D4	WSS3D3	WSS3D2	WSS3D1	WSS3D0
0x0C	R	WSS3_Valid3	WSS3_Valid2	WSS3_Valid1	WSS3_Valid0	WSP3_STB	WSS3_Mode	WSS3_New	WSS3D8
0x0D	R	WSS4D7	WSS4D6	WSS4D5	WSS4D4	WSS4D3	WSS4D2	WSS4D1	WSS4D0
0x0E	R	WSS4_Valid3	WSS4_Valid2	WSS4_Valid1	WSS4_Valid0	WSP4_STB	WSS4_Mode	WSS4_New	WSS4D8
0x0F	R	$WSS4_{OC}$	$WSS3_{OC}$	$WSS2_{OC}$	$WSS1_{OC}$	$WSS4_{FAULT}$	$WSS3_{FAULT}$	$WSS2_{FAULT}$	$WSS1_{FAULT}$
0x10	RW	GE8	GE7	GE6	GE5	GE4	GE3	GE2	GE1
0x11	RW	WD_Fault	0	OV_GMR	WD_EN	GE_PR	GE_MR	GE10	GE9
0x12	RW	WDH<1>	WDH<0>	WDL<1>	WDL<0>	PWM_{Freq1}	PWM_{Freq0}	WS_Cnt _MUX[1]	WS_Cnt _MUX[0]
0x13	RW	$PWM_{Q5<7>}$	$PWM_{Q5<6>}$	$PWM_{Q5<5>}$	$PWM_{Q5<4>}$	$PWM_{Q5<3>}$	$PWM_{Q5<2>}$	$PWM_{Q5<1>}$	$PWM_{Q5<0>}$
0x14	RW	0	0	0	0	$PWMQ5_{Phase<1>}$	$PWMQ5_{Phase<0>}$	$PWM_{Q5<9>}$	$PWM_{Q5<8>}$
0x15	RW	$PWM_{Q6<7>}$	$PWM_{Q6<6>}$	$PWM_{Q6<5>}$	$PWM_{Q6<4>}$	$PWM_{Q6<3>}$	$PWM_{Q6<2>}$	$PWM_{Q6<1>}$	$PWM_{Q6<0>}$
0x16	RW	0	0	0	0	$PWMQ6_{Phase<1>}$	$PWMQ6_{Phase<0>}$	$PWM_{Q6<9>}$	$PWM_{Q6<8>}$
0x17	RW	$PWM_{Q7<7>}$	$PWM_{Q7<6>}$	$PWM_{Q7<5>}$	$PWM_{Q7<4>}$	PWM_{Q7}<3>	$PWM_{Q7<2>}$	$PWM_{Q7<1>}$	$PWM_{Q7<0>}$
0x18	RW	0	0	0	0	$PWMQ7_{Phase<1>}$	$PWMQ7_{Phase<0>}$	$PWM_{Q7<9>}$	$PWM_{Q7<8>}$
0x19	RW	$PWM_{Q8<7>}$	$PWM_{Q8<6>}$	$PWM_{Q8<5>}$	$PWM4_{Q8<4>}$	PWM_{Q8}<3>	PWMQ8<2>	$PWM_{Q8<1>}$	$PWM_{Q8<0>}$
0x1A	RW	0	0	0	0	$PWMQ8_{Phase<1>}$	$PWMQ8_{Phase<0>}$	$PWM_{Q8<9>}$	$PWM_{Q8<8>}$
0x1B	RW	0	WSSP4	WSSP3	WSSP2	WSSP1	WSS_{TYPE}	WSSQ2	WSSQ1
0x1C	RW	$OCPR_{DIS}$	$STGPR_{DIS}$	$OCMR_{DIS}$	$STGMR_{DIS}$	WSLS4	WSLS3	WSLS2	WSLS1
0x1D	RW/R*	$VREF_{OK}$*	$FGPR_{DIS}$	$FGMR_{DIS}$	LMR_{DIS}	$WSP4_{ILIMIT}$	$WSP3_{ILIMIT}$*	$WSP2_{ILIMIT}$*	$WSP1_{ILIMIT}$*

Table 5-15. Description Of Control and Reporting Bits

BIT NAME	DESCRIPTION
Fail	Any fault on any digital or PWM low-side driver 0 = Fault not detected 1 = Fault detected
PORn	Power-on reset. Reset low when read by microcontroller. 0 = No power-on reset detected. Reset to this value when read by microcontroller. 1 = Power-on reset detected
HSDC1	High-side driver comparator1 for Master Relay (MR) 0 = Comparator output low 1 = Comparator output high
Erst	RST pin is pulled low by external source 0 = Fault not detected 1 = Fault detected
Fuv	Undervoltage on V_{BAT} 0 = Fault not detected 1 = Fault detected
Fov	Overvoltage on VBAT 0 = Fault not detected 1 = Fault detected
FHSD	Any fault on the high-side drivers (either GMR or GPR). If set, this bit is latched until Address 6 is read. Then, it clears on read. 0 = Fault not detected 1 = Fault detected
HSDC2	High-side driver comparator 2 for Master Relay (MR) 0 = Comparator output low 1 = Comparator output high
Sx	Open-load fault on the low-side output (S9 reports WLQ1 fault and S10 reports WLQ2 fault) 0 = Fault not detected on output x 1 = Fault detected on output x
Fx	Short-to-battery fault on the low-side output (F9 reports WLQ1 fault and F10 reports WLQ2 fault) 0 = Fault not detected on output x 1 = Fault detected on output x
WS_Fail_Cnt	CNT_EN and CNT_CLR set at the same time 0 = Fault not detected 1 = Fault detected
KI	Status bit for Kline current limit condition 0 = Fault not detected 1 = Fault detected
OTSD	Any overtemperature fault 0 = Fault not detected 1 = Fault detected
WS_OV_Cnt	Count overflow on the wheel-speed sensor (past 256) 0 = Overflow not detected 1 = Overflow detected

Table 5-15. Description Of Control and Reporting Bits (continued)

BIT NAME	DESCRIPTION
WSSx_Valid4 WSSx_Valid3 WSSx_Valid2 WSSx_Valid1	This word shows the valid number of bits in each wheel-speed channel.
WDCNT0	Status Bit 1 of three that is used to track the operation of the watchdog circuit (LSB)
WDCNT1	Status Bit 2 of three that is used to track the operation of the watchdog circuit
WDCNT2	Status Bit 3 of three that is used to track the operation of the watchdog circuit (MSB)
WDSTAT	Watchdog status bit 0 = Out-of-range 1 = In-range
$WSSQ1_{FAULT}$	Open load or short to ground on WSSQ1 0 = Fault not detected 1 = Fault detected
$WSSQ2_{FAULT}$	Open load or short to ground on WSSQ2 0 = Fault not detected 1 = Fault detected
$WSSQ1_{ILIMIT}$	Overcurrent on WSSQ1 0 = Fault not detected 1 = Fault detected
$WSSQ2_{ILIMIT}$	Overcurrent on WSSQ2 0 = Fault not detected 1 = Fault detected
OCMR	Overcurrent fault on MR 0 = Fault not detected 1 = Fault detected
STGMR	Short-to-ground fault on MR 0 = Fault not detected 1 = Fault detected
FGMR	GMR disabled by external circuitry 0 = GMR not disabled 1 = GMR disabled
LMR	Load-leakage fault on MR (Master Relay) 0 = Fault not detected 1 = Fault detected
FGPR	GPR disabled by external circuitry 0 = GPR not disabled 1 = GPR disabled
STGPR	Short-to-ground fault on PR 0 = Fault not detected 1 = Fault detected
OCPR	Overcurrent fault on PR 0 = Fault not detected 1 = Fault detected
VLD_{DEG}	This bit is a replica of FOV
WSS1Dx	VDA data bits for wheel-speed channel 1

Table 5-15. Description Of Control and Reporting Bits (continued)

BIT NAME	DESCRIPTION
WSS2Dx	VDA data bits for wheel-speed channel 2
WSS3Dx	VDA data bits for wheel-speed channel 3
WSS4Dx	VDA data bits for wheel-speed channel 4
WSSx_New	Flag bits that notify the availability of new data for each sensor channel 1 = new data since last read was performed 0 = old data since last read was performed
WSSx_Mode	Flag bits that notify the mode of operation for each sensor channel 1 = standstill mode 0 = normal mode
WSPx_STB	Flag bits that show a short to battery for each sensor channel in the off state 1 = short to battery 0 = normal operation
WS_Cnt_OUT7	Bit 7 of wheel-speed counter (value latched at CSN low-to-high transition)
WS_Cnt_OUT6	Bit 6 of wheel-speed counter
WS_Cnt_OUT5	Bit 5 of wheel-speed counter
WS_Cnt_OUT4	Bit 4 of wheel-speed counter
WS_Cnt_OUT3	Bit 3 of wheel-speed counter
WS_Cnt_OUT2	Bit 2 of wheel-speed counter
WS_Cnt_OUT1	Bit 1 of wheel-speed counter
WS_Cnt_OUT0	Bit 0 of wheel-speed counter
$WSSx_{FAULT}$	Open load or short to ground on WSSx pins 0 = Fault not detected 1 = Fault detected
$WSSx_{OC}$	Overcurrent fault on WSSx pins 0 = Fault not detected 1 = Fault detected
GE1	Enable and disable digital driver 1. It does not clear on Q1 fault
GE2	Enable and disable digital driver 2. It does not clear on Q2 fault
GE3	Enable and disable digital driver 3. It does not clear on Q3 fault
GE4	Enable and disable digital driver 4. It does not clear on Q4 fault
GE5	Enable and disable digital driver 5. It does not clear on Q5 fault
GE6	Enable and disable digital driver 6. It does not clear on Q6 fault
GE7	Enable and disable digital driver 7. It does not clear on Q7 fault
GE8	Enable and disable digital driver 8. It does not clear on Q8 fault
GE9	Enable and disable warning lamp driver 1. It does not clear on WLQ1 fault
GE10	Enable and disable warning lamp driver 2. It does not clear on WLQ2 fault
GE_MR	Enable and disable Master Relay (GMR). It clears on fault
GE_PR	Enable and disable pump motor relay (GPR). It clears on fault
WD_EN	Watchdog state machine enable. 1 = Enabled; Q1-Q8, GMR, GPR cannot be turned on unless WDSTAT =1 0 = Disabled; Q1-Q8, GMR, GPR can be controlled independent of WDstat. (WDSTAT =0 when WD_EN=0)
OV_GMR	Configure the response of GMR FET during overvoltage condition 0 = Maintain the previous state 1 = Disable GMR FET

Table 5-15. Description Of Control and Reporting Bits (continued)

BIT NAME	DESCRIPTION
WD_FAULT	Status bit that latches the watchdog fault WDSTAT=0. It clears on read and it is a read only bit 1 = watchdog fault has happened (WDSTAT =0) 0 = no watchdog fault has happened (WDSTAT =1)
WS_Cnt_MUX1 WS_Cnt_MUX0	Control bit 1 for wheel-speed sensor multiplexer Control bit 0 for wheel-speed sensor multiplexer
$PWM_{Freq<1:0>}$	Control bits to set the PWM frequency
WDH<1:0>	Control bits to set the watchdog upper window range 00 = 64 ms 01 = 32 ms 10 = 16 ms 11 = 8 ms
WDL<1:0>	Control bits to set the watchdog lower window range 00 = 32 ms 01 = 16 ms 10 = 8 ms 11 = 4 ms
$PWM_{Qx<9:0>}$	Control bits to set the duty cycle of each PWM channel. When changing from one duty cycle setting to another, the new setting takes place in the next period.
$PWMQx_{Phase<1:0>}$	Control bits to set the phase shift for the PWM drivers 00=0° 01=90° 10=180° 11=270°
WSSQ1	Enable and disable wheel-speed output WSSQ1. It clears only on VBAT overvoltage fault
WSSQ2	Enable and disable wheel-speed output WSSQ1. It clears only on VBAT overvoltage fault
WSS_{TYPE}	Type of sensor used 1 = Active 0 = Intelligent
WSPx	Control bit for the supply of the wheel-speed sensor. It clears only on VBAT overvoltage fault 1 = ON 0 = OFF
WSLSx	Control bit for the supply return of the wheel-speed sensor. It clears only on VBAT overvoltage fault 1 = ON 0 = OFF
$STGMR_{DIS}$	Enable and disable MR short-to-ground protection (STGMR) 0 = Disabled (default after reset) 1 = Enabled
$OCMR_{DIS}$	Enable and disable MR overcurrent protection (OCMR) 0 = Disabled (default after reset) 1 = Enabled
$STGPR_{DIS}$	Enable and disable PR short-to-ground protection (STGPR) 0 = Disabled (default after reset) 1 = Enabled
$OCPR_{DIS}$	Enable and disable PR overcurrent protection (OCPR) 0 = Disabled (default after reset) 1 = Enabled

Table 5-15. Description Of Control and Reporting Bits (continued)

BIT NAME	DESCRIPTION
$WSPx_{ILIMIT}$	Current limit fault on WSPx pins (read only bits) 0 = Fault not detected 1 = Fault detected
LMR_{DIS}	Enable and disable MR leakage protection (LMR) 0 = Disabled (default after reset) 1 = Enabled
$VREF_{OK}$	Status bit that indicates if V_{REF} pin is more than 0.75 V (read only) 0 = V_{REF} pin is less than 0.75 V 1 = V_{REF} pin is more than 0.75 V

6 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The TPIC7218-Q1 device, as typically used in anti-lock braking systems, requires very few external components; thus, the design is quite simple.

6.2 Typical Application

A simplified application diagram of the TPIC7218-Q1 device Figure 6-1 shows a simplified application diagram.

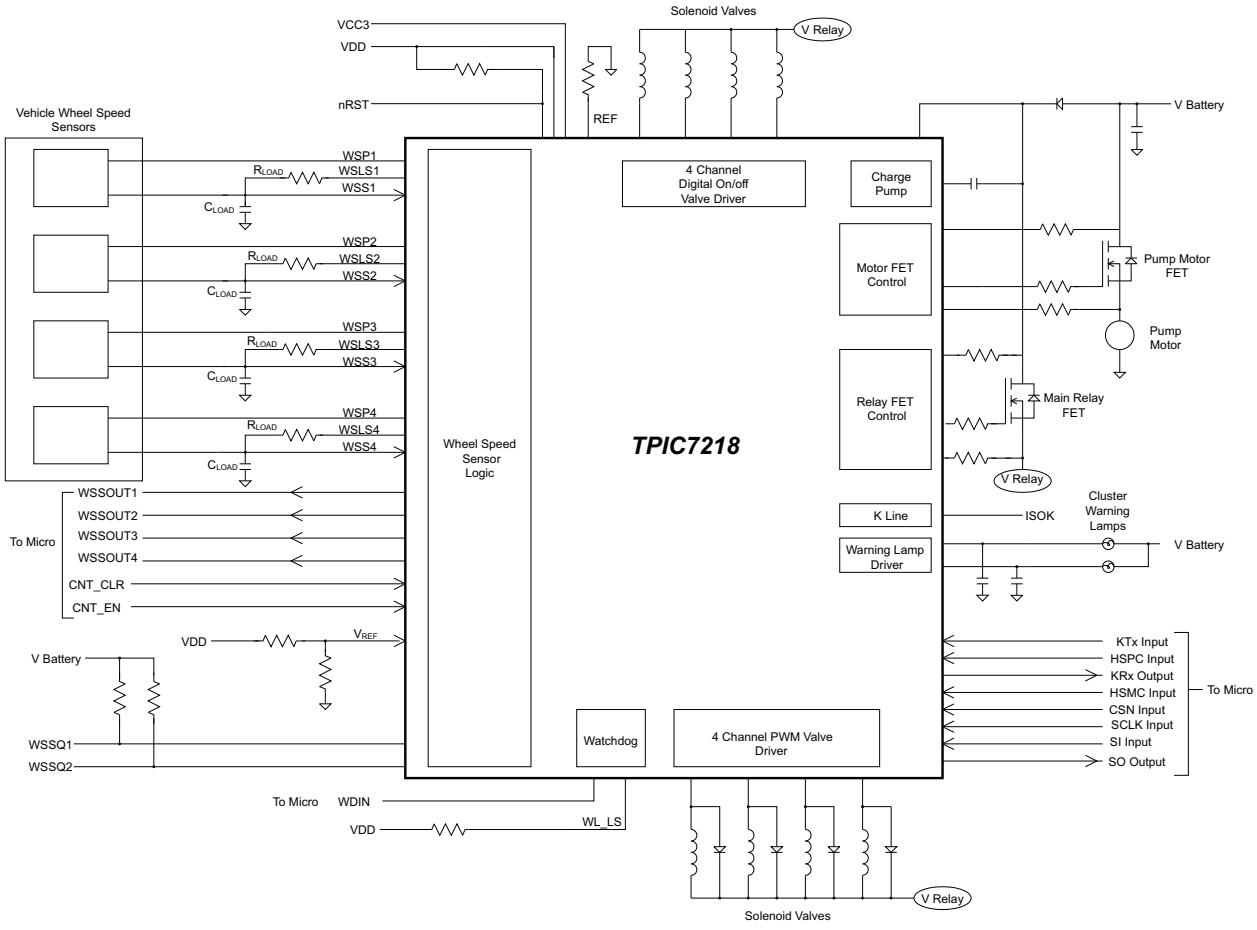


Figure 6-1. Simplified Application Diagram

6.2.1 Design Requirements

The design of the components needed for the wheel speed sensor interface (VREF voltage and R_{LOAD}) is described in Section 5.3.9. The only other major design requirement is in choice of the resistors connected to pins controlling the pump relay (PR) and main relay (MR) FETs as shown in Figure 6-2. The choice of these resistors is described in Section 6.2.2.

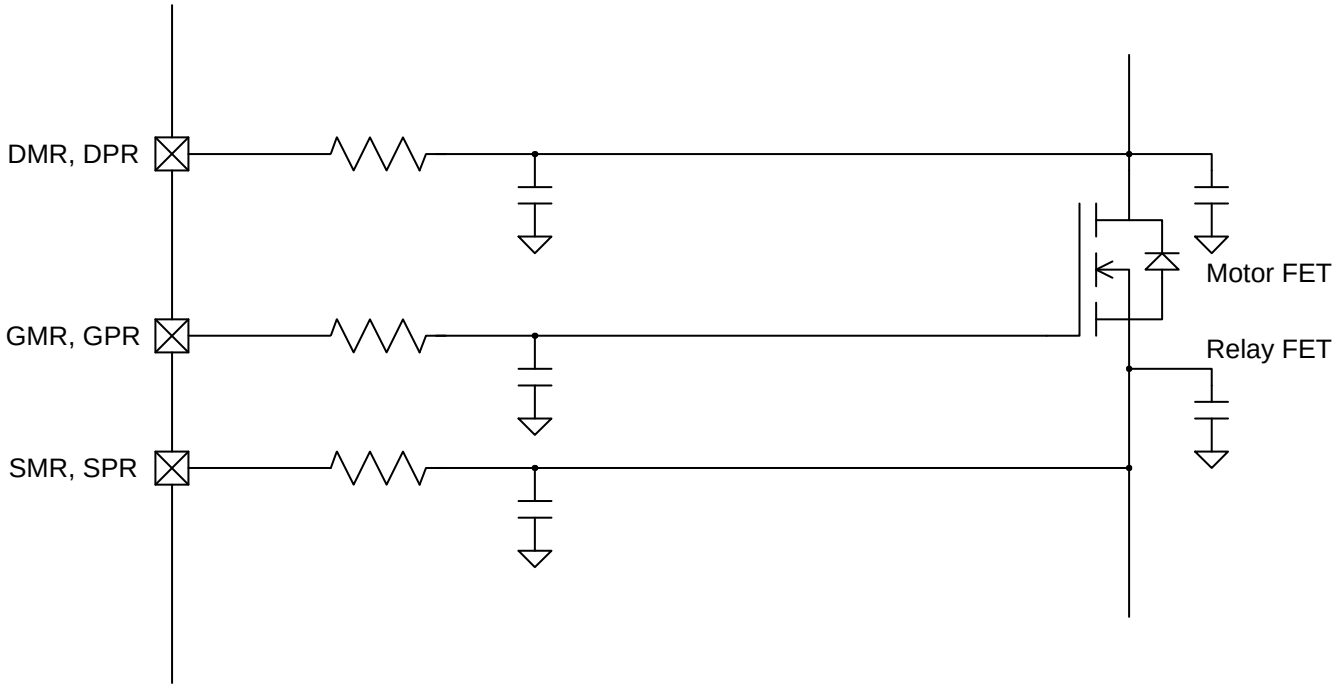


Figure 6-2. xPR and xMR Resistors in Application Diagram

6.2.2 Detailed Design Procedure

The resistor R_{DMR} is to be chosen based on the overcurrent detection value needed for the system relay and pump relay as explained in Section 5.3.8. R_{SMR} resistor value to be chosen to limit the current into the pin in a reverse battery situation - typically in the 1- to 2-kΩ range. See Section 6.2.2.1 for description of the GMR and GPR resistor design procedure.

6.2.2.1 Gatedrive circuit Motor FET

When the pump relay driver at the GPR pin is enabled, it is charged in three different ways. The internal pre-GPR node is shorted to the VBAT supply to give it battery voltage. There are also two current sources that are then enabled at the same time, I_{DC_GPR} and I_{TRAN_GPR} as shown in Figure 6-3. The I_{DC_GPR} current is on any time the pump relay is turned ON. The I_{TRAN_GPR} current source is only enabled for a time t_{STGPR} after the GPR is turned on. The final voltage will not exceed CHP. The maximum charging time can be obtained from the electrical characteristics table. The turnon time is set by the charging currents with the gate resistor not affecting it significantly. A typical turnon timing characteristic is shown in Figure 6-4, in this case with the IPB 80N06S3L-06 chosen as the pump relay FET.

When the pump relay driver is set to the off state all of the charging paths are disabled and the GPR pin is shorted to GND. The external gate resistance is the primary determinant of the turnoff time. The gate resistor should be sized based on the gate characteristics of the chosen FET and the desired turnoff time. A typical turnoff characteristic with a 10-kΩ resistor is shown in Figure 6-5.

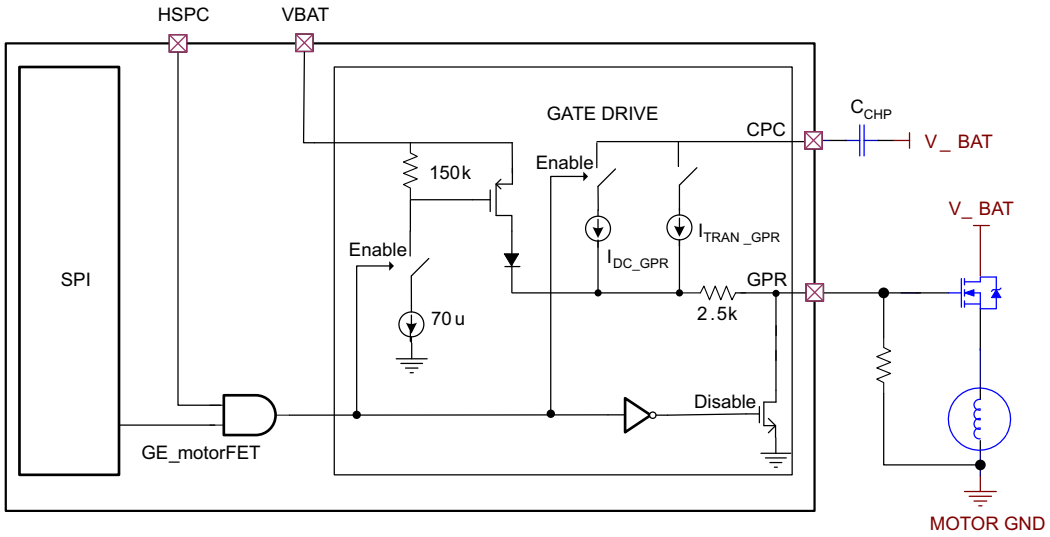


Figure 6-3. Pump Relay Gatedriver Circuit

6.2.2.2 Gatedrive circuit Master Relay FET

The circuit used for the gate drive for the master relay FET is similar to the pump motor FET gatedrive with changes in the drive strength as reflected in the turnon times from the electrical characteristics table. The gate resistor for the master relay FET should be chosen using the same procedure as for the pump motor relay driver.

6.2.3 Application Curves

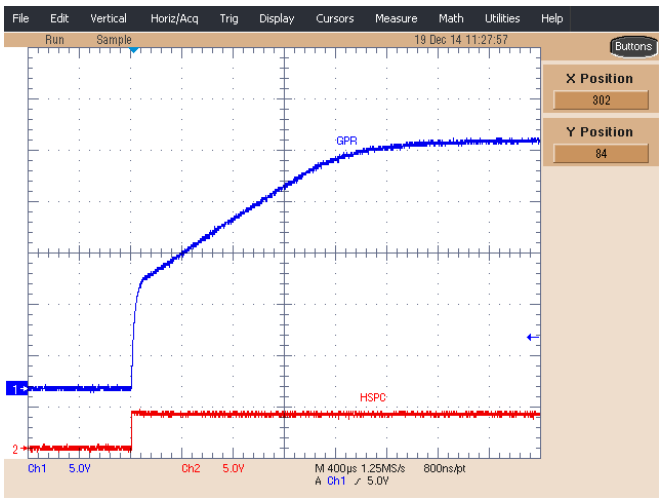


Figure 6-4. Turnon of the FET Gate With a 10-kΩ Gate Resistor.

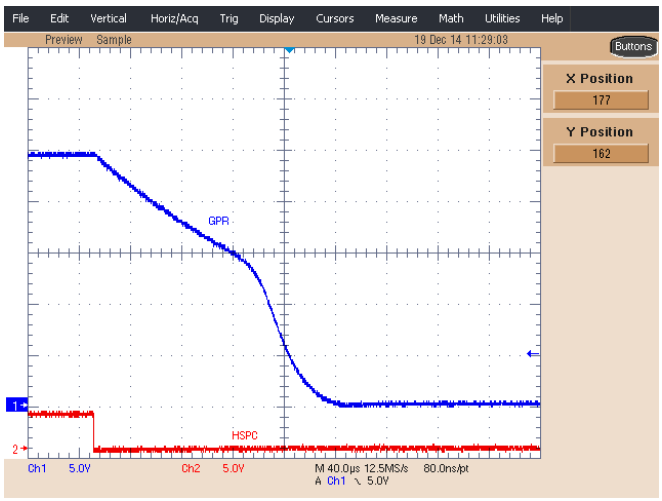


Figure 6-5. Turnon of the FET Gate With a 10-kΩ Gate Resistor.

7 Power Supply Recommendations

The TPIC7218-Q1 device requires three power supply input pins – (1) VBAT connected to the automotive battery, (2) VDD connected to a 5-V regulated output from the battery and (3) VIO which can be optionally connected to VDD or a 3.3-V regulated output. TI recommends that all power supply pins have decoupling capacitors. Use good circuit board layout techniques to ensure each capacitor provides instantaneous peak current to the TPIC7218-Q1 device. Care must be taken to avoid parasitic impedances which can degrade decoupling performance. Poorly decoupled power pins are likely to cause unsatisfactory EMC performance. TI recommends the following capacitor values:

- VBAT: recommended, 0.1 µF, X7R, 10%
- VDD: recommended, 0.1 µF, X7R, 10%
- VCC3: required, 100 pF, X7R, 10%

8 Layout

8.1 Layout Guidelines

8.1.1 Local Grounding Configuration

Route the ground pins 6, 24, 29, 30, 31, 32, 37, 63, 64, 69, 70, 71, 72 and 77 directly inward to pad. Maximize plane area under the TPIC7218-Q1 device to be consistent with PCB design rules. Ensure proper relief features for soldering thermal pad to plated through holes.

Add additional plated through holes as shown in the sketch to minimize loop area for ground return currents. See Figure 8-1 for more information.

8.1.2 Board Level Grounding Configuration, TPIC7218-Q1 to System Connector

Ideally the inner PCB layer under the TPIC7218-Q1 device should be dedicated as plane ground, with direct connection to wiring connector pin to vehicle ground. The layer should cover entire PCB area, with only clearance holes for vias and so forth. No breaks or divisions. See Figure 8-2 for more information.

8.1.3 VCC3 Bypass Capacitor

Place 0402 package bypass capacitor for VCC3 node to ground as close as possible to the TPIC7218-Q1 device, absolute minimum loop width and trace length. Do not connect ground side of capacitor to any plane; tie it directly with top layer trace to pin 6 as shown in Figure 8-3. Close placement, minimum loop area is a priority.

8.1.4 VDD Bypass Capacitor

VDD bypass capacitor needs to be close to the TPIC7218-Q1 device, but not as critical as VCC3 cap. The orientation and location shown in Figure 8-4 is just an example. Connection between capacitor and ground node to be made through a through to the inner ground plane layer.

8.1.5 VBAT and CHP Capacitors

Three capacitors are used for bypassing the VBAT node. Prioritize placing an 0402 as close as possible to pin 59. The other two need to be close but not as critical. Ground capacitors. Capacitor ground needs to be connected to inner plane. The 0805 package is suitable for the other two capacitors.

Two capacitors are used between pin 59 and 60, and as with VBAT node, the 0402 capacitor needs to be as close as possible to the TPIC7218-Q1 device. The 0805 package is suitable for the other capacitor. See Figure 8-5 for more information.

8.1.6 Multiple Plane Layer Assignments

Place components associated with VCC3 (pin 3), VDD (pin 9), VBAT (pin 59), CHP (pin 60), DMR (pin 55), SMR (pin 56), GMR (pin 57), GPR (pin 58), SPR (pin 61) and DPR (pin 62) on top layer. Assign first PCB layer under the top layer as an overall ground plane.

Placing components on top-side of board and assigning first inner layer as ground plane minimizes the path length and loop area for EMC bypassing. See Figure 8-6 for more information.

8.1.7 Duplicate Pad Under TPIC7218-Q1 on All Non-Ground Plane Inner Layers

Duplicate the top layer pad underneath the TPIC7218-Q1 device on all of the inner layers. For the first inner ground plane layer, entire plane is ground except for clearances around holes and unconnected vias. Bottom layer copper pad directly under the TPIC7218-Q1 device is sized and has relief features as required for the thermal slug. See Figure 8-6 for more information.

8.1.8 Flooding

Flooding places copper on all available area, subject to the clearance rules for the manufacture of the PCB. Flooded areas should be connected by vias to the inner ground plane layer. Small, insignificant flooded zones may be left unconnected or deleted from the design.

The additional copper connected to ground augments the effectiveness of the inner ground plane layer by providing parallel paths, and also improves heat sink performance by increasing the thermal mass of the PCB. See Figure 8-7 for more information.

8.2 Layout Example

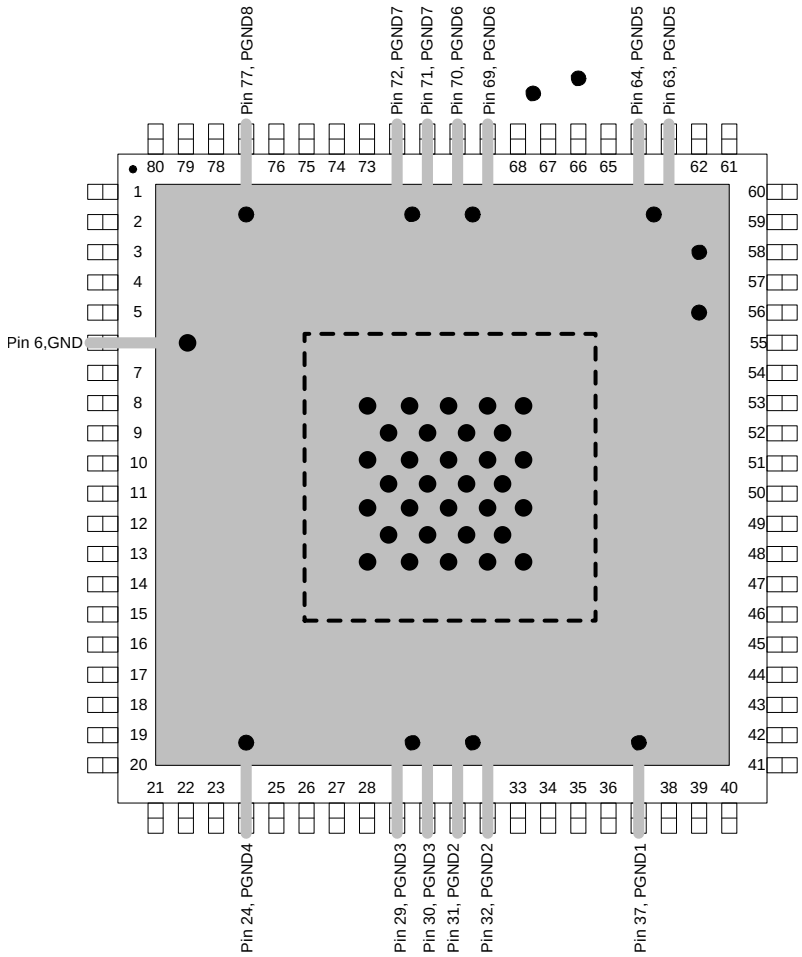


Figure 8-1. Local Grounding Configuration Layout Example

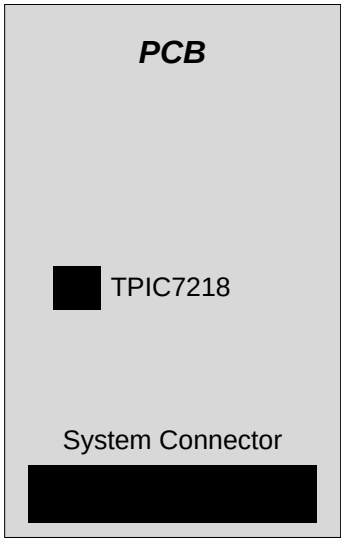


Figure 8-2. Board Level Grounding Configuration, TPIC7218-Q1 to System Connector Layout Example

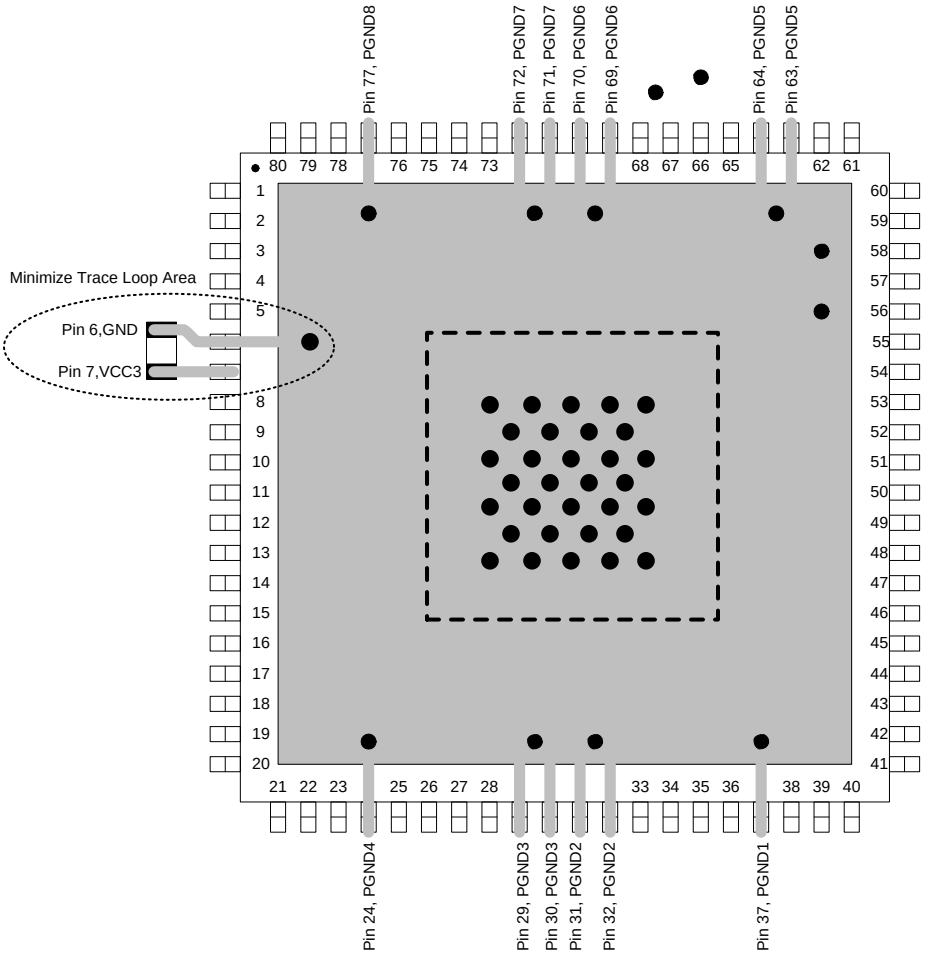


Figure 8-3. VCC3 Bypass Capacitor Layout Example

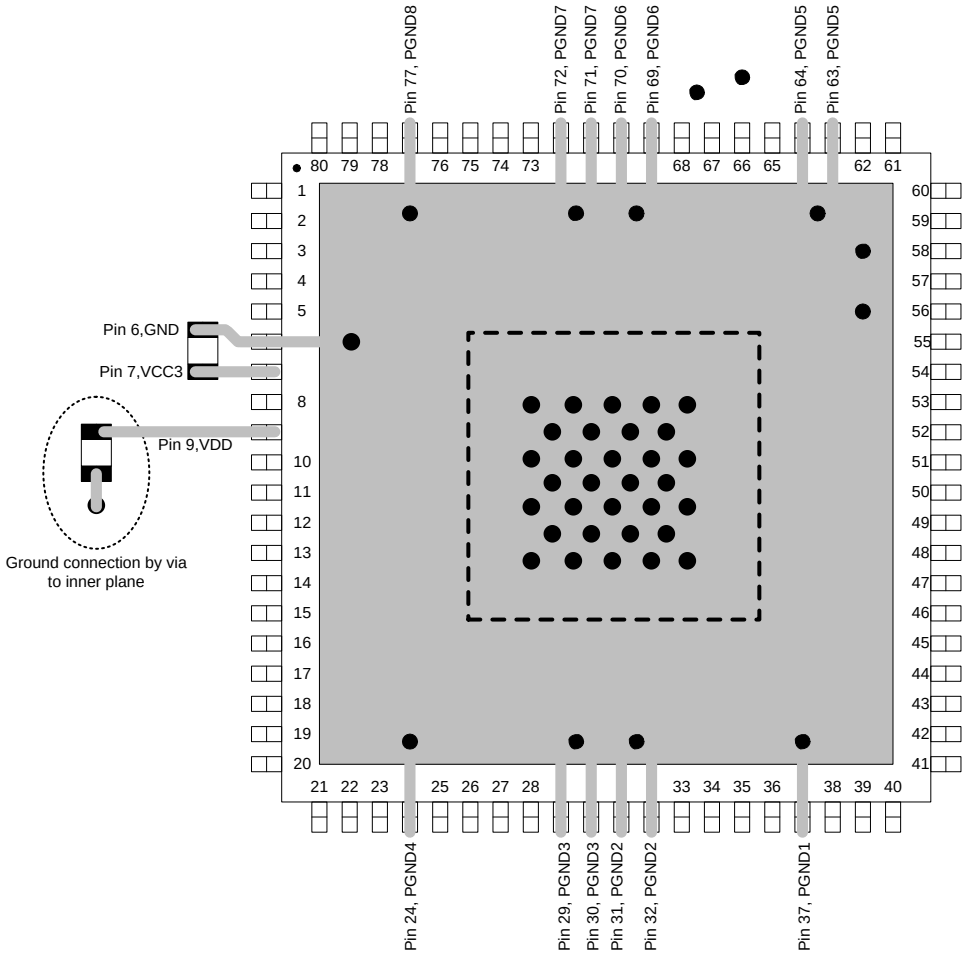


Figure 8-4. VDD Bypass Capacitor Layout Example

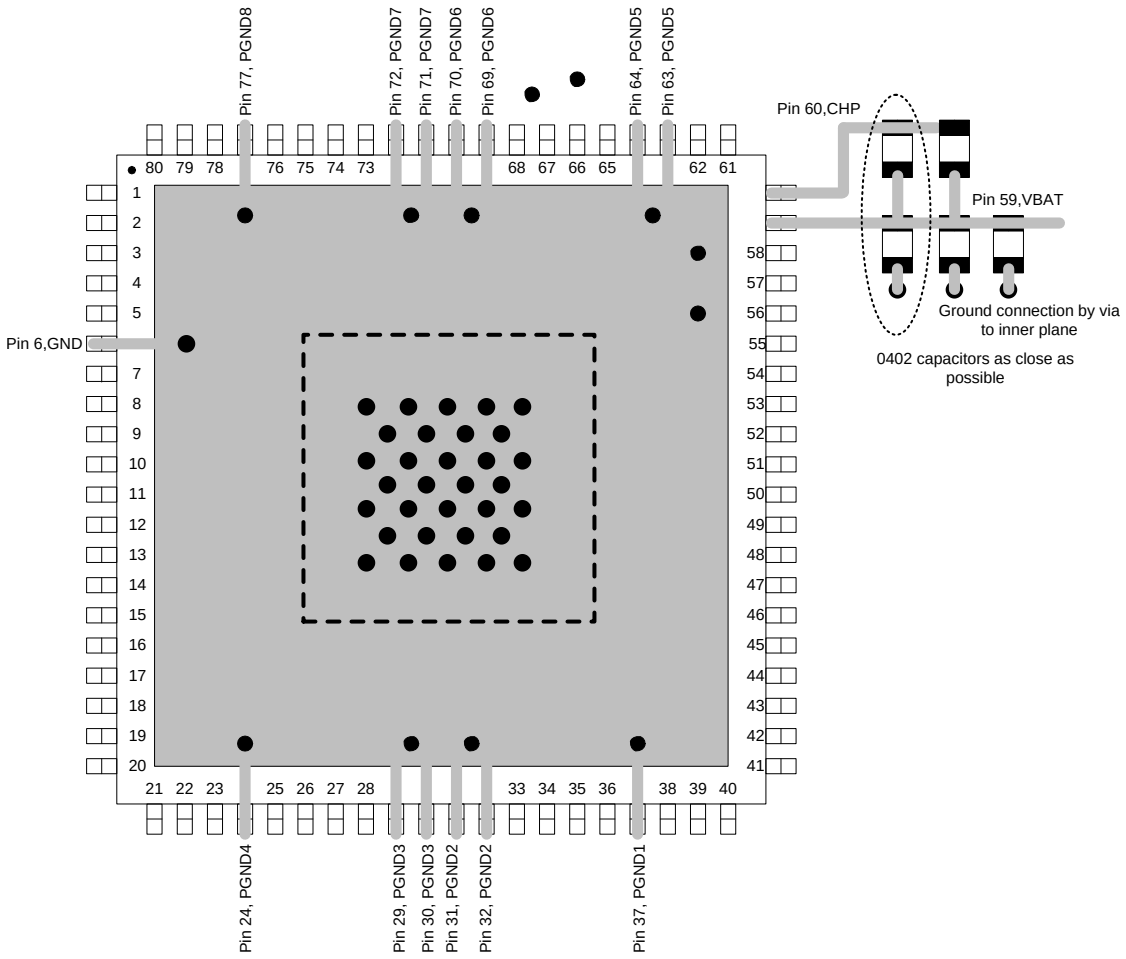


Figure 8-5. VBAT and CHP Capacitors Layout Example

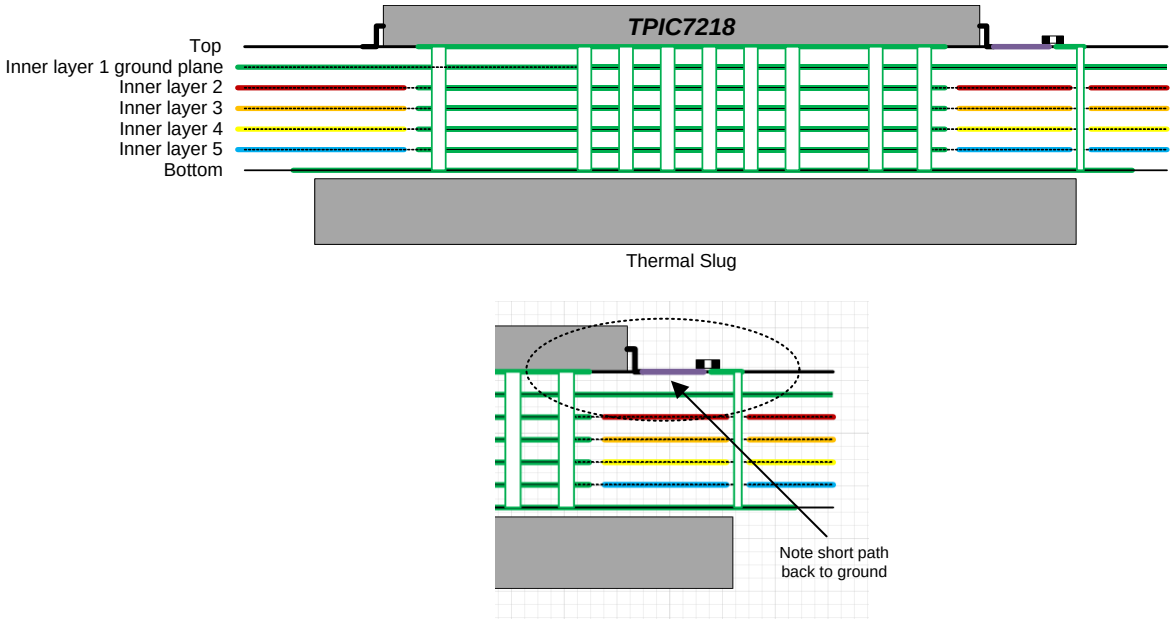


Figure 8-6. Multiple Plane Layer Assignments Layout Example

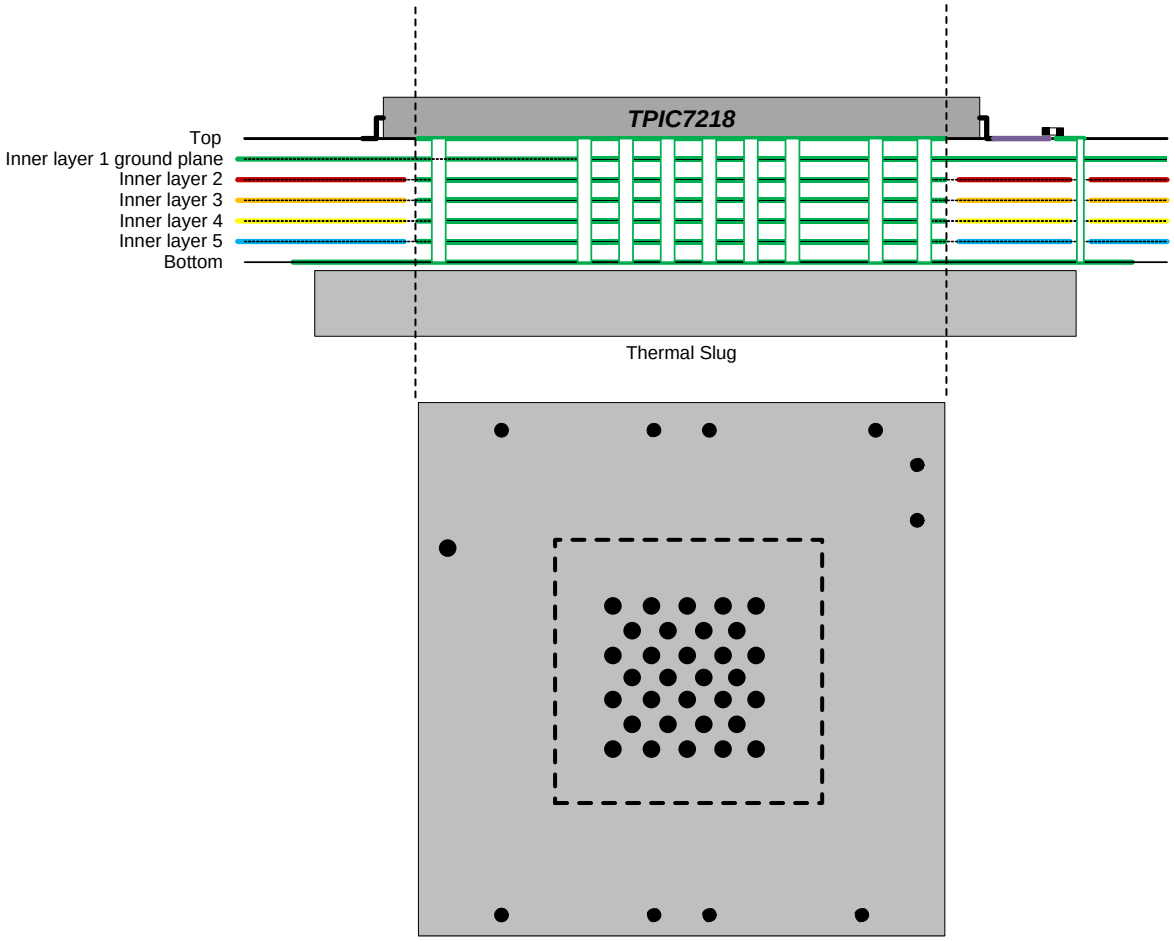


Figure 8-7. Thermal Slug Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following: *TPIC7218-Q1 Thermal Design Considerations and Solution*, SLDA013

9.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

9.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC7218QPFPRQ1	ACTIVE	HTQFP	PFP	80	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPIC7218Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

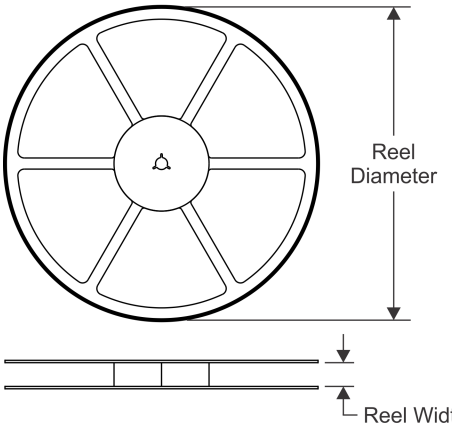
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

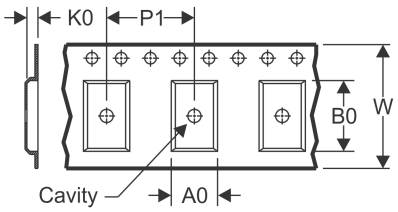
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

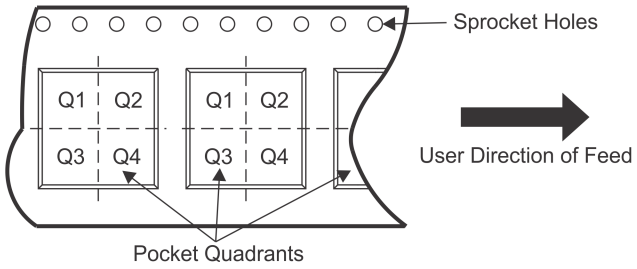


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

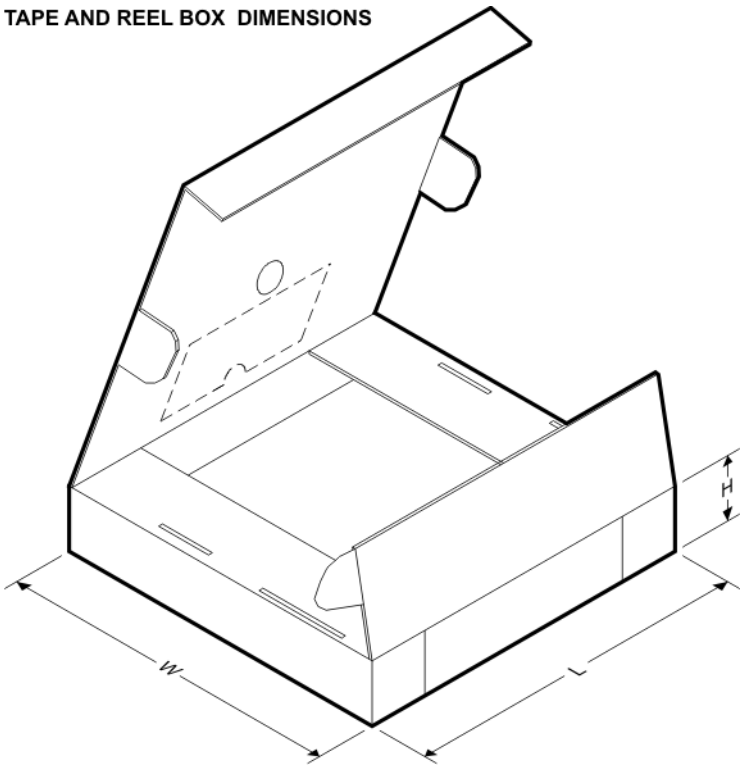
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC7218QPFPRQ1	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2

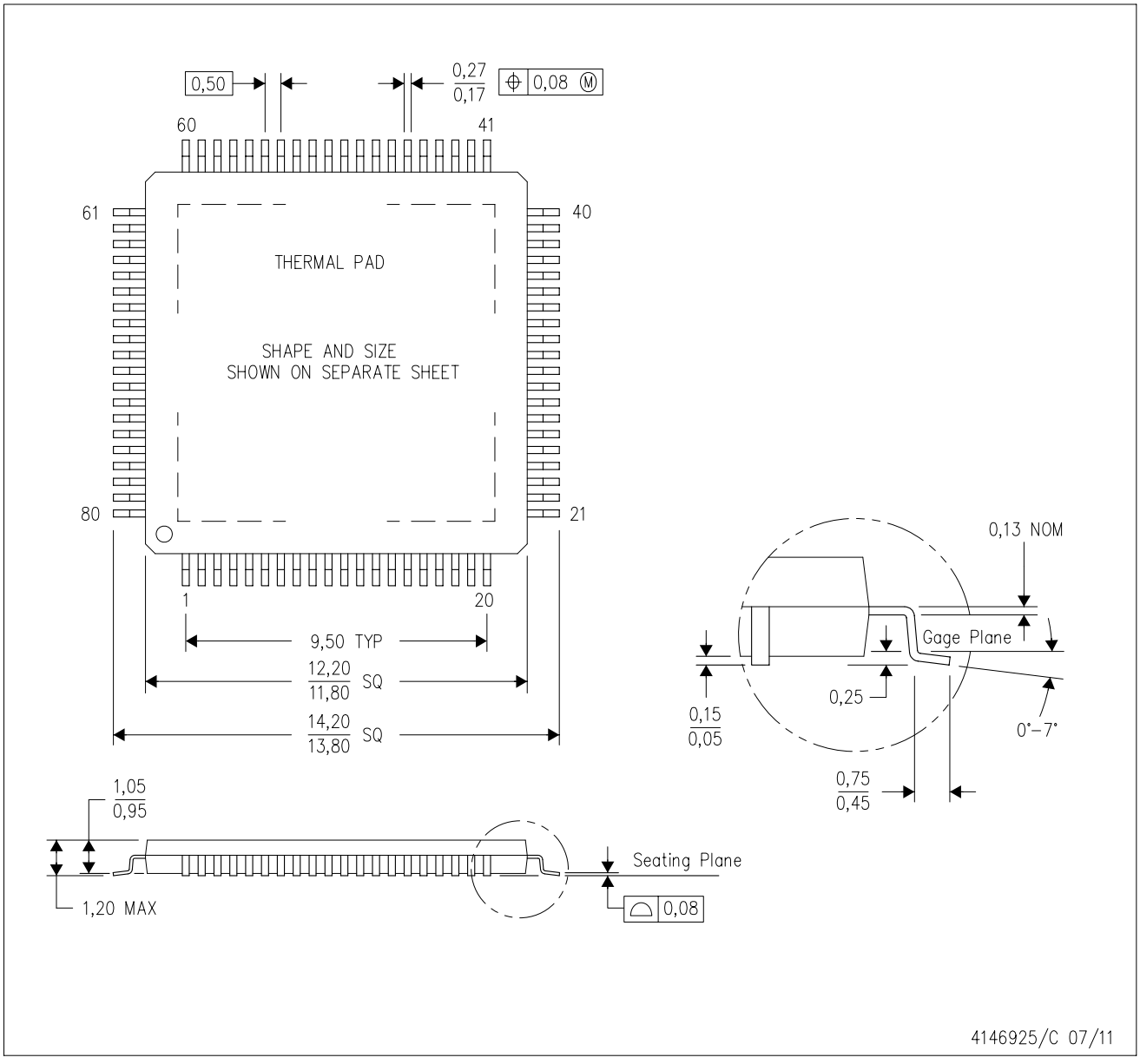
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC7218QPFPRQ1	HTQFP	PFP	80	1000	350.0	350.0	43.0

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

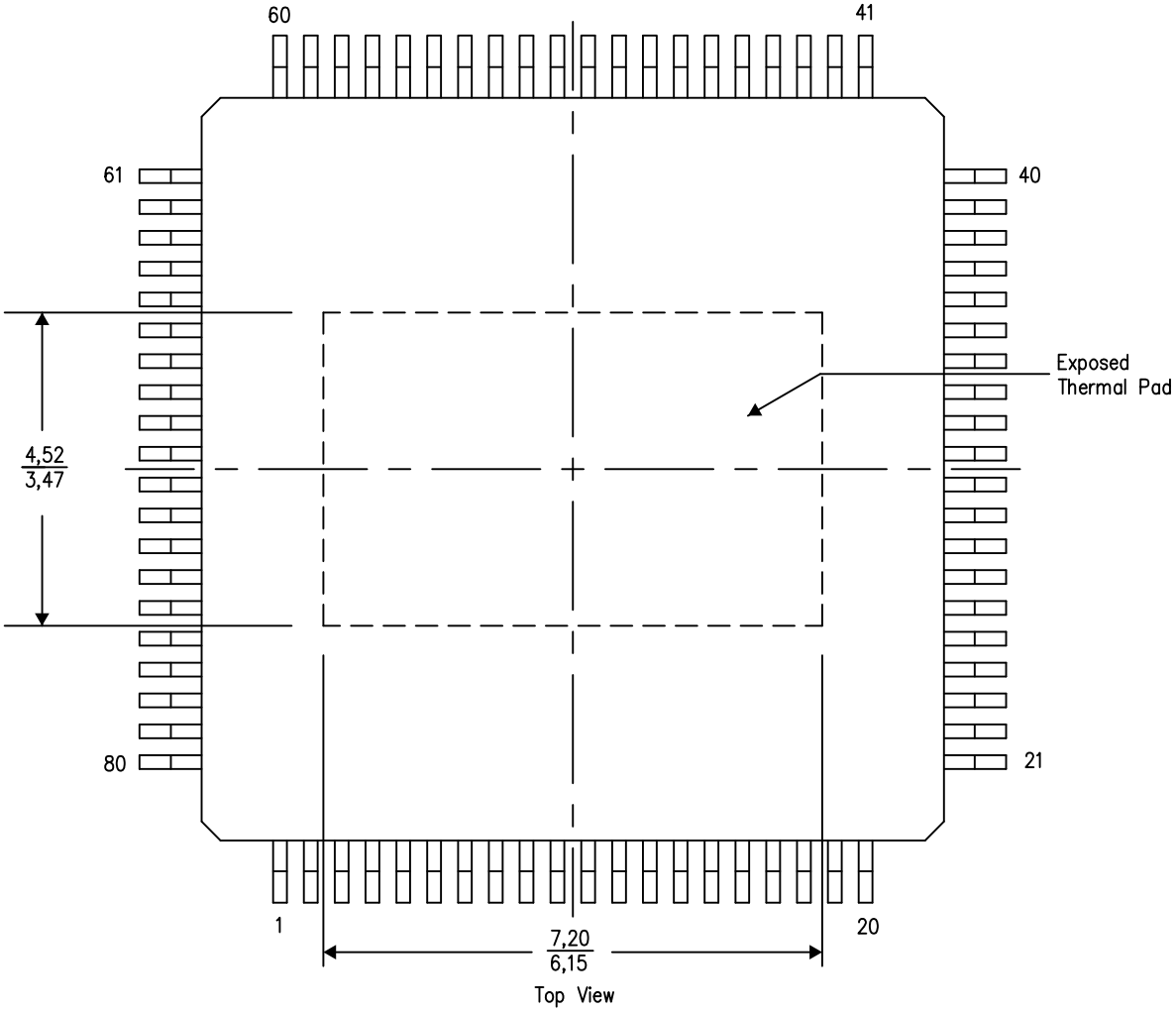
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206327–8/P 05/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

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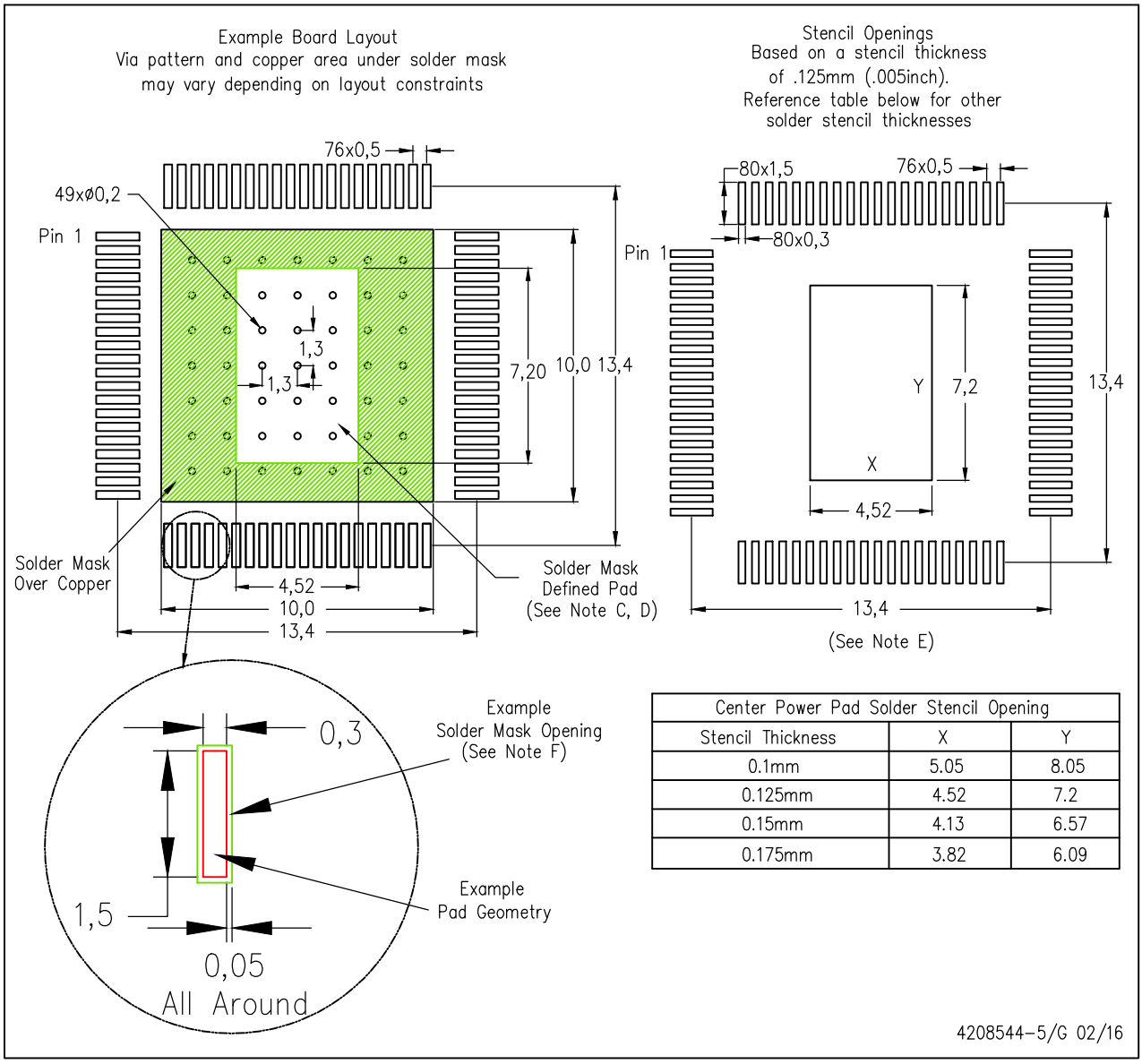

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.05	8.05
0.125mm	4.52	7.2
0.15mm	4.13	6.57
0.175mm	3.82	6.09

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–SM–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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