

NBSG53A

2.5 V/3.3 V SiGe Selectable Differential Clock and Data D Flip-Flop/Clock Divider with Reset and OLS*

The NBSG53A is a multi-function differential D flip-flop (DFF) or fixed divide by two (DIV/2) clock generator. This is a part of the GigaComm™ family of high performance Silicon Germanium products. A strappable control pin is provided to select between the two functions. The device is housed in a low profile 4x4 mm 16-pin Flip-Chip BGA (FCBGA) or a 3x3 mm 16 pin QFN package.

The NBSG53A is a device with data, clock, OLS*, reset, and select inputs. Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The OLS* input is used to program the peak-to-peak output amplitude between 0 and 800 mV in five discrete steps. The RESET and SELECT inputs are single-ended and can be driven with either LVECL or LVCMOS/LVTTL input levels.

Data is transferred to the outputs on the positive edge of the clock. The differential clock inputs of the NBSG53A allow the device to also be used as a negative edge triggered device.

Features

- Maximum Input Clock Frequency (DFF) > 8 GHz Typical (See Figures 3, 5, 7, 9, and 10)
- Maximum Input Clock Frequency (DIV/2) > 10 GHz Typical (See Figures 4, 6, 8, 9, and 10)
- 210 ps Typical Propagation Delay (OLS = FLOAT)
- 45 ps Typical Rise and Fall Times (OLS = FLOAT)
- DIV/2 Mode (Active with Select Low)
- DFF Mode (Active with Select High)
- Selectable Swing PECL Output with Operating Range: $V_{CC} = 2.375$ V to 3.465 V with $V_{EE} = 0$ V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.465 V
- Selectable Output Level (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak-to-Peak Output)
- 50 Ω Internal Input Termination Resistors on all Differential Inputs
- These are Pb-Free Devices

*Output Level Select



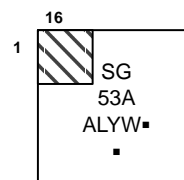
ON Semiconductor®

<http://onsemi.com>



QFN-16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

NBSG53A

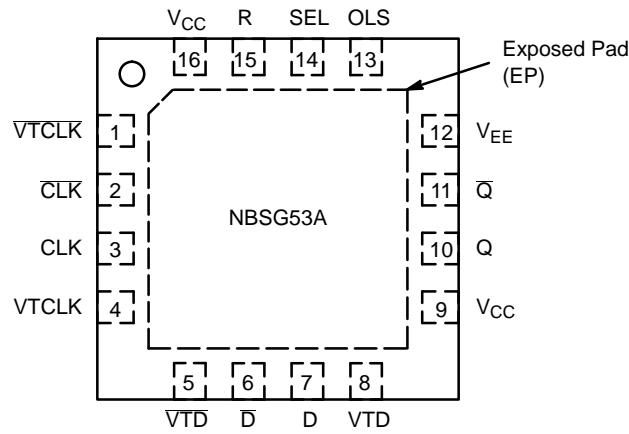


Figure 1. QFN-16 Pinout (Top View)

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|------|-----------------|--------------------------------------|---|
| 1 | VTCLK | – | Internal 50 Ω Termination Pin. See Table 4. |
| 2 | CLK | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Inverted Differential Input. |
| 3 | CLK | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Noninverted Differential Input. |
| 4 | VTCLK | – | Internal 50 Ω Termination Pin. See Table 4. |
| 5 | VTD | – | Internal 50 Ω termination pin. See Table 4. |
| 6 | D $\bar{}$ | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Inverted Differential Input. |
| 7 | D | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Noninverted Differential Input. |
| 8 | VTD | – | Internal 50 Ω Termination Pin. See Table 4. |
| 9,16 | V _{CC} | – | Positive Supply Voltage |
| 10 | Q | RSECL Output | NonInverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{TT} = V_{CC} - 2 V$. |
| 11 | Q $\bar{}$ | RSECL Output | Inverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{TT} = V_{CC} - 2 V$. |
| 12 | V _{EE} | – | Negative Supply Voltage |
| 13 | OLS* | Input | Input Pin for the Output Level Select (OLS). See Table 2. |
| 14 | SEL | LVECL, LVCMOS, LVTTTL Input | Select Logic Input. Internal 75 k Ω to V _{EE} . |
| 15 | R | LVECL, LVCMOS, LVTTTL Input | Reset D Flip-Flop. Internal 75 k Ω to V _{EE} . |
| – | EP | | The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die but may be electrically and thermally connected to V _{EE} on the PC board. |

1. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a heat-sinking conduit.
2. In the differential configuration when the input termination pins (VTD, VTD $\bar{}$, VTCLK, VTCLK $\bar{}$) are connected to a common termination voltage, and if no signal is applied then the device will be susceptible to self-oscillation.
3. When an output level of 400 mV is desired and V_{CC} – V_{EE} > 3.0 V, 2 k Ω resistor should be connected from OLS pin to V_{EE}.

NBSG53A

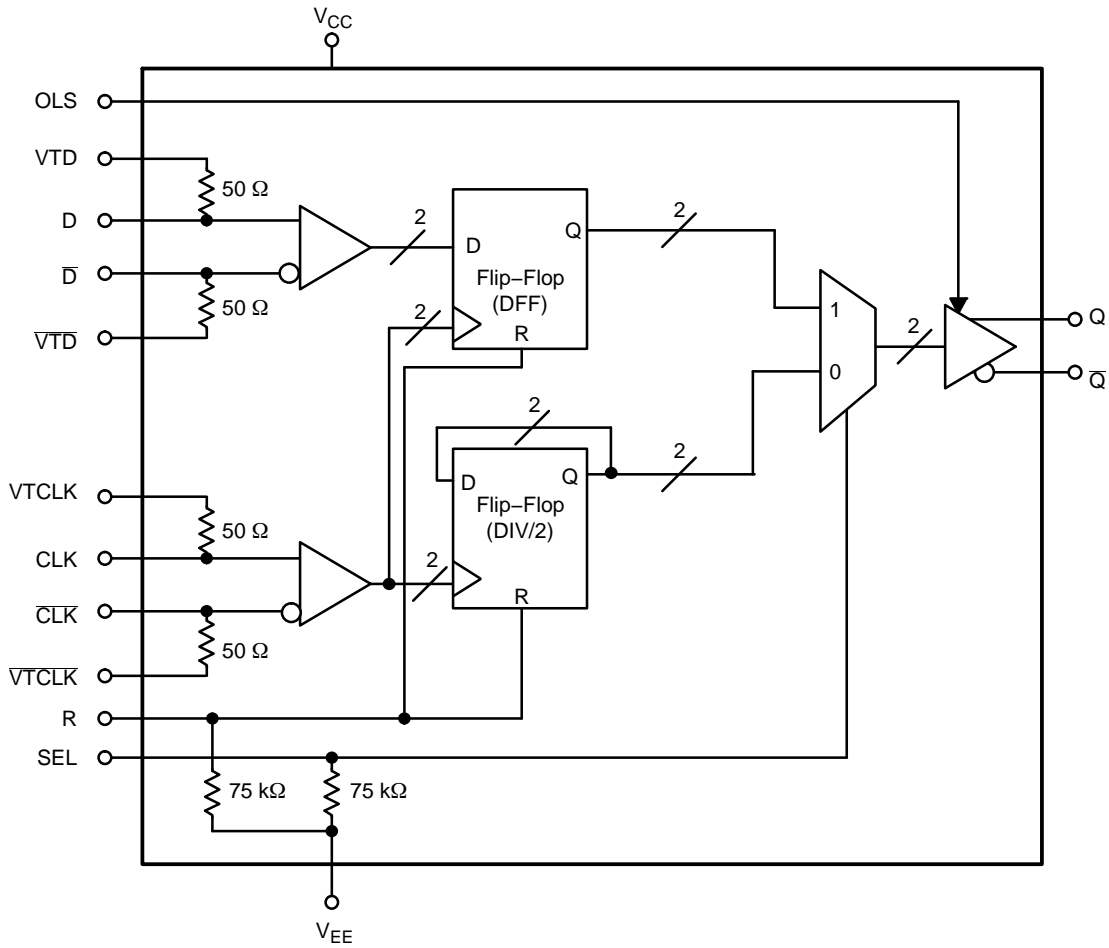


Figure 2. Simplified Logic Diagram

Table 2. OUTPUT LEVEL SELECT (OLS)

| OLS | Q/Q̄ VPP | OLS Sensitivity |
|--------------------------|----------|-----------------|
| V _{CC} | 800 mV | OLS - 75 mV |
| V _{CC} - 0.4 V | 200 mV | OLS ± 150 mV |
| V _{CC} - 0.8 V | 600 mV | OLS ± 100 mV |
| V _{CC} - 1.2 V | 0 | OLS ± 75 mV |
| V _{EE} (Note 4) | 400 mV | OLS + 100 mV |
| Float | 600 mV | N/A |

4. When an output level of 400 mV is desired and V_{CC} - V_{EE} > 3.0 V, 2.0 kΩ resistor should be connected from OLS to V_{EE}.

Table 3. TRUTH TABLE

| R | SEL | D | CLK | Q | Function |
|---|-----|---|-----|----|----------|
| H | x | x | x | L | Reset |
| L | H | L | Z | L | DFF |
| L | H | H | Z | H | DFF |
| L | L | x | Z | Q̄ | DIV/2 |

Z = LOW to HIGH Transition

Table 4. INTERFACING OPTIONS

| INTERFACING OPTIONS | CONNECTIONS |
|---------------------|--|
| CML | Connect VTCLK, VTD and VTCLK, VTD to V _{CC} |
| LVDS | Connect VTCLK, VTD and VTCLK, VTD Together |
| AC-COUPLED | Bias VTCLK, VTD and VTCLK, VTD Inputs within Common Mode Range (V _{IHCMR}) |
| RSECL, PECL, NECL | Standard ECL Termination Techniques |
| LVTTL, LVCMOS | An External Voltage (V _{th}) should be Applied to the Unused Complementary Differential Input. Nominal V _{th} is 1.5 V for LVTTL and V _{CC} /2 for LVCMOS Inputs. This Voltage must be within the V _{th} Specification. |

NBSG53A

Table 5. ATTRIBUTES

| Characteristics | Value |
|---|---|
| Positive Operating Voltage Range for V_{CC} ($V_{EE} = 0$ V) | 2.375 V to 3.465 V |
| Negative Operating Voltage Range for V_{EE} ($V_{CC} = 0$ V) | -2.375 V to -3.465 V |
| Internal Input Pulldown Resistor (R, SEL) | 75 k Ω |
| ESD Protection | Human Body Model Machine Model Charged Device Model |
| | > 1.5 kV > 50 V > 4 kV |
| Moisture Sensitivity (Note 5) | Level 1 |
| Flammability Rating | UL 94 V-0 @ 0.125 in |
| Oxygen Index | 28 to 34 |
| Transistor Count | 482 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

5. For additional information, refer to Application Note AND8003/D.

Table 6. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|---------------|--|---|--|----------------------------|----------------|
| V_{CC} | Positive Power Supply | $V_{EE} = 0$ V | | 3.6 | V |
| V_{EE} | Negative Power Supply | $V_{CC} = 0$ V | | -3.6 | V |
| V_I | Positive Input Negative Input | $V_{EE} = 0$ V $V_{CC} = 0$ V | $V_I \leq V_{CC}$ $V_I \geq V_{EE}$ | 3.6 -3.6 | V |
| V_{INPP} | Differential Input Voltage $ D - \bar{D} $ | $V_{CC} - V_{EE} \geq 2.8$ V $V_{CC} - V_{EE} < 2.8$ V | | 2.8 $ V_{CC} - V_{EE} $ | V |
| I_{IN} | Input Current Through R_T (50 Ω Resistor) | Static Surge | | 45 80 | mA |
| I_{OUT} | Output Current | Continuous Surge | | 25 50 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | $^{\circ}$ C |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}$ C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) (Note 6) | 0 lfpm 500 lfpm | | 41.6 35.2 | $^{\circ}$ C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | 2S2P (Note 6) | | 4.0 | $^{\circ}$ C/W |
| T_{sol} | Wave Solder Pb-Free | < 3 sec @ 260 $^{\circ}$ C | | 265 | $^{\circ}$ C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

NBSG53A

Table 7. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT ($V_{CC} = 2.5\text{ V}$; $V_{EE} = 0\text{ V}$) (Note 7)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------|----------------|-------|-----|-----|------|-----|-----|------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |

POWER SUPPLY CURRENT

| | | | | | | | | | | | |
|----------|-------------------------------|----|----|----|----|----|----|----|----|----|----|
| I_{EE} | Negative Power Supply Current | 33 | 45 | 57 | 33 | 45 | 57 | 33 | 45 | 57 | mA |
|----------|-------------------------------|----|----|----|----|----|----|----|----|----|----|

PECL OUTPUTS (Note 8)

| | | | | | | | | | | | |
|-------------|---|------|------|------|------|------|------|------|------|------|----|
| V_{OH} | Output HIGH Voltage | 1460 | 1510 | 1560 | 1490 | 1540 | 1590 | 1515 | 1565 | 1615 | mV |
| V_{OL} | Output LOW Voltage | | | | | | | | | | mV |
| | (OLS = V_{CC}) | 555 | 705 | 855 | 595 | 745 | 895 | 625 | 775 | 925 | |
| | (OLS = $V_{CC} - 0.4\text{ V}$) | 1235 | 1295 | 1385 | 1270 | 1330 | 1420 | 1295 | 1355 | 1445 | |
| | (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) | 775 | 895 | 1015 | 810 | 930 | 1050 | 840 | 960 | 1080 | |
| | (OLS = $V_{CC} - 1.2\text{ V}$) | 1455 | 1505 | 1585 | 1490 | 1540 | 1620 | 1510 | 1560 | 1640 | |
| | (OLS = V_{EE}) | 1005 | 1095 | 1215 | 1040 | 1130 | 1250 | 1065 | 1155 | 1275 | |
| V_{OUTPP} | Output Voltage Amplitude | | | | | | | | | | mV |
| | (OLS = V_{CC}) | 670 | 800 | | 660 | 795 | | 655 | 790 | | |
| | (OLS = $V_{CC} - 0.4\text{ V}$) | 125 | 215 | | 120 | 210 | | 120 | 210 | | |
| | (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) | 510 | 615 | | 505 | 610 | | 500 | 605 | | |
| | (OLS = $V_{CC} - 1.2\text{ V}$) | 0 | 5 | | 0 | 0 | | 0 | 0 | | |
| | (OLS = V_{EE}) | 325 | 415 | | 320 | 410 | | 320 | 410 | | |

DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 13 & 15) (Note 9)

| | | | | | | | | | | | | |
|-----------|--|-------------------------------------|--------------|--|-----------------------|--------------|--|-----------------------|--------------|--|------------------------|----|
| V_{IH} | Input HIGH Voltage | CLK, invCLK, D, \bar{D} R, SEL | 1200 1290 | | V_{CC} V_{CC} | 1200 1355 | | V_{CC} V_{CC} | 1200 1415 | | V_{CC} V_{CC} | mV |
| V_{IL} | Input LOW Voltage | CLK, invCLK, D, \bar{D} R, SEL | 0 0 | | $V_{IH} - 150$ 890 | 0 0 | | $V_{IH} - 150$ 955 | 0 0 | | $V_{IH} - 150$ 1015 | mV |
| V_{th} | Input Threshold Voltage Range (Note 10) | | 1125 | | $V_{CC} - 75$ | 1125 | | $V_{CC} - 75$ | 1125 | | $V_{CC} - 75$ | mV |
| V_{ISE} | Single-Ended Input Voltage ($V_{IH} - V_{IL}$) | | 150 | | 2600 | 150 | | 2600 | 150 | | 260 | mV |

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 14 & 16) (Note 11)

| | | | | | | | | | | | | |
|-------------|---|--|---------|-----------|----------------|---------|-----------|----------------|---------|-----------|----------------|----|
| V_{IHD} | Differential Input HIGH Voltage | | 1200 | | V_{CC} | 1200 | | V_{CC} | 1200 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | | 0 | | $V_{IHD} - 75$ | 0 | | $V_{IHD} - 75$ | 0 | | $V_{IHD} - 75$ | mV |
| V_{ID} | Differential Input Voltage ($V_{IHD} - V_{ILD}$) | | 75 | | 2600 | 75 | | 2600 | 75 | | 2600 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Note 12) (Figure 17) | | 1200 | | 2500 | 1200 | | 2500 | 1200 | | 2500 | mV |
| I_{IH} | Input HIGH Current (@ V_{IH}) R, SEL CLK, inv_CLK, D, inv_D | | 35 5 | 100 50 | | 35 5 | 100 50 | | 35 5 | 100 50 | μA | |
| I_{IL} | Input LOW Current (@ V_{IL}) R, SEL CLK, inv_CLK, D, inv_D | | 20 5 | 100 50 | | 20 5 | 100 50 | | 20 5 | 100 50 | μA | |

TERMINATION RESISTORS

| | | | | | | | | | | | |
|-----------|-------------------------------------|----|----|----|----|----|----|----|----|----|----------|
| R_{TIN} | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
|-----------|-------------------------------------|----|----|----|----|----|----|----|----|----|----------|

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC} .
- All outputs loaded with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
- V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.
- V_{IHD} , V_{ILD} , V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.
- V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NBSG53A

Table 8. DC CHARACTERISTICS, INPUT WITH PECL OUTPUT ($V_{CC} = 3.3\text{ V}$; $V_{EE} = 0\text{ V}$) (Note 13)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------|----------------|-------|-----|-----|------|-----|-----|------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |

POWER SUPPLY CURRENT

| | | | | | | | | | | | |
|----------|-------------------------------|----|----|----|----|----|----|----|----|----|----|
| I_{EE} | Negative Power Supply Current | 35 | 47 | 59 | 35 | 47 | 59 | 35 | 47 | 59 | mA |
|----------|-------------------------------|----|----|----|----|----|----|----|----|----|----|

PECL OUTPUTS (Note 14)

| | | | | | | | | | | | |
|-------------|---|------|------|------|------|------|------|------|------|------|----|
| V_{OH} | Output HIGH Voltage | 2260 | 2310 | 2360 | 2290 | 2340 | 2390 | 2315 | 2365 | 2415 | mV |
| V_{OL} | Output LOW Voltage | | | | | | | | | | mV |
| | (OLS = V_{CC}) | 1320 | 1470 | 1620 | 1360 | 1510 | 1660 | 1390 | 1540 | 1690 | |
| | (OLS = $V_{CC} - 0.4\text{ V}$) | 2030 | 2090 | 2180 | 2065 | 2125 | 2215 | 2090 | 2150 | 2240 | |
| | (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) | 1550 | 1670 | 1790 | 1585 | 1705 | 1825 | 1615 | 1735 | 1855 | |
| | (OLS = $V_{CC} - 1.2\text{ V}$) | 2260 | 2310 | 2390 | 2290 | 2340 | 2420 | 2315 | 2365 | 2445 | |
| | ** (OLS = V_{EE}) | 1785 | 1875 | 1995 | 1820 | 2030 | 2030 | 1850 | 1940 | 2060 | |
| V_{OUTPP} | Output Voltage Amplitude | | | | | | | | | | mV |
| | (OLS = V_{CC}) | 705 | 815 | | 695 | 805 | | 590 | 800 | | |
| | (OLS = $V_{CC} - 0.4\text{ V}$) | 130 | 220 | | 125 | 215 | | 125 | 215 | | |
| | (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) | 535 | 640 | | 530 | 635 | | 525 | 630 | | |
| | (OLS = $V_{CC} - 1.2\text{ V}$) | 0 | 0 | | 0 | 0 | | 0 | 0 | | |
| | ** (OLS = V_{EE}) | 345 | 435 | | 340 | 430 | | 335 | 425 | | |

DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 13 & 15) (Note 15)

| | | | | | | | | | | | |
|-----------|--|------|--|----------------|------|--|----------------|------|--|----------------|----|
| V_{IH} | Input HIGH Voltage (Single-Ended) | 1200 | | V_{CC} | 1200 | | V_{CC} | 1200 | | V_{CC} | mV |
| | CLK, invCLK, D, \bar{D} R, SEL | 2090 | | V_{CC} | 2155 | | V_{CC} | 2215 | | V_{CC} | |
| V_{IL} | Input LOW Voltage (Single-Ended) | 0 | | $V_{IH} - 150$ | 0 | | $V_{IH} - 150$ | 0 | | $V_{IH} - 150$ | mV |
| | CLK, invCLK, D, \bar{D} R, SEL | 0 | | 1690 | 0 | | 1755 | 0 | | 1815 | |
| V_{th} | Input Threshold Voltage Range (Note 16) | 1125 | | $V_{CC} - 75$ | 1125 | | $V_{CC} - 75$ | 1125 | | $V_{CC} - 75$ | mV |
| V_{ISE} | Single-Ended Input Voltage ($V_{IH} - V_{IL}$) | 150 | | 2600 | 150 | | 2600 | 150 | | 260 | mV |

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 14 & 16) (Note 17)

| | | | | | | | | | | | |
|-------------|--|------|----|----------------|------|----|----------------|------|----|----------------|---------------|
| V_{IHD} | Differential Input HIGH Voltage | 1200 | | V_{CC} | 1200 | | V_{CC} | 1200 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | 0 | | $V_{IHD} - 75$ | 0 | | $V_{IHD} - 75$ | 0 | | $V_{IHD} - 75$ | mV |
| V_{ID} | Differential Input Voltage ($V_{IHD} - V_{ILD}$) | 75 | | 2600 | 75 | | 2600 | 75 | | 2600 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Note 18) (Figure 17) | 1200 | | 3300 | 1200 | | 3300 | 1200 | | 3300 | mV |
| I_{IH} | Input HIGH Current (@ V_{IH}) | | 35 | 100 | | 35 | 100 | | 35 | 100 | μA |
| | CLK, inv_CLK, D, inv_D R, SEL | | 5 | 50 | | 5 | 50 | | 5 | 50 | |
| I_{IL} | Input LOW Current (@ V_{IL}) | | 20 | 100 | | 20 | 100 | | 20 | 100 | μA |
| | CLK, inv_CLK, D, inv_D R, SEL | | 5 | 50 | | 5 | 50 | | 5 | 50 | |

TERMINATION RESISTORS

| | | | | | | | | | | | |
|-----------|-------------------------------------|----|----|----|----|----|----|----|----|----|----------|
| R_{TIN} | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
|-----------|-------------------------------------|----|----|----|----|----|----|----|----|----|----------|

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a 2 k Ω resistor should be connected from OLS to V_{EE} .

13. Input and output parameters vary 1:1 with V_{CC} .

14. All outputs loaded with 50 Ω to $V_{CC} - 2.0\text{ V}$.

15. V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.

16. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.

17. V_{IHD} , V_{ILD} , V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.

18. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NBSG53A

Table 9. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT

($V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V) (Note 19)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------|----------------|-------|-----|-----|------|-----|-----|------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |

POWER SUPPLY CURRENT

| | | | | | | | | | | | |
|----------|-------------------------------|----|----|----|----|----|----|----|----|----|----|
| I_{EE} | Negative Power Supply Current | 35 | 47 | 59 | 35 | 47 | 59 | 35 | 47 | 59 | mA |
|----------|-------------------------------|----|----|----|----|----|----|----|----|----|----|

NECL OUTPUTS (Note 20)

| | | | | | | | | | | | |
|---|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|----|
| V_{OH} | Output HIGH Voltage | -1040 | -990 | -940 | -1010 | -960 | -910 | -985 | -935 | -885 | mV |
| V_{OL} | Output LOW Voltage | | | | | | | | | | mV |
| | $-3.465\text{ V} \leq V_{EE} \leq -3.0\text{ V}$ | | | | | | | | | | |
| | (OLS = V_{CC}) | -1980 | -1830 | -1680 | -1940 | -1790 | -1640 | -1910 | -1760 | -1610 | |
| | (OLS = $V_{CC} - 0.4\text{ V}$) | -1270 | -1210 | -1120 | -1235 | -1175 | -1085 | -1210 | -1150 | -1060 | |
| | (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) | -1750 | -1630 | -1510 | -1715 | -1595 | -1475 | -1685 | -1565 | -1445 | |
| | (OLS = $V_{CC} - 1.2\text{ V}$) | -1040 | -990 | -910 | -1010 | -960 | -880 | -985 | -935 | -855 | |
| | ** (OLS = V_{EE}) | -1515 | -1425 | -1305 | -1480 | -1390 | -1270 | -1450 | -1360 | -1240 | |
| | $-3.0\text{ V} < V_{EE} \leq -2.375\text{ V}$ | | | | | | | | | | |
| | (OLS = V_{CC}) | -1945 | -1795 | -1645 | -1905 | -1755 | -1605 | -1875 | -1725 | -1575 | |
| | (OLS = $V_{CC} - 0.4\text{ V}$) | -1265 | -1205 | -1115 | -1230 | -1170 | -1080 | -1205 | -1145 | -1055 | |
| (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) | -1725 | -1605 | -1485 | -1690 | -1570 | -1450 | -1660 | -1540 | -1420 | | |
| (OLS = $V_{CC} - 1.2\text{ V}$) | -1045 | -995 | -915 | -1010 | -960 | -880 | -900 | -940 | -860 | | |
| (OLS = V_{EE}) | -1495 | -1405 | -1285 | -1460 | -1370 | -1250 | -1435 | -1345 | -1225 | | |
| V_{OUTPP} | Output Voltage Amplitude | | | | | | | | | | mV |
| | $-3.465\text{ V} \leq V_{EE} \leq -3.0\text{ V}$ | | | | | | | | | | |
| | (OLS = V_{CC}) | 705 | 815 | | 695 | 805 | | 690 | 800 | | |
| | (OLS = $V_{CC} - 0.4\text{ V}$) | 130 | 220 | | 125 | 215 | | 125 | 215 | | |
| | (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) | 535 | 640 | | 530 | 635 | | 525 | 630 | | |
| | (OLS = $V_{CC} - 1.2\text{ V}$) | 0 | 0 | | 0 | 0 | | 0 | 0 | | |
| | ** (OLS = V_{EE}) | 345 | 435 | | 340 | 430 | | 335 | 425 | | |
| | $-3.0\text{ V} < V_{EE} \leq -2.375\text{ V}$ | | | | | | | | | | |
| | (OLS = V_{CC}) | 670 | 800 | | 660 | 795 | | 655 | 790 | | |
| | (OLS = $V_{CC} - 0.4\text{ V}$) | 125 | 215 | | 120 | 210 | | 120 | 210 | | |
| (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) | 510 | 615 | | 505 | 610 | | 500 | 605 | | | |
| (OLS = $V_{CC} - 1.2\text{ V}$) | 0 | 5 | | 0 | 0 | | 0 | 5 | | | |
| (OLS = V_{EE}) | 325 | 415 | | 320 | 410 | | 320 | 410 | | | |

DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Figures 13 & 15) (Note 21)

| | | | | | | | | | | | |
|-----------|--|--------------------------|--|-------------------------|--------------------------|--|-------------------------|--------------------------|--|-------------------------|----|
| V_{IH} | Input HIGH Voltage (Single-Ended) CLK, invCLK, D, \bar{D} R, SEL | $V_{EE} + 1200$ -1210 | | V_{CC} V_{CC} | $V_{EE} + 1200$ -1145 | | V_{CC} V_{CC} | $V_{EE} + 1200$ -1085 | | V_{CC} V_{CC} | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) CLK, invCLK, D, \bar{D} R, SEL | V_{EE} V_{EE} | | $V_{IH} - 150$ -1690 | V_{EE} V_{EE} | | $V_{IH} - 150$ -1545 | V_{EE} V_{EE} | | $V_{IH} - 150$ -1485 | mV |
| V_{th} | Input Threshold Voltage (Note 22) | $V_{EE} + 1125$ | | $V_{CC} - 75$ | $V_{EE} + 1125$ | | $V_{CC} - 75$ | $V_{EE} + 1125$ | | $V_{CC} - 75$ | mV |
| V_{ISE} | Single-Ended Input Voltage ($V_{IH} - V_{IL}$) | 150 | | 2600 | 150 | | 2600 | 150 | | 260 | mV |

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 14 & 16) (Note 23)

| | | | | | | | | | | | |
|-------------|---|-----------------|---------|----------------|-----------------|---------|----------------|-----------------|---------|----------------|---------------|
| V_{IHD} | Differential Input HIGH Voltage | $V_{EE} + 1200$ | | V_{CC} | $V_{EE} + 1200$ | | V_{CC} | $V_{EE} + 1200$ | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | V_{EE} | | $V_{IHD} - 75$ | V_{EE} | | $V_{IHD} - 75$ | V_{EE} | | $V_{IHD} - 75$ | mV |
| V_{ID} | Differential Input Voltage ($V_{IHD} - V_{ILD}$) | 75 | | 2600 | 75 | | 2600 | 75 | | 2600 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 24) (Figure 17) | $V_{EE} + 1200$ | | 0.0 | $V_{EE} + 1200$ | | 0.0 | $V_{EE} + 1200$ | | 0.0 | mV |
| I_{IH} | Input HIGH Current (@ V_{IH}) R, SEL CLK, inv_CLK, D, inv_D | | 35 5 | 100 50 | | 35 5 | 100 50 | | 35 5 | 100 50 | μA |

NBSG53A

Table 9. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT (continued)

($V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V) (Note 19)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--|---|-------|---|---|------|---|---|------|---|---|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 14 & 16) (Note 23) | | | | | | | | | | | |
| I_{IL} | Input LOW Current (@ V_{IL}) R, SEL CLK, inv_CLK, D, inv_D | | 20 5 | 100 50 | | 20 5 | 100 50 | | 20 5 | 100 50 | μA |
| I_{OLS} | OLS Input Current (see Figure 11) (OLS = V_{CC}) (OLS = $V_{CC} - 0.4\text{ V}$) (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) (OLS = $V_{CC} - 1.2\text{ V}$) $-3.465\text{ V} \leq V_{EE} \leq -3.0\text{ V}$ *(OLS = V_{EE}) $-3.0\text{ V} < V_{EE} \leq -2.375\text{ V}$ (OLS = V_{EE}) | | 300 100 5 -100 -1500 -1000 | 900 300 100 -100 -600 -400 | | 300 100 5 -100 -1500 -1000 | 900 300 100 -100 -600 -400 | | 300 100 5 -100 -1500 -1000 | 900 300 100 -100 -600 -400 | μA |

TERMINATION RESISTORS

| R_{TIN} | Internal Input Termination Resistor | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | Ω |
|-----------|-------------------------------------|----|----|----|----|----|----|----|----|----|----------|
|-----------|-------------------------------------|----|----|----|----|----|----|----|----|----|----------|

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*Typicals used for testing purposes.

**When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a 2 k Ω resistor should be connected from OLS to V_{EE} .

19. Input and output parameters vary 1:1 with V_{CC} .

20. All outputs loaded with 50 Ω to $V_{CC} - 2.0\text{ V}$.

21. V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.

22. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$.

23. V_{IHD} , V_{ILD} , V_{ID} and V_{IHCMR} parameters must be complied with simultaneously.

24. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

NBSG53A

Table 10. AC CHARACTERISTICS

($V_{CC} = 0\text{ V}$; $V_{EE} = -3.465\text{ V}$ to -2.375 V or $V_{CC} = 2.375\text{ V}$ to 3.465 V ; $V_{EE} = 0\text{ V}$)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------|--|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Input Clock Frequency (See Figures 3, 5, 7, 9, and 10) DFF (See Figures 4, 6, 8, 9, and 10) (Note 25) DIV/2 | | 8 | | 8 | | | 8 | | | GHz |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential (Note 29) CLK→Q, \bar{Q} SEL→Q, \bar{Q} R→Q, \bar{Q} $D_{IN}/2$ DFF | 150 100 215 195 | 215 190 280 270 | 285 280 375 345 | 150 100 215 195 | 215 190 280 270 | 285 280 375 345 | 150 100 215 195 | 215 190 280 270 | 285 280 375 345 | ps |
| t_{SKEW} | Duty Cycle Skew (Notes 26 and 28) DFF | | 5 | 20 | | 5 | 20 | | 5 | 20 | ps |
| t_{JITTER} | RMS Random Clock Jitter $f_{in} \leq 8\text{ GHz}$ (See Figures 3 and 5) (Note 25) Peak-to-Peak Data Dependent Jitter $f_{in} = 8\text{ Gb/s}$ | | 0.5 | 1 | | 0.5 | 1 | | 0.5 | 1 | ps |
| V_{INPP} | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 27) | 75 | | 2600 | 75 | | 2600 | 75 | | 2600 | mV |
| t_r t_f | Output Rise/Fall Times (20% – 80%) @ 1 GHz Q, \bar{Q} (OLS = V_{CC}) (OLS = $V_{CC} - 0.4\text{ V}$) (OLS = $V_{CC} - 0.8\text{ V}$, OLS = FLOAT) **(OLS = V_{EE}) | 28 15 25 20 | 40 40 35 35 | 65 65 65 65 | 28 15 25 20 | 40 40 35 35 | 65 65 65 65 | 28 15 25 20 | 40 40 35 35 | 65 65 65 65 | ps |
| t_s | Setup Time D→CLK | 30 | 14 | | 30 | 10 | | 30 | 13 | | ps |
| t_h | Hold Time D→CLK | 25 | 12 | | 25 | 7 | | 25 | 0 | | ps |
| t_{rr} | Reset Recovery DFF, DIV/2 | 40 | 9 | | 40 | 12 | | 40 | 10 | | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

25. Measured using a 500 mV source, 50% duty cycle clock source. Repetitive 1010 input data pattern. All outputs loaded with 50 Ω to $V_{CC} - 2.0\text{ V}$. Input edge rates is 40 ps (20% – 80%).

26. See Figure 18. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% differential clock input waveform.

27. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$ (Applicable only when $V_{CC} - V_{EE} < 2600\text{ mV}$).

28. See Figure 9. Duty Cycle % vs. Frequency.

29. For all OLS Configuration.

**When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a 2 k Ω resistor should be connected from OLS to V_{EE} .

NBSG53A

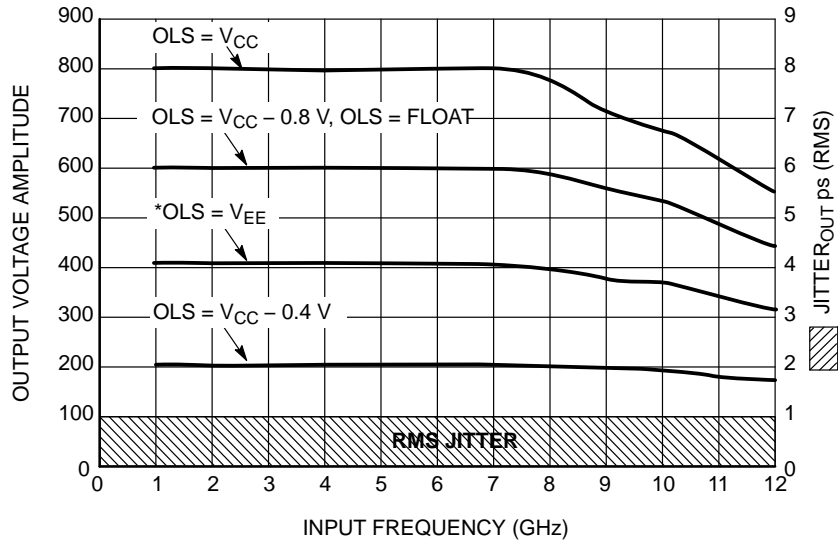


Figure 3. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for DFF Mode ($V_{CC} - V_{EE} = 3.3\text{ V}$ @ 25°C ; Repetitive 1010 Input Data Pattern)

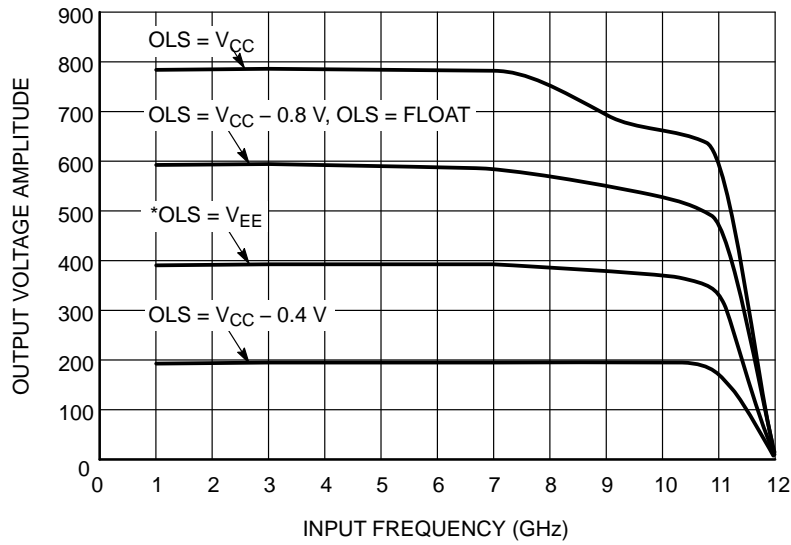


Figure 4. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for DIV/2 Mode ($V_{CC} - V_{EE} = 3.3\text{ V}$ @ 25°C)

*When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a $2\text{ k}\Omega$ resistor should be connected from OLS to V_{EE} .

NBSG53A

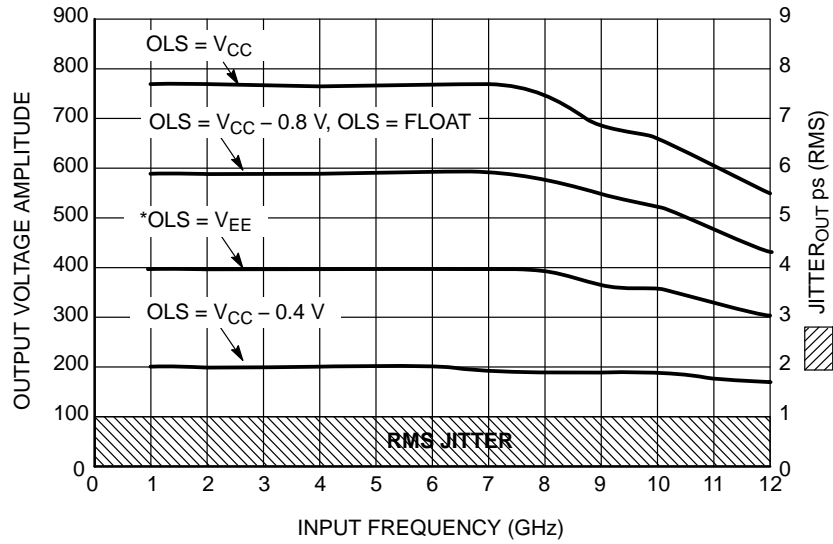


Figure 5. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for DFF Mode ($V_{CC} - V_{EE} = 2.5\text{ V}$ @ 25°C ; Repetitive 1010 Input Data Pattern)

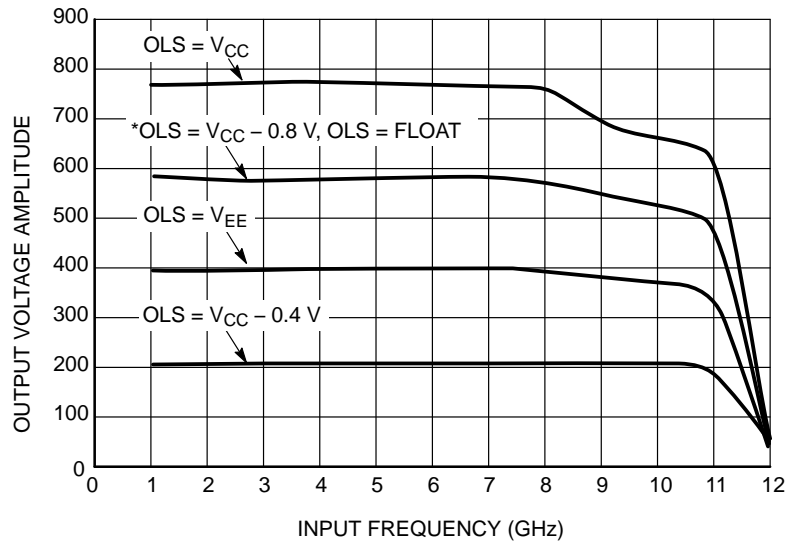


Figure 6. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for DIV/2 Mode ($V_{CC} - V_{EE} = 2.5\text{ V}$ @ 25°C)

*When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0\text{ V}$, a $2\text{ k}\Omega$ resistor should be connected from OLS to V_{EE} .

NBSG53A

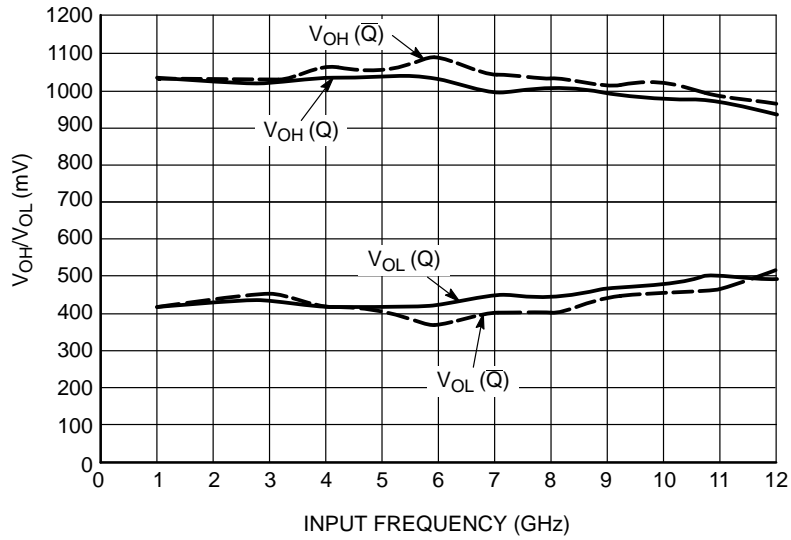


Figure 7. V_{OH}/V_{OL} (Q/ \bar{Q}) vs. Input Frequency (f_{in}) for DFF Mode ($V_{CC} - V_{EE} = 3.3$ V @ 25°C and OLS = $V_{CC} - 0.8$ V, OLS = FLOAT)

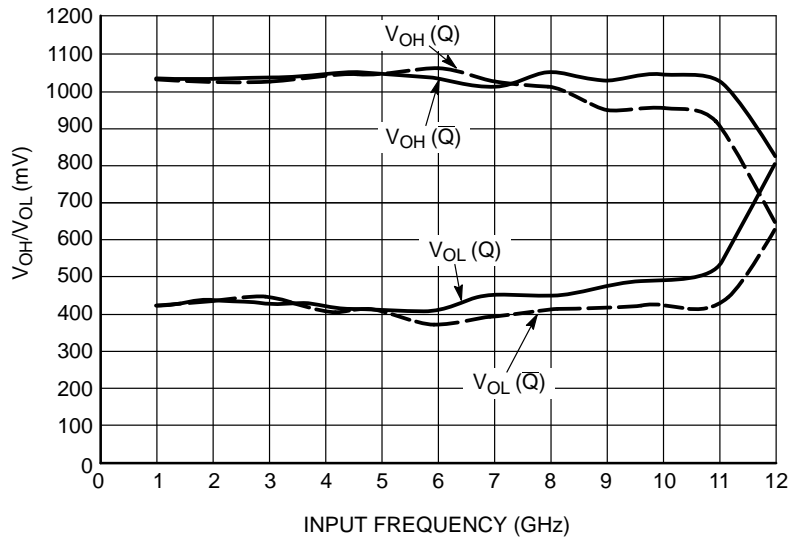


Figure 8. V_{OH}/V_{OL} (Q/ \bar{Q}) vs. Input Frequency (f_{in}) for DIV/2 Mode ($V_{CC} - V_{EE} = 3.3$ V @ 25°C and OLS = $V_{CC} - 0.8$ V, OLS = FLOAT)

NBSG53A

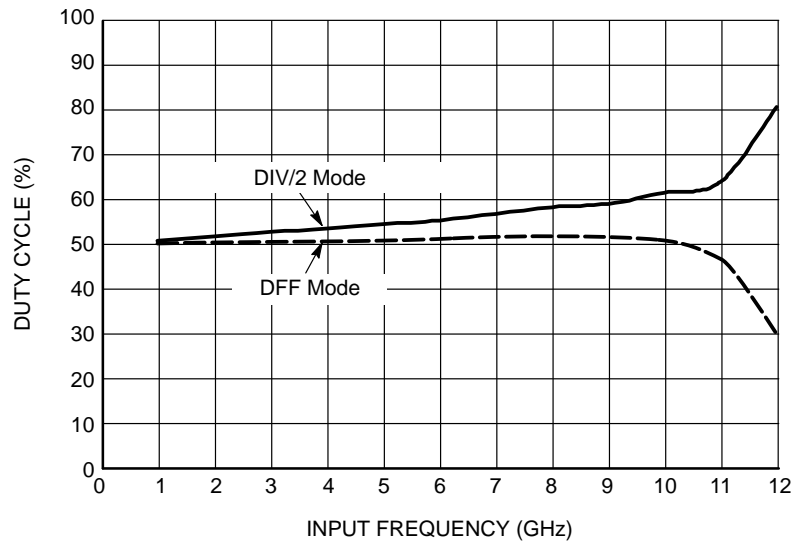


Figure 9. Duty Cycle % vs. Input Frequency (f_{in})
($V_{CC} - V_{EE} = 3.3 \text{ V @ } 25^{\circ}\text{C}$)

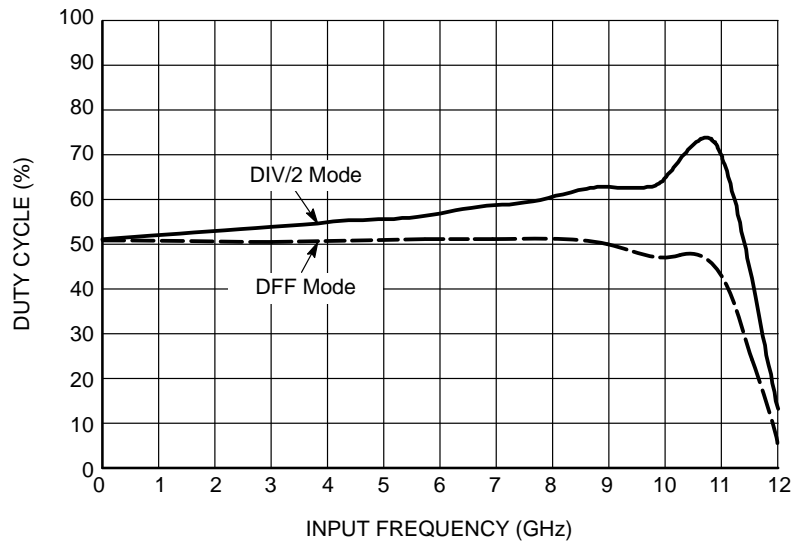


Figure 10. Duty Cycle % vs. Input Frequency (f_{in})
($V_{CC} - V_{EE} = 2.5 \text{ V @ } 70^{\circ}\text{C}$)

NBSG53A

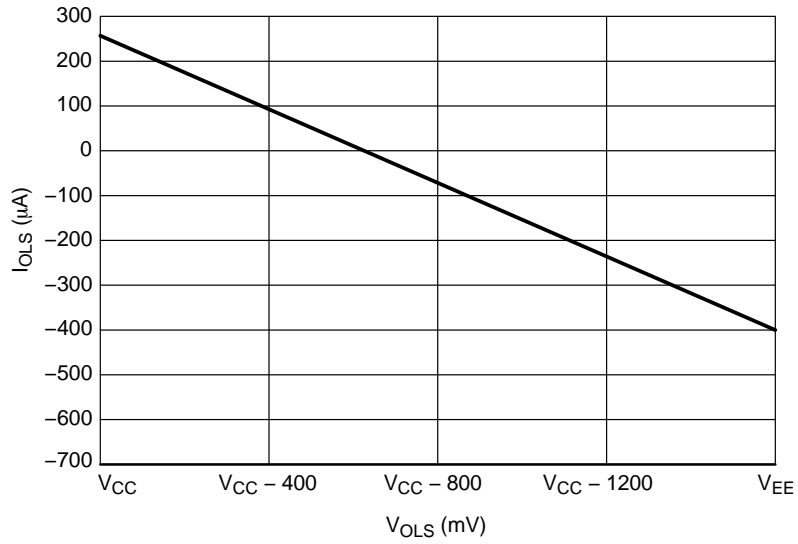


Figure 11. Typical OLS Input Current vs. OLS Input Voltage
 $(V_{CC} - V_{EE} = 3.3 \text{ V @ } 25^\circ\text{C})$

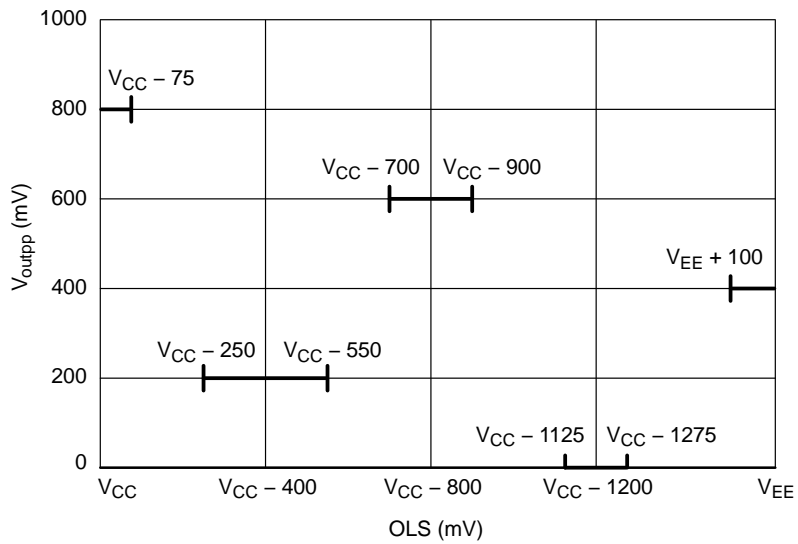


Figure 12. OLS Operating Area

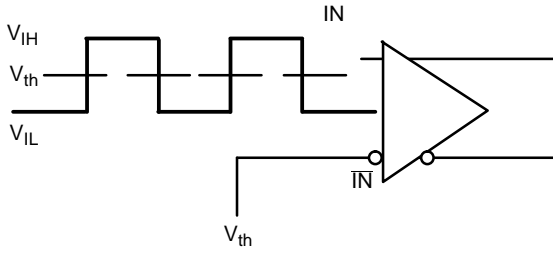


Figure 13. Differential Input Driven Single-Ended

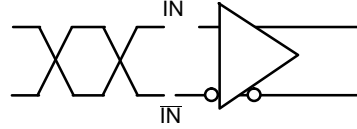


Figure 14. Differential Inputs Driven Differentially

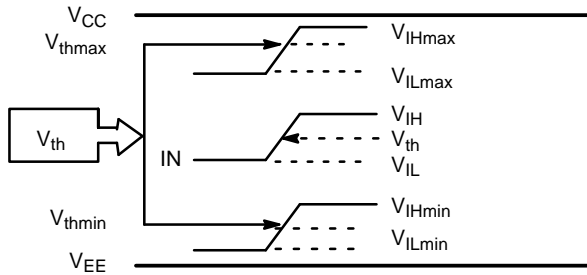


Figure 15. V_{th} Diagram

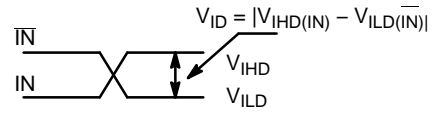


Figure 16. Differential Inputs Driven Differentially

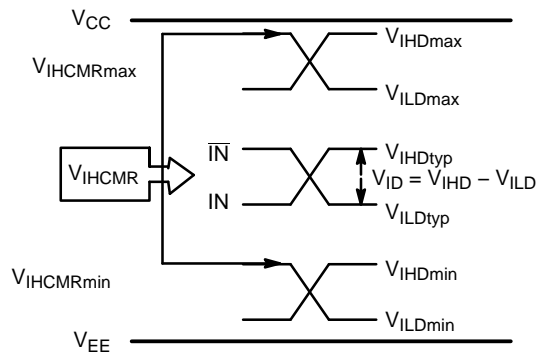


Figure 17. V_{IHCMR} Diagram

NBSG53A

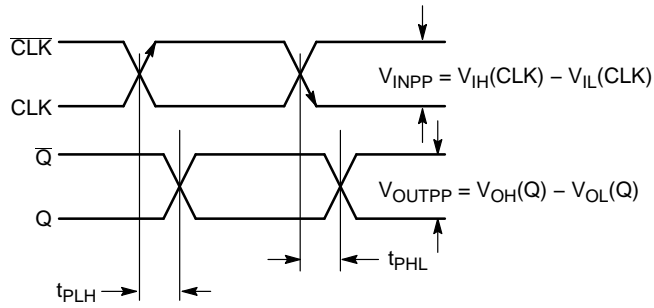


Figure 18. AC Reference Measurement

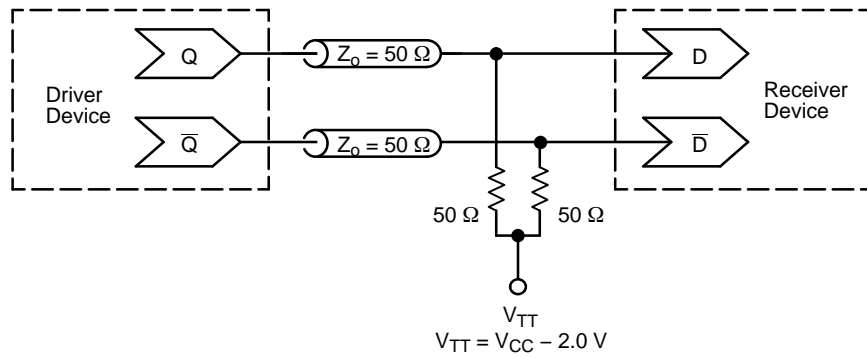


Figure 19. Typical Termination for Output Driver and Device Evaluation
(Refer to Application Note AND8020/D – Termination of ECL Logic Devices)

ORDERING INFORMATION

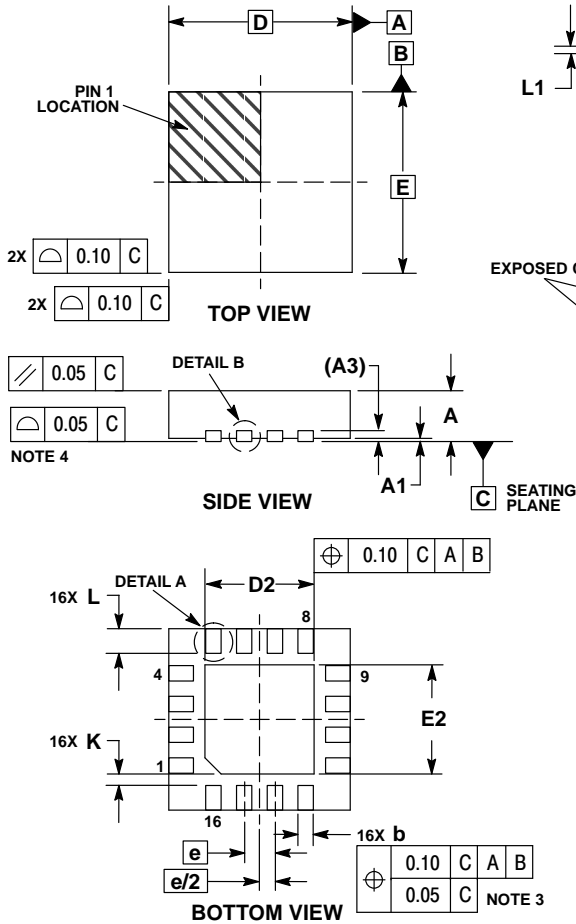
| Device | Package Type | Shipping [†] |
|---------------|---|-----------------------|
| NBSG53AMNG | QFN-16, 3x3 mm (Pb-Free / Halide-Free) | 123 Units / Tube |
| NBSG53AMNR2G | QFN-16, 3x3 mm (Pb-Free / Halide-Free) | 3000 / Tape & Reel |
| NBSG53AMNHTBG | QFN-16 (Pb-Free / Halide-Free) | 100 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NBSG53A

PACKAGE DIMENSIONS

QFN16 3x3, 0.5P
CASE 485G
ISSUE F

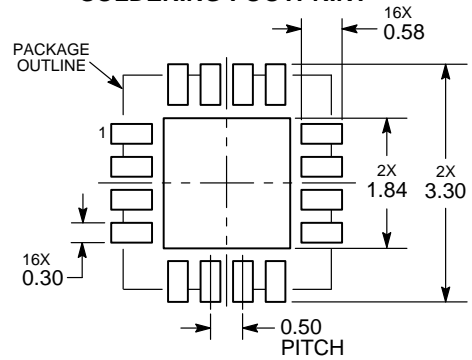


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.03 | 0.05 |
| A3 | 0.20 REF | | |
| b | 0.18 | 0.24 | 0.30 |
| D | 3.00 BSC | | |
| D2 | 1.65 | 1.75 | 1.85 |
| E | 3.00 BSC | | |
| E2 | 1.65 | 1.75 | 1.85 |
| e | 0.50 BSC | | |
| K | 0.18 TYP | | |
| L | 0.30 | 0.40 | 0.50 |
| L1 | 0.00 | 0.08 | 0.15 |

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The products described herein (NBSG53A), may be covered by U.S. patents including 6,362,644. There may be other patents pending. GigaComm is a trademark of Semiconductor Components Industries, LLC.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor:](#)

[NBSG53AMNG](#) [NBSG53AMNR2G](#) [NBSG53AMNHTBG](#)