# LED Drivers with Active Power Factor Correction and Phase Dimming Decoder

## Check for Samples: LM3450

## FEATURES

- **Critical Conduction Mode PFC**
- **Over-Voltage Protection**
- **Feedback Short Circuit Protection**
- **70:1 PWM Decoded From Phase Dimmer**
- **Analog Dimming**
- **Programmable Dimming Range**
- **Digital Angle and Dimmer Detection**
- **Dynamic Holding Current**
- **Smooth Dimming Transitions**
- **Low Power Operation**
- **Start-Up Pre-Regulator Bias**
- **Precision Voltage Reference**

## APPLICATIONS

- **Dimmable Downlights, Troffers, and Lowbays**
- **Large Form Factor Bulbs**
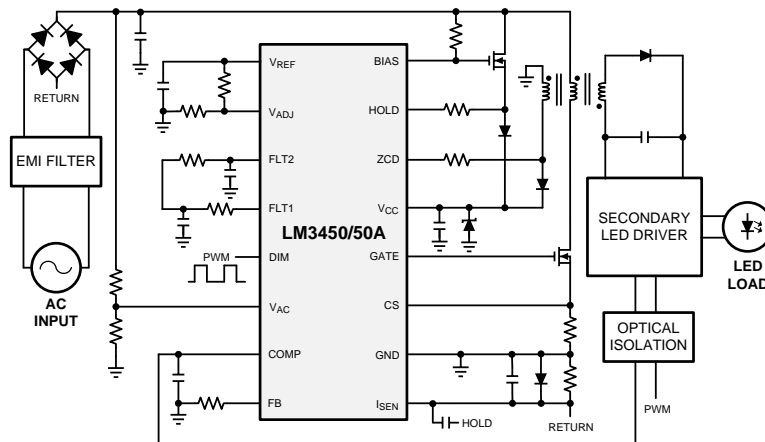- **Indoor and Outdoor Area SSL**
- **Power Supply PFC**

## DESCRIPTION

The LM3450/50A is a power factor controller (PFC) with separate phase dimming decoder. The PFC regulates the output voltage while maintaining excellent power factor. The phase dimming decoder interprets the phase angle and remaps it to a 500Hz PWM output. This device is ideal for implementing a dimmable off-line LED driver for 10-100W loads.

The phase dimming decoder has several unique features. The input-output mapping is programmable for design flexibility, while a dynamic filter and variable sampling rate provide smooth uniform dimming. A dynamic hold circuit ensures that the phase dimmer angle is decoded properly while minimizing extra power loss.

The LM3450A is identical to the LM3450 with the exception of one circuit operation. The dynamic hold current is sampled in the LM3450 while it continuously operates in the LM3450A. This difference between the two devices defines the suitable applications for each. The following is a general guideline for choosing the correct device:

- Any 120V designs with $P_{OUT}$ > 15W - LM3450A
- Any 230V designs with $P_{OUT}$ > 25W - LM3450A
- 120V 2-Stage designs with $P_{OUT}$ < 15W - LM3450
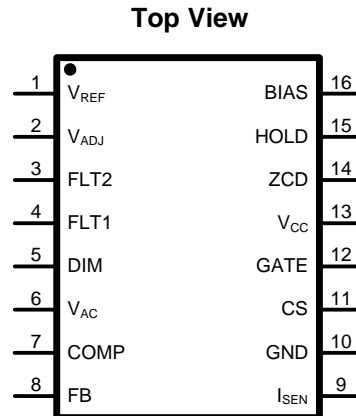- 230V 2-Stage designs with $P_{OUT}$ < 25W - LM3450

## Typical Application

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## Connection Diagram

**Top View**



**Figure 1. 16-Lead TSSOP
Package Number PW**

## PIN DESCRIPTIONS

| Pin | Name | Description | Application Information |
|-----|------|-------------|-------------------------|
| 1 | $V_{REF}$ | 3V Reference | Reference Output: Connect directly to $V_{ADJ}$ or to resistor divider feeding $V_{ADJ}$ and to necessary external circuits. |
| 2 | $V_{ADJ}$ | Analog Adjust | Analog Dim and Phase Dimming Range Input: Connect directly to $V_{REF}$ to force standard 70% phase dimming range. Connect to resistor divider from $V_{REF}$ to extend usable range of some phase dimmers or for analog dimming. Connect to GND for low power mode. |
| 3 | FLT2 | Filter 2 | Ramp Comparator Input: Connect a series resistor from FLT1 capacitor and a capacitor to GND to establish second filter pole. |
| 4 | FLT1 | Filter 1 | Angle Decoder Output: Connect a series resistor to a capacitor to GND to establish first filter pole. |
| 5 | DIM | 500 Hz PWM Output | Open Drain PWM Dim Output: Connect to dimming input of output stage LED driver (directly or with isolation) to provide decoded dimming command. |
| 6 | $V_{AC}$ | Sampled Rectified Line | Multiplier and Angle Decoder Input: Connect to resistor divider from rectified AC line. |
| 7 | COMP | Compensation | Error Amplifier Output and PWM Comparator Input: Connect a capacitor to GND to set the compensation. |
| 8 | FB | Feedback | Error Amplifier Inverting Input: Connect to output voltage via resistor divider to control PFC voltage loop for non-isolated designs. Connect a 5.11kΩ resistor to GND for isolated designs (bypasses error amplifier). Also includes over-voltage protection and shutdown modes. |
| 9 | $I_{SEN}$ | Input Current Sense | Input Current Sense Non-Inverting Input: Connect to diode bridge return and resistor to GND to sense input current for dynamic hold. Connect a 0.1µF capacitor and Schottky diode to GND, and a 0.22µF capacitor to HOLD. |
| 10 | GND | Power Ground | System Ground |
| 11 | CS | Current Sense | MosFET Current Sense Input: Connect to positive terminal of sense resistor in PFC MosFET source. |
| 12 | GATE | Gate Drive | Gate Drive Output: Connect to gate of main power MosFET for PFC. |
| 13 | $V_{CC}$ | Input Supply | Power Supply Input: Connect to primary bias supply. Connect a 0.1µF bypass capacitor to ground. |
| 14 | ZCD | Zero Crossing Detector | Demagnetization Sense Input: Connect a 100kΩ resistor to transformer/inductor winding to detect when all energy has been transferred. |
| 15 | HOLD | Dynamic Hold | Open Drain Dynamic Hold Input: Connect to holding resistor which is connected to source of passFET. |
| 16 | BIAS | Pre-regulator Gate Bias | Pre-regulator Gate Bias Output: Connect to gate of passFET and through resistor to rectified AC (drain of passFET) to aid with startup. |

Product Folder Links: *LM3450*

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS [1][2]

| | |
|---|---|
| $V_{CC}$, HOLD, DIM, BIAS | -0.3V to 25.0V |
| HOLD Power | 250 mW Continuous |
| BIAS Current | 5.0mA Continuous |
| ZCD Current | +/- 10mA |
| COMP, FB, $V_{AC}$, FLT1, FLT2, $V_{REF}$, CS, $V_{ADJ}$ | -0.3V to 7.0V |
| $I_{SEN}$ | -7.0V to 7.0V |
| GATE | -0.3V to 18V Continuous<br>-2.5V for 100ns<br>20.5V for 100ns<br>-1mA to +1mA Continuous |
| Continuous Power Dissipation | Internally Limited |
| Maximum Junction Temperature | Internally Limited |
| Storage Temperature Range | -65°C to +150°C |
| Maximum Lead Temperature (Solder and Reflow) [3] | 260°C |
| ESD Susceptibility [4] | HBM | 2kV |
| | MM | 200V |
| | FICDM | 750V |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and do not imply ensured performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin, unless otherwise specified.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Refer to http://www.ti.com/packaging for more detailed information and mounting techniques.
(4) Human Body Model, applicable std. JESD22-A114-C. Machine Model, applicable std. JESD22-A115-A. Field Induced Charge Device Model, applicable std. JESD22-C101-C.

## OPERATING CONDITIONS [1]

| | |
|---|---|
| $V_{CC}$ Range | 8.5V to 20V |
| Junction Temperature Range | -40°C to +125°C |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and do not imply ensured performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin, unless otherwise specified.

# ELECTRICAL CHARACTERISTICS[1]

Unless otherwise specified $V_{CC}$ = 14V. Specifications in standard type face are for $T_J$ = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J$ = −40°C to +125°C). Typical values represent the most likely parametric norm at $T_A = T_J$ = +25°C, and are provided for reference purposes only.

| Symbol | Parameter | Conditions | Min[2] | Typ[3] | Max[2] | Units |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE INPUT (V$_{CC}$)** | | | | | | |
| $V_{CC-RISE}$ | Controller Enable Threshold | $V_{CC}$ Rising | **12.2** | 13.0 | **13.6** | V |
| $V_{CC-FALL}$ | Controller Disable Threshold | $V_{CC}$ falling | **7.4** | 7.9 | **8.5** | |
| | Glitch Filter Delay | | | 9 | | μs |
| | Turn-on Delay | | | 40 | | |
| $I_Q$ | $V_{CC}$ Quiescent Current | No Switching | | 1.6 | | mA |
| $I_{Q-SD}$ | $V_{CC}$ Shutdown Current | $V_{FB}$ = 0V | | 515 | **625** | μA |
| **ERROR AMPLIFIER & COMPENSATION (FB, COMP)** | | | | | | |
| $V_{FB}$ | FB Reference (Normal Operation) | | **2.43** | 2.50 | **2.57** | V |
| | Input Bias Current | $V_{FB}$ = 2.5V | | 100 | | nA |
| $G_M$ | Transconductance | $V_{FB}$ =2.5V | **69** | 115 | **161** | μS |
| | Output Source / Sink Capability | | **60** | 85 | **110** | μA |
| | FB Pull-up Current Source | $V_{FB}$ < 1.8V | **43** | 51 | **59** | |
| | COMP Pull-up Resistor | | | 5 | | kΩ |
| $V_{CMP-B}$ | COMP Low Threshold (Burst) | $V_{CMP}$ Falling | | $V_{THM}$ -0.08 | | V |
| | COMP Low Hysteresis | | | 20 | | mV |
| $V_{FB-SD}$ | Low Threshold (Shutdown) | $V_{FB}$ Falling | **150** | 168 | **186** | |
| | FB Low Hysteresis | | | 20 | | |
| $V_{FB-EAD}$ | FB Mid Threshold (EA Disabled) | $V_{FB}$ Falling | **328** | 346 | **368** | |
| | FB Mid Hysteresis | | | 20 | | |
| $V_{FB-OV}$ | FB High Threshold (Over-voltage) | | | 1.20 x $V_{FB}$ | **1.22 x V$_{FB}$** | V |
| | COMP Pre-bias Source Current | $V_{CMP}$= 0.5V | | 415 | | μA |
| $V_{THM}$ | Minimum COMP Voltage (Normal) | | | 1.47 | | V |
| **ANGLE DEMODULATION & MULTIPLIER (COMP, V$_{AC}$)** | | | | | | |
| $V_{AC-DET}$ | $V_{AC}$ Angle Detection Threshold | | **334** | 356 | **378** | mV |
| | Angle Demodulation Delay Time | Both edges | | 8 | | μs |
| | VAC Dynamic Input Voltage Range | | 0 to 5.5 | | | V |
| | COMP Dynamic Input Voltage Range | | $V_{THM}$ to $V_{THM}$+2 | | | |
| | $V_{AC}$ Input Impedance | | | 500 | | kΩ |
| $K_M$ | Multiplier Gain (Includes Internal Resistor Divider) | $V_{AC}$ = 3V, $V_{CMP}$ = $V_{THM}$+1.5V | | 0.5 | | 1/V |
| **ZERO CURRENT DETECTOR (ZCD)** | | | | | | |
| $V_{ZCD-RIS}$ | ZCD Input Threshold | $V_{ZCO}$Rising | **1.45** | 1.5 | **1.55** | V |
| | Hysteresis | | **150** | 200 | **250** | mV |
| | Delay to Output | | | 135 | | ns |
| $V_{ZCD-H}$ | Positive Clamp Voltage | $I_{ZCO}$ = 1mA | | 6.0 | | V |
| $V_{ZCD-L}$ | Negative Clamp Voltage | $I_{ZCO}$ = −50μA | | 0.61 | | |
| **PWM COMPARATOR (CS)** | | | | | | |
| $V_{OS}$ | PWM Comparator Input Offset Voltage | | | 30 | | mV |

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified and do not imply ensured performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table. All voltages are with respect to the potential at the GND pin, unless otherwise specified.

(2) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

(3) Typical numbers are at 25°C and represent the most likely norm.

# ELECTRICAL CHARACTERISTICS[1] (continued)

Unless otherwise specified $V_{CC}$ = 14V. Specifications in standard type face are for $T_J$ = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** ( $T_J$ = −40°C to +125°C). Typical values represent the most likely parametric norm at $T_A = T_J$ = +25°C, and are provided for reference purposes only.

| Symbol | Parameter | Conditions | Min[2] | Typ[3] | Max[2] | Units |
|---|---|---|---|---|---|---|
| | PWM Comparator Input Bias Current | | | 20 | | nA |
| $V_{LIM}$ | CS Current Limit Threshold | | **1.40** | 1.50 | **1.60** | V |
| | CS Delay to Output | | | 100 | | ns |
| | CS Blanking Sinking Impedance | | | 1 | | kΩ |
| $t_{LEB}$ | Leading Edge Blanking (LEB) Time | | | 140 | | ns |
| **ANALOG ADJUST INPUT ($V_{ADJ}$)** | | | | | | |
| $V_{ADJ-LP}$ | $V_{ADJ}$ Low Threshold (Low Power Mode) | $V_{ADJ}$ Falling | **56** | 75 | | mV |
| | $V_{ADJ}$ Low Hysteresis | | | 50 | | |
| | $V_{ADJ}$ Pull-up Current Source | | | 1 | | µA |
| | $V_{ADJ}$ Open Voltage | $V_{ADJ}$ Open | | 3 | | V |
| **DYNAMIC HOLD CIRCUIT (HOLD, $I_{SEN}$)** | | | | | | |
| $R_{DSON-HD}$ | HOLD MosFET On-Resistance | ISEN Short to GND | **22** | 30 | **42** | Ω |
| $V_{SEN-REF}$ | $I_{SEN}$ Reference Voltage | | **162** | 200 | **232** | mV |
| | $I_{SEN}$ Bias Current | | | 5 | | µA |
| **PRE-REGULATOR GATE DRIVE OUTPUT (BIAS)** | | | | | | |
| $V_{BIAS}$ | BIAS High Voltage @ 100µA | $V_{CC} < V_{CC-FALL}$ | **18.8** | 21 | **22.6** | V |
| | BIAS Low Voltage @ 100µA | $V_{CC} > V_{CC-RISE}$ | **13.5** | 14 | **14.5** | |
| **GATE DRIVER OUTPUT (GATE)** | | | | | | |
| $V_{GATE-H}$ | GATE Voltage High | $I_{GATE}$ = 20mA | | 11.5 | | V |
| | | $I_{GATE}$ = 200mA | | 10.5 | | |
| | GATE Pull Down Resistance | | | 2 | **8** | Ω |
| | GATE Peak Current | | | [4]±1.5 | | A |
| **REFERENCE VOLTAGE OUTPUT ($V_{REF}$)** | | | | | | |
| $V_{REF}$ | Reference Voltage | No Load | **2.85** | 3 | **3.15** | V |
| | Current Limit | | **1.5** | 2.0 | **3.0** | mA |
| **DIMMING OUTPUT (DIM, FLT1, FLT2)** | | | | | | |
| | FLT1 Output Impedance | Standby Mode | | 500 | | kΩ |
| | | Transition mode | | 1.6 | | |
| | Triangle Waveform Compared to FLT2 | High | | 1.49 | | V |
| | | Low | | 15 | | mV |
| $f_{DIM}$ | DIM Frequency | | **180** | 460 | **700** | Hz |
| **OFF-TIMERS** | | | | | | |
| $t_{OFF-MAX}$ | Maximum Off-Time (Normal Operation) | | | 340 | | µs |
| $t_{OFF-LP}$ | Off-Time (Low Power Mode) | | | 42 | | |
| **THERMAL SHUTDOWN** | | | | | | |
| | Thermal Limit Threshold | [4] | | 160 | | °C |
| | Thermal Limit Hysteresis | | | 20 | | |
| **THERMAL RESISTANCE** | | | | | | |
| $\theta_{JA}$ | Junction to Ambient | TSSOP-16 [4][5] | | 38.0 | | °C/W |
| $\theta_{JC}$ | Junction to Case | | | 10.0 | | |

(4) These electrical parameters are specified by design, and are not verified by test.
(5) Junction-to-ambient thermal resistance is highly board-layout dependent. In applications where high maximum power dissipation exists, namely driving a large MOSFET at high switching frequency from a high input voltage, special care must be paid to thermal dissipation issues during board design. In high-power dissipation applications, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A-MAX}$) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C for Q1, or 150°C for Q0), the maximum power dissipation of the device in the application ($P_{D-MAX}$), and the junction-to ambient thermal resistance of the package in the application ($\theta_{JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} − (\theta_{JA} \times P_{D-MAX})$.

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$=+25°C and $V_{CC}$ = 14V unless otherwise specified
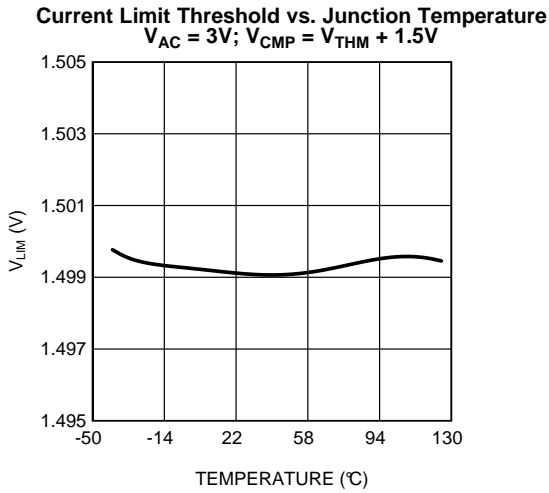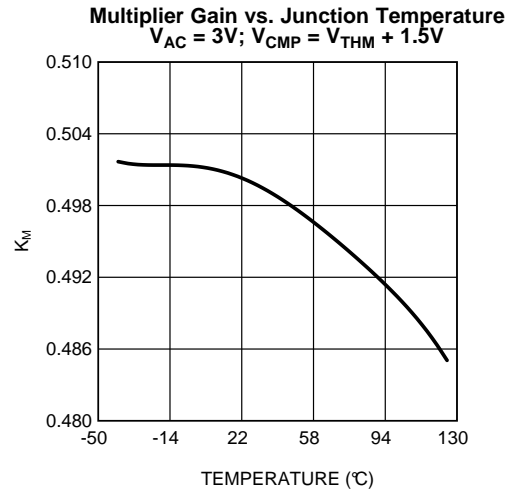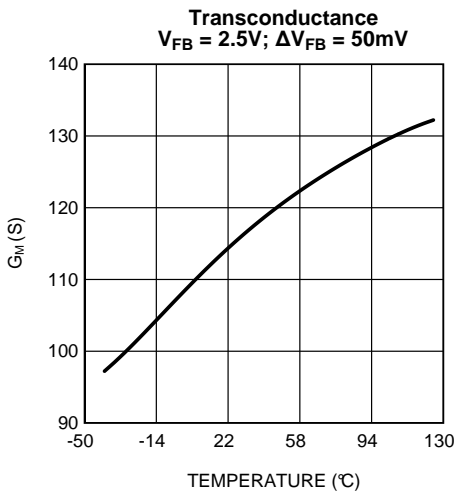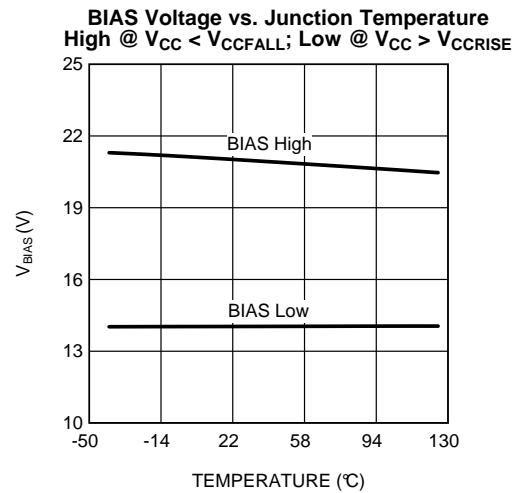
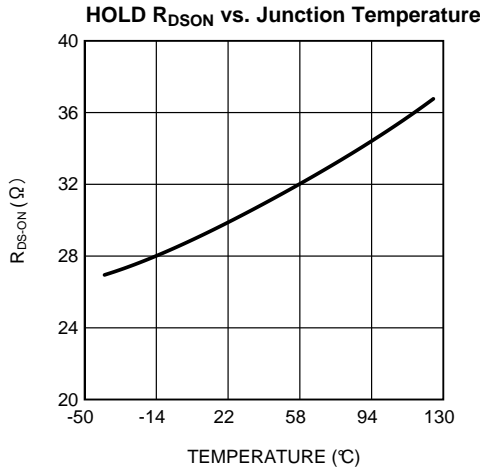**HOLD $R_{DSON}$ vs. Junction Temperature**
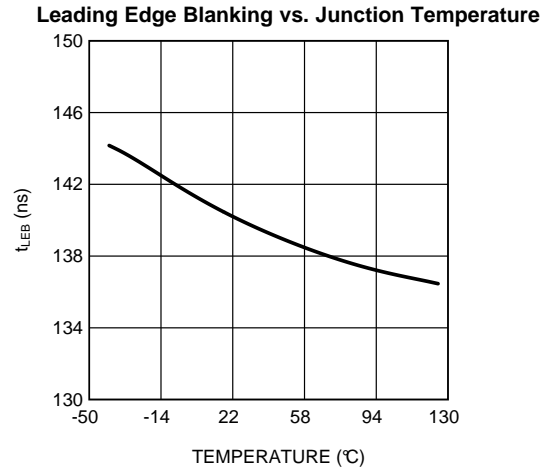


**Figure 2.**

**Leading Edge Blanking vs. Junction Temperature**



**Figure 3.**

**Current Limit Threshold vs. Junction Temperature**
$V_{AC}$ = 3V; $V_{CMP}$ = $V_{THM}$ + 1.5V



**Figure 4.**

**Multiplier Gain vs. Junction Temperature**
$V_{AC}$ = 3V; $V_{CMP}$ = $V_{THM}$ + 1.5V



**Figure 5.**

**Transconductance**
$V_{FB}$ = 2.5V; $\Delta V_{FB}$ = 50mV



**Figure 6.**

**BIAS Voltage vs. Junction Temperature**
High @ $V_{CC}$ < $V_{CCFALL}$; Low @ $V_{CC}$ > $V_{CCRISE}$



**Figure 7.**

Product Folder Links: *LM3450*

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$=+25°C and $V_{CC}$ = 14V unless otherwise specified

**$V_{CC}$ UVLO Threshold vs. Junction Temperature**
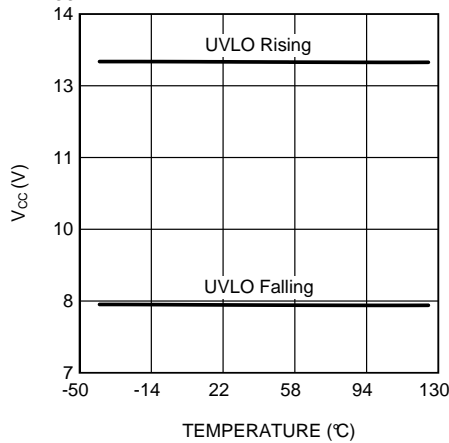


**Figure 8.**

**Shutdown Current vs. Junction Temperature**
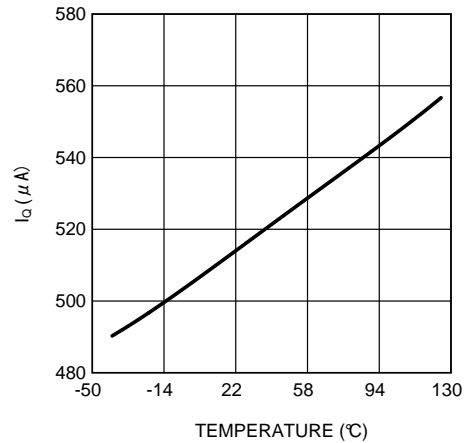


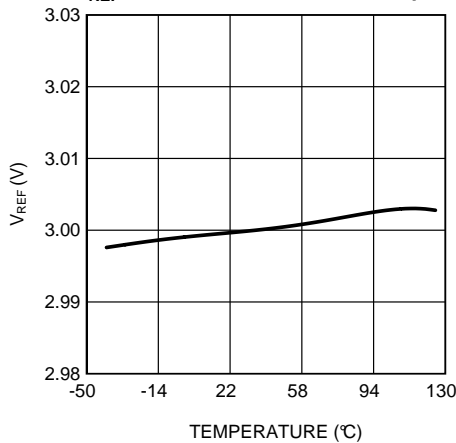**Figure 9.**

**$V_{REF}$ Reference vs. Junction Temperature**

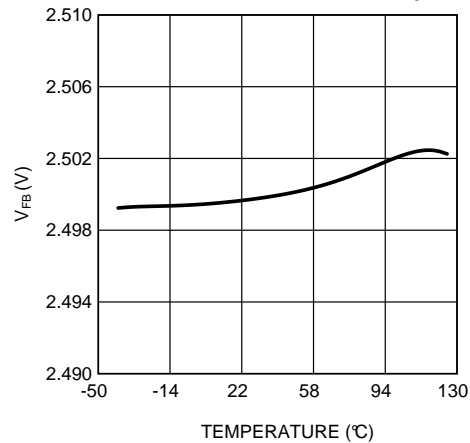

**Figure 10.**

**FB Reference vs. Junction Temperature**
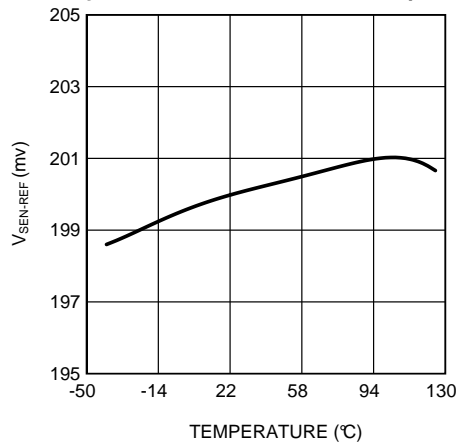


**Figure 11.**

**$I_{SEN}$ Reference vs. Junction Temperature**



**Figure 12.**
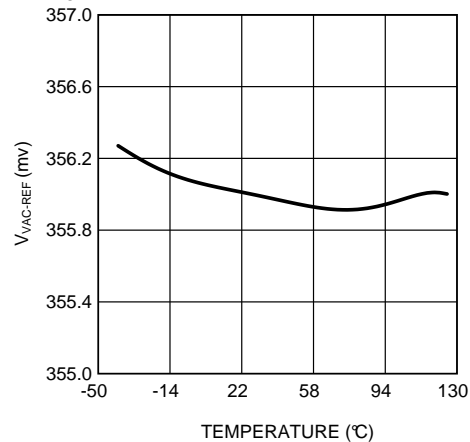
**$V_{AC}$ Detection Threshold vs. Junction Temperature**



**Figure 13.**

Product Folder Links: *LM3450*

# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$T_A$=+25°C and $V_{CC}$ = 14V unless otherwise specified

**Transconductance vs. $V_{FB}$**



**Figure 14.**

**Current Sense Threshold vs. $V_{COMP}$ and $V_{AC}$**



**Figure 15.**
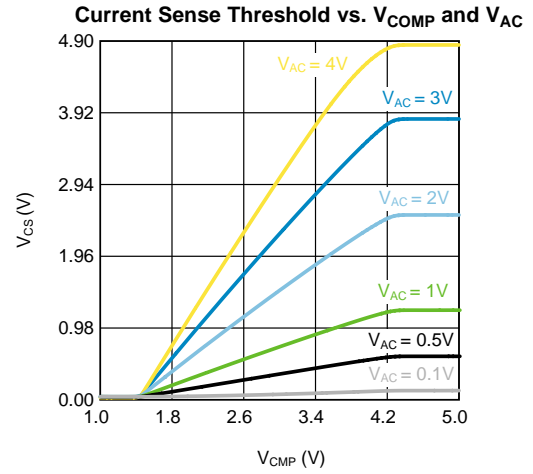
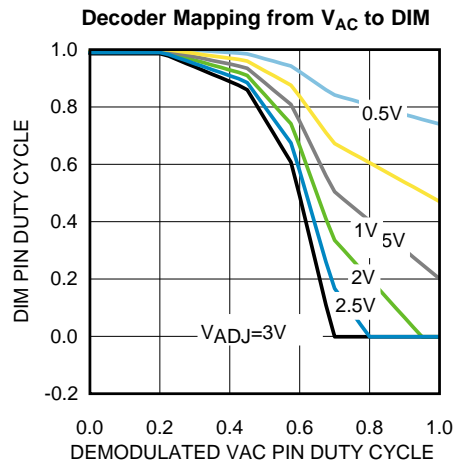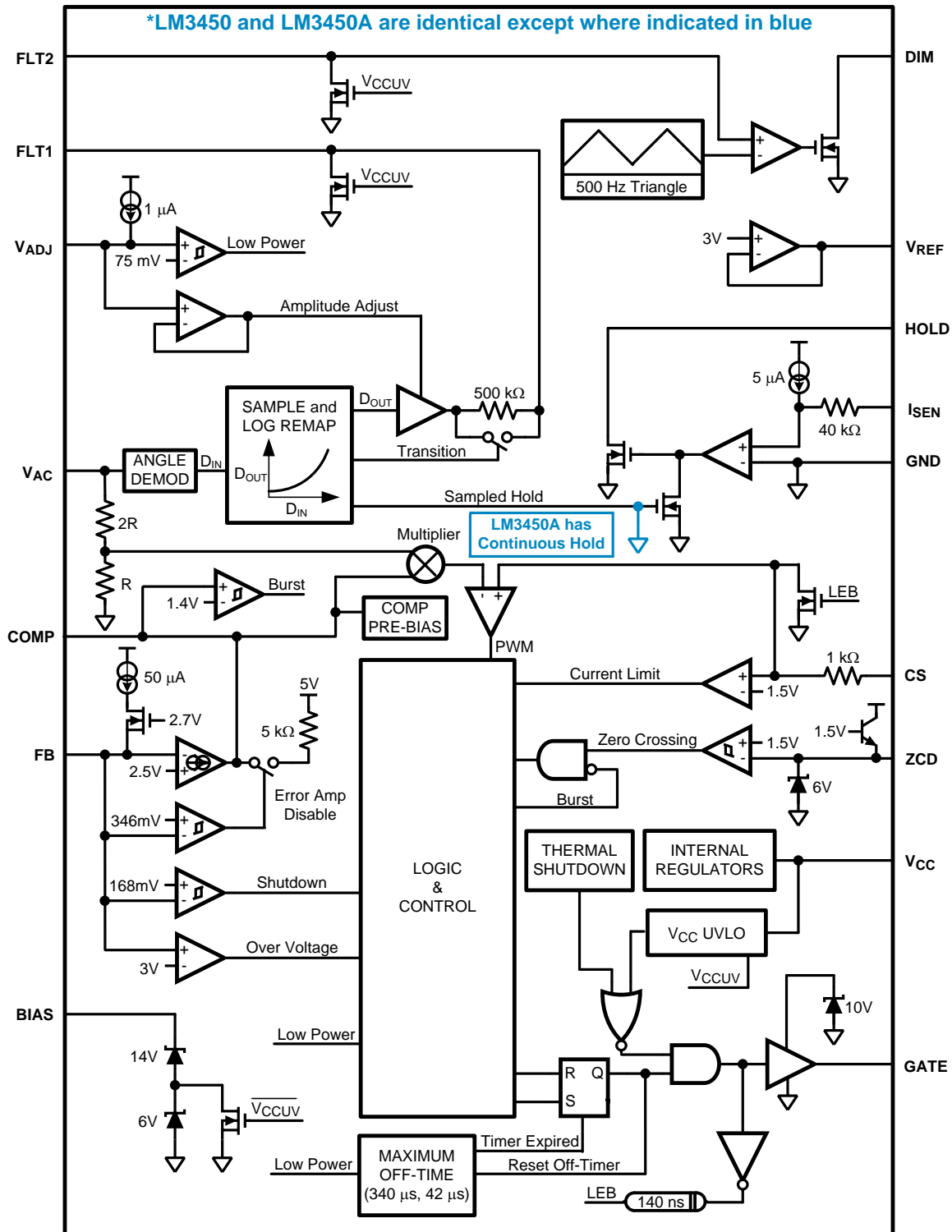**Decoder Mapping from $V_{AC}$ to DIM**
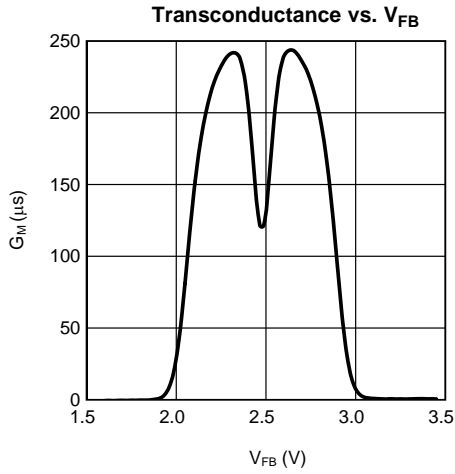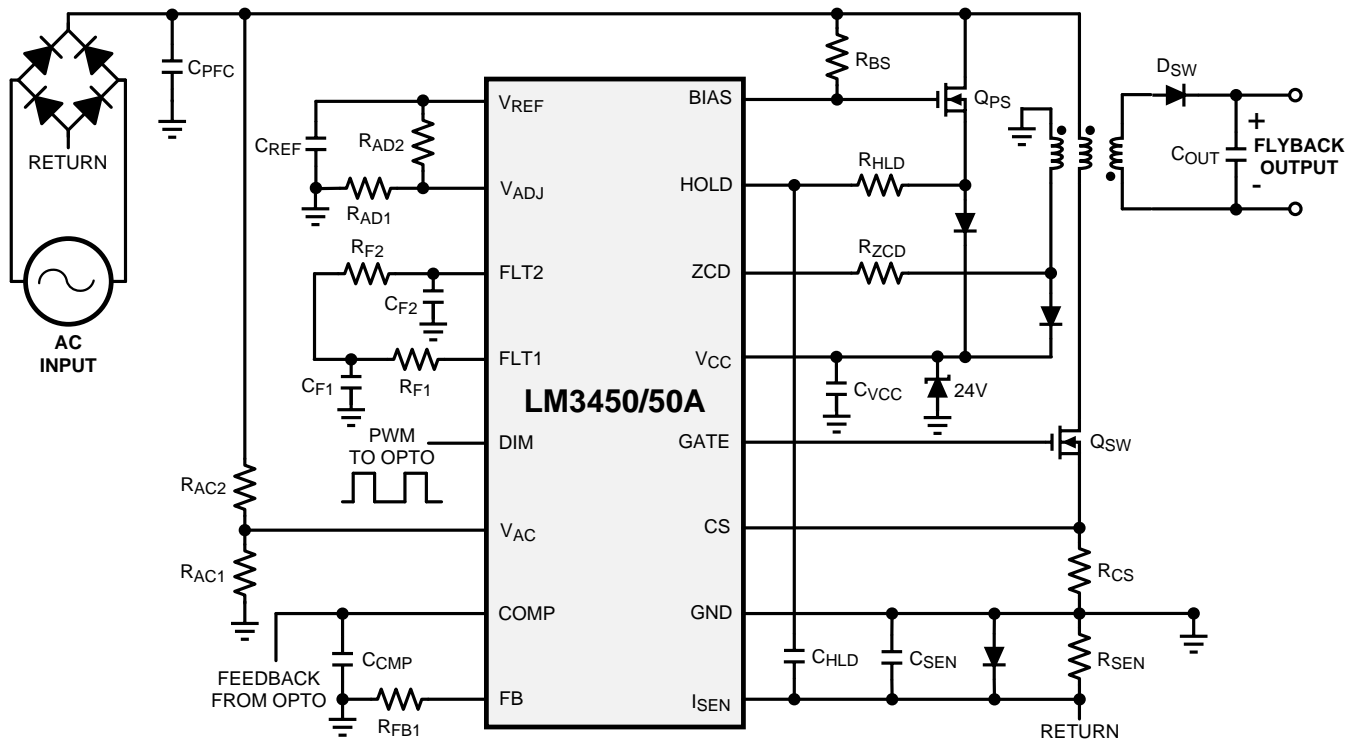


**Figure 16.**

# BLOCK DIAGRAM

**Figure 17. Typical Flyback Application**

## THEORY OF OPERATION

The LM3450/50A is a single device with both power factor control (PFC) and phase dimming decoder functions. This device is designed to control isolated flyback converters and provide active power factor correction. In addition to being a PFC, the LM3450/50A can interpret a phase dimming (frequently called triac dimming) input and provide a corresponding PWM output to properly dim an LED load. This combination of features provides an excellent method to convert a standard AC mains input to a dimmable LED output of 10-100W. It should be noted that the LM3450/50A can control a boost converter in a similar manner. However, this datasheet will focus mostly on the flyback topology due to the high demand for isolated LED driver applications. Discussion of the LM3450/50A functionality will refer to Figure 17 component designators.

The PFC control operates in critical conduction mode (CRM) using zero crossing detection (ZCD) to terminate the off-time. The PFC portion of this device includes an error amplifier, multiplier, current sense circuit, zero crossing detector, and gate driver. The internal error amplifier is used for feedback of the output voltage in non-isolated designs. However, it can be disabled for isolated designs where the error amplifier needs to be on the secondary side.

The phase dimmer decoder detects the dimming angle of the rectified AC line, decodes, filters and remaps it to a 500Hz PWM output. The PWM output can then be sent directly, or through optical isolation, to the dimming input of a second stage LED driver. To ensure the decoder properly interprets the dimming angle, dynamic hold is provided which prevents the phase dimmer from misfiring. The input current is sensed and when the current drops below a preset minimum, the system adds more current.

Both the dynamic hold and the decoder are sampled synchronously in the LM3450 to reduce the overall efficiency drop due to the additional hold current. When a decoding sample period occurs, the dynamic hold is activated to ensure a proper angle is decoded. Because of this sampling method, non-sampled cycles will potentially cause the phase dimmer to misfire but should not affect the output LED current regulation.

For higher power applications, where the dynamic hold provides much less current on average, the LM3450A can be used. The LM3450A has continuous dynamic hold which prevents the dimmer from ever misfiring. This is extremely helpful when designing for single stage solutions, where there is no second stage to provide good line rejection. The continuous dynamic hold is also helpful for the higher power two stage applications where the input capacitance is larger.

One last feature of the phase decoder is a dynamic filter that, combined with the variable sampling rate, provides fast, smooth dimming transitions.
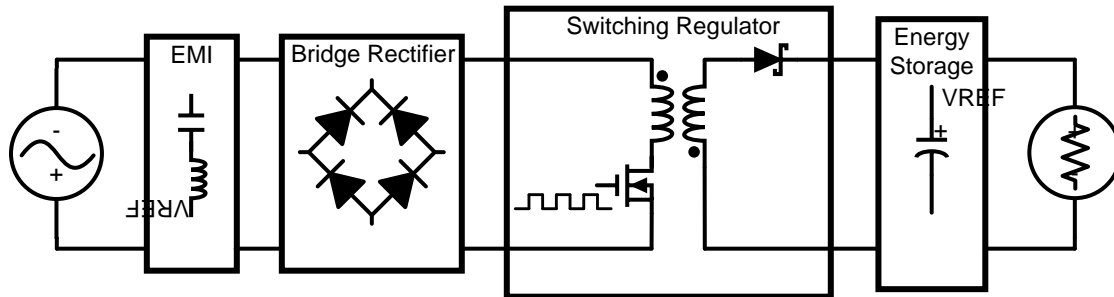


**Figure 18. PFC System Architecture**

## PFC BACKGROUND

Power factor (PF) is a number between 0 and 1 that indicates how well energy is transmitted from input to output of a system. It can be described by average power ($P_{AVG}$), RMS voltage ($V_{RMS}$), and RMS current ($I_{RMS}$):

$$PF = \frac{P_{AVG}}{V_{RMS} \times I_{RMS}}$$

(1)

Or by distortion factor ($K_{DIST}$) and displacement factor ($K_{DISP}$):

$$PF = K_{DIST} \times K_{DISP}$$

(2)

With a purely resistive system, PF = 1. The addition of reactive elements necessary in any converter, such as EMI filters and energy storage, will induce some amount of displacement (phase shift between the input voltage and input current). The addition of switching devices will also create distortion (energy present in the harmonics relative to the switching frequencies). These non-idealities decrease the PF towards zero.

Active power factor correction attempts to make the input impedance look as resistive as possible to the power source. Since the output of the converter is usually a regulated voltage or current, there is a need for large energy storage elements to remove the twice line frequency (100Hz or 120Hz) ripple. A power factor control architecture, as shown in Figure 18, has very little capacitance at the input. Instead, the twice line frequency content is removed with large energy storage capacitance at the output.

Using this control architecture, the converter is able to provide two important functions at the same time:
• Shape the input current
• Regulate the output voltage

The PFC control approach requires two separate control loops to achieve both functions: a fast loop which shapes the input current, and a slow loop that regulates the output voltage.

The fast control loop shapes the input current to have the same sinusoidal shape as the AC input voltage. Assuming both are perfect sinusoids with zero distortion or phase shift, the power factor will be perfect (unity). Unfortunately, distortion is always present in switching converters. An input filter, which is required to comply with EMI standards, helps to attenuate the switching content, thereby reducing distortion. However, the added filter capacitance will increase the phase shift at the same time. Though perfect PF is not achievable within real applications, extremely high PF (>.99) is possible using most active PFCs.

The output voltage has to be regulated slowly to ensure the converter ignores the twice line frequency ripple present on the output. Therefore, the voltage loop containing the error amplifier should have a bandwidth at least an order of magnitude slower (<20Hz is common). Sometimes the bandwidth is increased to improve transient response, which is the case with off-line dimmable LED drivers. Though PF decreases with the increase in bandwidth, high PF (>.95) is still possible.
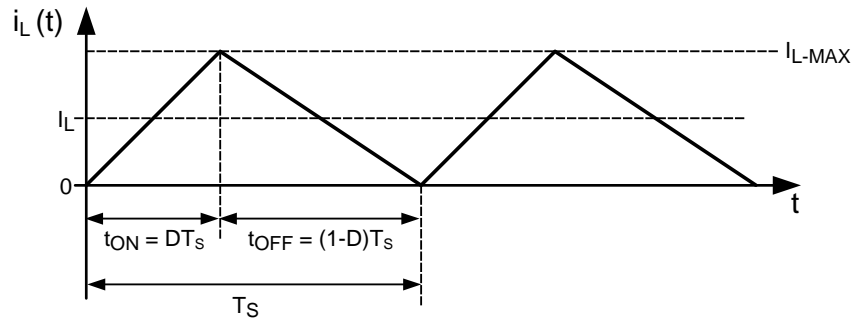


**Figure 19. Basic CRM Inductor Current Waveform**

## CRM BACKGROUND

During critical conduction mode (CRM), a converter operates at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM). This is usually implemented as follows. The main switching MosFET ($Q_{SW}$) is turned on and the inductor current rises to a peak threshold. $Q_{SW}$ is then turned off and the current falls until it reaches zero. At this point, $Q_{SW}$ is turned on and the cycle repeats. Near zero voltage switching, enabled by the inductor current return to zero, gives CRM topologies an efficiency improvement compared to CCM topologies. Figure 19 shows the resulting inductor current waveform, where the average inductor current ($I_L$) is half of the peak current ($I_{L-MAX}$).

In a CRM flyback PFC application, the rectified AC input is fed forward to the control loop, creating a sinusoidal primary peak current envelope ($I_{P-pk}$) as shown in Figure 20. The secondary peak current envelope ($I_{S-pk}$) will simply be a scaled version of the primary according to the turns ratio of the transformer. Assuming good attenuation of the switching ripple via the EMI filter, the average input current ($I_{IN}$), represented by the red line in Figure 20, can also be approximated as a sinusoid proportional to the duty cycle (D(t)):

$$I_{in}(t) = \frac{I_{P-PK} \times D(t)}{2}$$

(3)

Since CRM operation is hysteretic and the input voltage is fed-forward, the input current shaping loop is as fast as possible. Only the output voltage needs to be regulated with a narrow bandwidth error amplifier, which greatly simplifies the system dynamics.
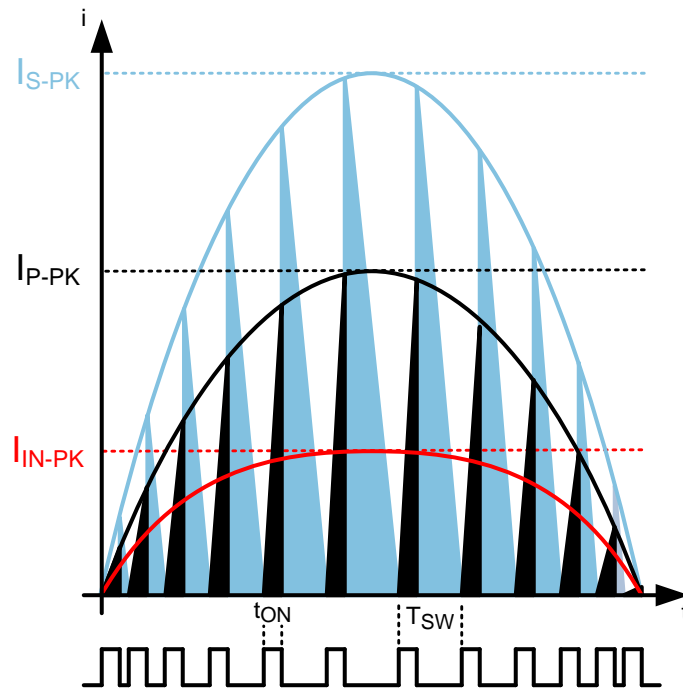
Product Folder Links: *LM3450*

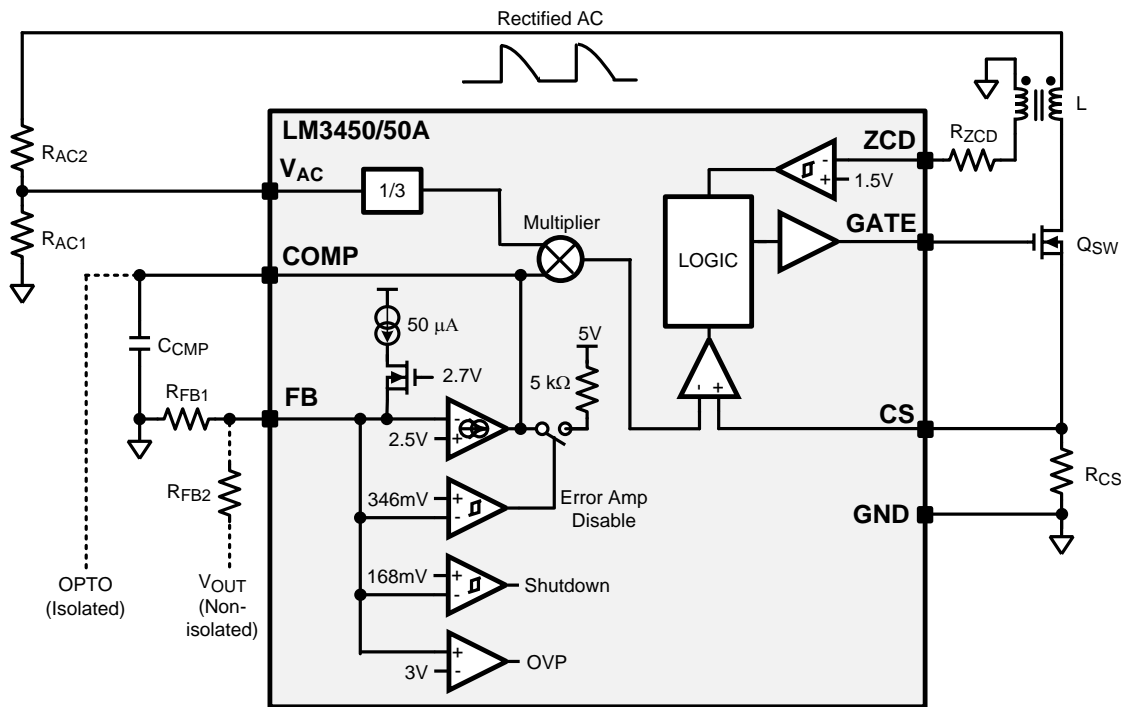**Figure 20. CRM Flyback Current Waveforms**



**Figure 21. PFC Control Circuit**

## POWER FACTOR CONTROLLER

The LM3450/50A uses CRM control to regulate the output voltage and provide power factor correction. In a non-isolated boost topology, an external voltage divider ($R_{FB1}$, $R_{FB2}$) is used to sense the output voltage, as shown in Figure 21. The divider is connected to the inverting input (FB) of the internal error amplifier. The LM3450/50A regulates the feedback voltage ($V_{FB}$) to 2.5V in a closed loop fashion.

The FB pin has a shutdown mode to protect against a feedback short and an OVP mode which terminates switching when output over-voltage is sensed.

With the FB shutdown mode, it is necessary to have a preliminary biasing method for the output of the error amplifier (COMP). Otherwise, the converter would never start. COMP is pre-biased with a 415µA current until the voltage at COMP ($V_{CMP}$) exceeds the minimum operational voltage ($V_{THM}$).

For an isolated flyback topology, where the error amplifier is on the secondary, the LM3450/50A internal error amplifier can be bypassed using a single 5.11kΩ resistor ($R_{FB1}$) from FB to GND. This engages an internal 5kΩ pull-up resistor at COMP. COMP can then be connected directly to the optical isolation as shown in Figure 21.

COMP and the sensed rectified AC input voltage ($V_{AC}$), provided via a resistor divider ($R_{AC1}$, $R_{AC2}$), are inputs to the multiplier. The current through the sense resistor ($R_{CS}$) produces a voltage ($V_{CS}$) that is compared to the multiplier output. When $V_{CS}$ exceeds the multiplier output, $Q_{SW}$ is turned off. The peak detect threshold and the current slope during an on-time are proportionally changing which yields a nearly constant on-time, shown in Figure 20:

$$t_{ON} = \frac{L \times I_{P\text{-}PK}}{V_{IN\text{-}PK}}$$

(4)

Once $Q_{SW}$ is turned off, the LM3450/50A waits until the inductor (boost) or transformer (flyback) is demagnetized to turn $Q_{SW}$ on again. Demagnetization, sensed at ZCD, occurs when the current through the magnetic component falls to zero. Since the output voltage is regulated, the slope of the current remains relatively constant and, coupled with the variable peak detect, creates a variable off-time.

The sinusoidal peak detection envelope creates an input current that is sinusoidal and in phase with the input voltage providing excellent PF. The PWM comparator 30mV input offset voltage ensures current is drawn at the zero-crossings of the AC line, reducing distortion and further improving PF.

## CURRENT SENSE

The LM3450/50A senses current through $Q_{SW}$ via a sense resistor ($R_{CS}$) between the source of $Q_{SW}$ and GND. When $V_{CS}$ exceeds the output of the multiplier ($V_{MLT}$), $Q_{SW}$ is turned off. $V_{MLT}$ is variable over the line cycle and is a function of the scaled rectified AC voltage ($V_{AC}$), the COMP voltage referenced from its operational minimum ($V_{COMP}$-$V_{THM}$), the multiplier gain ($K_M$) and the PWM comparator offset ($V_{OS}$):

$$V_{MLT} = K_M \times V_{AC} \times \left( V_{COMP} - V_{THM} \right) + V_{OS}$$

(5)

The LM3450/50A has a leading edge blanking (LEB) circuit that pulls the current sense input to the PWM comparator low for 140µs at the beginning of each on-time. The LEB blanks the current spike and associated ringing due to the turn-on transient of $Q_{SW}$, limiting the minimum achievable duty cycle.

## OVER CURRENT PROTECTION

The LM3450/50A has a current limit threshold ($V_{LIM}$ = 1.5V) at CS to protect the system from over-current conditions. If $V_{CS}$ exceeds $V_{LIM}$, $Q_{SW}$ is immediately turned off until ZCD triggers a new on-time.
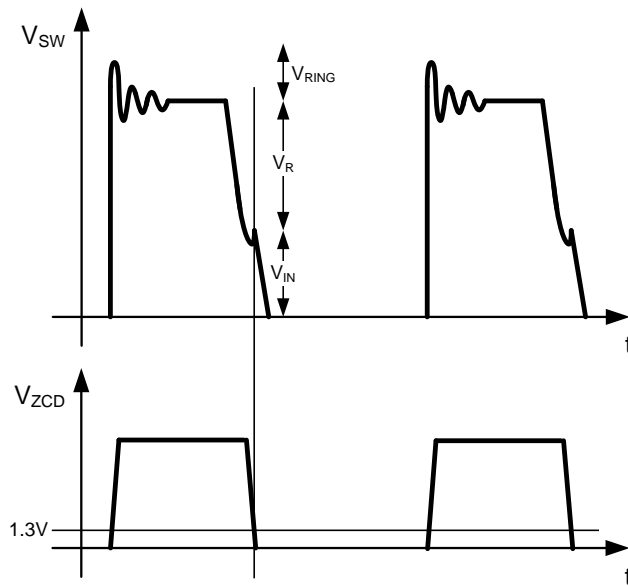
Product Folder Links: *LM3450*

**Figure 22. ZCD Waveforms for Flyback Design**

## ZERO CURRENT DETECTION

ZCD is implemented with a 100kΩ resistor from the ZCD pin to a coupled winding on the transformer or inductor as shown in Figure 21. This winding is also used to bootstrap $V_{CC}$ after start-up. When $Q_{SW}$ turns off, the voltage at the ZCD pin ($V_{ZCD}$) increases as energy is transferred through the auxiliary winding. The circuit arms when $V_{ZCD}$ exceeds 1.5V. Then, when the energy is fully transferred, $V_{ZCD}$ decreases towards zero. When $V_{ZCD}$ falls below 1.3V, the transformer is assumed to be demagnetized, the circuit disarms, and $Q_{SW}$ is turned back on as shown in Figure 22. The ZCD pin voltage will remain low until $Q_{SW}$ is turned off via peak detection and the cycle repeats.

## SWITCHING FREQUENCY

With a constant on-time and variable off-time, there is a variable switching frequency:

$$f_{SW} = D(t) \times \left( \frac{V_{IN-PK}}{L \times I_{P-PK}} \right)$$

(6)

Figure 20 shows that the minimum switching frequency occurs at the peak of the rectified AC waveform, while the maximum switching frequency occurs at the valley.

## ERROR AMPLIFIER

The LM3450/50A internal error amplifier is used for non-isolated designs (boost) where the output voltage can be directly sensed, via a resistor divider, at the FB pin. The FB pin is the inverting input of the trans-conductance amplifier which is regulated to 2.5V. The COMP pin is the output of the amplifier and external compensation is placed from COMP to GND in the form of a single capacitor ($C_{CMP}$) as shown in Figure 21, a series resistor and capacitor, or both. The output of the amplifier sources or sinks current as necessary to force the inputs of the amplifier to be equal. The compensation method depends upon the transient performance desired and requires a loop gain analysis. This analysis can be somewhat complex and cumbersome. A detailed analysis can be found Application Notes AN-2098 (literature number SNVA463) and/or AN-2150 (literature number SNVA485).

If the COMP pin voltage ($V_{CMP}$) falls below 1.4V at any time, the device enters burst mode where the GATE is off for 340µs then is turned on. If $V_{CMP}$ is still below 1.4V at the end of the on-time then another 340µs off-time occurs. However, if $V_{CMP}$ has risen above 1.4V, the converter continues switching until it falls below the threshold again. This feature is necessary to prevent the output of the converter from rising arbitrarily high because the minimum on-time of the device prevents less energy transfer.

The LM3450/50A also implements both feedback short circuit protection and output over-voltage protection (OVP) functions at the FB pin. If $V_{FB}$ exceeds 3V, then OVP is engaged and the part stops switching until $V_{FB}$ falls below 3V. In the same manner, if $V_{FB}$ falls below 168mV, then shutdown is engaged and switching stops until $V_{FB}$ exceeds 188mV.

The flyback topology is frequently used to provide isolation from input to output. Since, the current transfer ratio (CTR) of standard optical isolation varies over temperature, proper regulation using primary error amplifiers is difficult. An error amplifier is usually placed in the secondary to regulate the output voltage accurately. To accommodate isolated designs, the LM3450/50A internal error amplifier can be bypassed by placing a 5.11kΩ resistor from FB to GND. This engages a 5kΩ pull-up resistor from COMP to an internal 5V rail.

## SECONDARY ERROR AMPLIFIER

For isolated designs, the error amplifier on the secondary should take the form of a proportional integral (PI) compensator. The amplifier is frequently implemented with an LMV431. The output voltage resistor divider ($R_{FB1}$, $R_{FB2}$) provides the sensed output voltage to the LMV431 inverting input. The PI compensation is achieved by connecting $R_{SC}$ and $C_{SC}$ in between the LMV431 input and output, shown in Figure 23. In addition, $C_{CMP}$ is placed from COMP to GND on the primary for higher frequency noise attenuation.

In addition to the basic error amplifier, a soft-start circuit can be implemented using a capacitor, two diodes and a Zener diode as shown in Figure 23. This secondary softstart circuit has no restart mechanism, therefore a primary side softstart is recommended as described in the SOFTSTART section of this document.



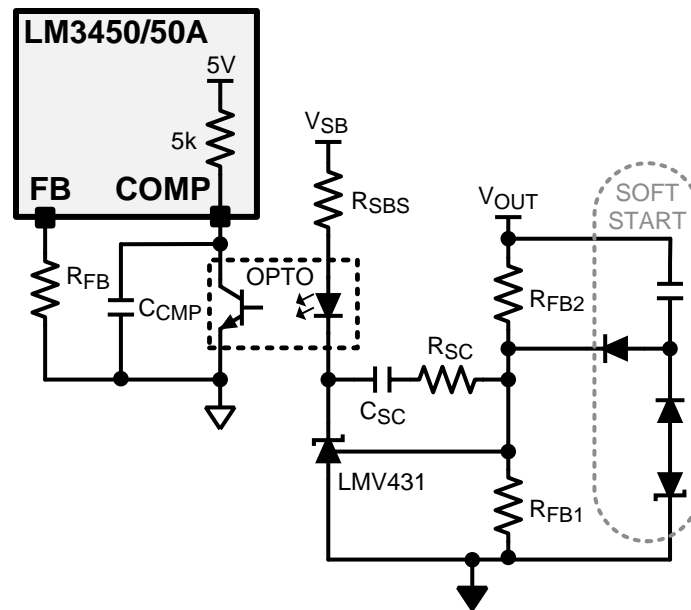**Figure 23. Secondary Error Amplifier**

## PRECISION VOLTAGE REFERENCE

The LM3450/50A provides a 3V voltage reference ($V_{REF}$) for biasing the $V_{ADJ}$ pin as well as any external circuitry. $V_{REF}$ is regulated once $V_{CC}$ exceeds 3V. There is a 2mA current limit for the reference. A 10nF ceramic bypass capacitor should be placed from $V_{REF}$ to GND.

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## LOW POWER SHUTDOWN

The LM3450/50A can be placed into a low power shutdown by grounding the $V_{ADJ}$ pin (any voltage below 75mV). During low power shutdown, the device will turn on the GATE for one cycle followed by a fixed off-time of 42µs and the cycle repeats. During shutdown, the DIM output will be high (zero light output) since the buffer rail at FLT1 will be at or near zero. This feature is designed to hold up the PFC output voltage while removing the load (turning the LEDs off).

## THERMAL SHUTDOWN

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. The threshold for thermal shutdown is 160°C with a 20°C hysteresis. During thermal shutdown GATE is disabled.
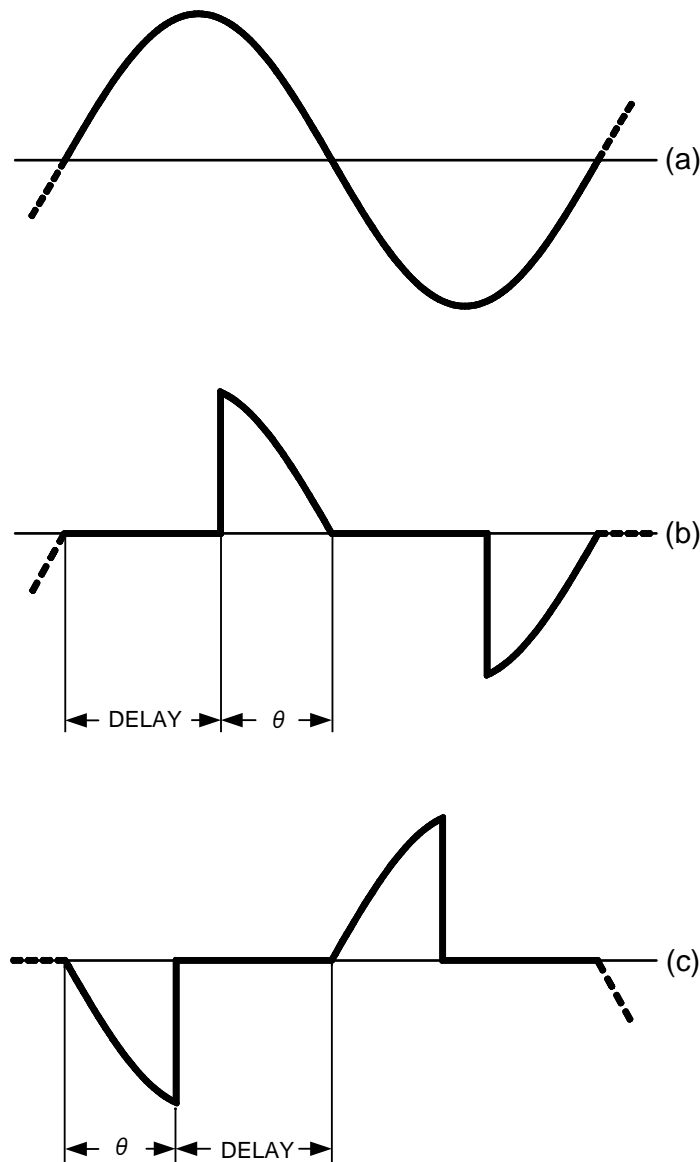
**Figure 24. Phase Dimming Waveforms**

## PHASE DIMMER OPERATION

A simplified schematic of a phase dimmer is shown in Figure 25. An RC network consisting of R1, R2, and C1 delay the turn-on of the triac until the voltage on C1 reaches the trigger voltage of the diac. Increasing the resistance of the potentiometer (wiper moving downward) increases the turn-on delay which decreases the on-time or "conduction angle" of the triac (θ). This reduces the average power delivered to the load.
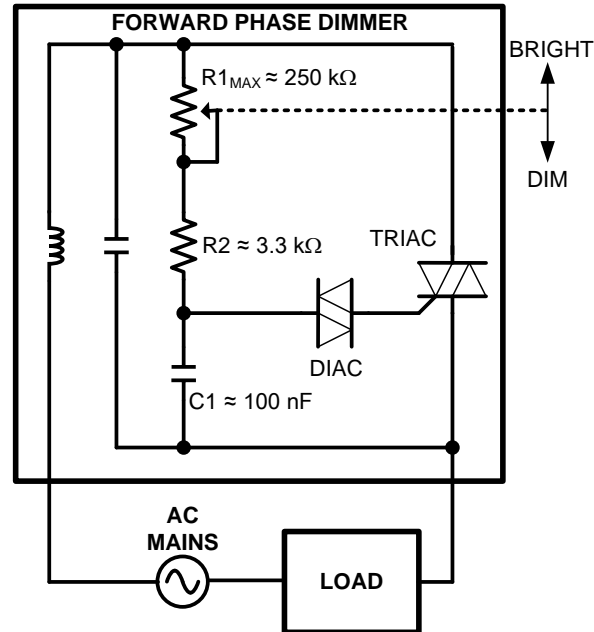


**Figure 25. Basic Forward Phase Dimmer**

Phase dimmer voltage waveforms are shown in Figure 24.

Figure 24a shows the full sinusoid of the input voltage. Even when set to full brightness; few dimmers will provide 100% conduction angle.

Figure 24b shows a waveform from a forward phase dimmer. The off-time can be referred to as the firing angle and is simply 180° – θ.

Figure 24c shows the waveform of a reverse phase dimmer (also called an electronic dimmer in the lighting industry). These typically or more expensive, microcontroller based dimmers that use switching devices other than triacs. Note that the conduction angle starts from the zero-crossing, and terminates some time later. This method of control reduces the noise spike at the transition.

Any form of phase dimming modulates the incoming AC waveform by chopping part of the sinusoid, reducing the average power to the load. These dimmers work very well with standard incandescent bulbs, but not with power converters. A converter attempts to regulate the load in with presence of any input, effectively ignoring the phase angle. To implement a dimmable converter, the angle must be sensed at the input, decoded and used to properly control the LED current regulator.
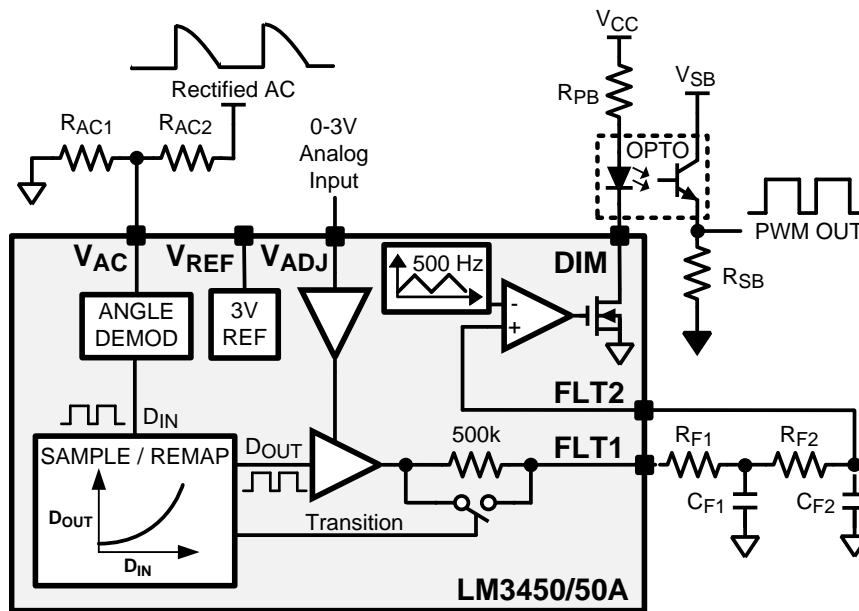
Product Folder Links: *LM3450*

**Figure 26.  Dimming Decoder Circuit**

## PHASE DIMMING DECODER

The LM3450/50A uses the rectified AC line voltage to interpret the conduction angle. Figure 26 shows the LM3450/50A decoder circuit with associated external circuitry. The rectified AC line voltage is scaled via a resistor divider ($R_{AC1}$, $R_{AC2}$) and connected to the $V_{AC}$ pin. $V_{AC}$ is compared to a 356mV reference to generate a twice line frequency PWM signal with corresponding duty cycle as shown in Figure 27.
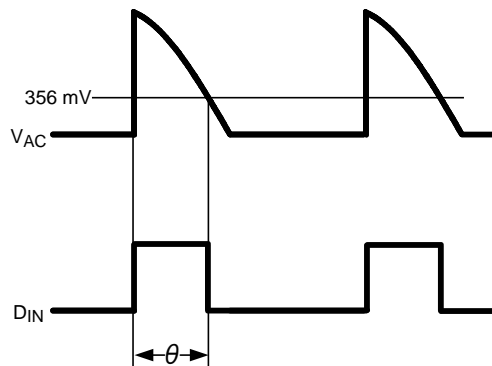


**Figure 27.  Phase Angle Demodulation**

For best results, $R_{AC1}$ and $R_{AC2}$ are suggested to be sized so that the $V_{AC}$ voltage crosses the 356mV threshold when the rectified AC line is as follows:

- 120V systems: 25V to 45V
- 230V systems: 40V to 70V

The demodulated duty cycle is sampled and logarithmically remapped to a 300Hz PWM signal improving the resolution of low dimming levels to the human eye. A minimum duty cycle limits the maximum achievable contrast ratio to approximately 70:1. The remapped PWM signal is buffered and output at FLT1 with amplitude equal to $V_{ADJ}$ as shown in Figure 28.

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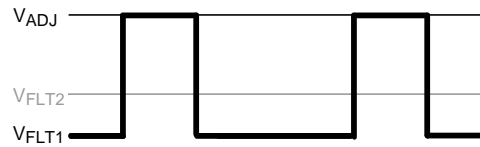
**Figure 28. FLT1 to FLT2 Mapping**

The FLT1 signal is routed through a 2 pole low pass filter ($R_{F1}$, $C_{F1}$, $R_{F2}$, $C_{F2}$), as shown in Figure 26, to remove the twice line frequency ripple. The resulting analog signal at FLT2 is compared to a 500Hz Triangle wave to create the inverted PWM signal at the DIM pin as shown in Figure 29:



**Figure 29. FLT2 to DIM Mapping**

This PWM signal at the DIM pin can be used as the dim input to a secondary LED driver. DIM is an open drain output designed for isolated solutions. Optical isolation is used to transmit signals across the isolation boundary. With mos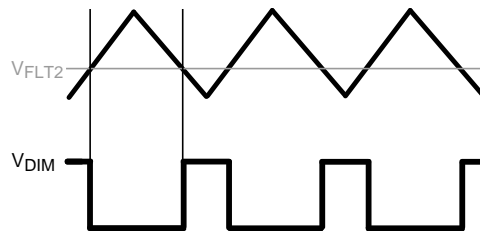t opto-isolators, the edge rate is dependent on the amount of drive current through the photodiode. The open-drain configuration allows the primary bias supply ($V_{CC}$) to provide the current as shown in Figure 26. The choice of resistor ($R_{PB}$) between $V_{CC}$ and the photodiode anode will set the drive current. This enables the user to trade-off PWM accuracy with system efficiency.

The open drain configuration also ensures that the secondary has a resistor from the phototransistor's emitter to secondary ground (not from collector to secondary bias). During system turn-off, this prevents an undesired LED blink because the secondary stage LED driver is forced off.

A variable sample rate and dynamic filter ensure fast, smooth dimming transitions (movement of the dimmer) while maintaining robust flicker-free behavior when the dimmer is static. The sample rate depends on past and present angle information. The dynamic filter is a dual mode filter. During standby mode, when a transition has not been made and the dimmer is static, a 500kΩ series resistor is connected between the buffered output and FLT1 as shown in Figure 26.

The 500kΩ resistor is shorted when the LM3450/50A senses a large transition of the dimmer. This increases the filter speed while the dimmer is transitioning between levels to improve response time.

The FLT1 and FLT2 poles created by each RC pair ($R_{F1}$ and $C_{F1}$, $R_{F2}$ and $C_{F2}$) should be set as follows:
- $C_{F1}$ and $C_{F2}$ can be 1µF ceramic capacitors for all designs.
- $R_{F1}$ and $R_{F2}$ should be set between 15kΩ (~10Hz) and 75kΩ (~2Hz).

2 Hz poles provide a "smooth fade" while 10Hz poles create a "snappy" response.

These component values ensure that the static filter condition in standby mode has 1 pole approximately a decade lower than the nominal in order to provide good noise immunity to the system.
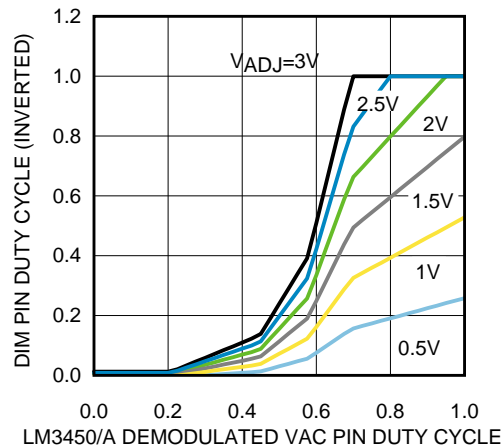
**Figure 30.  Complete Decoder Mapping**

Since the buffered decoder output has amplitude equal to $V_{ADJ}$ and the resulting PWM signal is filtered into an analog voltage at FLT2, the $V_{ADJ}$ pin can be used to change the mapping as shown in Figure 30. The maximum LED current (DIM = 0) when $V_{ADJ}$ = 3V corresponds to decoded angles of 70% or greater. Some dimmers have a maximum angle greater than this. If $V_{ADJ}$ is reduced to 2.5V, the maximum LED current will correspond to an angle of 80% and at $V_{ADJ}$ = 2V the maximum will occur at a decoded angle of 95%.

The $V_{ADJ}$ pin can also be used to implement a standard analog adjust function. If the demodulated phase angle at $V_{AC}$ is above 85%, then the fast filter is always enabled (500kΩ shorted) and the $V_{ADJ}$ pin can solely be used to scale the DIM pin duty cycle. When $V_{ADJ}$ is pulled below 75mV the part enters low power shutdown so the maximum attainable contrast ratio using $V_{ADJ}$ only is approximately 40:1.

Both FLT1 and FLT2 have pull-down MosFETs that are turned on when $V_{CC}$ UVLO falling threshold is triggered. This provides a quick discharge path for the capacitors and eliminates the possibility of an undesired light level at the next startup.



**Figure 31.  Dynamic Hold Circuit**

## DYNAMIC HOLD

A forward phase "triac" dimmer requires a minimum amount of current to be flowing through it during the entire conduction angle. This is referred to as hold current. If the minimum hold current requirement is not met, the triac will shut off (misfire). During normal operation, the converter will demand some amount of input current. However, at any point during the cycle, the input current can be low enough to cause a misfire.
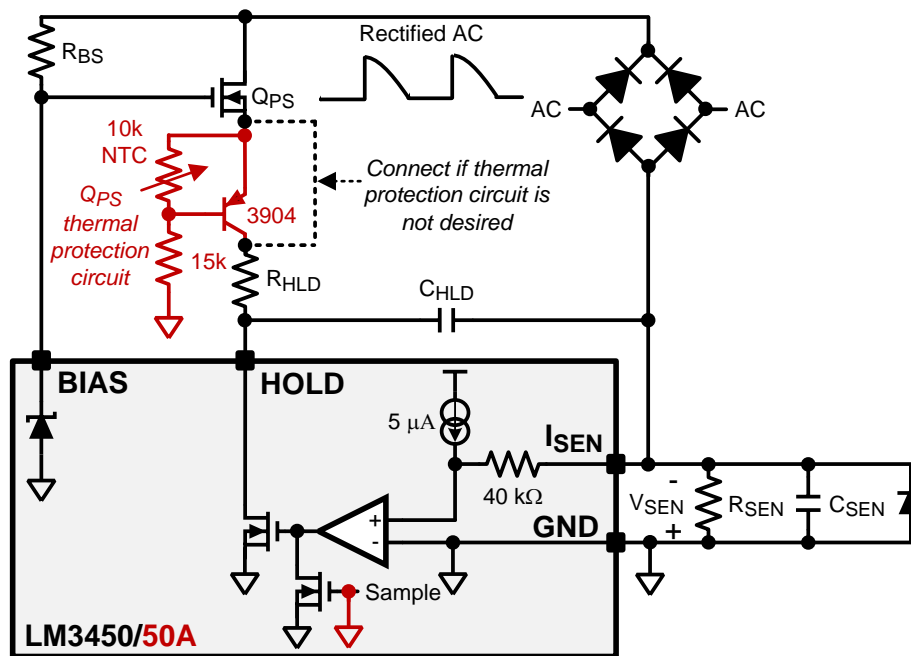
During an LM3450/50A sampling period, the triac should not misfire or the decoded angle will be inaccurate as shown in Figure 32. Since the triac is asymmetrical phase-to-phase, misfires can occur at different points in the waveform. After the triac misfires, the voltage returns to zero exponentially. This can create a large difference between decoded angles which can be observed as a "fluttering" of the light.
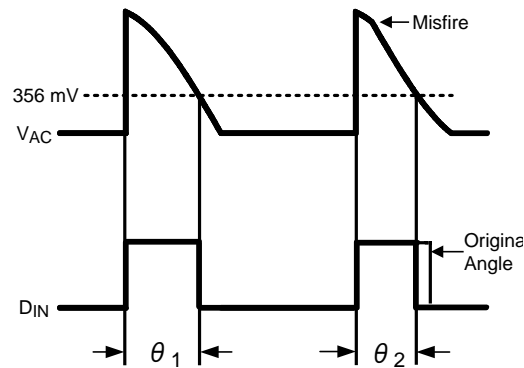


**Figure 32. Forward Phase Waveform**

To ensure the triac does not misfire during a sampling period and the angle is correctly decoded, a dynamic hold function is enabled. The input current is sensed with a resistor ($R_{SEN}$) from GND to $I_{SEN}$ (the return of the full bridge rectifier). If the voltage across this resistor is less than 200mV, the device adds holding current via the HOLD circuitry to maintain 200mV across $R_{SEN}$.

The hold current is added by linearly adjusting the gate voltage of $Q_{HLD}$ as shown in Figure 31. As the gate voltage of $Q_{HLD}$ is increased, the HOLD pin voltage decreases, forcing a voltage across the resistance ($R_{HLD}$) from the source of $Q_{PS}$ to HOLD. This extra current is drawn from the input through the triac, but is not processed by the converter. Figure 33 shows a typical dynamic hold waveform of the LM3450 where interval 1 is a non-sampled conduction angle, 2 is the firing angle, and 3 is a sampled conduction angle. It should be noted that using the LM3450A will ensure every conduction angle looks like interval 3 in Figure 33.
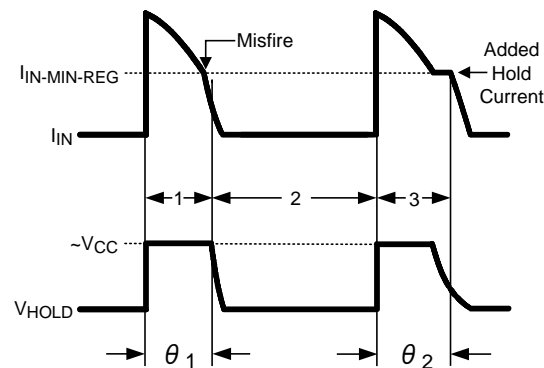


**Figure 33. Dynamic Hold Waveform**

The dynamic hold function is also necessary for reverse phase dimmers, but for a different reason. Reverse phase dimmers do not use triacs, therefore they do not require a minimum "holding" current. Instead, they need what is commonly called bleeder current. When a reverse phase dimmer turns off, the AC voltage is at a high value. There is an RC time constant associated with discharging the total effective input capacitance (EMI capacitors, PFC capacitor, damper capacitance). The decoder does not record the angle until the voltage reaches the 356mV threshold. This can cause the decoded angle to be much larger than it actually is and dependent on the RC time constant as shown in Figure 34.
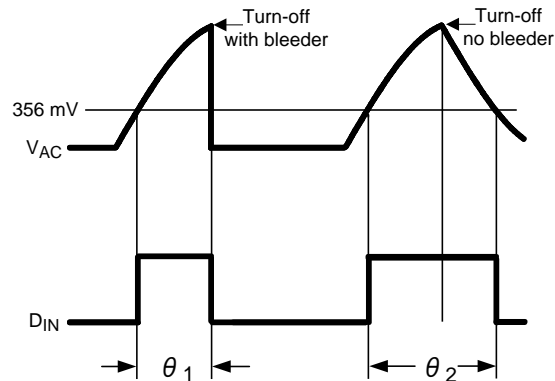


**Figure 34. Reverse Phase Waveforms**

The dynamic hold will quickly bleed off the excess charge in an attempt to regulate the voltage across $R_{SEN}$. This will preserve the accuracy of the decoded phase angle.

During the conduction angle (θ), dynamic hold is enabled only during a sample period for the LM3450. However, during the firing angle (delay time), dynamic hold is always enabled with the LM3450. This will ensure the rectified line voltage does not begin to rise due to leakage currents through the phase dimmer. Again, with the LM3450A the dynamic hold is continuously active during all conduction and firing angles.

The minimum regulated input current can be calculated:

$$I_{IN\text{-}MIN\text{-}REG} = \frac{200 \text{ mV}}{R_{SEN}}$$

(7)

The maximum possible additional holding current (which can occur when HOLD is still transitioning usually at the rising edge of the triac firing) can be approximated:

$$I_{HOLD\text{-}MAX} = \frac{V_{CC}}{R_{HLD} + 30\Omega}$$

(8)

It is recommended that the maximum hold current is set 10-15% higher than the minimum regulated input current.

A minimum of 0.1µF capacitance should be placed between $I_{SEN}$ and HOLD to limit the bandwidth of the dynamic hold circuit to well below the switching frequency. However, if too large a capacitor is used, the bandwidth will be too low to respond to line transients. A maximum of 0.47µF should ensure good performance.

Finally, a small Schottky diode should be placed from GND to $I_{SEN}$ to absorb the large current spikes associated with the triac firing edge. This diode should have a forward voltage above 200mV at the worst-case operating temperature so that it won't interfere with dynamic hold regulation.

## THERMAL PROTECTION

With the LM3450A, $Q_{PS}$ has to dissipate more power than with the LM3450. During worst case conditions such as open LED load, the converter will be demanding very little current regardless of the triac position. If the phase dimmer conduction angle is large and the load is not present, $Q_{PS}$ has to dissipate many watts since the dynamic hold is attempting to regulate the current to ten's of mA. Using the LM3450, this is nominally not a problem since it is sampling the dynamic hold infrequently. However, the LM3450A is drawing the hold current every cycle which becomes a problem very quickly. It should be noted that If the input AC line is very noisy, the VAC input to the decoder could have enough variation in steady state to cause the decoder to think the dimmer is transitioning all of the time. This would increase the sampling rate dramatically, putting much more thermal strain on the passFET in LM3450 applications as well.

To mitigate these problems, a thermal protection circuit should be implemented on the LM3450A designs (and can be on the LM3450 designs as well) as shown in red in Figure 31. The NTC thermistor should be placed on the opposite side of the PCB directly under the drain of $Q_{PS}$. This will provide the best thermal coupling while maintaining the necessary high voltage spacing constraints. At startup the NTC is at a high resistance value, turning the PNP fully on which provides the dynamic hold path. As the NTC heats up the resistance decreases and the base voltage increases. Eventually, the PNP will transition into linear mode and the effective resistance from collector to emitter will increase. This will decrease the maximum holding current, thereby decreasing the thermal stress on $Q_{PS}$. Given enough headroom, the circuit should reach thermal equilibrium in a safe controlled manner.

Since this method of thermal protection linearly reduces the maximum hold current with increasing temperature, the foldback will not be perceptible to the consumer. Instead, the result of the foldback will simply be a reduction of contrast ratio, meaning the minimum achievable LED current will increase as the temperature increases beyond the foldback level.



**Figure 35. Primary Bias Circuitry**
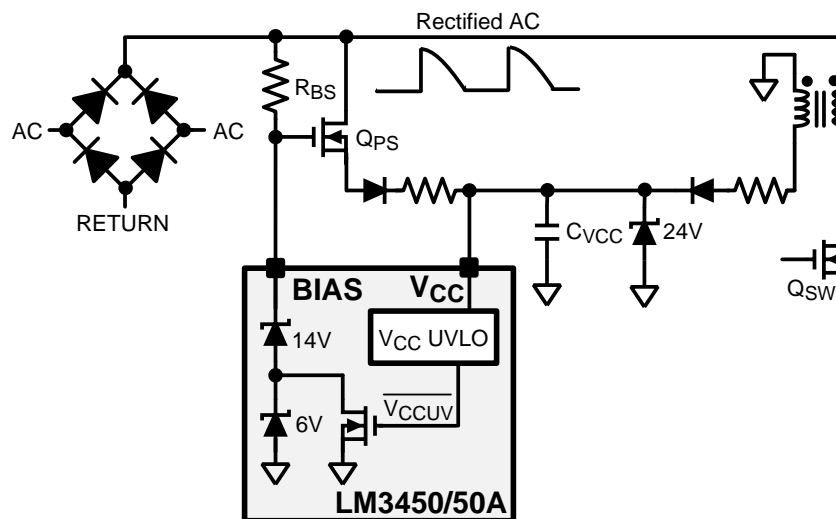
## PRIMARY BIAS SUPPLY

The LM3450/50A requires a supply voltage at $V_{CC}$, not to exceed 25V. The device has $V_{CC}$ under-voltage lockout (UVLO) with rising and falling thresholds of 12.9V and 7.9V respectively. A 24V Zener diode should be placed from the $V_{CC}$ pin to GND to protect the device from substantial spikes that could cause damage.

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Figure 35 shows how the LM3450/50A provides a quick way to generate the necessary primary bias supply at start-up. Since the AC line peak voltage is always higher than the rating of the controller, all designs require an N-channel MosFET (passFET). The passFET ($Q_{PS}$) is connected with its drain attached to the rectified AC. The gate of $Q_{PS}$ is connected to the BIAS pin which has a stack of 2 Zener diodes internal to the device. These diodes are then biased from the rectified AC line through series resistance ($R_{BS}$). The source of $Q_{PS}$ is held at a $V_{GS}$ below the Zener voltage and current flows through $Q_{PS}$ to charge up whatever capacitance is present. If the capacitance is large enough, the source voltage will remain relatively constant over the line cycle and this becomes the input bias supply at $V_{CC}$.

This bias circuit enables instant turn-on. However, once the circuit is operational it is desirable to bootstrap $V_{CC}$ to an auxiliary winding of the inductor or transformer (also used for ZCD). The two bias paths are each connected to $V_{CC}$ through a diode to ensure the higher of the two is providing $V_{CC}$ current. This bootstrapping greatly improves efficiency when quick start-up is necessary.

To ensure that the auxiliary winding is powering $V_{CC}$ at all times except start-up, the LM3450/50A has a dual BIAS mode. The BIAS voltage at startup is 20V through two Zener diodes. When the $V_{CC}$ UVLO rising threshold is exceeded and the device turns on, the BIAS pin voltage is reduced to 14V (bottom 6V Zener is shorted). Once the $V_{CC}$ UVLO falling threshold is reached again, the BIAS pin will return to 20V to attempt to restart the device.

It should be noted that the large hysteresis of $V_{CC}$ UVLO and the dual BIAS mode allow for a large variation of the auxiliary bias circuitry easing the design of the magnetics.

## SOFTSTART

As in any off-line system, softstart is an important part of the design. Since the LM3450/50A are used with phase dimming applications, the typical startup problems are magnified since a phase dimmer is frequently turned on and off rapidly. This requires a softstart mechanism that quickly resets when the LM3450/50A turns off. Since the LM3450/50A has two distinct functional parts (PFC and phase decoder), ideally both should be softstarted simultaneously. This will ensure the most controlled start-up possible.

The circuit in Figure 36 provides this exact functionality. Both $V_{ADJ}$ and COMP are diode or'ed into an RC charging circuit fed from $V_{CC}$. The reset mechanism is accomplished using an 18V Zener from BIAS, a current limiting resistor and an NPN transistor. The reset is activated when VCC uvlo falling is triggered and BIAS transitions to 20V. This discharges the RC to zero and as soon as $V_{CC}$ uvlo rising is passed BIAS transitions to 14V again, releasing the clamp on the RC softstart circuit. The RC will charge up to the 3.9V Zener clamp (which is above the dynamic range of COMP and $V_{ADJ}$ and become effectively out of the circuit until the next turn-off.
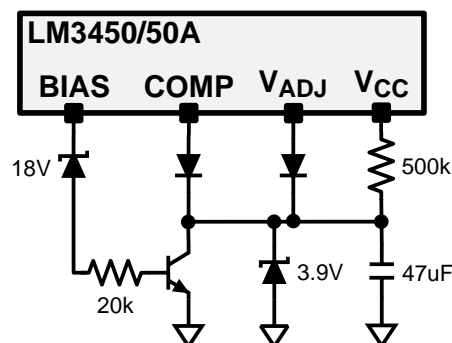


**Figure 36. Dual Softstart Circuit**

# DESIGN INFORMATION

## HOW TO SELECT THE CORRECT DEVICE (LM3450 or LM3450A)

What application(s) are suitable for the LM3450, and when is the LM3450A appropriate? The difference centers on the power dissipation in the passFET. The passFET stands off the high AC voltage from the LM3450/50A, and provides a path for the hold current. The passFET operates in the linear region and dissipates power equal to the product of the voltage across it and the current through it.

The LM3450 was designed to minimize the power dissipation in the passFET by applying holding current in a sampled form. The standby sampling rate (when the dimmer is not moving) is infrequent, allowing minimal impact on the thermal considerations of the passFET. Sampling of the dynamic hold is not desired for some applications although. An example where the sampled hold current may cause undesirable effects is the single stage flyback topology where the output of the flyback is directly connected to the LEDs. If the phase dimmer is allowed to misfire or create erratic differences in the input voltage and current waveforms, this behavior will appear as a "fluttering" of the LED light output at the sampling rate when the single stage topology is used. The light flutter is most observable at low input currents (dimming). A small perturbation in the input voltage due to phase dimmer misfire can create a visible difference in the output light. Using a secondary LED driver stage eliminates this problem.

Cost sensitive applications may drive the design to a single stage solution, and the LM3450A was developed to address this market. The LM3450A provides continuous dynamic hold current on every AC cycle preventing the phase dimmer from misfire, and the sampling frequency from appearing at the output. Another design consideration where continuous dynamic hold may be advantageous is the reduced stresses on input EMI R/C snubber networks.

The designer must pay close attention to the power loss of the passFET when using the LM3450A. Designers must consider worst case possibilities with any power conversion designs. Worst case operating conditions with the LM3450A are usually found with the largest triac holding current requirements. Many phase dimmers require 25mA-40mA of holding current, and frequently designers are choosing 50mA as their minimum holding current requirement. The passFET package for common LM3450/50A designs should be capable of dissipating between 1W and 1.5W. The pass-FET can always be increased in size and/or the hold current can be reduced. Power calculations for the dynamic hold circuit as well as effective thermal protection are both described in the DYNAMIC HOLD section.

The LM3450 and LM3450A is best differentiated in terms of the appropriate applications for each device. The Table 1 can be used as a general guide for when to use each part.

**Table 1. Device Selection Guide**

| Product | AC Input | Output Power | Device | Topology |
|---|---|---|---|---|
| High End Downlight | 120V | $P_{OUT} < 15W$ | LM3450 | Two Stage Design |
| | | $P_{OUT} > 15W$ | LM3450A | |
| | 230V | $P_{OUT} < 25W$ | LM3450 | |
| | | $P_{OUT} > 25W$ | LM3450A | |
| Low Cost Downlight or Large High End Bulb | 120V | $P_{OUT} > 15W$ | LM3450A | Single Stage Design |
| | 230V | $P_{OUT} > 25W$ | | |

Product Folder Links: *LM3450*

## Applications Information

See AN-2098 (literature number SNVA463) and/or AN-2150 (literature number SNVA485) for detailed design and application information.

**TWO STAGE LED DRIVER – LM3450 PRIMARY AND LM3409HV SECONDARY**

Product Folder Links: *LM3450*
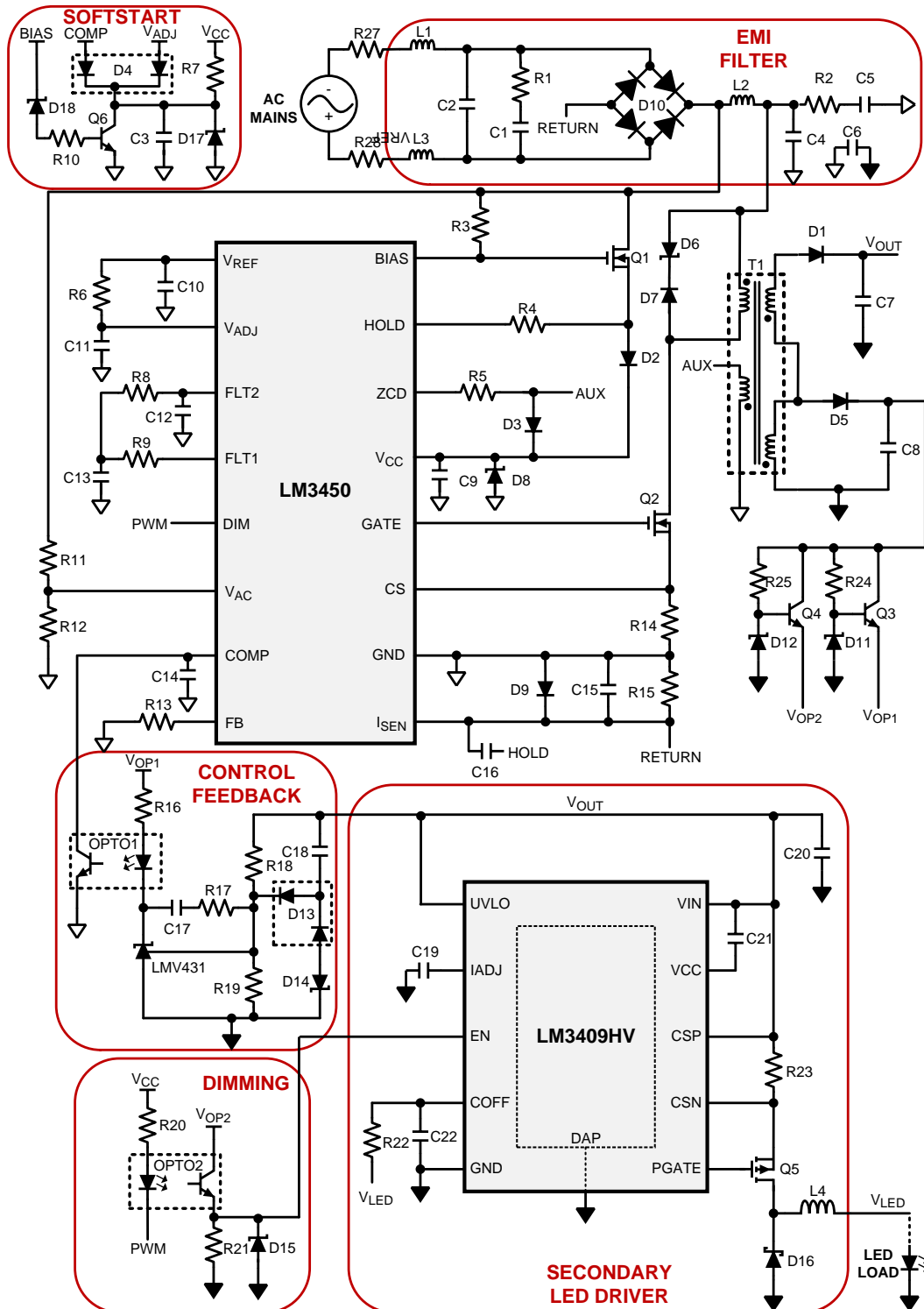
## 15W TWO STAGE DESIGN SPECIFICATIONS

AC Input Voltage: 120$V_{AC}$ nominal (90$V_{AC}$ - 135$V_{AC}$) or 230$V_{AC}$ nominal (180$V_{AC}$ - 265$V_{AC}$)

Regulated Flyback Output Voltage: 50V

Regulated LED Current: 350mA

LED Stack Voltage Maximum: 45V

### Table 2. Bill of Materials[1]

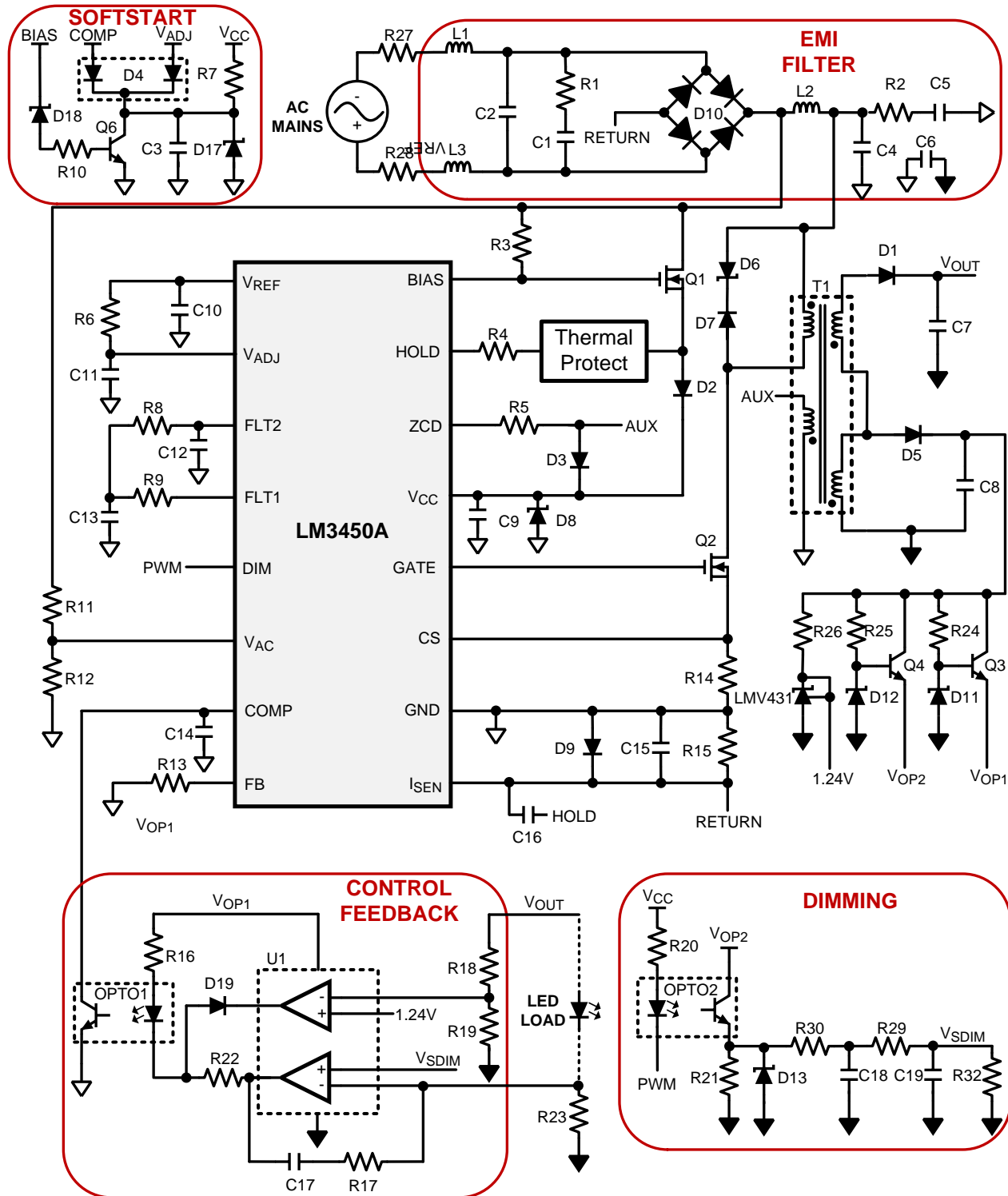| Reference Designator | | Description | Manufacturer | Part Number |
|---|---|---|---|---|
| LM3450 | | IC PFC CONT 16-TSSOP | TI | LM3450MT |
| LM3409HV | | IC LED DRIVR 10-eMSOP | TI | LM3409HVMY |
| LMV431 | | IC SHUNT REG SOT-23 | TI | LMV431AIM5 |
| C1a, C1b, C5a, C5b | 120V | CAP CER 0.22µF 250V 1210 | MURATA | GRM32DR72E224KW01L |
| | 230V | CAP CER 68nF 250V 1210 | MURATA | GRM32QR72E683KW01L |
| C2 | | CAP MPY 33nF 250VAC X1 RAD | EPCOS | B32912A3333M |
| C3 | | CAP CER 47µF 6.3V 0805 | TAIYO YUDEN | JMK212BJ476MG-T |
| C4 | 120V | CAP MPY 0.1µF 400V RAD | EPCOS | B32612A4104J008 |
| | 230V | CAP MPY 33nF 1000V RAD | WIMA | MKP10 - .033/1000/10 |
| C6 | | CAP CER 4.7nF 500VAC Y1 RAD | EPCOS | VY1472M63Y5UQ63V0 |
| C7a | | CAP ELEC 470µF 63V RAD | NICHICON | UPW1J471MHD3 |
| C7b, C8b, C9b, C11, C15 | | CAP CER 0.1µF 50V 1206 | MURATA | GRM188R71H104KA93D |
| C8a, C9a | | CAP ELEC 100µF 50V RAD | NICHICON | UHE1H101MPD |
| C10 | | CAP CER 10nF 25V 0603 | MURATA | GRM188R71E103KA01D |
| C12, C13 C14, C21 | | CAP CER 1µF 16V 0603 | MURATA | GRM188R71C105KA12D |
| C16 | | CAP CER 0.22µF 16V 0603 | TDK | C1608X7R1C224K |
| C17 | | CAP CER 10µF 16V 1206 | MURATA | GRM31CR71C106KAC7L |
| C18, C20 | | CAP CER 1µF 100V 1206 | TDK | C3216X7R2A105M |
| C19 | | CAP CER 2.2µF 6.3V 0603 | TDK | C1608X5R0J225M |
| C22 | | CAP CER 470pF 100V 0603 | TDK | C1608C0G2A471J |
| D1 | 120V | DIODE ULTRAFAST 200V 1A SMA | FAIRCHILD | ES1D |
| | 230V | DIODE FAST 400V 1A DO-214AC | FAIRCHILD | ES1G |
| D2 | | DIODE ULTRAFAST 200V 1A SMA | FAIRCHILD | ES1D |
| D3, D5 | | DIODE ULTRAFAST 100V 0.2A SOT-23 | FAIRCHILD | MMBD914 |
| D4 | | DIODE DUAL SCHOTTKY 20V 0.5A SOT-23 | NXP SEMI | PMEG3005CT,215 |
| D6 | 120V | DIODE TVS 150V 600W UNI SMB | LITTLEFUSE | SMBJ150A |
| | 230V | DIODE TVS 220V 600W UNI SMB | LITTLEFUSE | SMBJ220A |
| D7 | | DIODE ULTRAFAST 600V 1A SMA | FAIRCHILD | ES1J |
| D8 | | DIODE ZENER 24V 1.5W SMA | MICRO-SEMI | SMAJ5934B-TP |
| D9 | | DIODE SCHOTTKY 20V 3A SMA | FAIRCHILD | ES2AA-13-F |
| D10 | | DIODE RECT 600V 0.5A Minidip | COMCHIP | HD06 |
| D11, D12 | | DIODE ZENER 10V 500mW SOD-123 | FAIRCHILD | MMSZ5240B |
| D13 | | DIODE ULTRAFAST 70V 0.2A SOT-23 | FAIRCHILD | BAV99 |
| D14 | | DIODE ZENER 3.3V 500mW SOD-123 | ON-SEMI | MMSZ3V3T1G |
| D15 | | DIODE ZENER 1.8V 500MW SOD-123 | ON-SEMI | MMSZ4678T1G |
| D16 | | DIODE SCHOTTKY 60V 2A SMB | ON-SEMI | SS26T3G |
| D17 | | DIODE ZENER 3.9V 500MW SOD-123 | ON-SEMI | MMSZ4686T1G |
| D18 | | DIODE ZENER 18V 500MW SOD-123 | ON-SEMI | MMSZ5248T1G |
| L1, L2, L3 | | IND SHIELD 1mH 0.46A SMT | COILCRAFT | MSS1038-105KL |

(1)   Components are used in both versions unless otherwise noted

## Table 2. Bill of Materials[1] (continued)

| Reference Designator | | Description | Manufacturer | Part Number |
|---|---|---|---|---|
| L4 | | IND SHIELD 470µH 1.06A SMT | COILCRAFT | MSS1278-474KLB |
| Q1 | | MOSFET N-CH 800V 3A DPAK | ST MICRO | STD4NK80ZT4 |
| Q2 | 120V | MOSFET N-CH 600V 4.4A DPAK | INFINEON | IPD60R950C6 |
| | 230V | MOSFET N-CH 800V 3A DPAK | ST MICRO | STD4NK80ZT4 |
| Q3, Q4 | | TRANS NPN 40V 0.6A SOT-23 | FAIRCHILD | MMBT4401 |
| Q5 | | MOSFET P-CH 70V 5.7A DPAK | ZETEX | ZXMP7A17K |
| Q6 | | TRANS PNP 40V 0.2A SOT-23 | FAIRCHILD | MMBT3904 |
| R1 | 120V | RES 330Ω 5% 1W 2512 | VISHAY | CRCW2512330RJNEG |
| | 230V | RES 510Ω 5% 1W 2512 | VISHAY | CRCW2512510RJNEG |
| R2 | 120V | RES 430Ω 5% 1W 2512 | VISHAY | CRCW2512430RJNEG |
| | 230V | RES 1.6kΩ 5% 1W 2512 | VISHAY | CRCW25121K60JNEG |
| R3 | 120V | RES 402kΩ 1% 0.25W 1206 | VISHAY | CRCW1206402KFKEA |
| | 230V | RES 953kΩ 1% 0.25W 1206 | VISHAY | CRCW1206953KFKEA |
| R4 | | RES 100Ω 1% 1W 2512 | VISHAY | WSL2512100RFKEA |
| R5 | | RES 100kΩ 1% 0.1W 0603 | VISHAY | CRCW0603100KFKEA |
| R6 | | RES 6.04kΩ 1% 0.1W 0603 | VISHAY | CRCW06036K04FKEA |
| R7 | | RES 499kΩ 1% 0.1W 0603 | VISHAY | CRCW0603499KFKEA |
| R8, R9 | | RES 75.0kΩ 1% 0.1W 0603 | VISHAY | CRCW060375K0FKEA |
| R10 | | RES 20.0kΩ 1% 0.1W 0603 | VISHAY | CRCW060320K0FKEA |
| R11 | 120V | RES 1.00MΩ 1% 0.25W 1206 | VISHAY | CRCW12061M00FKEA |
| | 230V | RES 2.00MΩ 1% 0.25W 1206 | VISHAY | CRCW12062M00FKEA |
| R12 | | RES 15.0kΩ 1% 0.1W 0603 | VISHAY | CRCW060315K0FKEA |
| R13 | | RES 5.11kΩ 1% 0.1W 0603 | VISHAY | CRCW06035K11FKEA |
| R14a | | RES 10Ω 1% 0.25W 1206 | VISHAY | CRCW120610R0FKEA |
| R14b | | RES 1.00Ω 1% 0.33W 1210 | VISHAY | CRCW12101R00FNEA |
| R15a, R15b | | RES 5.62Ω 1% 0.25W 1206 | VISHAY | CRCW12065R62FNEA |
| R16 | | RES 2.00kΩ 1% 0.125W 0805 | VISHAY | CRCW08052K00FKEA |
| R17 | 120V | RES 20.0kΩ 1% 0.1W 0603 | VISHAY | CRCW060320K0FKEA |
| | 230V | RES 10.0kΩ 1% 0.1W 0603 | VISHAY | CRCW060310K0FKEA |
| R18 | | RES 105kΩ 1% 0.125W 0805 | VISHAY | CRCW0805105KFKEA |
| R19 | | RES 2.67kΩ 1% 0.1W 0603 | VISHAY | CRCW06032K67FKEA |
| R20 | | RES 6.04kΩ 1% 0.125W 0805 | VISHAY | CRCW08056K04FKEA |
| R21 | | RES 10.0kΩ 1% 0.125W 0805 | VISHAY | CRCW080510K0FKEA |
| R22 | | RES 80.6kΩ 1% 0.1W 0603 | VISHAY | CRCW060380K6FKEA |
| R23 | | RES .62Ω 1% 0.5 2010 SMD | ROHM | MCR50JZHFLR620 |
| R24, R25 | | RES 10kΩ 1% 0.1W 0603 | VISHAY | CRCW060310K0FKEA |
| R27, R28 | 120V | RES 10Ω 10% 2W FILM | WELWYN | EMC2-10R0 |
| | 230V | RES 22Ω 10% 2W FILM | WELWYN | EMC2-22R0 |
| OPTO1, OPTO2 | | OPTO-ISOLATOR SMD | LITE ON | CNY17F-3S |
| T1 | 120V | XFORMER 120V 15W OUTPUT 50V | WURTH | 750813550 |
| | 230V | XFORMER 230V 15W OUTPUT 50V | WURTH | 750817550 |

## SINGLE STAGE LED DRIVER – LM3450A FLYBACK

## 30W SINGLE STAGE DESIGN SPECIFICATIONS

AC Input Voltage: $120V_{AC}$ nominal ($90V_{AC}$ - $135V_{AC}$) or $230V_{AC}$ nominal ($180V_{AC}$ - $265V_{AC}$)

Flyback Output Voltage Maximum: 60V

Regulated LED Current: 700mA

### Table 3. Bill of Materials[1]

| Reference Designator | | Description | Manufacturer | Part Number |
|---|---|---|---|---|
| LM3450A | | IC PFC CONT 16-TSSOP | TI | LM3450AMT |
| LMV431 | | IC SHUNT REG SOT-23 | TI | LMV431AIM5 |
| U1 | | IC DUAL OP-AMP | TI | LM2904 |
| C1a, C1b, C1c, C5a, C5b, C5c | 120V | CAP CER 0.22µF 250V 1210 | MURATA | GRM32DR72E224KW01L |
| | 230V | CAP CER 68nF 250V 1210 | MURATA | GRM32QR72E683KW01L |
| C2 | | CAP MPY 33nF 250VAC X1 RAD | EPCOS | B32912A3333M |
| C3 | | CAP CER 47µF 6.3V 0805 | TAIYO YUDEN | JMK212BJ476MG-T |
| C4 | 120V | CAP MPY 0.22µF 400V RAD | WIMA | MKP10-.22/400/20 |
| | 230V | CAP MPY 62nF 1000V RAD | VISHAY | BFC238330623 |
| C6 | | CAP CER 4.7nF 500VAC Y1 RAD | EPCOS | VY1472M63Y5UQ63V0 |
| C7a | | CAP ELEC 1mF 63V RAD | NICHICON | UPW1J102MHD |
| C7b, C8b, C9b, C11, C15 | | CAP CER 0.1µF 50V 1206 | MURATA | GRM188R71H104KA93D |
| C8a, C9a | | CAP ELEC 220µF 50V RAD | NICHICON | UHE1H221MPD |
| C10 | | CAP CER 10nF 25V 0603 | MURATA | GRM188R71E103KA01D |
| C12, C13, C14, C18, C19 | | CAP CER 1µF 16V 0603 | MURATA | GRM188R71C105KA12D |
| C16 | | CAP CER 0.22µF 16V 0603 | TDK | C1608X7R1C224K |
| C17 | | CAP CER 10µF 16V 1206 | MURATA | GRM31CR71C106KAC7L |
| D1a, D1b | 120V | DIODE ULTRAFAST 200V 1A SMA | FAIRCHILD | ES1D |
| | 230V | DIODE FAST 400V 1A DO-214AC | FAIRCHILD | ES1G |
| D2 | | DIODE ULTRAFAST 200V 1A SMA | FAIRCHILD | ES1D |
| D3, D5 | | DIODE ULTRAFAST 100V 0.2A SOT-23 | FAIRCHILD | MMBD914 |
| D4 | | DIODE DUAL SCHOTTKY 20V 0.5A SOT-23 | NXP SEMI | PMEG3005CT,215 |
| D6 | 120V | DIODE TVS 150V 600W UNI SMB | LITTLEFUSE | SMBJ150A |
| | 230V | DIODE TVS 220V 600W UNI SMB | LITTLEFUSE | SMBJ220A |
| D7 | | DIODE ULTRAFAST 600V 1A SMA | FAIRCHILD | ES1J |
| D8 | | DIODE ZENER 24V 1.5W SMA | MICRO-SEMI | SMAJ5934B-TP |
| D9 | | DIODE SCHOTTKY 20V 3A SMA | FAIRCHILD | ES2AA-13-F |
| D10 | | DIODE RECT 600V 0.5A Minidip | COMCHIP | HD06 |
| D11, D12 | | DIODE ZENER 10V 500mW SOD-123 | FAIRCHILD | MMSZ5240B |
| D13 | | DIODE ZENER 1.8V 500MW SOD-123 | ON-SEMI | MMSZ4678T1G |
| D17 | | DIODE ZENER 3.9V 500MW SOD-123 | ON-SEMI | MMSZ4686T1G |
| D18 | | DIODE ZENER 18V 500MW SOD-123 | ON-SEMI | MMSZ5248T1G |
| D19 | | DIODE SCHOTTKY 30V 200mA SOT-23 | FAIRCHILD | BAT54 |
| L1 | | IND LINE FILTER 6mH 0.3A 11M | PANASONIC | ELF-11M030E |
| L1, L2, L3 | | IND SHIELD 1mH 1.18A SMT | COILCRAFT | MSS1278-105KL |
| L4 | | IND SHIELD 270µH 2.34A SMT | COILCRAFT | MSS1278-274KLB |
| Q1 | | MOSFET N-CH 800V 3A DPAK | ST MICRO | STD4NK80ZT4 |
| Q2 | 120V | MOSFET N-CH 500V 9A DPAK | ST MICRO | STD11NM50N |
| | 230V | MOSFET N-CH 800V 6A DPAK | INFINEON | SPD06N80C3 |
| Q3, Q4 | | TRANS NPN 40V 0.6A SOT-23 | FAIRCHILD | MMBT4401 |
| Q6 | | TRANS NPN 40V 0.2A SOT-23 | FAIRCHILD | MMBT3904 |

(1)  Components are used in both versions unless otherwise noted

## Table 3. Bill of Materials[1] (continued)

| Reference Designator | | Description | Manufacturer | Part Number |
|---|---|---|---|---|
| R1 | 120V | RES 330Ω 5% 1W 2512 | VISHAY | CRCW2512330RJNEG |
| | 230V | RES 510Ω 5% 1W 2512 | VISHAY | CRCW2512510RJNEG |
| R2 | 120V | RES 430Ω 5% 1W 2512 | VISHAY | CRCW2512430RJNEG |
| | 230V | RES 1.6kΩ 5% 1W 2512 | VISHAY | CRCW25121K60JNEG |
| R3 | 120V | RES 402kΩ 1% 0.25W 1206 | VISHAY | CRCW1206402KFKEA |
| | 230V | RES 953kΩ 1% 0.25W 1206 | VISHAY | CRCW1206953KFKEA |
| R4 | | RES 100Ω 1% 1W 2512 | VISHAY | WSL2512100RFKEA |
| R5 | | RES 100kΩ 1% 0.1W 0603 | VISHAY | CRCW0603100KFKEA |
| R6 | | RES 6.04kΩ 1% 0.1W 0603 | VISHAY | CRCW06036K04FKEA |
| R7 | | RES 499kΩ 1% 0.1W 0603 | VISHAY | CRCW0603499KFKEA |
| R8, R9 | | RES 49.9kΩ 1% 0.1W 0603 | VISHAY | CRCW060349K9FKEA |
| R10 | | RES 20kΩ 1% 0.1W 0603 | VISHAY | CRCW060320K0FKEA |
| R11 | 120V | RES 1.00MΩ 1% 0.25W 1206 | VISHAY | CRCW12061M00FKEA |
| | 230V | RES 2.00MΩ 1% 0.25W 1206 | VISHAY | CRCW12062M00FKEA |
| R12 | | RES 15.0kΩ 1% 0.1W 0603 | VISHAY | CRCW060315K0FKEA |
| R13 | | RES 5.11kΩ 1% 0.1W 0603 | VISHAY | CRCW06035K11FKEA |
| R14a, R14b, R23a, R23b, R23c | | RES 1.00Ω 1% 0.33W 1206 | VISHAY | CRCW12061R00FKEA |
| R15a, R15b | | RES 5.62Ω 1% 0.25W 1206 | VISHAY | CRCW12065R62FKEA |
| R16 | | RES 1.00kΩ 1% 0.125W 0805 | VISHAY | CRCW08051K00FKEA |
| R17 | 120V | RES 30.1kΩ 1% 0.1W 0603 | VISHAY | CRCW060330K1FKEA |
| | 230V | RES 15.0kΩ 1% 0.1W 0603 | VISHAY | CRCW060315K0FKEA |
| R18 | | RES 105kΩ 1% 0.125W 0805 | VISHAY | CRCW0805105KFKEA |
| R19 | | RES 2.49kΩ 1% 0.1W 0603 | VISHAY | CRCW06035K49FKEA |
| R20 | | RES 6.04kΩ 1% 0.125W 0805 | VISHAY | CRCW08056K04FKEA |
| R21 | | RES 10.0kΩ 1% 0.125W 0805 | VISHAY | CRCW080510K0FKEA |
| R22 | | RES 1.4kΩ 1% 0.125W 0805 | VISHAY | CRCW08051K40FKEA |
| R24, R25 | | RES 10kΩ 1% 0.1W 0603 | VISHAY | CRCW060310K0FKEA |
| R26 | 120V | RES 2.49kΩ 1% 0.125W 0805 | VISHAY | CRCW08052K49FKEA |
| | 230V | RES 4.99kΩ 1% 0.125W 0805 | VISHAY | CRCW08054K99FKEA |
| R27, R28 | 120V | RES 5Ω 10% 3W WIREWOUND | VISHAY | PAC300005008FAC000 |
| | 230V | RES 10Ω 10% 3W WIREWOUND | VISHAY | PAC300001009FAC000 |
| R29, R30 | | RES 4.99kΩ 1% 0.1W 0603 | VISHAY | CRCW06034K99FKEA |
| R32 | | RES 909Ω 1% 0.1W 0603 | VISHAY | CRCW0603909RFKEA |
| OPTO1, OPTO2 | | OPTO-ISOLATOR SMD | LITE ON | CNY17F-3S |
| T1 | 120V | XFORMER 120V 30W OUTPUT 50V | WURTH | 750813651 |
| | 230V | XFORMER 230V 30W OUTPUT 50V | WURTH | 750817651 |
| Thermal Protect | | see DYNAMIC HOLD section | | |

Product Folder Links: *LM3450*

# REVISION HISTORY

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM3450AMT/NOPB | ACTIVE | TSSOP | PW | 16 | 92 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-1-260C-UNLIM | | LM3450 AMT | Samples |
| LM3450AMTX/NOPB | ACTIVE | TSSOP | PW | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-1-260C-UNLIM | | LM3450 AMT | Samples |
| LM3450MT/NOPB | ACTIVE | TSSOP | PW | 16 | 92 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LM3450 MT | Samples |
| LM3450MTX/NOPB | ACTIVE | TSSOP | PW | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LM3450 MT | Samples |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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