DAC7741EVM

This user's guide describes the DAC7741 evaluation module. It covers the operating procedures and characteristics of the EVM board along with the device that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

Contents

List of Figures

List of Tables

1 Information About Cautions and Warnings

This manual may contain cautions and warnings.

CAUTION

This is an example of a CAUTION statement.

A CAUTION statement describes a situation that could potentially damage this EVM board, your software, or equipment.

WARNING

This is an example of a WARNING statement.

A WARNING statement describes a situation that could potentially cause HARM to **you**.

The information in a caution or a warning is provided for your protection. Read each caution and warning carefully.

2 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this manual by its title and literature number. Updated documents can also be obtained through the TI Web site at http://www.ti.com.

Data Sheets:	Literature Number:	Data Sheets:	Literature Number:
DAC7741	SBAS248	SN74AHC541	SCLS261
REF102	SBVS022	SN74AHC138	SCLS258
OPA627	SBOS165	SN74AHC1G04	SCLS318
OPA2277	SBOS079	SN74AHC1G08	SCLS314
SN74ALVC16245	SCAS419	SN74AUP1G57	SCES503

3 Questions about this or other Data Converter EVM's?

If you have questions about this or other Texas Instruments Data Converter evaluation modules, contact the Data Converter Application Team by e-mail at dataconvapps@list.ti.com. Include the product you have questions or concerns with in the subject heading .

4 FCC Warnings

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his expense will be required to take whatever measures may be required to correct this interference.

Trademarks

TMS320 is a trademark of Texas Instruments.

5 EVM Overview

This section gives a general overview of the DAC7741 evaluation module (EVM), and describes some of the factors that must be considered in using this module.

5.1 Features

This EVM features the DAC7741 digital-to-analog converter. The DAC7741 EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality of the high resolution, single-channel, and parallel input DAC. This EVM features a parallel interface to communicate to any host processor base system

5.2 Power Requirements

The following sections describe the power requirements of this EVM.

5.2.1 Supply Voltage

The dc power supply requirement for the digital section of this EVM is typically 5 V connected to the J12-3 or via J6-10 terminal (when plugged in with another EVM board or interface card) and is referenced to ground through the J12-2 and J6-5 terminal. The dc power supply requirement for the analog section (V_{CC} and V_{SS}) of this EVM range from 15.75 V to -15.75 V maximum and connects through J11-3 and J11-1 or through J6-1 and J6-2 terminals and is referenced to analog ground through J11-2, J12-2, and J6-6 terminals.

The dc source of ±15 V supply required to provide the rails for the external output operational amplifier is derived from V_{CC} and V_{SS} as described above. The output operational amplifier, U2, is used for output signal conditioning or boost capacitive load drive and for other output modes of application.

CAUTION

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board. Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

5.2.2 Reference Voltage

Although the DAC7741 has a built-in 10-V voltage reference, an external reference circuit is provided in the EVM board. The external reference circuit can be isolated if the internal reference voltage is selected.

The 10-V precision voltage reference is provided to supply the external voltage reference for the DAC through REF102, U3, via jumper W4 by shorting pins 1 and 2. An adjustable 100-kΩ potentiometer, R11, is installed in series with 20-kΩ, R10, to allow the user to adjust the reference voltage to its desired settings. TP1 and TP2 are also provided, as well as J2-20 or J4-20 terminals via jumper W31, to allow the user to connect another external reference source if the onboard reference circuit is not desired. The external voltage reference should not exceed 10-V dc.

The REF102 precision reference derives its supply power of 15 V through J11 or J6 terminal as described earlier regarding supply voltages.

The DAC7741 has a $\overline{\text{REFEN}}$ pin to enable the internal reference circuit or disable it and select an external reference source. The $\overline{\text{REFEN}}$ pin can be hardware-driven through W2 jumper. Likewise, it can also be software-driven through J3-17 terminal via W2 jumper by shorting pins 1 and 2. The REF_{OUT} pin of the DAC7741 must be connected to the REF_{IN} pin to use the internal voltage reference. This is done through the W3 jumper by shorting pins 1 and 2. Shorting pins 2 and 3 of W3 selects the external voltage reference source.

The on-chip reference buffer output is funneled out through V_{REF} pin, which is used to set up the DAC7741 output amplifier into one of three voltage output modes. V_{REF} can also be used to drive other system components that require external voltage reference. See the data sheet for more information regarding the internal reference feature.

CAUTION

When applying an external voltage reference through TP1, J2-20, or J4-20, make sure that it does not exceed 14.35 V maximum. Otherwise, this can permanently damage the DAC7741, U1, device under test.

6 EVM Basic Functions

The DAC7741 EVM is a functional evaluation platform to test certain functional characteristics of the DAC7741 digital-to-analog converter. Functional evaluation of the DAC device can be accomplished with the use of any microprocessor, TMS320™ DSP family, or some sort of a signal/waveform generator.

The headers, J1 and J3, are provided to connect the necessary control signals and data needed to interface a microprocessor/microcontroller, TI's DSP Starter Kit, or waveform generator to the DAC7741 EVM. A custom cable can be built for this purpose if using the EVM without the use of TI's 5-6k interface adapter board or the HPA449 platform.

The 5-6k interface adapter board is used for most of TI's DSP Starter Kits (DSK). Hence, if using the TMS320C5x™ DSP generation and TMS320C6x™ DSP generation DSKs, the 5-6k interface adapter board proves practical, as no cabling is required. In addition, the HPA449 platform is also available for use if the MSP430 microcontroller is desired as the host processor. Call or e-mail TI for more information regarding the adapter interface board.

The output of the DAC can be monitored through one of two terminals J2 or J4. Shorting pins 1 and 2 of jumper W30, allows the DAC output to be seen on J4 pins 2, 4, 6, and 8. The 6-pin header, W13, provides different options of the DAC output, but requires the output operational amplifier, U2, to first be configured correctly for the desired waveform characteristic. Shorting pins 1 and 2 of W13 allows the user to monitor the raw output of the DAC7741.

A block diagram of the EVM is shown below in the Figure 1.

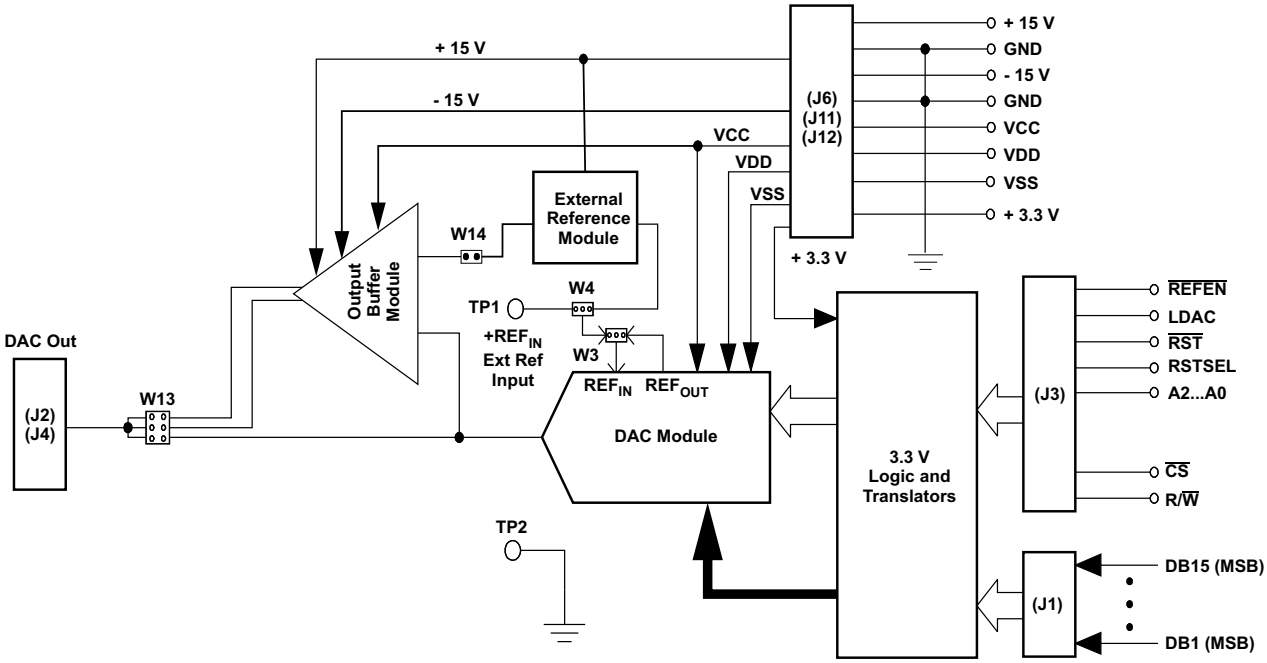


Figure 1. EVM Block Diagram

7 Physical Description

This section describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

7.1 PCB Layout

The EVM is constructed on a four-layer printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 96,52 mm (3.80 inch) X 102,87 mm (4.050 inch), and the board thickness is 1,57 mm (0.062 inch). Figure 2 through Figure 6 show the individual artwork layers.

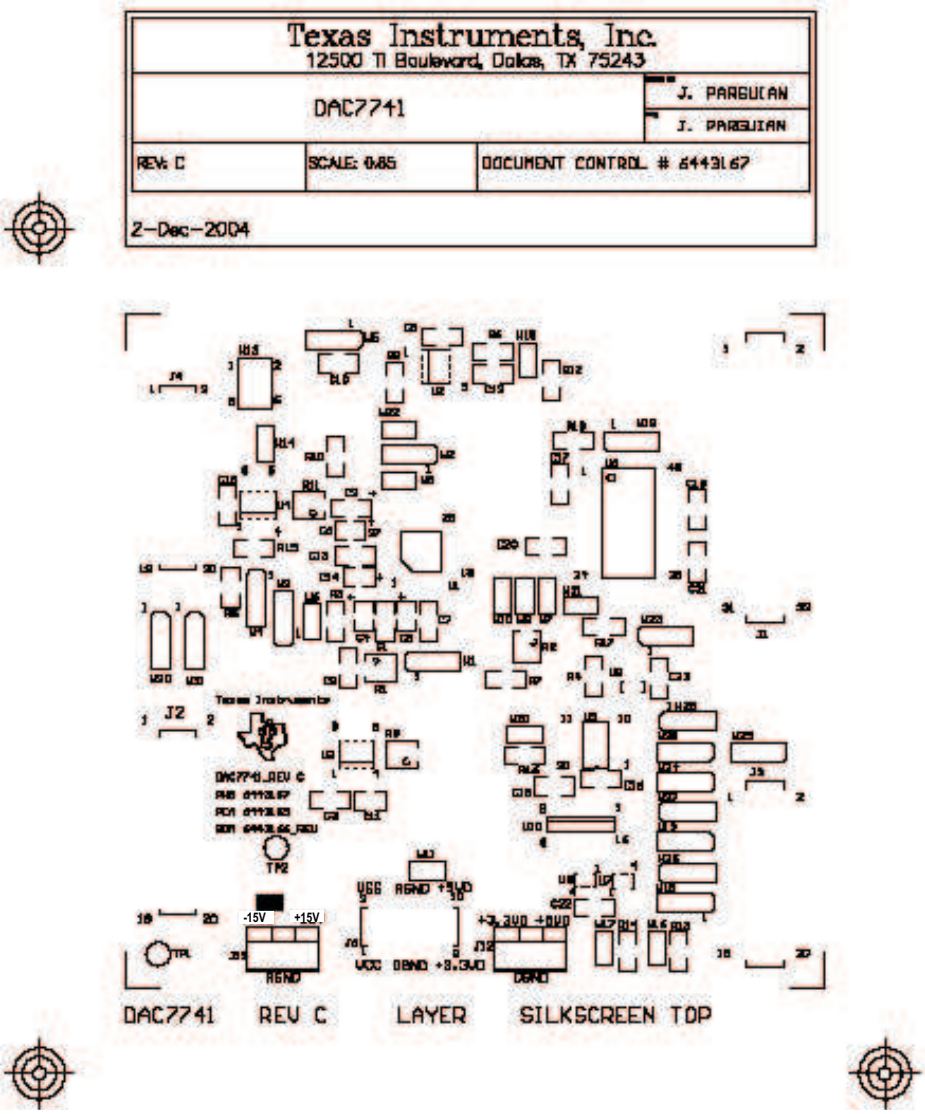


Figure 2. Top Silkscreen

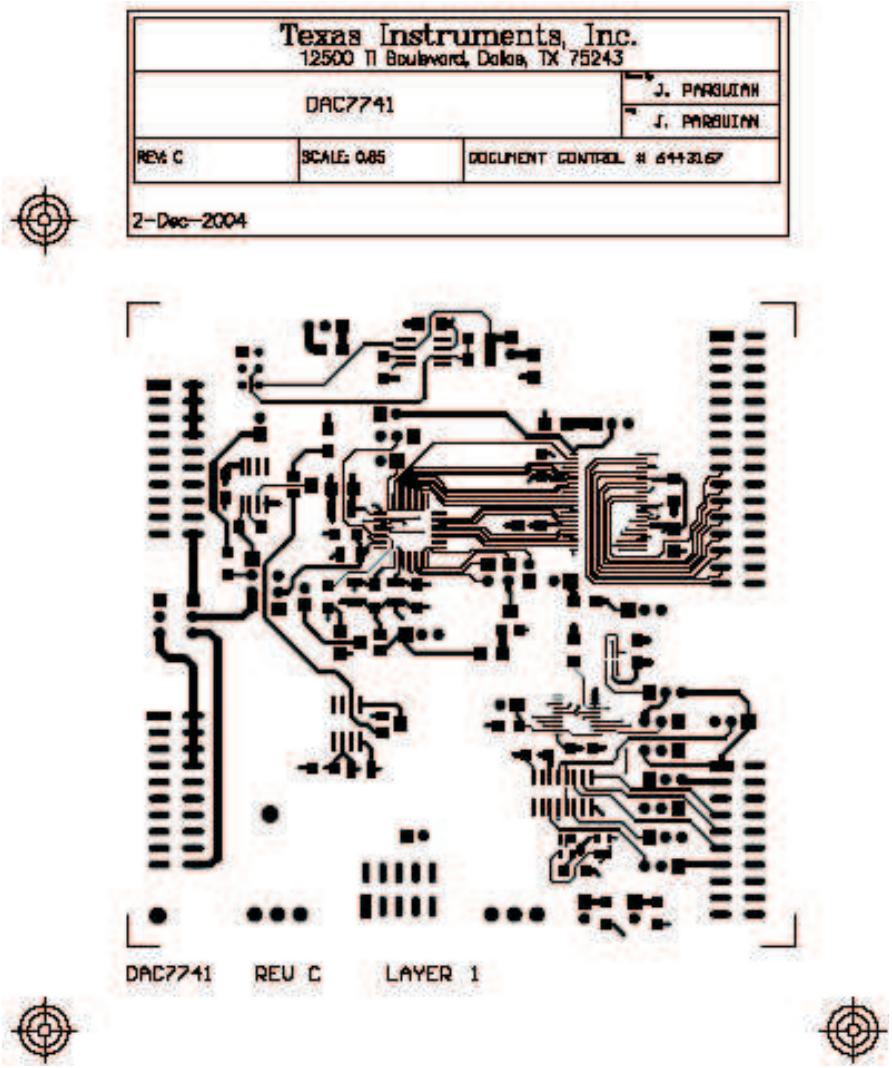


Figure 3. Layer One (Top Signal Plane)

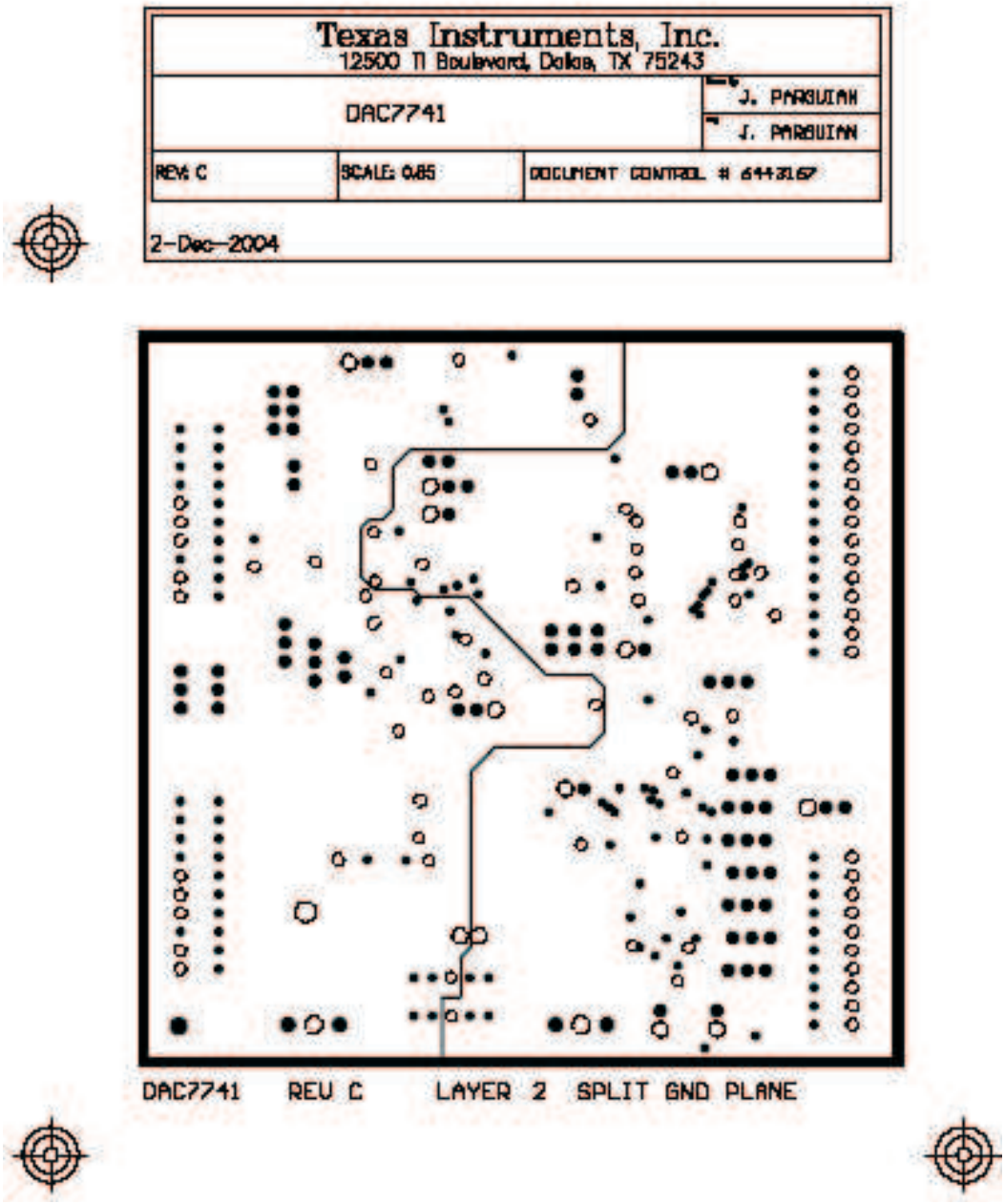


Figure 4. Layer Two (Split Ground Plane)

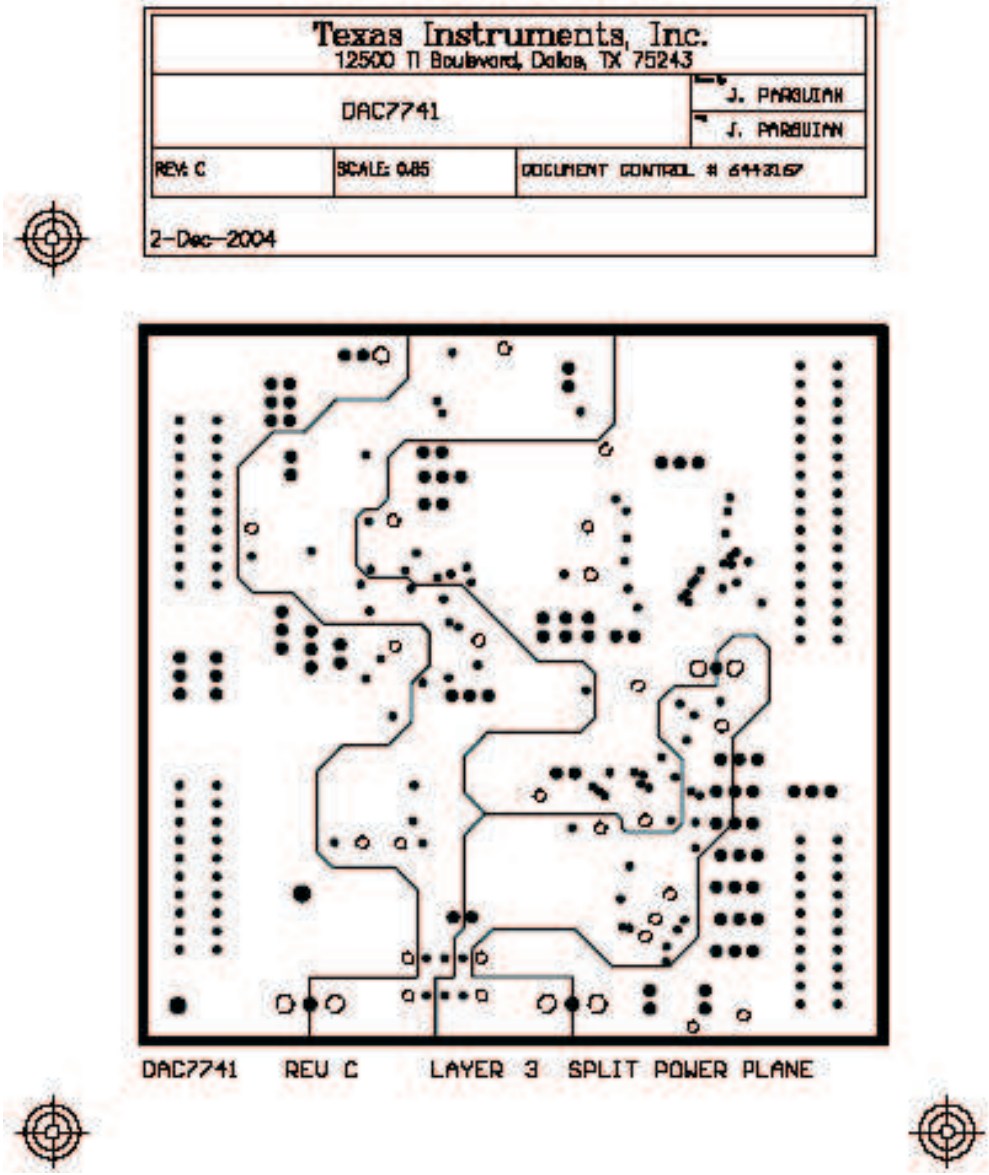


Figure 5. Layer Three (Split Power Plane)

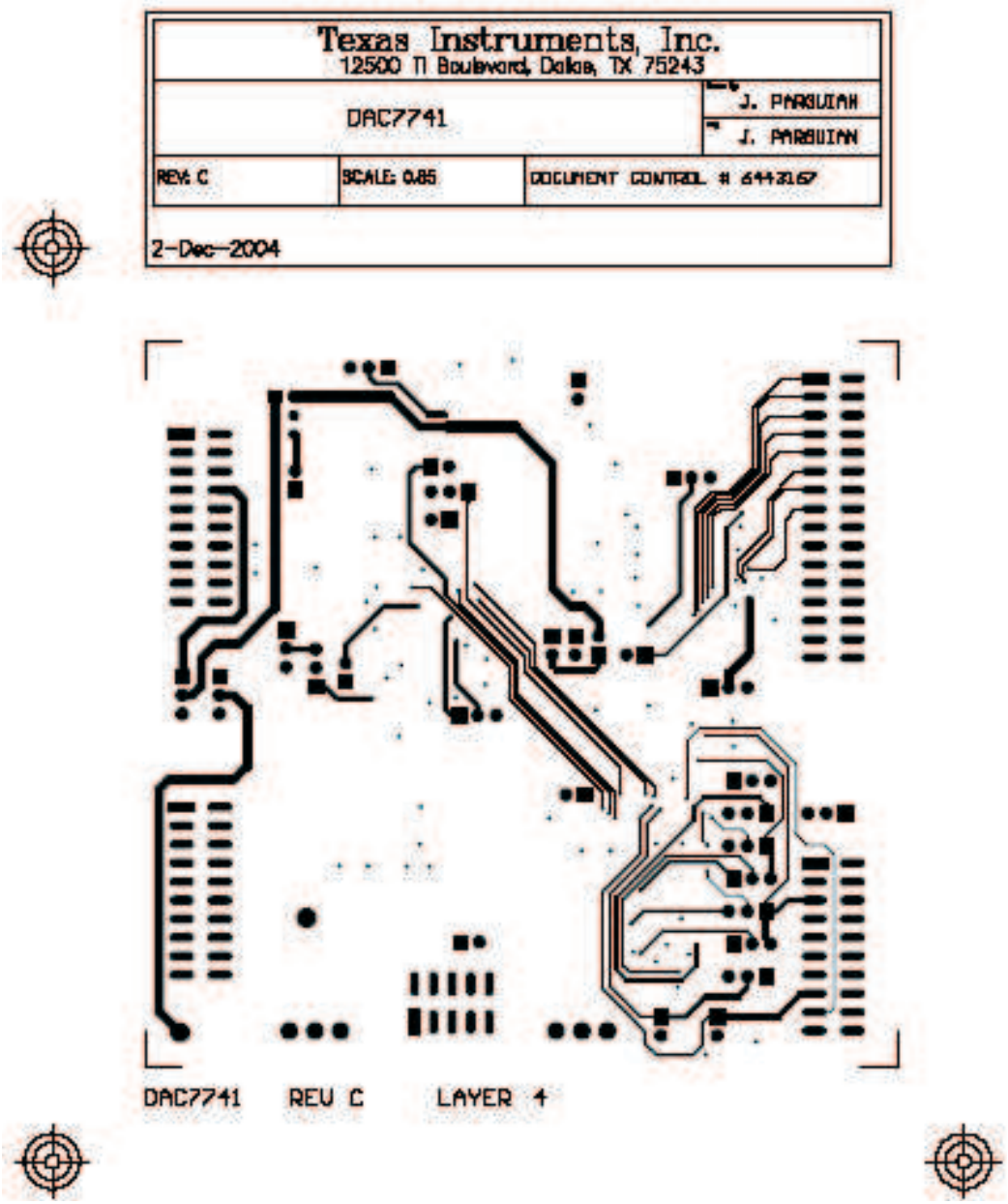


Figure 6. Layer Four (Bottom Signal Plane)

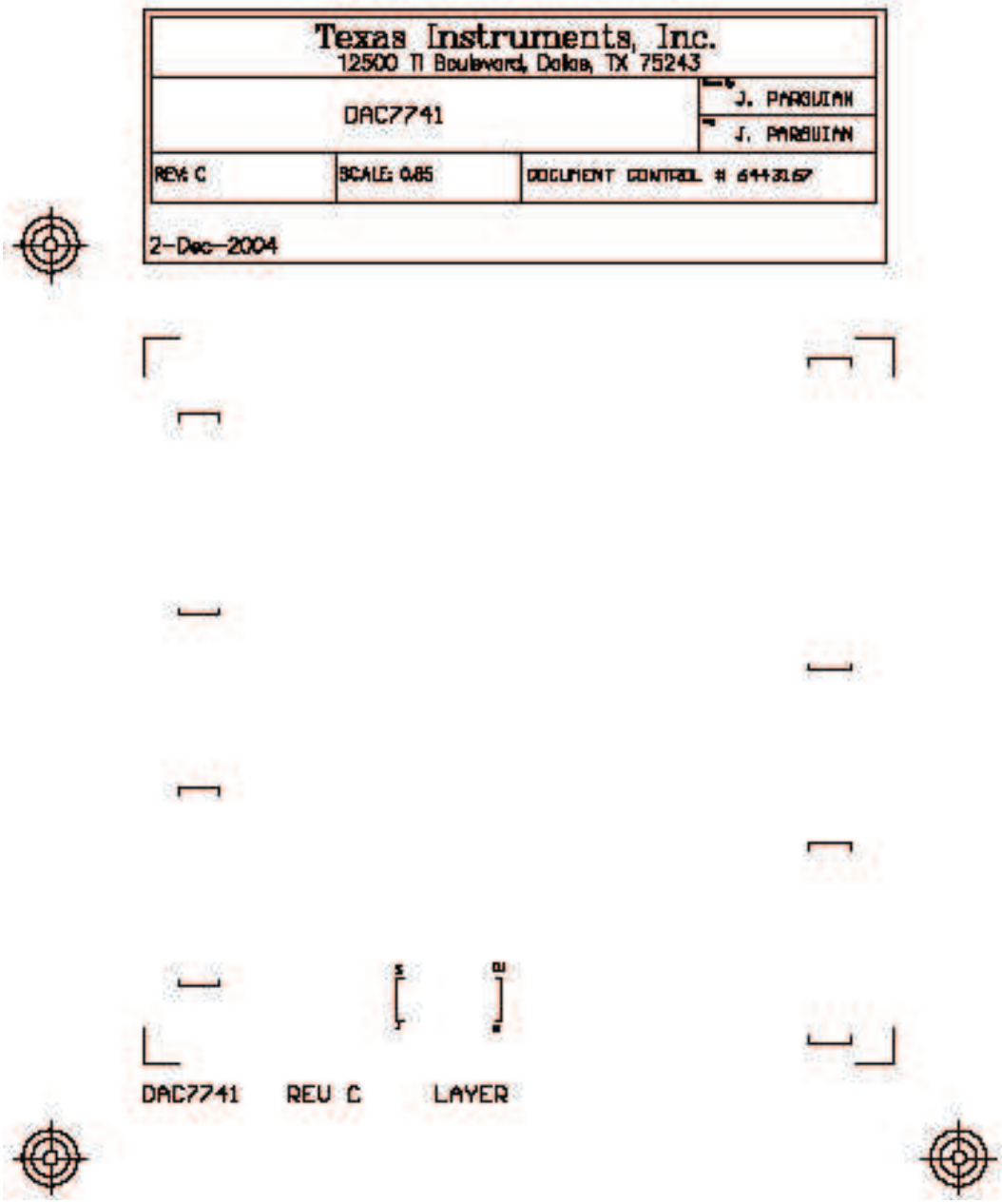


Figure 7. Bottom Silkscreen

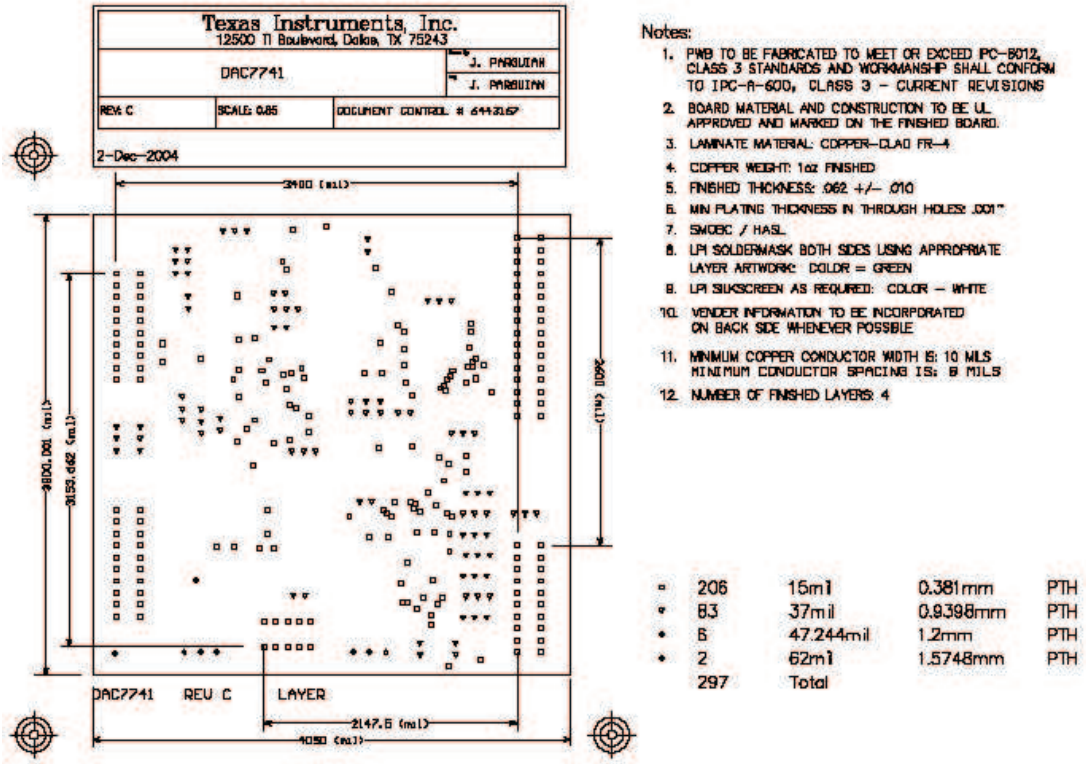


Figure 8. Drill Drawing

8 Bill Of Materials

Table 1. Parts List

Item	Quantity	Designators	Manufacturer	Part Number	Description
1	2	R8, R15	Panasonic	ERJ-8GEY0R00V	0 Ohm
2	1	C8	TDK	C3216C0G1H105JT	1 µF
3	14	C1, C2, C3, C7, C13(1), C15, C16, C17, C18, C19, C20, C21, C22, C23	TDK	C3216C0G1E104JT	0.1 µF(1)
4	2	C9, C10	TDK	C3216X7RJ103KT	0.01 µF
5	1	C12	TDK	C3216C0G2J102JT	1 nF
6	11	W6, W7, W8, W9, W10, W11, W16, W17, W20, W21, W22	Molex	22-03-2021	2 CIRCUIT HEADER, .100 STRAIGHT
7	17	W1, W2, W3, W4, W5, W12, W18, W19, W23, W24, W25, W26, W27, W28, W29, W30, W31	Molex	22-03-2031	3 CIRCUIT HEADER, .100 STRAIGHT
8	1	P6	Samtec	SSW-105-22-F-D-VS-K	10-PIN Isolated Power Socket, .100 (2)
9	9	R4, R5, R6, R12, R13, R14, R16 R17, R18	Panasonic	ERJ-8ENF1002V	10-K Ohms 1206 1/4W 5% Chip Resistor
10	2	R1, R2	Bourns	3214W-103E	10-K potentiometer
11	1	R10	Panasonic	ERJ-8ENF2002V	20K Ohms 1206 1/4W 5% Chip Res.
12	1	R11	Bourns	3214W-104E	100-K potentiometer
13	1	R9	Bourns	3214W-203E	20-K potentiometer
14	5	C4, C5, C6, C11, C14(1)	TDK	C3225X5R1C106KT	10 µF(1)
15	3	J2, J3, J4	Samtec	TSM-110-01-S-DV-M	20-PIN IDC
16	1	J6	Samtec	TSM-105-01-T-DV	10-PIN IDC
17	3	P2, P3, P4	Samtec	SSW-110-22-S-D-VS-P	20-PIN IDC (2)
18	2	J11, J12	On-Shore Tech.	ED555/3DS	3-Pin Terminal Connector
19	1	J1	Samtec	TSM-116-01-S-DV-M	32-PIN IDC
20	1	P1	Samtec	SSW-116-22-S-D-VS-P	32-PIN IDC(2)
21	1	U1	TI	DAC7741	DAC7741
22	1	U2	TI	OPA227UA	8-SOP (D)
23	1	U3	TI	REF102AU	8-SOP (D)
24	1	U4	TI	OPA2277UA	8-SOP (D)
25	1	U5	TI	SN74AHC541PW	20-Pin TSSOP 9PW)
26	1	U6	TI	SN74ALVC164245DL	48-SSOP (DL)
27	1	U7	TI	SN74AHC1G08DBVR	5-SOT (DBV)
28	1	U8	TI	SN74AHC1G04DBVR	5-SOT (DBV)
29	1	U9	TI	SN74AUP1G57DBVR	SOT23-6 (DBV)
30	1	U10	TI	SN74AHC138D	16-SOP (D)
31	2	TP1, TP2	Mill-Max	2348-2-01-00-00-07-0	TP_TURRENT

(1) C13 and C14 are not populated. Use only when an external reference source is derived from TP1, J2-20, or J4-20 (particularly with an unclean source).

(2) P1, P2, P3, P4, and P6 parts are not shown in the schematic diagram. All the P-designated parts are installed in the bottom side of the PC board opposite the J-designated counterpart. Example, J1 is installed on the top side while P1 is installed in the bottom side opposite of J1.

9 EVM Operation

This section covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC, and how to interface the EVM to a specific host processor.

See the DAC7741 data sheet, SBAS248, for information about its parallel interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

9.1 Factory Default Settings

The EVM board is set to its default configuration from factory as described on the table below to operate in bipolar ±10-V mode of operation using the external reference.

Table 2. Factory Default Jumper Settings

Reference	Jumper Position	Function
W1	OPEN	V_{REF} output pin is floated and not used for offset adjustment.
W2	OPEN	$\overline{REFEN}$ pin is not used to enable 10-V internal reference.
W3	2-3	External reference source, U3, is routed to REF_{IN} to provide 10-V reference.
W4	1-2	Onboard external reference through U3 is connected.
W5	1-2	Negative supply rail of the U2 operational amplifier is supplied with -15 V.
W6	OPEN	REFADJ pin is floated.
W7	CLOSE	RFB2 pin is strapped to V_{OUT} pin for DAC output feedback.
W8	CLOSE	TEST pin is tied to DGND.
W9	OPEN	SJ pin is floated.
W10	OPEN	RFB1 is floated.
W11	CLOSE	AGND and DGND are tied together to a common point.
W12	2-3	The LDAC signal used is address decoded, and translated to the DSP_LDAC.
W13	3-4	Buffered output of DAC is fed through W30 and to J4 terminal.
W14	OPEN	External reference is disconnected from the negative input of U2 to configure U2 for unity gain.
W15	OPEN	Configure U2 operational amplifier for unity gain.
W16	OPEN	RSTSEL pin is tied high to set DAC reset value to mid-scale.
W17	OPEN	$\overline{RST}$ pin is tied high by default.
W18	1-2	U6 direction control, DIR, set to A-to-B direction.
W19	OPEN	$\overline{RST}$ pin not driven.
W20	CLOSED	The U5 output enable pins, $\overline{OE1}$ and $\overline{OE2}$, are enabled.
W21	OPEN	The U6 enable pins, $\overline{1G}$ and $\overline{2G}$, are enabled.
W22	OPEN	The U6 direction pin, DIR, is not controlled by the R/$\overline{W}$ signal.
W23	2-3	The U6 is powered with 3.3 VD.
W24	2-3	The DC_CSa# signal is used to control the R/$\overline{W}$ function.
W25	1-2	The DSP_R/$\overline{W}$ pin is used to control the $\overline{CS}$ function.
W26	1-2	The C6x_RD pin is routed for the combination DSP_R/$\overline{W}$ control signal.
W27	1-2	The C6x_$\overline{WR}$ pin is routed for the combination DSP_R/$\overline{W}$ control signal.
W28	OPEN	The DSP_$\overline{CS}$ pin is not used (C5x™ DSP only).
W29	1-2	The DC_CSa# is used to control the enable function of U10.
W30	1-2	V_{OUT} is routed to J4 terminal.
W31	OPEN	External reference source via pin 20 of J2 or J4 is not used.

9.2 Host Processor Operations

The host processor basically drives the DAC; so, the DAC proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interfacing to the host processor through J3 header connector for the control signals, and J1 header connector for the data input. An interface adapter card for a specific DSP starter kits or an HPA449 platform is also available as mentioned in section 1 of this manual.

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. This is set to a unity gain configuration by default. Regardless, the raw output of the DAC can be probed through W13 pin 2 so that it can be compared with the output of U2, if necessary. The output terminals J2 and J4 are provided to monitor the desired output of the DAC by shorting the respective pins of W13 and selecting the position of W30.

The following sections describe the different configurations of the output amplifier, U2.

9.2.1 Unity Gain Output

The buffered output configuration is used to prevent loading the DAC7741 and should closely match the raw output of the DAC with maybe some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match the desired wave shape by simply desoldering R6 and C12 and replacing them with the desired values. If desired, the user can simply delete R6 and C12 altogether, and solder a 0-Ω resistor in place of R6.

Table 3 shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar or bipolar mode.

Table 3. Unity Gain Output Jumper Settings

Reference	Jumper Setting		Function
	Unipoar	Bipolar	
W5	2-3	1-2	Supplies the voltage for the negative rail of the operational amplifier.
W13	3-4	3-4	DAC output is sent to the output terminals.
W14	Open	Open	exREFin is disconnected from the negative input of the operational amplifier.
W15	Open	Open	Disconnect negative input of the operational amplifier from GND

9.2.2 Output Gain of Two

This configuration allows the DAC output with a gain of two but is limited to the effective rails of the operational amplifier. When the DAC7741 is configured to operate in bipolar mode, the DAC output must be within the range of 12 V_{PP} or less. Anywhere above the range of 12 V_{PP} clips the output of the operational amplifier. Likewise, when operating the DAC in unipolar mode, the DAC output must not exceed 6 V_{PP}.

Table 4 shows the proper jumper settings of the EVM for the 2x gain output of the DAC.

Table 4. Gain of Two Output Jumper Settings

Reference	Jumper Setting	Function
W5	1-2 (Bipolar) 2-3 (Unipolar)	Negative rail of the operational amplifier tied to -15 V for bipolar operation or AGND for unipolar operation.
W13	3-4	Amplified output of DAC is sent to the output terminal.
W14	Open	Disconnect exREFin from negative input of the operational amplifier.
W15	Open	Configures the operational amplifier for a 2x gain output.

9.2.3 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive load requirement. However, all operational amplifiers under certain conditions may become unstable depending on the operational amplifier configuration, gain, and load value. These are just few factors that can affect operational amplifiers stability performance and should be considered when implementing.

In unity gain, the OPA627 operational amplifier, U2, performs well with large capacitive loads. Increasing the gain enhances the amplifier's ability to drive even more capacitance, and by adding a load resistor would even improve the capacitive load drive capability.

Table 5 shows the jumper setting configuration for a capacitive load drive.

Table 5. Capacitive Load Drive Output Jumper Settings

Reference	Jumper Setting	Function
W5	1-2 (Bipolar) 2-3 (Unipolar)	Negative rail of the operational amplifier tied to -15 V for bipolar operation or AGND for unipolar operation.
W13	3-4	Capacitive load drive output of DAC is channeled to the output terminals
W14	Open	Disconnect exREFin from negative input of the operational amplifier.
W15	Open	Disconnect R12 (1)

(1) If there is a need to incrementally adjust the capacitive load output, replace R12 with a capacitor with the desired capacitance value and close W15.

9.3 Jumper Setting

The figures in Table 6 shows the function of each jumper on the EVM.

Table 6. Jumper Setting Function

Reference	Jumper Setting	Function
W1		R_{OFFSET} is strapped to V_{REF} to set $V_{(SJ)}$ (summing junction) to $V_{REF}/2$. See the data sheet for offset adjustment.
		R_{OFFSET} is not connected to set $V_{(SJ)}$ (summing junction) to $V_{REF}/3$. See the data sheet for offset adjustment.
		R_{OFFSET} is strapped to AGND to set $V_{(SJ)}$ (summing junction) to $V_{REF}/6$. See the data sheet for offset adjustment.
W2		Disables the internal reference voltage.
		Enables the internal reference voltage of 10 V.
W3		REF_{IN} is strapped to REF_{OUT} to allow the internal 10 V to supply the DAC reference voltage.
		REF_{IN} is strapped to exREFin to allow either the onboard adjustable reference or user-supplied reference to supply the DAC reference voltage.
W4		Routes the onboard 10-V reference through the adjustable potentiometer to W3 and W14.
		Routes the user-supplied reference from TP1 or J4-20 through the adjustable potentiometer to W3 and W14.
W5		Negative supply rail of operational amplifier is powered by -15 V.
		Negative supply rail of operational amplifier is tied to AGND.
W6		REFADJ pin is not connected.
		REFADJ pin is connected to R1 potentiometer for gain adjustment input when internal reference is used.
W7		RFB2 pin is not connected to the V_{OUT} pin.
		RFB2 pin is strapped to the V_{OUT} pin for feedback.
W8		TEST pin not connected to DGND.
		TEST pin connected to DGND (default mode).
W9		SJ (summing junction) pin of the DAC output amplifier is not connected.
		SJ (summing junction) pin of the DAC output amplifier is connected to R2 potentiometer to allow small amount of current for offset adjustment.
W10		RFB1 pin is not connected.
		RFB1 pin is strapped to RFB2 pin for DAC V_{OUT} feedback.
W11		Disconnects AGND from DGND.
		Connects AGND and DGND together.

Table 6. Jumper Setting Function (continued)

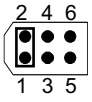
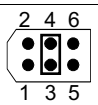
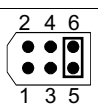
Reference	Jumper Setting	Function
W12		Positive supply rail of operational amplifier is powered by 15 V.
		Positive supply rail of operational amplifier is powered by V_{CC}.
W13		Routes the raw output of the DAC7741 to J4-2 and J5 output terminals.
		Routes the output of U2 to J4-2 and J5 output terminals. Used for unipolar and bipolar modes of operation.
		Routes the output of U2 to J4-2 and J5 output terminals. Used for capacitive load driving.
W14		Disconnects exREFin from the negative input terminal of U2.
		Allows exREFin to be routed to the negative input terminal of U2 used for experimentation purposes only.
W15		Disconnects the negative terminal of U2 to AGND and disables 2x gain.
		Configures U2 for a 2x gain output.
W16		$\overline{\text{RSTSEL}}$ pin is pulled high and configures the DAC to mid-scale when POR or reset is initiated.
		$\overline{\text{RSTSEL}}$ pin is pulled low and configures the DAC to min-scale when POR or reset is initiated.
W17		$\overline{\text{RST}}$ pin is pulled high and configures the DAC not to reset (default state).
		$\overline{\text{RST}}$ pin is pulled low and holds the DAC to reset state.
W18		The U6 DIR control pin is tied high for direction flow from A-to-B.
		The U6 DIR control pin is tied low for direction flow from B-to-A.
W19		The HPA449_$\overline{\text{RST}}$ pin (via J3-13) is used to drive the $\overline{\text{RST}}$ signal.
		The DSP_$\overline{\text{RST}}$ pin (via U10-11) is used to drive the $\overline{\text{RST}}$ signal.
W20		U5 is disabled.
		U5 is enabled.
W21		U6 is disabled.
		U6 is enabled.
W22		R/$\overline{\text{W}}$ is not routed through to control U6 direction pin, DIR.
		R/$\overline{\text{W}}$ is routed through to control U6 direction pin, DIR.

Table 6. Jumper Setting Function (continued)

Reference	Jumper Setting	Function
W23		U6 is powered with 5 VD.
		U6 is powered with 3.3 VD.
W24		The $\overline{WR}$ signal (via J3-3) controls the R/$\overline{W}$ function.
		The DC_CSa# signal (via J3-1) controls the R/$\overline{W}$ function.
W25		The DSP_R/$\overline{W}$ signal (if using C6x™ DSP) is used to control the $\overline{CS}$ function.
		The DSP_$\overline{CS}$ signal (if using C5x™ DSP) or the HPA449_$\overline{CS}$ signal (if using HPA449) is used to control the $\overline{CS}$ function. Works with W28.
W26		The C6x_RD signal is routed for the combination DSP_R/$\overline{W}$ signal function.
		The RD signal (if using C5x™ DSP) is routed for the combination DSP_R/$\overline{W}$ signal function.
W27		The C6x_$\overline{WR}$ signal is routed for the combination DSP_R/$\overline{W}$ signal function.
		$\overline{WR}$ signal (if using C5x™ DSP) is routed for the combination DSP_R/$\overline{W}$ signal function.
W28		The combination $\overline{CE}$ signal (if using C5x™ DSP) is used to generate the DSP_$\overline{CS}$ signal.
		The DC_CSa# signal (if using C5x™ DSP) or HPA449_$\overline{CS}$ signal (if using HPA449) is used to control the $\overline{CS}$ function. Works with W25.
W29		The DC_CSa# signal is used to control the enable pins of U6.
		The enable pin of U6 is tied low, which enables the device all the time.
W30		DAC V_{OUT} is routed to J4 terminal.
		DAC V_{OUT} is routed to J2 terminal.
W31		External reference source through J4-20 is routed in.
		External reference source through J2-20 is routed in.
Legend:		Indicates the corresponding pins that are shorted or closed.

9.4 Schematic

A schematic of the DAC7741 is found on the following page.

Revision History		
REV	ECN Number	Approved
A	Original Release	
B	Added Logic to accomodate 5-6K card	
C	Added option of selecting output terminal and corrected DSP CS & R/nW logic.	

[DB15..DB0]

J1: 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

+5VD
R18 10K
DIR
W18

U6 SN74ALVC164245

1	1DIR	1G	48	EN	
DB15 2	1B1	1A1	47	D15	
DB14 3	1B2	1A2	46	D14	
4	GND	GND	45		
DB13 5	1B3	1A3	44	D13	
DB12 6	1B4	1A4	43	D12	
7	VCC	VCC	42		
DB11 8	1B5	1A5	41	D11	
DB10 9	1B6	1A6	40	D10	
10	GND	GND	39		
DB9 11	1B7	1A7	38	D9	
DB8 12	1B8	1A8	37	D8	
DB7 13	2B1	2A1	36	D7	
DB6 14	2B2	2A2	35	D6	
15	GND	GND	34		
DB5 16	2B3	2A3	33	D5	
DB4 17	2B4	2A4	32	D4	
18	VCC	VCC	31		
DB3 19	2B5	2A5	30	D3	
DB2 20	2B6	2A6	28	D2	
21	GND	GND	28		
DB1 22	2B7	2A7	27	D1	
DB0 23	2B8	2A8	26	D0	
DIR 24	2DIR	2G	25	EN	

+5VD C17 0.1µF
+5VD C20 0.1µF
+5VD +3.3VD W23 VCCA
C19 0.1µF
VCCA C21 0.1µF
+5VD W21 R17 10K

+5VD C16 0.1µF R16 10K W20

+5VD R13 10k R14 10k
W16 W17 RST RSTSEL

U5 SN74AHC541

20	VCC	OE1	1
19	OE2	A1	2 CS
CS_B 18	Y1	A2	3 R/W
R/W_B 17	Y2	A3	4 LDAC
LDAC_B 16	Y3	A4	5 RST
RST_B 15	Y4	A5	6
RSTSEL_B 14	Y5	A6	7
REFen_B 13	Y6	A7	8
12	Y7	A8	9
11	Y8	GND	10

Control_Signals

DSP_R/W W25
WR (HPA449_R/W) DSP_CS (HPA449_CS)
W24 DC_CSa#
RD (HPA449_LDAC) W12 DSP_LDAC
HPA449_RST W19 DSP_RST
RSTSEL REFen R4 10K +5VD

+3.3VD C18 0.1µF
+3.3VD DC_CSa# W29

U10 SN74AHC138

A0 1	VCC	Y0	15
A1 2	B	Y1	14 C6x_RD
A2 3	C	Y2	13 C6x_WR
		Y3	12 DSP_LDAC
6	G1	Y4	11 DSP_RST
4	G2A	Y5	10
5	G2B	Y6	9
	GND	Y7	7
8			

DAC7741 DAC7741_Sheet2.Sch
Control_Signals Control_Signals
[DB15..DB0] OUTPUT [DB15..DB0]
U2_VOUT W30

J4: 2 1 4 3 6 5 8 7 10 9 12 11 14 13 16 15 18 17 20 19

+3.3VD C22 0.1µF
W26 U8 SN74AHC1G04
W27 U7 SN74AHC1G08 DSP_R/W

+REFin W31

J2: 2 1 4 3 6 5 8 7 10 9 12 11 14 13 16 15 18 17 20 19

+3.3VD+1.8VD +5VA VCC VSS -5VA +3.3VA +5VD
J6: 1 2 3 4 5 6 7 8 9 10

J11 J12
VSS VCC +3.3VD +5VD
W11

DIR W22 R/W_B

U4B OPA2227UA

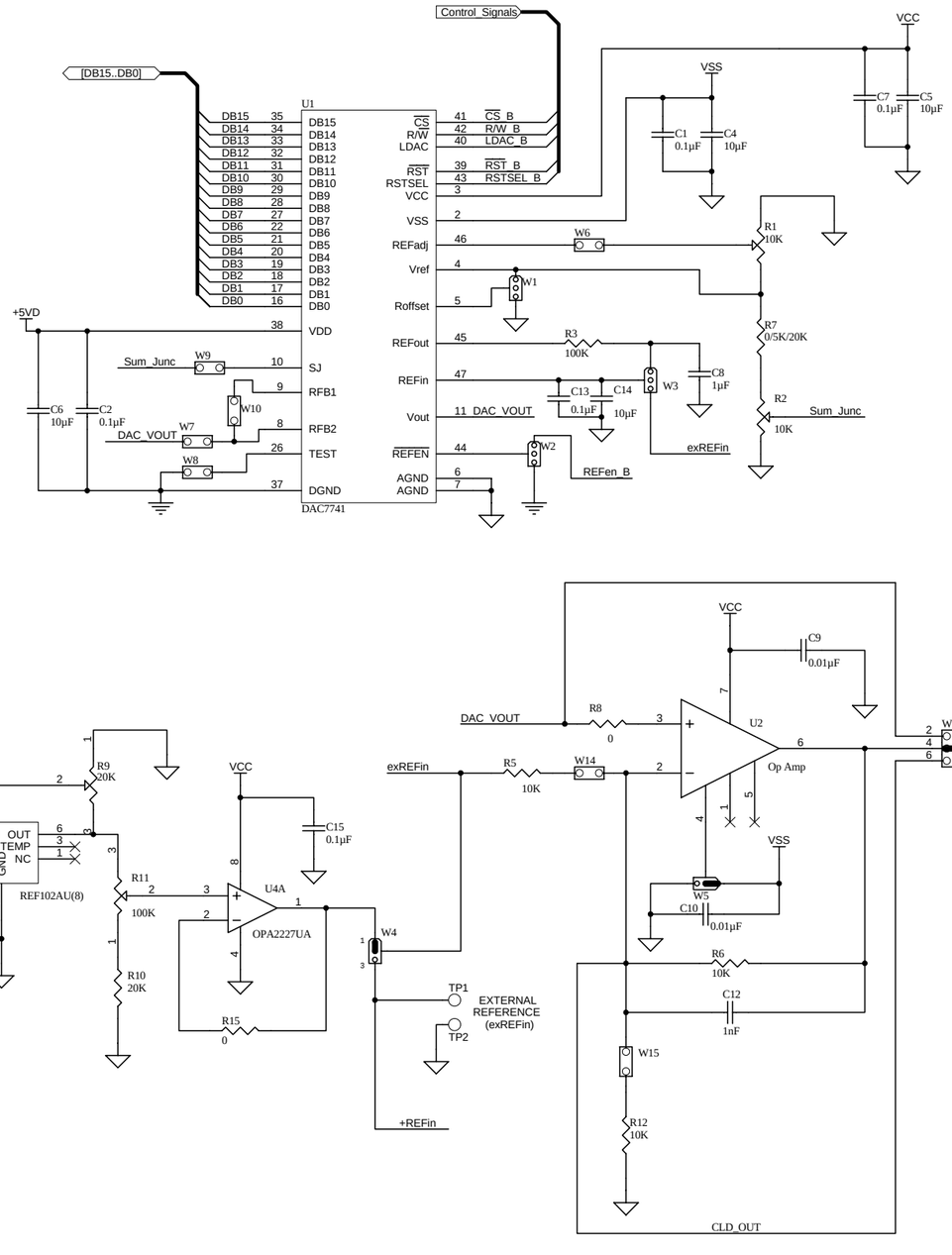
+3.3VD C23 0.1µF
U9 SN74AUP1G57
CE W28 DSP_CS
DC_CSa# (HPA449_CS)

J3: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
DC_CSa#(HPA449_CS)
WR (HPA449_R/W)
RD (HPA449_LDAC)
A0 A1 A2
HPA449_RST
RSTSEL
REFen

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title:	CONNECTORS AND LOGIC		
DOCUMENTCONTROL #	6443168		REV: C
DATE: 10-May-2005	SIZE:	SHEET: 1	OF: 2
Engineer: J. PARGUIAN			
Drawn By:			
FILE: DAC7741_Sheet1.Sch			

Revision History		
REV	ECN Number	Approved



Engineer: J. PARGUIAN	
Drawn By:	
FILE: DAC7741_Sheet2.Sch	

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Title: DAC7741			
DOCUMENTCONTROL # 6443168			REV: C
DATE: 10-May-2005	SIZE:	SHEET: 2	OF: 2

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE Liable to the other FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ±15 V and the output voltage range of ±10 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above ° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2005, Texas Instruments Incorporated

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265