PCM175x-Q1 24-Bit 192-kHz Sampling Enhanced Multi-Level Delta-Sigma Audio Digital-to-Analog Converter

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- 24-Bit Resolution
- Analog Performance (V_{CC} = 5 V)
  - Dynamic Range: 106 dB
  - SNR: 106 dB, Typical
  - THD+N: 0.002%, Typical
  - Full-Scale Output: 4 V_{PP}, Typical
- 4× and 8× Oversampling Digital Filter
  - Stop-Band Attenuation: –50 dB
  - Pass-Band Ripple: ±0.04 dB
- Sampling Frequency: 5 kHz to 200 kHz
- System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S, 1152 f_S with Auto Detect
- Hardware Control (PCM1754-Q1)
  - I^2S and 16-Bit Word, Right-Justified
  - 44.1 kHz Digital De-Emphasis
  - Soft Mute
  - Zero Flag for L-, R-Channel Common Output
- Power Supply: 5-V Single Supply
- Small 16-Lead SSOP Package, Lead-Free

2 Applications

- Automotive Infotainment and Cluster
- A/V Receivers
- HDTV Receivers
- Car Audio Systems
- Other Applications Requiring 24-Bit Audio

3 Description

The PCM175x-Q1 family of devices is a CMOS, monolithic, integrated circuit, which includes stereo digital-to-analog converters and support circuitry in a small 16-lead SSOP package. The data converters use TI's enhanced multilevel delta-sigma architecture, which employs 4th-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM175x-Q1 family of devices accepts industry-standard audio data formats with 16- to 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 200 kHz are supported. A full set of user-programmable functions is accessible through a three-wire serial control port, which supports register write functions.

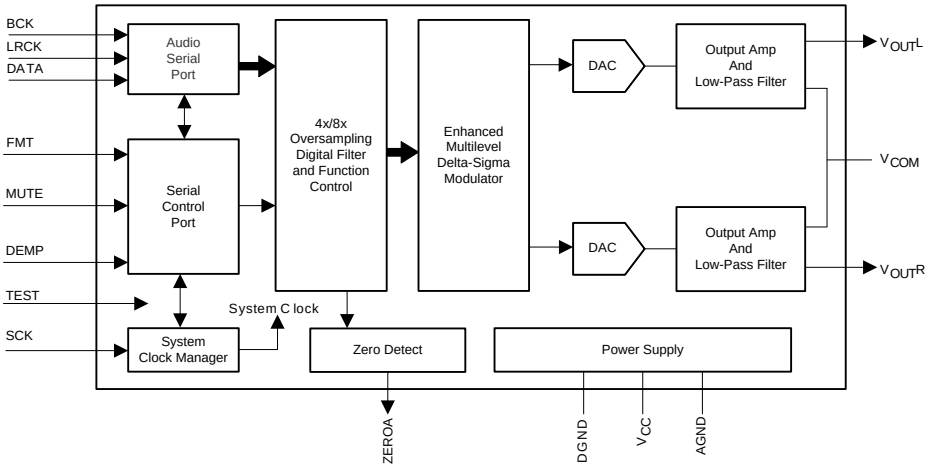
The PCM1753-Q1 device is pin-compatible with the PCM1748, PCM1742, and PCM1741 devices, except for pin 5.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM1753-Q1	SSOP (16)	4.90 mm × 3.90 mm
PCM1754-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2012) to Revision D — **Page**

- Changed device temperature grade from 1 to 2 in the *Features* list ... 1
- Added the *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (December 2011) to Revision C — **Page**

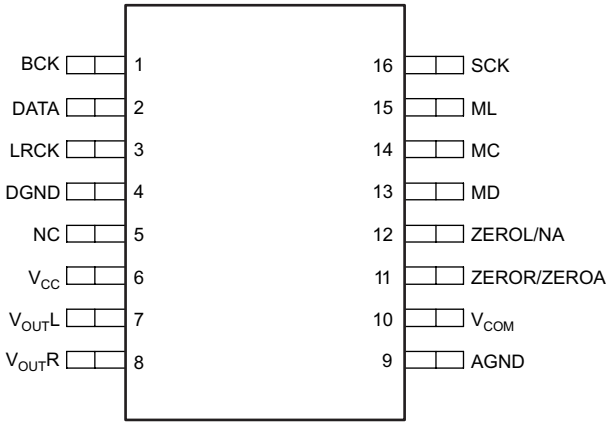
- Added AEC-Q100 info to Features ... 1
- Removed DVD Movie Players, DVD Add-On Cards for High-End PCs, and DVD Audio Players from Applications. ... 1
- Added ESD ratings to Abs Max table. ... 5

5 Device Comparison Table

FEATURE	PCM1753-Q1	PCM1754-Q1
Audio-data interface format	I^2S, standard, left-justified	I^2S, standard
Audio-data bit length	16-bit, 18-bit, 20-bit, and 24-bit selectable	16-bit and 24-bit I^2S, 16-bit standard
Audio data format	MSB first, 2s complement	

6 Pin Configuration Functions

PCM1753-Q1 DBQ Package
16-Pin SSOP
Top View

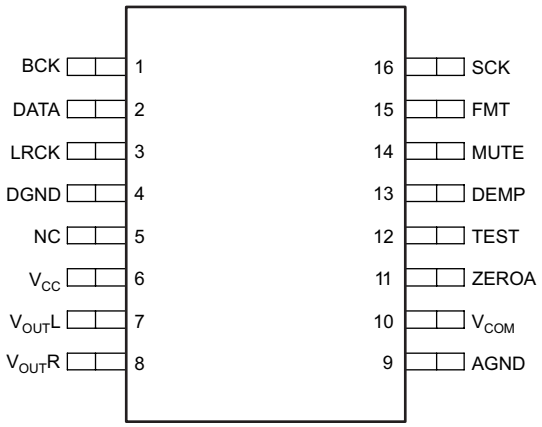


Pin Functions—PCM1753-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	9	—	Analog ground
BCK	1	I	Audio–data bit–clock input
DATA	2	I	Audio–data digital input
DGND	4	I	Digital ground
LRCK	3	—	L-channel and R-channel audio data latch enable input
MC	14	I	Mode control clock input(1)
MD	13	I	Mode control data input(1)
ML	15	I	Mode control latch input(1)
NC	5	—	No connection
SCK	16	I	System clock input
V_{CC}	6	I	Analog power supply, 5 V
V_{COM}	10	—	Common voltage decoupling
$V_{OUT}L$	7	—	Analog output for the L-channel
$V_{OUT}R$	8	O	Analog output for the R-channel
ZEROR/ZEROA	11	O	Zero flag output for the R-channel. This pin is also the zero flag output for the L-channel and R-channel(2).
ZEROL/NA	12	O	Zero flag output fo the L-channel. Not assigned(2)

(1) Schmitt-trigger input with internal pulldown
(2) Open-drain output.

PCM1754-Q1 DBQ Package
16-Pin SSOP
Top View



Pin Functions—PCM1754-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	9	—	Analog ground
BCK	1	I	Audio–data bit–clock input
DATA	2	I	Audio–data digital input
DEMP	13	I	De–emphasis control(1)
DGND	4	—	Digital ground
FMT	15	I	Data format select(1)
LRCK	3	I	L–channel and R–channel audio data latch enable input
MUTE	14	I	Analog mixing control(1)
NC	5	—	No connection
SCK	16	I	System clock input
TEST	12	I	Test pin. Ground or open(1)
V_{CC}	6	—	Analog power supply, 5 V
V_{COM}	10	—	Common voltage decoupling
$V_{OUT}L$	7	O	Analog output for the L–channel
$V_{OUT}R$	8	O	Analog output for the R–channel
ZEROA	11	O	Zero flag output for the L-channel and R-channel

(1) Schmitt-trigger input with internal pulldown

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.3	6.5	V
Ground voltage differences	AGND, DGND	–0.1	0.1	V
Input voltage		–0.3	6.5	V
Input current (any pins except supplies)		–10	10	mA
Ambient temperature under bias		–40	105	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100–002(1)		±2000	V
		Charged device model (CDM), per AEC Q100–011	Corner pins (1, 8, 9, and 16)	±750	
			Other pins	±500	

(1) AEC Q100–002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS–001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Voltage range	4.5	5	5.5	VDC

7.4 Thermal Information

THERMAL METRIC(1)		PCM175x-Q1 DBQ (SSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			24		Bits
DATA FORMAT						
f_S	Sampling frequency		5		200	kHz
	System clock frequency(1)			128 f_S 192 f_S 256 f_S 384 f_S 512 f_S 768 f_S 1152 f_S		kHz
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	Input logic level, high		2			VDC
V_{IL}	Input logic level, low				0.8	VDC
I_{IH}	Input logic current, high (SCK, BCK, DATA, and LRCK pins)	$V_{IN} = V_{CC}$			10	µA
I_{IL}	Input logic current, low (SCK, BCK, DATA, and LRCK pins)	V_{IN} = 0 V			–10	µA
I_{IH}	Input logic current, high (TEST, DEMP, MUTE, and FMT pins)	$V_{IN} = V_{CC}$		65	100	µA
I_{IL}	Input logic current, low (TEST, DEMP, MUTE, and FMT pins)	V_{IN} = 0 V			–10	µA
V_{OH}	Output logic level, high (ZEROA pin)	I_{OH} = –1 mA	2.4			VDC
V_{OL}	Output logic level, low (ZEROA pin)	I_{OL} = 1 mA			0.4	VDC
DYNAMIC PERFORMANCE(2)(3)						
	THD+N at VOUT = 0 dB	f_S = 44.1 kHz		0.00%	0.01%	
		f_S = 96 kHz		0.00%		
		f_S = 192 kHz		0.00%		
	THD+N at VOUT = -60 dB	f_S = 44.1 kHz		0.65%		
		f_S = 96 kHz		0.80%		
		f_S = 192 kHz		0.95%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	100	106		dB
		A-weighted, f_S = 96 kHz		104		
		A-weighted, f_S = 192 kHz		102		
	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	100	106		dB
		A-weighted, f_S = 96 kHz		104		
		A-weighted, f_S = 192 kHz		102		
	Channel separation	f_S = 44.1 kHz	97	103		dB
		f_S = 96 kHz		101		
		f_S = 192 kHz		100		
	Level linearity error	VOUT = -90 dB		±0.5		dB

(1) System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S, 1152 f_S with auto detect.
(2) Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.
(3) Conditions in 192-kHz operation are system clock = 128 f_S and oversampling rate = 64 f_S of register 18.

Electrical Characteristics (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
	Gain error			±1	±6	% of FSR
	Gain mismatch, channel-to-channel			±1	±3	% of FSR
	Bipolar zero error	VOUT = 0.5 V_{CC} at BPZ		±30	±60	mV
ANALOG OUTPUT						
	Output voltage	Full scale (0 dB)	80% of V_{CC}			V_{PP}
	Center voltage		50% of V_{CC}			VDC
	Load impedance	AC-coupled load	5			kΩ
DIGITAL FILTER PERFORMANCE						
FILTER CHARACTERISTICS (SHARP ROLLOFF)						
	Pass band	±0.04 dB			0.454 f_S	
	Stop band		0.546 fs			
	Pass-band ripple				±0.04	dB
	Stop-band attenuation	Stop band = 0.546 f_S	–50			dB
ANALOG FILTER PERFORMANCE						
	Frequency response	At 20 kHz		–0.03		dB
		At 44 kHz		–0.20		
POWER SUPPLY REQUIREMENTS(3)						
V_{CC}	Voltage range		4.5	5	5.5	VDC
I_{CC}	Supply current	f_S = 44.1 kHz		16	21	mA
		f_S = 96 kHz		25		
		f_S = 192 kHz		30		
	Power dissipation	f_S = 44.1 kHz		80	105	mW
		f_S = 96 kHz		125		
		f_S = 192 kHz		150		
TEMPERATURE RANGE						
	Operation temperature		–40		105	°C
$R_{\theta JA}$	Thermal resistance	16-pin SSOP		115		°C/W

7.6 System Clock Input Timing

For more information, see the *System Clock Input* section.

			MIN	NOM	MAX	UNIT
$t_{(SCKH)}$	System clock pulse duration, high	See Figure 20.	7			ns
$t_{(SCKL)}$	System clock pulse duration, low		7			ns
$t_{(SCY)}$	System clock pulse cycle time			See (1)		ns

(1) 1/128 f_S, 1/256 f_S, 1/384 f_S, 1/512 f_S, 1/768 f_S, or 1/1152 f_S

7.7 Audio Interface Timing

For more information, see the *Audio Data Formats and Timing* section.

			MIN	MAX	UNIT
$t_{(BCY)}$	BCK pulse cycle time	See Figure 22.	1/(32 f_S) 1/(48 f_S) 1/(64 f_S) (1)		ns
$t_{(BCH)}$	BCK high–level time		35		ns
$t_{(BCL)}$	BCK low–level time		35		ns
$t_{(BL)}$	BCK rising edge to LRCK edge		10		ns
$t_{(LB)}$	LRCK falling edge to BCK rising edge		10		ns
$t_{(DS)}$	DATA setup time		10		ns
$t_{(DH)}$	DATA hold time		10		ns

(1) f_S is the sampling frequency (such as, 44.1 kHz, 48 kHz, 96 kHz, and so on).

7.8 Control Interface Timing Requirements

These timing parameters are critical for proper control port operation.

			MIN	NOM	MAX	UNIT
$t_{(MCY)}$	MC pulse cycle time	See Figure 1.	100			ns
$t_{(MCL)}$	MC low-level time		50			ns
$t_{(MCH)}$	MC high-level time		50			ns
$t_{(MCH)}$	ML high-level time		See (1)			ns
$t_{(MLS)}$	ML falling edge to MC rising edge		20			ns
$t_{(MLH)}$	ML hold time (2)		20			ns
$t_{(MDH)}$	MD hold time		15			ns
$t_{(MDS)}$	MD setup time		20			ns

(1) $\frac{3}{256 \times f_S}$ seconds (min); f_S: sampling rate.
(2) MC rising edge for LSB to ML rising edge.

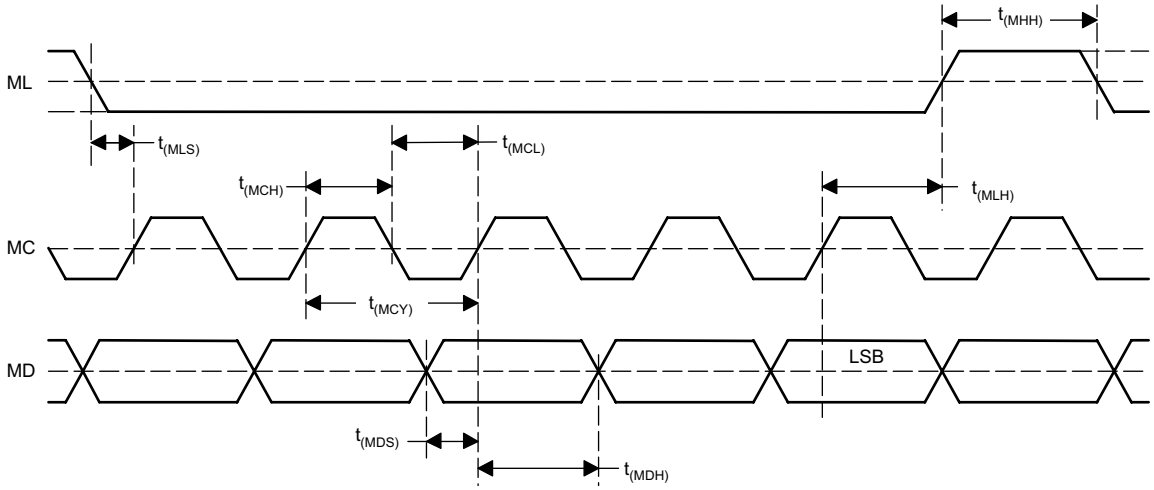
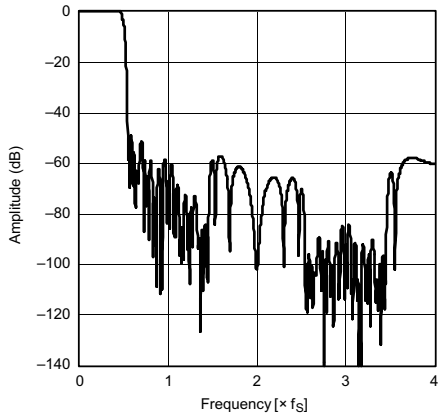


Figure 1. Control Interface Timing

7.9 Typical Characteristics

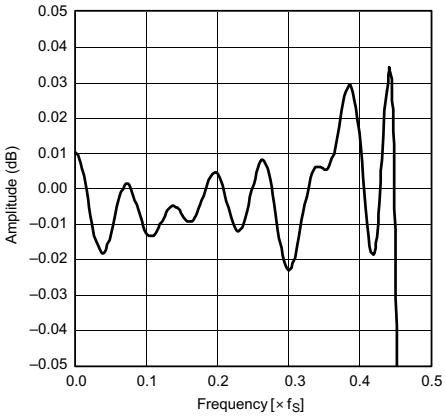
7.9.1 Digital Filter (De-Emphasis Off)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)



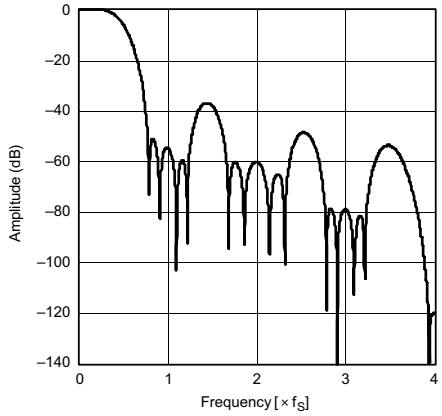
Frequency response Sharp rolloff

Figure 2. Amplitude vs Frequency



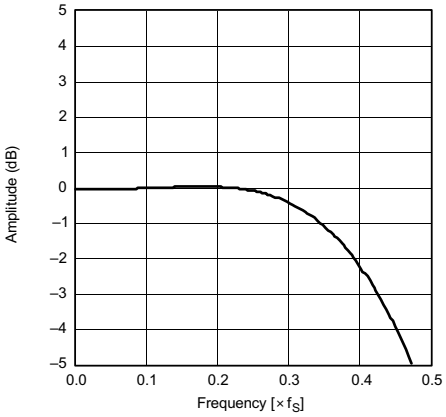
Pass-band ripple Sharp rolloff

Figure 3. Amplitude vs Frequency



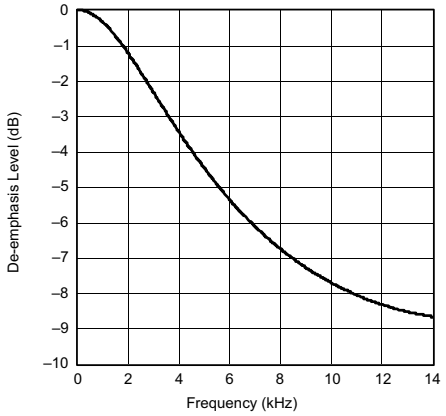
Frequency response Slow rolloff

Figure 4. Amplitude vs Frequency



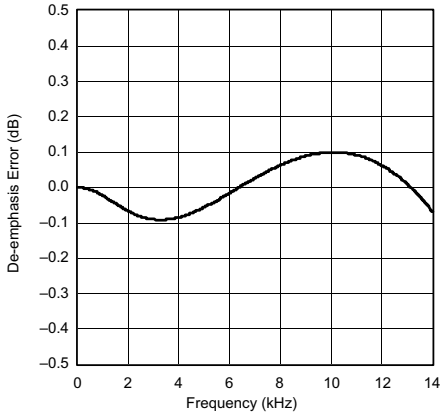
Transition characteristics Slow rolloff

Figure 5. Amplitude vs Frequency



f_S = 32 kHz

Figure 6. De-Emphasis Level vs Frequency

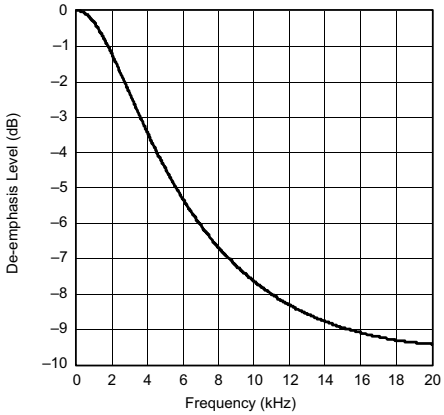


f_S = 32 kHz

Figure 7. De-Emphasis Error vs Frequency

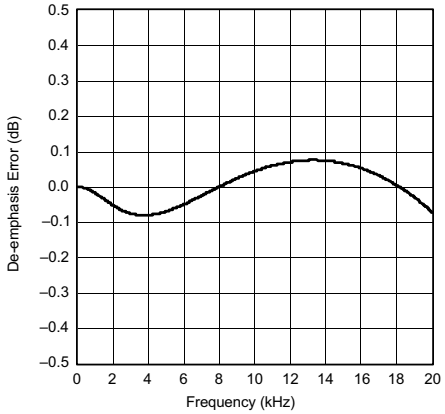
Digital Filter (De-Emphasis Off) (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)



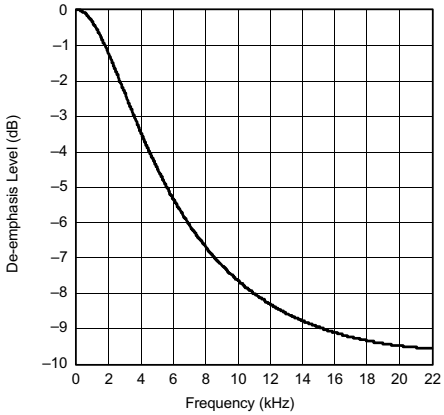
f_S = 44.1 kHz

Figure 8. De-Emphasis Level vs Frequency



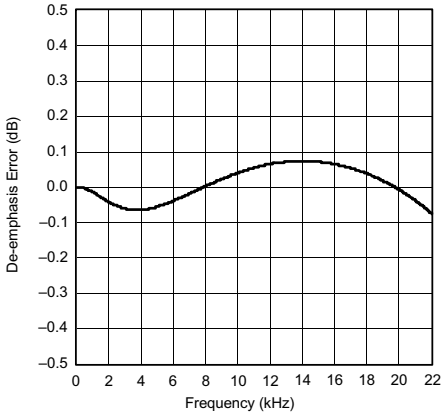
f_S = 44.1 kHz

Figure 9. De-Emphasis Error vs Frequency



f_S = 48 kHz

Figure 10. De-Emphasis Level vs Frequency



f_S = 48 kHz

Figure 11. De-Emphasis Error vs Frequency

7.9.2 Analog Dynamic Performance (Supply Voltage Characteristics)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

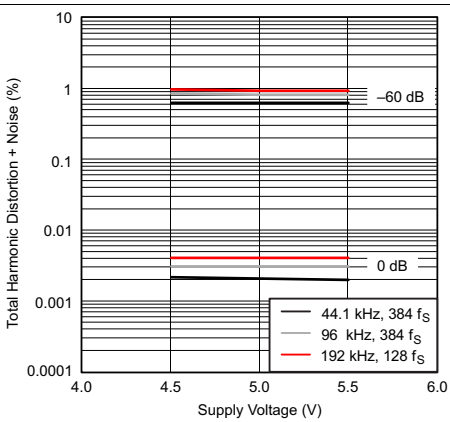


Figure 12. Total Harmonic Distortion + Noise vs Supply Voltage

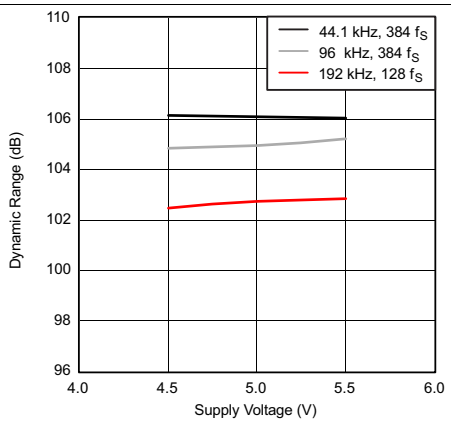


Figure 13. Dynamic Range vs Supply Voltage

Analog Dynamic Performance (Supply Voltage Characteristics) (continued)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

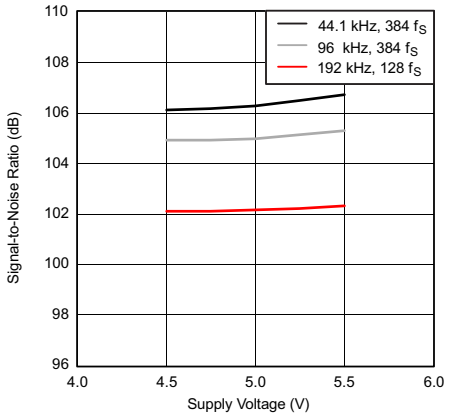


Figure 14. Signal-to-Noise Ratio vs Supply Voltage

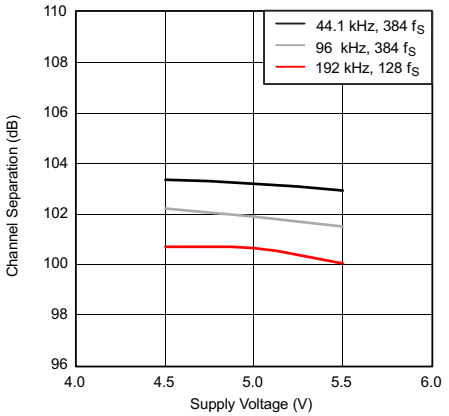


Figure 15. Channel Separation vs Supply Voltage

7.9.3 Analog Dynamic Performance (Temperature Characteristics)

All specifications at T_A = 25°C, V_{CC} = 5 V, f_S = 44.1 kHz, system clock = 384 f_S, and 24-bit data, (unless otherwise noted)

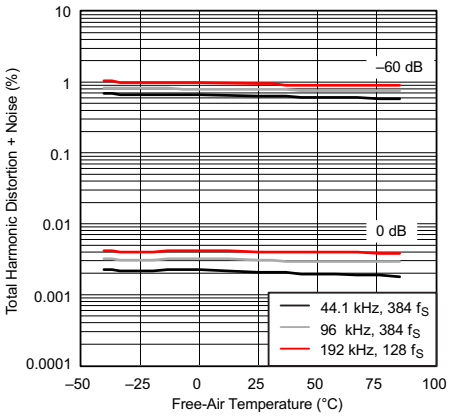


Figure 16. Total Harmonic Distortion + Noise vs Free-Air Temperature

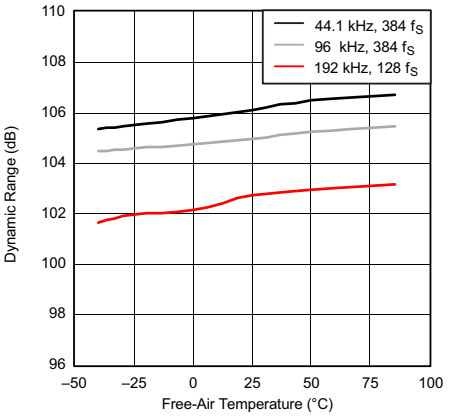


Figure 17. Dynamic Range vs Free-Air Temperature

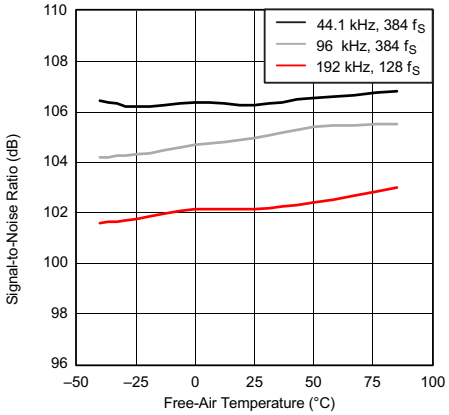


Figure 18. Signal-to-Noise Ratio vs Free-Air Temperature

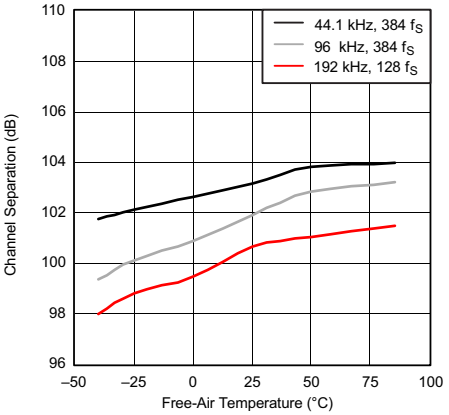


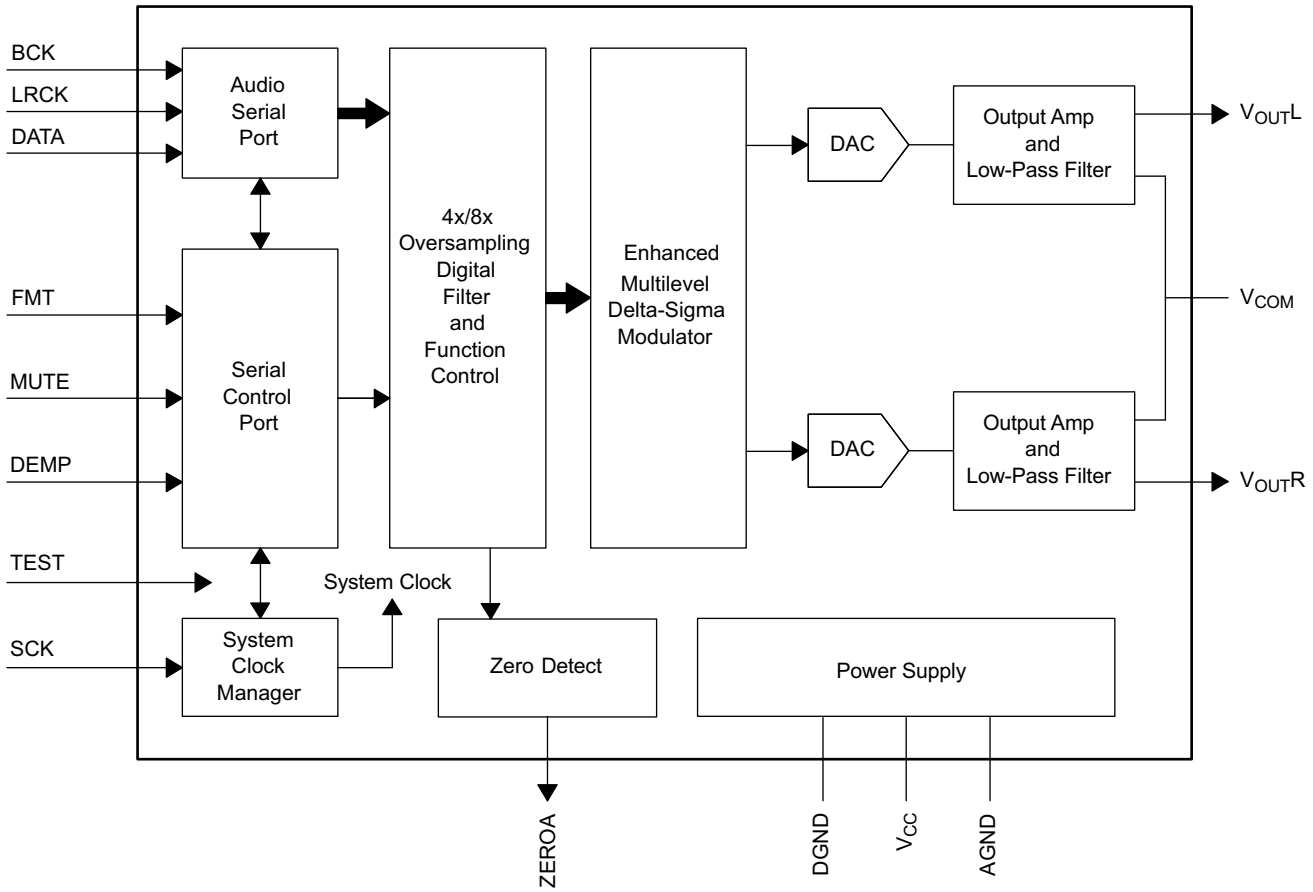
Figure 19. Channel Separation vs Free-Air Temperature

8 Detailed Description

8.1 Overview

The PCM175x-Q1 family of devices are stereo digital-to-analog converters (DACs) based on TI's enhanced delta-sigma architecture which employs 4th-order noise shaping and 8-level amplitude quantization to achieve excellent dynamic performance and improved clock jitter tolerance. The PCM175x-Q1 family of devices easily interface with an audio DSP and decoder chips because of the device supports industry-standard audio data formats with 16- and 24-bit data. The PCM1754-Q1 device also offers hardware control.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 System Clock and Reset Functions

8.3.1.1 System Clock Input

The PCM175x-Q1 family of devices requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCK input (pin 16). Table 1 lists examples of system clock frequencies for common audio sampling rates.

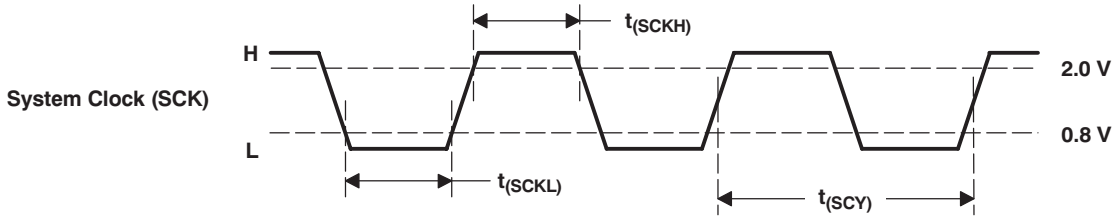
Figure 20 shows and the *System Clock Input Timing* table lists the timing requirements for the system clock input. For optimal performance, use a clock source with low phase-jitter and noise. TI's PLL170x family of multiclock generators is an excellent choice for providing the PCM175x-Q1 system clock.

Feature Description (continued)

Table 1. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)						
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1152 f_S
8 kHz	1.024	1.536	2.048	3.072	4.096	6.144	9.216
16 kHz	2.048	3.072	4.096	6.144	8.192	12.288	18.432
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576	36.864
44.1 kHz	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688	See (1)
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864	See (1)
88.2 kHz	11.2896	16.9344	22.5792	33.8688	45.1584	See (1)	See (1)
96 kHz	12.288	18.432	24.576	36.864	49.152	See (1)	See (1)
192 kHz	24.576	36.864	See (1)	See (1)	See (1)	See (1)	See (1)

(1) This system clock rate is not supported for the given sampling frequency.



For timing specifications, see the *System Clock Input Timing* table.

Figure 20. System Clock Input Timing

8.3.1.2 Power-On Reset Functions

The PCM175x-Q1 family of devices includes a power-on reset function. Figure 21 shows the operation of this function. With the system clock active and V_{CC} > 3 V (typical, 2.2 V to 3.7 V), the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{CC} > 3 V (typical, 2.2 V to 3.7 V).

During the reset period (1024 system clocks), the analog output is forced to the bipolar zero level, or V_{CC} / 2. After the reset period, an internal register is initialized in the next 1 / f_S period and if SCK, BCK, and LRCK are provided continuously, the PCM175x-Q1 family of devices provides proper analog output with unit group delay against the input data.

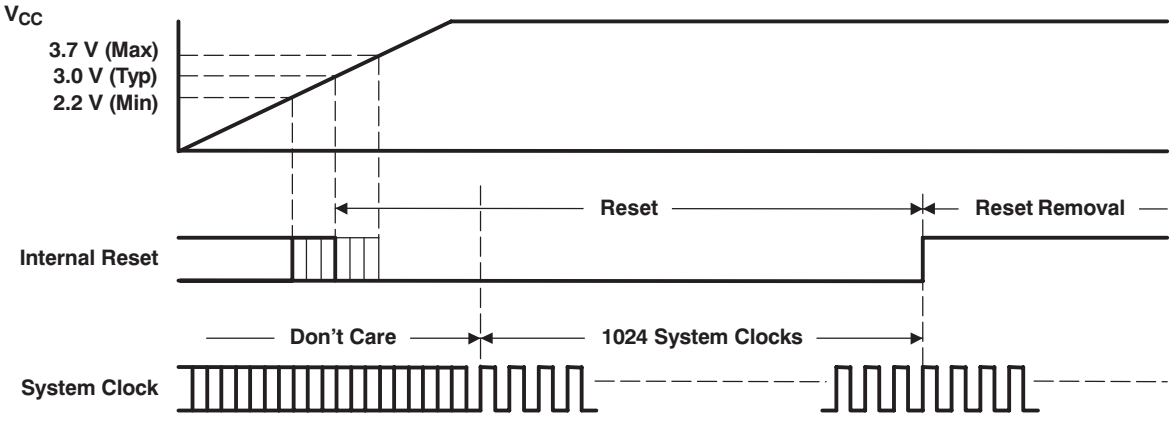


Figure 21. Power-On Reset Timing

8.3.2 Audio Serial Interface

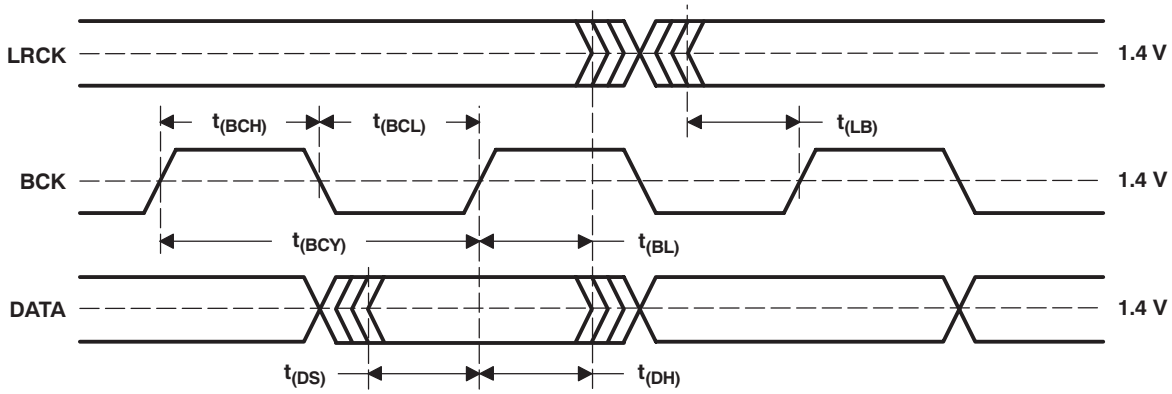
The audio serial interface for the PCM175x-Q1 family of devices consists of a 3-wire synchronous serial port. The interface includes LRCK (pin 3), BCK (pin 1), and DATA (pin 2). The BCK pin is the serial audio bit clock, and is used to clock the serial data present on the DATA pin into the serial shift register of the audio interface. Serial data is clocked into the PCM175x-Q1 family of devices on the rising edge of BCK. The LRCK pin is the serial audio left and right word clock. This pin is used to latch serial data into the internal registers of the serial audio interface.

Both the LRCK and BCK pins should be synchronous to the system clock. Ideally, TI recommends that the LRCK and BCK pins be derived from the system clock input, SCK. The LRCK pin is operated at the sampling frequency, f_S. The BCK pin can operate at 32, 48, or 64 times the sampling frequency for standard (right-justified) format, and 32 times the sampling frequency of the BCK pin is limited to 16-bit right-justified format only. The BCK pin can operate at 48 or 64 times the sampling frequency for the I^2S and left-justified formats, and 48 times the sampling frequency of the BCK pin is limited to 192, 384, and 768 f_S SCKI.

Internal operation of the PCM175x-Q1 family of devices is synchronized with the LRCK pin. Accordingly, internal operation is held when the sampling rate clock of the LRCK pin changes or when the SCK pin, BCK pin, or both pins are interrupted for a 3-bit clock cycle or longer. If the SCK, BCK, and LRCK pins are provided continuously after this held condition, the internal operation is re-synchronized automatically in a period of less than 3 / f_S. External resetting is not required.

8.3.2.1 Audio Data Formats and Timing

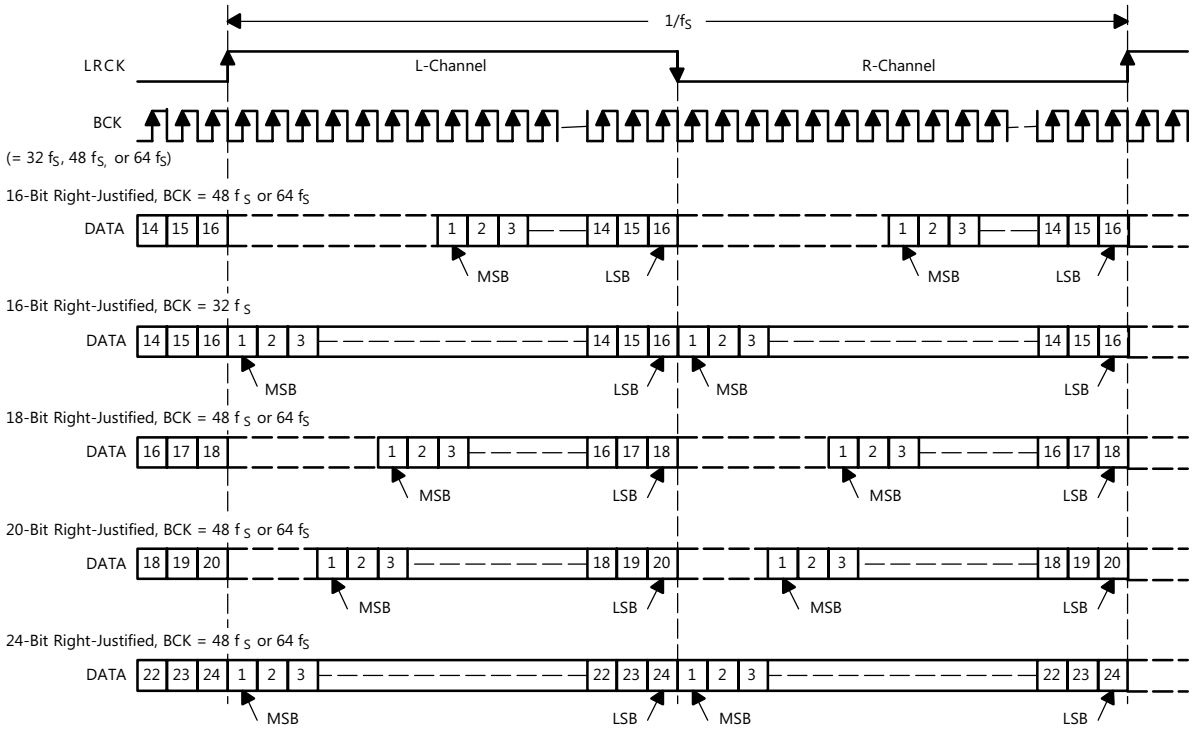
The PCM1753-Q1 device supports industry-standard audio data formats, including right-justified, I^2S, and left-justified. The PCM1754-Q1 device supports I^2S and 16-bit-word right-justified audio data formats. Figure 23 shows the data formats. Data formats are selected using the format bits, FMT[2:0], located in control register 20 of the PCM1753-Q1 device, and are selected using the FMT pin on the PCM1754-Q1 device. The default data format is 24-bit left-justified. All formats require binary 2s-complement MSB-first audio data. Figure 22 shows a detailed timing diagram for the serial audio interface. The *Audio Interface Timing* table lists the audio interface timing requirements.



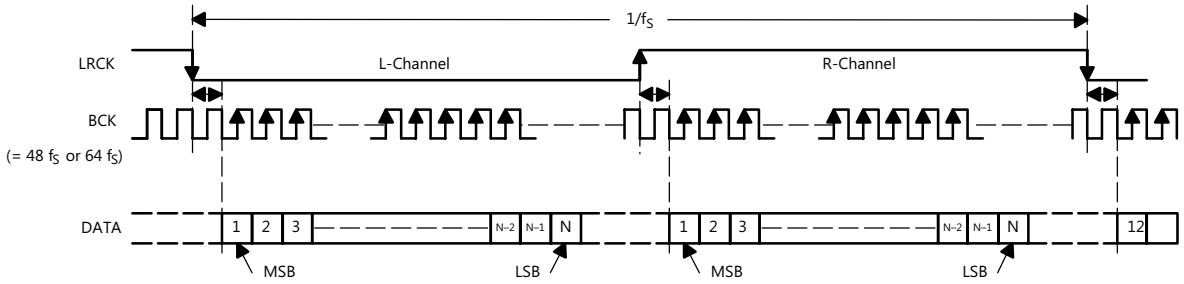
For timing specifications, see the *Audio Interface Timing* table.

Figure 22. Audio Interface Timing

(1) Standard Data Format; L-Channel = HIGH, R-Channel = LOW



(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW

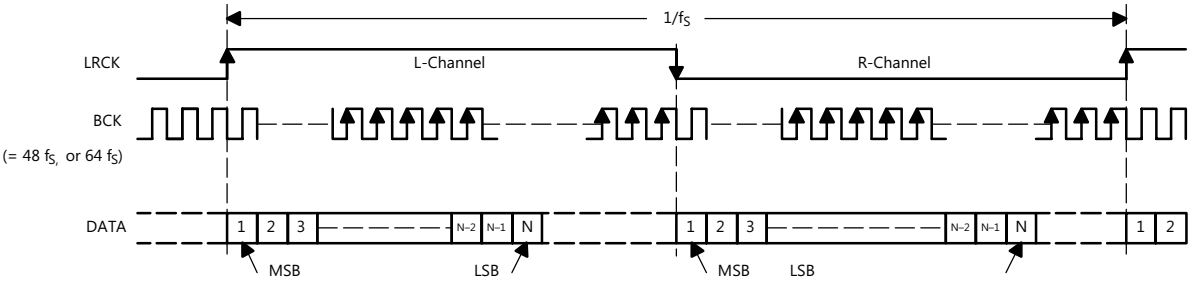


Figure 23. Audio Data Input Formats

8.3.3 Zero Flag (PCM1754-Q1)

The PCM1754-Q1 device has a ZERO flag pin, ZEROA (pin 11). The ZEROA pin is the L-channel and R-channel common zero flag pin. If the data for L-channel and R-channel remains at a 0 level for 1024 sampling periods (or LRCK clock periods), the ZEROA pin is set to a logic 1 state.

8.3.4 Zero Flag (PCM1753-Q1)

Zero-Detect Condition

Zero detection for either output channel is independent from the other channel. If the data for a given channel remains at a 0 level for 1024 sample periods (or LRCK clock periods), a zero-detect condition exists for that channel.

8.3.5 Zero Flag Outputs

If a zero-detect condition exists for one or more channels, the zero flag pins for those channels are set to a logic 1 state. Each channel has zero flag pins, ZEROL (pin 12) and ZEROR (pin 11). These pins can operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally controlled function. The active polarity of the zero flag outputs can be inverted by setting the ZREV bit of control register 22 to 1. The reset default is active-high output, or ZREV set to 0. The L-channel and R-channel common zero flag can be selected by setting the AZRO bit of control register 22 to 1. The reset default is independent zero flags for L-channel and R-channel, or AZRO set to 0.

8.3.6 Analog Outputs

The PCM1753-Q1 device includes two independent output channels, $V_{OUT}L$ and $V_{OUT}R$. These are unbalanced outputs, each capable of driving 4 V_{PP} typical into a 5-kΩ ac-coupled load. The internal output amplifiers for $V_{OUT}L$ and $V_{OUT}R$ are biased to the dc common-mode (or bipolar zero) voltage, equal to 0.5 V_{CC}.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise shaping characteristics of the PCM1754-Q1 delta-sigma DAC. The frequency response of this filter is shown in Figure 24. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for many applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the Applications Information section of this data sheet.

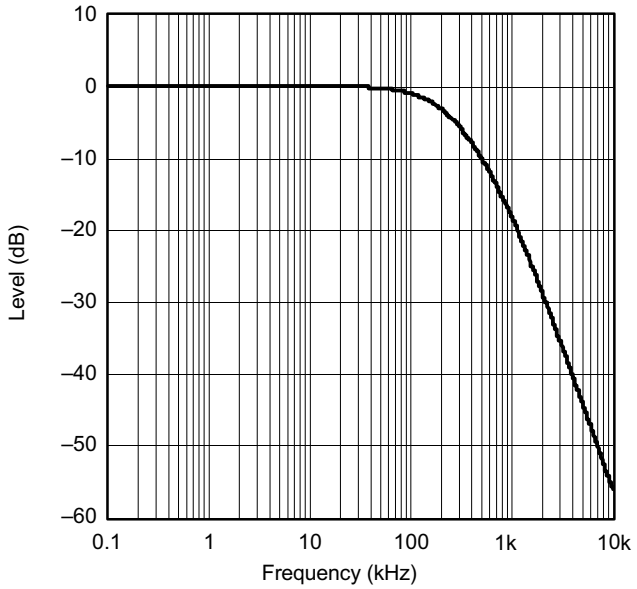
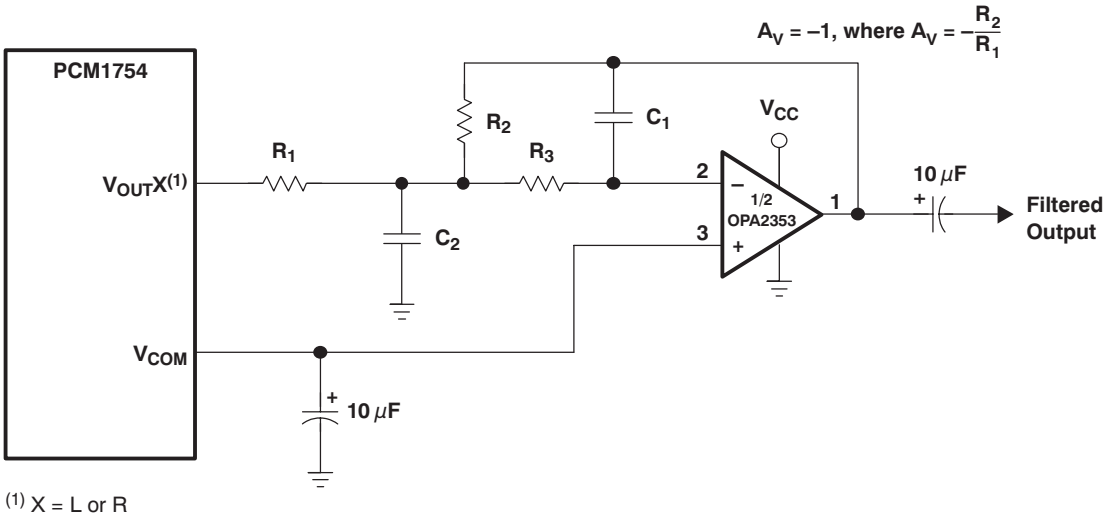


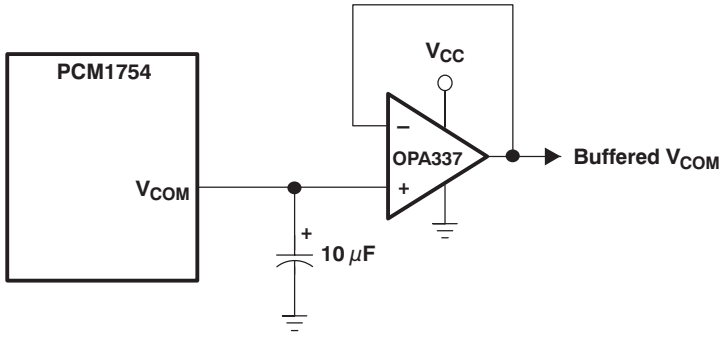
Figure 24. Level vs Frequency
Output Filter Frequency Response

8.3.6.1 V_{COM} Output

One unbuffered common-mode voltage output pin, V_{COM} (pin 10) is brought out for decoupling purposes. This pin is nominally biased to a DC-voltage level that is equal to 0.5 V_{CC}. This pin can be used to bias external circuits. Figure 25 shows an example of using the V_{COM} pin for external biasing applications.



(a) Using V_{COM} to Bias a Single-Supply Filter Stage



(b) Using a Voltage Follower to Buffer V_{COM} When Biasing Multiple Nodes

Figure 25. Biasing External Circuits Using the V_{COM} Pin

8.4 Device Functional Modes

8.4.1 Hardware Control (PCM1754-Q1)

The digital functions of the PCM1754-Q1 device are capable of hardware control. Table 2 lists selectable formats, Table 3 lists de-emphasis control, and Table 4 lists mute control.

Table 2. Data Format Select

FMT (PIN 15)	DATA FORMAT
LOW	16– to 24–bit, I^2S format
HIGH	16–bit right–justified

Table 3. De-Emphasis Control

DEMP (PIN 13)	DE–EMPHASIS FUNCTION
LOW	44.1 kHz de–emphasis OFF
HIGH	44.1 kHz de–emphasis ON

Table 4. Mute Control

MUTE (PIN 14)	MUTE
LOW	Mute OFF
HIGH	Mute ON

8.4.2 Oversampling Rate Control (PCM1754-Q1)

The PCM1754-Q1 device automatically controls the oversampling rate of the delta-sigma DACs with the system clock rate. The oversampling rate is set to 64× oversampling with every system clock and sampling frequency.

8.5 Programming

8.5.1 Software Control (PCM1753-Q1)

The PCM1753-Q1 device has many programmable functions which can be controlled in the software control mode. The functions are controlled by programming the internal registers using ML, MC, and MD.

The serial control interface is a 3-wire serial port, which operates asynchronously to the audio serial interface. The serial control interface is used to program the on-chip mode registers. The control interface includes the MD (pin 13), MC (pin 14), and ML (pin 15) pins. The MD pin is the serial data input, used to program the mode registers. The MC pin is the serial bit clock, used to shift data into the control port. The ML pin is the control port latch clock.

8.5.1.1 Register Write Operation

All write operations for the serial control port use 16-bit data words. Figure 26 shows the control data word format. The most significant bit must be a 0. There are seven bits, labeled IDX[6:0], that set the register index (or address) for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 27 shows the functional timing diagram for writing to the serial control port. ML is held at a logic 1 state until a register needs to be written. To begin the register write cycle, ML is set to logic 0. Sixteen clocks are then provided on the MC pin, corresponding to the 16 bits of the control data word on MD. After the sixteenth clock cycle has completed, ML is set to logic 1 to latch the data into the indexed mode control register.

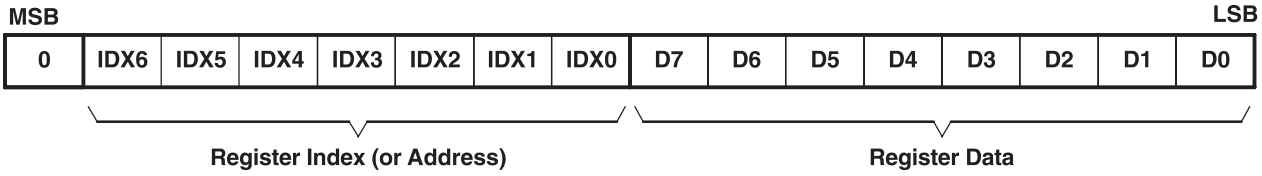


Figure 26. Control Data Word Format for MD

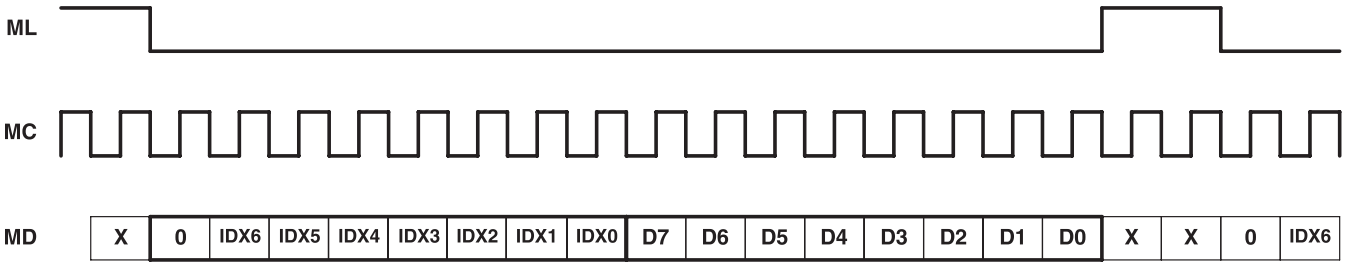


Figure 27. Register Write Operation

8.6 Register Maps

8.6.1 Mode Control Registers (PCM1753-Q1)

8.6.1.1 User-Programmable Mode Controls

The PCM1753-Q1 device includes a number of user programmable functions, which are accessed through control registers. The registers are programmed using the serial control interface, which was previously discussed in this data sheet. Table 5 lists the available mode control functions, along with the corresponding reset default conditions and associated register index.

Table 5. User-Programmable Mode Controls

FUNCTION	RESET DEFAULT	REGISTER	BIT(s)
Digital attenuation control, 0 dB to –63 dB in 0.5-dB steps	0 dB, no attenuation	16 and 17	AT1[7:0], AT2[7:0]
Soft mute control	Mute disabled	18	MUT[2:0]
Oversampling rate control (64 f_S or 128 f_S)	64 f_S oversampling	18	OVER
Soft reset control	Reset disabled	18	SRST
DAC operation control	DAC1 and DAC2 enabled	19	DAC[2:1]
De-emphasis function control	De-emphasis disabled	19	DM12
De-emphasis sample rate selection	44.1 kHz	19	DMF[1:0]
Audio data format control	24-bit left-justified	20	FMT[2:0]
Digital filter rolloff control	Sharp rolloff	20	FLT
Zero flag function select	L-, R-channel independent	22	AZRO
Output phase select	Normal phase	22	DREV
Zero flag polarity select	High	22	ZREV

The mode control register map is shown in Table 6. Each register includes an index (or address) indicated by the IDX[6:0] bits.

Table 6. Mode Control Register Map(1)

IDX (B8–B14)	REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
10h	Register 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
11h	Register 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
12h	Register 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1
13h	Register 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1
14h	Register 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0
16h	Register 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	AZRO	ZREV	DREV

(1) RSV: Reserved for test operation. It should be set to 0 for regular operation.

8.6.1.2 Register Definitions

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20

8.6.1.2.1 ATx[7:0]: Digital Attenuation Level Setting

With x = 1 or 2, corresponding to the DAC output $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 1111 1111b

Each DAC channel ($V_{OUT}L$ and $V_{OUT}R$) includes a digital attenuation function. The attenuation level can be set from 0 dB to –63 dB in 0.5-dB steps. Changes in attenuator levels are made by incrementing or decrementing one step (0.5 dB) for every 8/fS time internal until the programmed attenuator setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute).

The attenuation data for each channel can be set individually. The attenuation level is set using Equation 1.

$$\text{Attenuation level (dB)} = 0.5 \times (\text{ATx}[7:0]_{DEC} - 255) \quad (1)$$

where

- $\text{ATx}[7:0]_{DEC}$ = 0 through 255.

For ATx[7:0]DEC = 0 through 128, attenuation is set to infinite attenuation.

The table in Figure 28 shows the attenuation levels for various settings.

ATx[7:0]	DECIMAL VALUE	ATTENUATION LEVEL SETTING
1111 1111b	255	0 dB, No Attenuation. (default)
1111 1110b	254	–0.5 dB
1111 1101b	253	–1.0 dB
⋮	⋮	⋮
1000 0011b	131	–62.0 dB
1000 0010b	130	–62.5 dB
1000 0001b	129	–63.0 dB
1000 0000b	128	Mute
⋮	⋮	⋮
$0000\ 0000_B$	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	OVER	RSV	RSV	RSV	RSV	MUT2	MUT1

Figure 28. Attenuation Level Settings

8.6.1.2.2 MUTx: Soft Mute Control

With x = 1 or 2, corresponding to the DAC outputs $V_{OUT}L$ (x = 1) and $V_{OUT}R$ (x = 2).

Default value: 0

MUTx = 0	Mute disabled (default)
MUTx = 1	Mute enabled

The mute bits, MUT1 and MUT2, are used to enable or disable the soft mute function for the corresponding DAC outputs, VOUTL and VOUTR. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to infinite attenuation, one attenuator step (0.5 dB) for every 8 / f_S seconds. This provides pop-free muting of the DAC output.

By setting MUTx = 0, the attenuator is increased one step for every 8/f_S seconds to the previously programmed attenuation level.

8.6.1.2.3 OVER: Oversampling Rate Control

Default value: 0

System clock rate = 256 f_S, 384 f_S, 512 f_S, 768 f_S, or 1152 f_S:

OVER = 0	64· oversampling (default)
OVER = 1	128· oversampling

System clock rate = 128 f_S or 192 f_S:

OVER = 0	32· oversampling (default)
OVER = 1	64· oversampling

The OVER bit is used to control the oversampling rate of the delta-sigma DAC. The OVER = 1 setting is recommended when the sampling rate is 192 kHz (system clock rate is 128 f_S or 192 f_S).

8.6.1.2.4 SRST: Reset

Default value: 0

SRST = 0	Reset disabled (default)
SRST = 1	Reset enabled

The SRST bit is used to enable or disable the soft reset function. The operation is the same as power-on reset. All registers are initialized.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	DMF1	DMF0	DM12	RSV	RSV	DAC2	DAC1

8.6.1.2.5 DACx: DAC Operation Control

With x = 1 or 2, corresponding to the DAC output V_{OUT}L (x = 1) or V_{OUT}R (x = 2).

Default value: 0

DACx = 0	DAC operation enabled (default)
DACx = 1	DAC operation disabled

The DAC operation controls are used to enable and disable the DAC outputs, V_{OUT}L and V_{OUT}R. When DACx = 0, the corresponding output generates the audio waveform dictated by the data present on the DATA pin. When DACx = 1, the corresponding output is set to the bipolar zero level, or 0.5 V_{CC}.

8.6.1.2.6 DM12: Digital De-Emphasis Function Control

Default value: 0

DM12 = 0	De-emphasis disabled (default)
DM12 = 1	De-emphasis enabled

The DM12 bit is used to enable or disable the digital de-emphasis function. See the plots shown in the *Typical Characteristics* section of this data sheet.

8.6.1.2.7 DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function

Default value: 00

The DMF[1:0] bits are used to select the sampling frequency used for the digital de-emphasis function when it is enabled.

DMF[1:0]	De-Emphasis Sample Rate Selection
00	44.1 kHz (default)
01	48 kHz
10	32 kHz
11	Reserved

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 20	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	RSV	FMT2	FMT1	FMT0

8.6.1.2.8 FMT[2:0]: Audio Interface Data Format

Default value: 101

The FMT[2:0] bits are used to select the data format for the serial audio interface. The table in Figure 29 shows the available format options.

FMT[2:0]	Audio Data Format Selection
000	24-bit standard format, right-justified data
001	20-bit standard format, right-justified data
010	18-bit standard format, right-justified data
011	16-bit standard format, right-justified data
100	16- to 24-bit I^2S format
101	16- to 24-bit left-justified format (default)
110	Reserved
111	Reserved

Figure 29. Audio Data Format Options

8.6.1.2.9 FLT: Digital Filter Rolloff Control

Default value: 0

FLT = 0	Sharp rolloff (default)
FLT = 1	Slow rolloff

The FLT bit allows the user to select the digital filter rolloff that is best suited to the application. Two filter rolloff selections are available, sharp and slow. The filter responses for these selections are shown in the *Typical Characteristics* section of this data sheet.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 22	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	AZRO	ZREV	DREV

8.6.1.2.10 DREV: Output Phase Select

Default value: 0

DREV = 0	Normal output (default)
DREV = 1	Inverted output

The DREV bit is the output analog signal phase control.

8.6.1.2.11 ZREV: Zero Flag Polarity Select

Default value: 01h

ZREV = 0	High on zero flag pins indicates a zero detect (default)
ZREV = 1	Low on zero flag pins indicates a zero detect

The ZREV bit allows the user to select the polarity of zero flag pins.

8.6.1.2.12 AZRO: Zero Flag Function Select

Default value: 0

AZRO = 0	L-/R-channel independent zero flags (default)
AZRO = 1	L-/R-channel common zero flag

The AZRO bit allows the user to select the function of zero flag pins.

AZRO = 0:	Pin 11: ZEROR, zero flag output for R-channel
	Pin 12: ZEROL, zero flag output for L-channel
AZRO = 1:	Pin 11: ZEROA, zero flag output for L-/R-channels
	Pin 12: NA, not assigned

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The delta-sigma section of the PCM175x-Q1 family of devices is based on an 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format. Figure 32 shows a block diagram of the 8-level delta-sigma modulator. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the interpolation filter is 64 f_S.

Figure 35 and Figure 36 show the theoretical quantization noise performance of the 8-level delta-sigma modulator. The enhanced multilevel delta-sigma architecture also has advantages for input clock jitter sensitivity because of the multilevel quantizer, with the simulated jitter sensitivity shown in Figure 37.

9.2 Typical Application

Figure 30 shows a basic connection diagram with the necessary power supply bypassing and decoupling components. TI recommends using the component values shown in Figure 30 for all designs.

The use of series resistors (22 Ω to 100 Ω) is recommended for the SCK, LRCK, BCK, and DATA inputs. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter, which reduces high-frequency noise emissions and helps to dampen glitches and ringing present on clock and data lines.

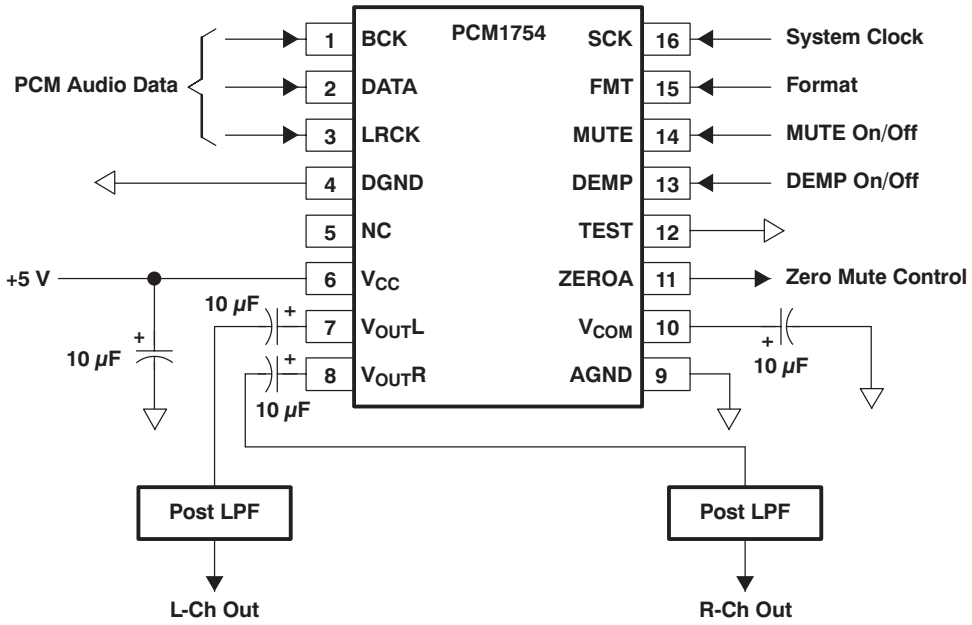


Figure 30. Basic Connection Diagram

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Power Supplies and Grounding

The PCM1754-Q1 device requires 5 V for V_{CC}.

Proper power supply bypassing is shown in Figure 30. The 10-µF capacitors should be tantalum or aluminum electrolytic.

9.2.1.2 DAC Output Filter Circuits

Delta-sigma DAC use noise-shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or f_S / 2. The out-of-band noise must be low-pass filtered in order to provide the optimal converter performance which is accomplished by a combination of on-chip and external low-pass filtering.

Figure 25(a) and Figure 31 show the recommended external low-pass active filter circuits for single- and dual-supply applications. These circuits are second-order Butterworth filters using the multiple feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, see the Burr-Brown application bulletin, *Dynamic Performance Testing of Digital audio D/A Converters* (SBAA055).

Because the overall system performance is defined by the quality of the DAC and the associated analog output circuitry, high-quality audio operational amplifiers are recommended for the active filters. TI's OPA2353 and OPA2134 dual operational amplifiers are shown in Figure 25(a) and Figure 31, and are recommended for use with the PCM1754-Q1 device.

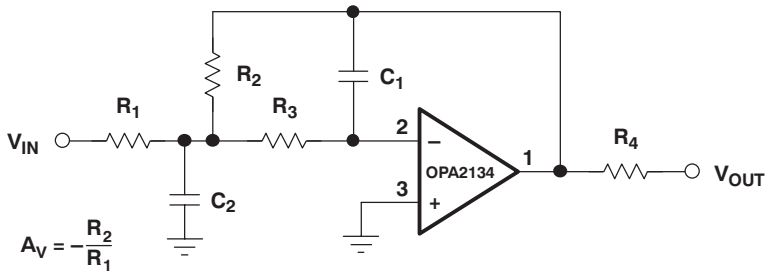


Figure 31. Dual-Supply Filter Circuit

9.2.2 Detailed Design Procedure

This section provides information on how to measure key dynamic performance parameters for the PCM175x-Q1 family of devices. In all cases, an Audio Precision System Two Cascade audio measurement system or equivalent is used to perform the testing.

9.2.2.1 Total Harmonic Distortion + Noise

Total harmonic distortion + noise (THD+N) is a significant figure of merit for audio DAC because it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The average value of the distortion and noise is referred to as THD+N.

For the PCM175x-Q1 family of devices, THD+N is measured with a full-scale, 1-kHz digital sine wave as the test stimulus at the input of the DAC (see Figure 33). The digital generator is set to 24-bit audio word length and a sampling frequency of 44.1 kHz or 96 kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted through a coaxial cable to the digital audio receiver on the DEM-DAI1753 demonstration board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band limited using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

Typical Application (continued)

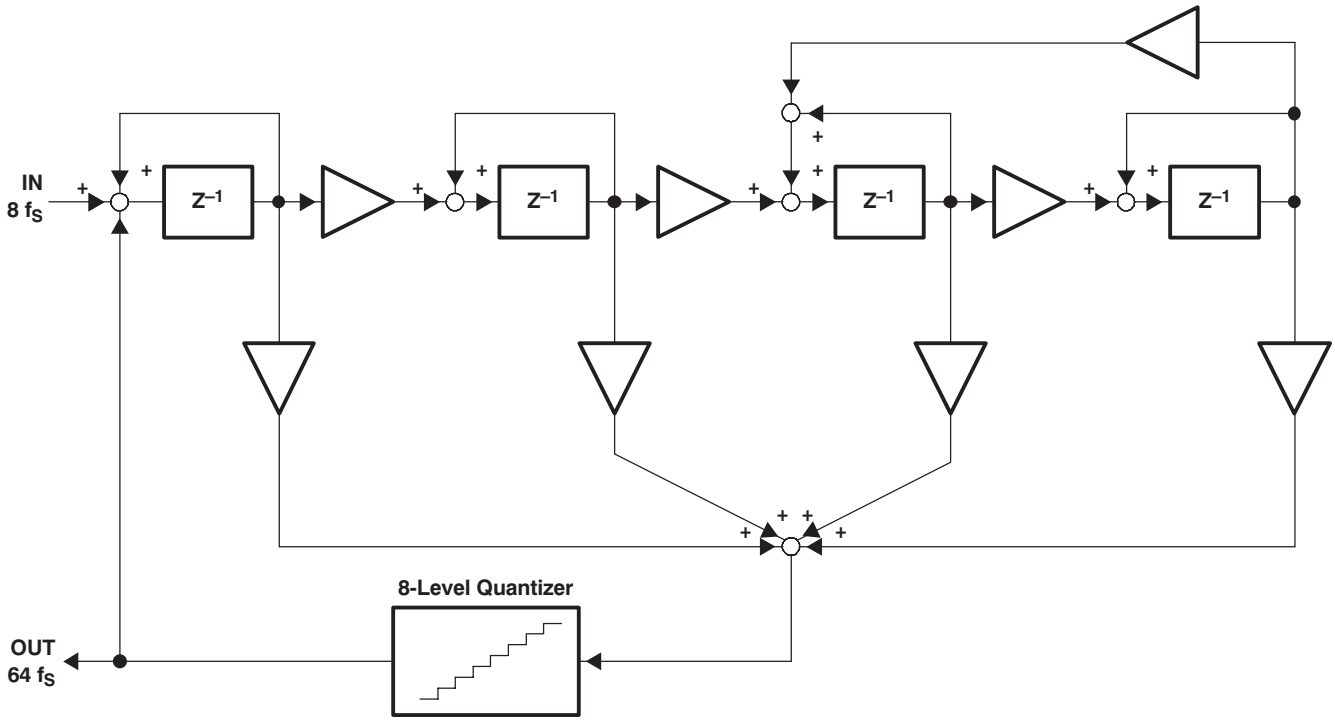


Figure 32. Eight-Level Delta-Sigma Modulator

9.2.2.2 Dynamic Range

Dynamic range is specified as A-weighted THD+N measured with a –60-dB full-scale, 1-kHz digital sine wave stimulus at the input of the DAC. This measurement is designed to give a good indicator of how the DAC performs given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 34, and is similar to the THD+N test setup discussed previously. The differences include the band limit filter selection, the additional A-weighting filter, and the –60-dB full-scale input level.

Typical Application (continued)

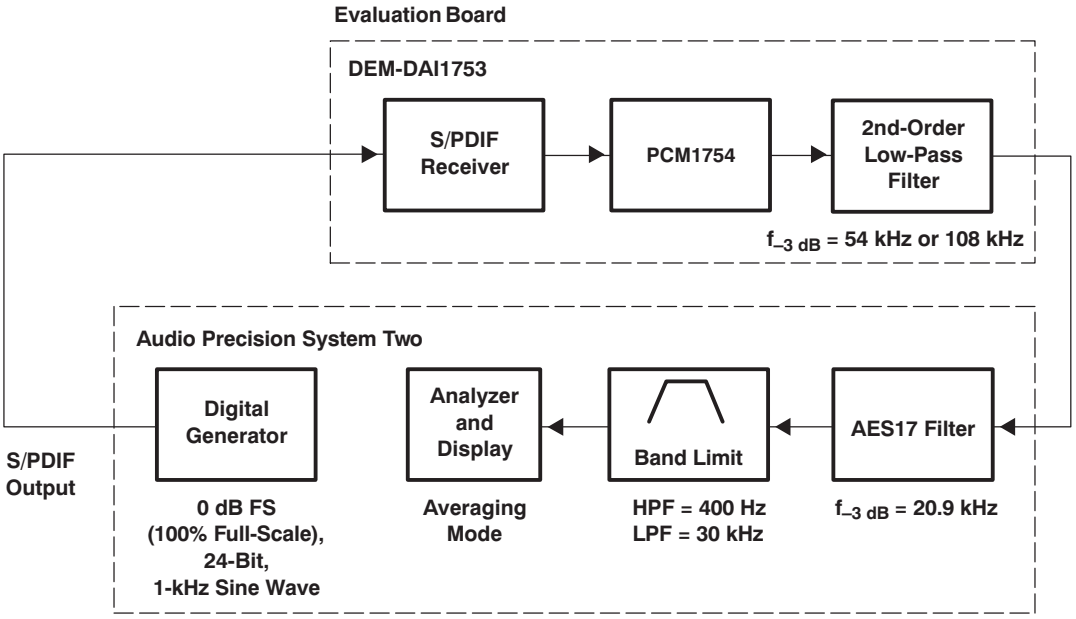


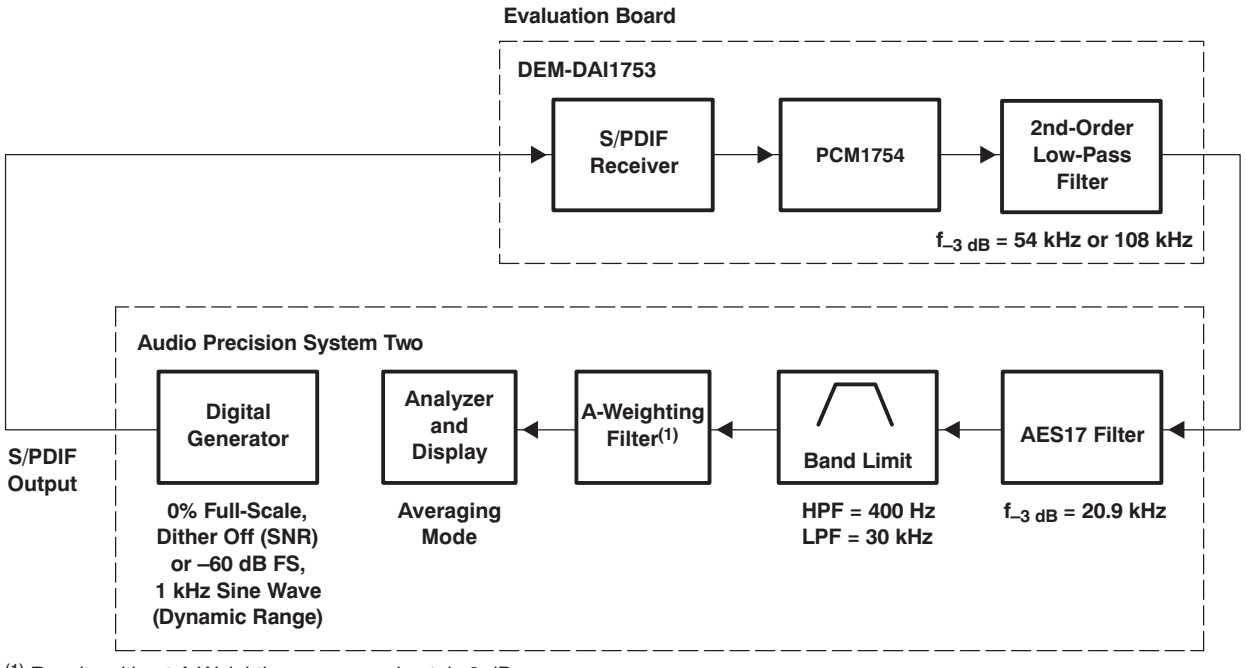
Figure 33. Test Setup for THD+N Measurement

9.2.2.3 Idle Channel Signal-to-Noise Ratio (SNR)

The SNR test provides a measure of the noise floor of the DAC. The input to the DAC is all–0s data, and the dither function of the digital generator must be disabled to ensure an all–0s data stream at the input of the DAC.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level.

See the note provided in Figure 34.



(1) Results without A-Weighting are approximately 3 dB worse.

Figure 34. Test Setup for Dynamic Range and SNR Measurement

Typical Application (continued)

9.2.3 Application Curves

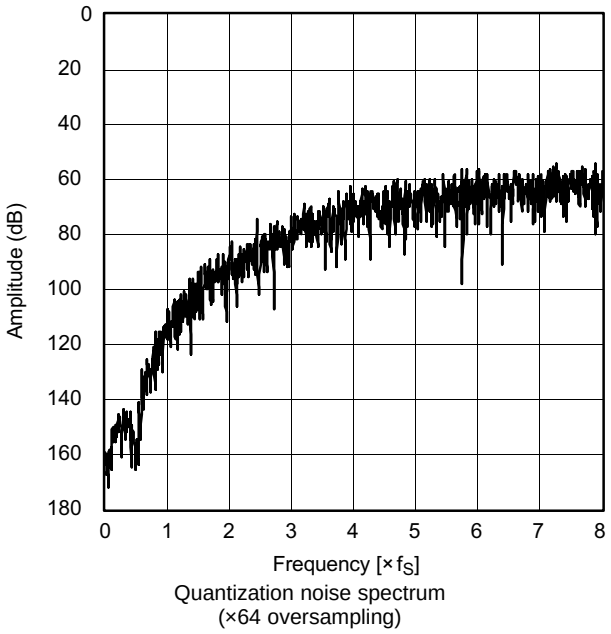


Figure 35. Amplitude vs Frequency

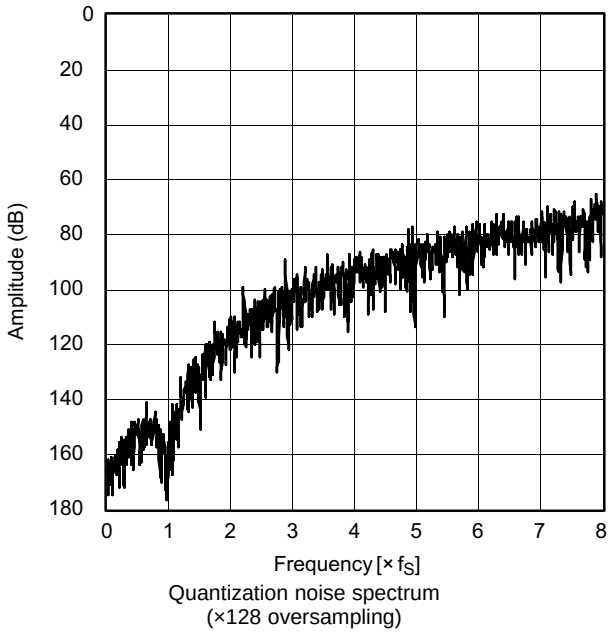


Figure 36. Amplitude vs Frequency

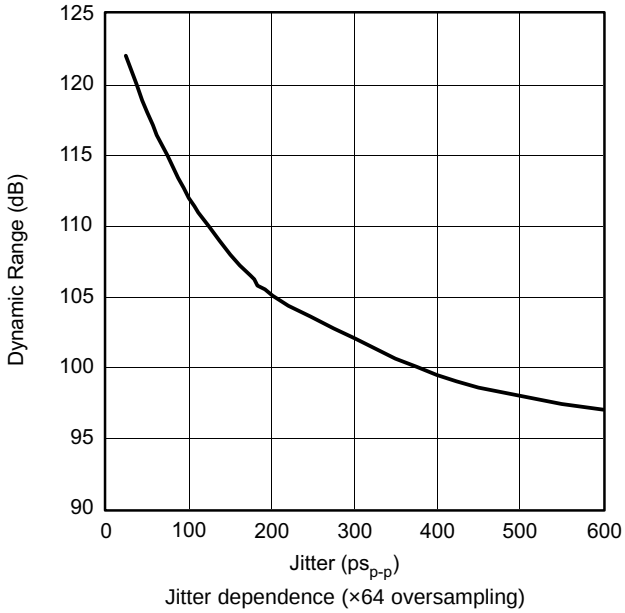


Figure 37. Dynamic Range vs Jitter

10 Power Supply Recommendations

The PCM175x-Q1 family of devices is designed to operate from a power supply from 4.5 V to 5.5 V. Ensure that the power supply is clean and use high-quality decoupling capacitors to reduce noise. The bulk capacitances can be from either tantalum or aluminum capacitors.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM175x-Q1 family of devices. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 39 shows the recommended approach for single-supply applications.

11 Layout

11.1 Layout Guidelines

Figure 38 shows a typical PCB floor plan for the PCM175x-Q1 family of devices. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM175x-Q1 family of devices should be oriented with the digital I/O pins facing the ground plane split or cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

11.2 Layout Example

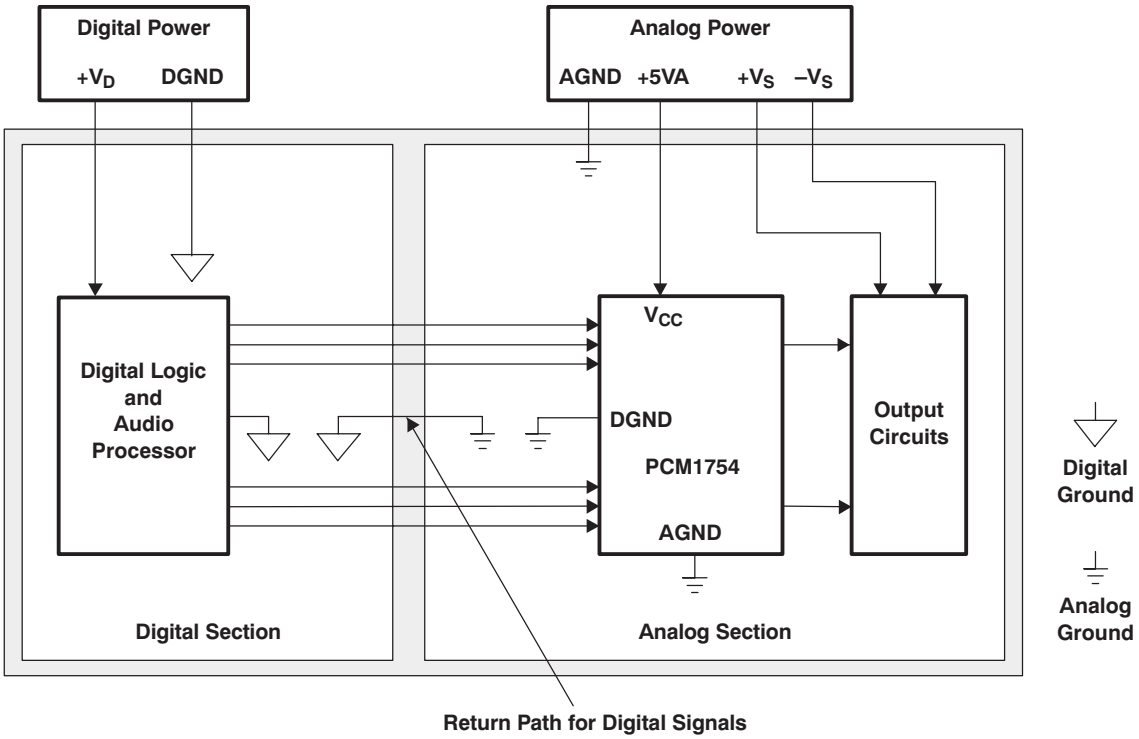


Figure 38. Recommended PCB Layout

Layout Example (continued)

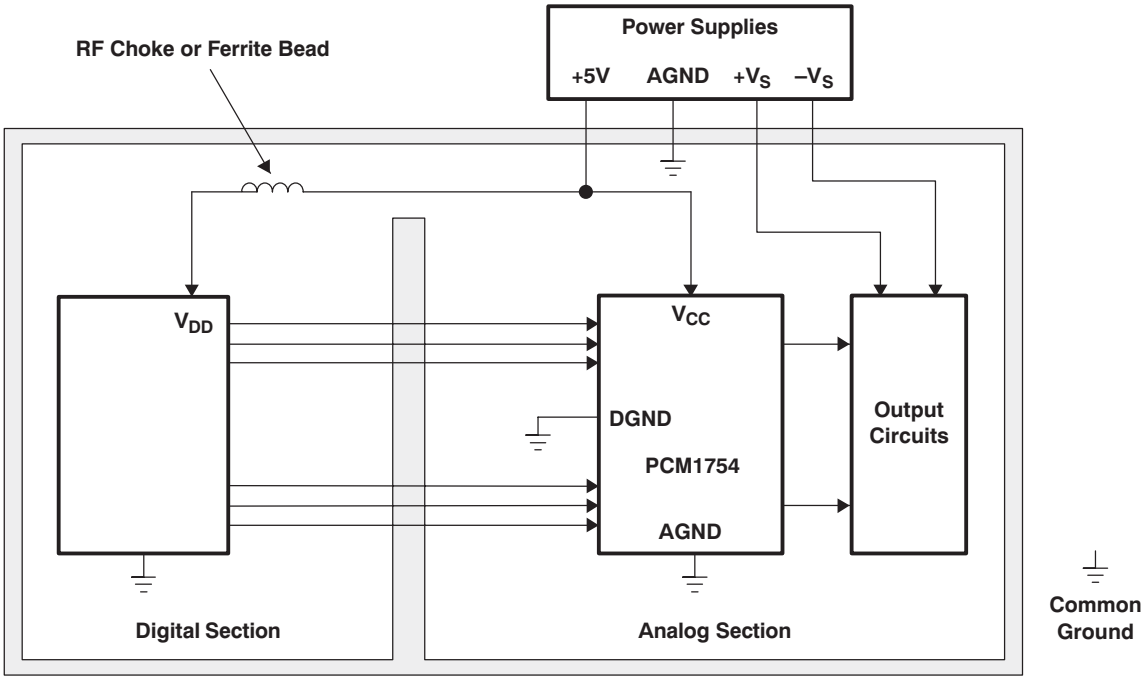


Figure 39. Single-Supply PCB Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Dynamic Performance Testing of Digital Audio D/A Converters*, SBAA055
- OPA2353, *High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier™ Series*, SBOS103
- OPA2134, *SoundPlus™ High Performance Audio Operational Amplifiers*, SBOS058
- PLL1705, PLL1706 *3.3-V Dual PLL Multiclock Generator*, SLES046

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
PCM1754-Q1	Click here	Click here	Click here	Click here	Click here
PCM1753-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
System Two, Audio Precision are trademarks of Audio Precision, Inc.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1753TDBQRQ1	ACTIVE	SSOP	DBQ	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	P1753T	Samples
PCM1754TDBQRQ1	ACTIVE	SSOP	DBQ	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	P1754Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF PCM1753-Q1, PCM1754-Q1 :

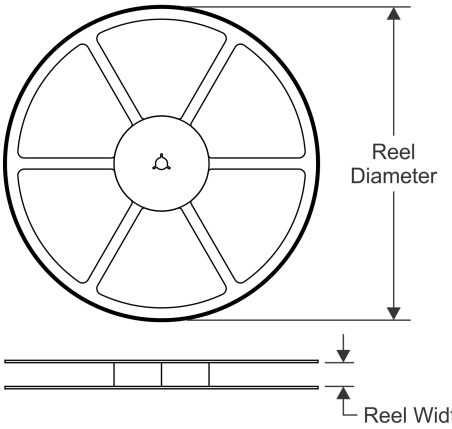
- Catalog: PCM1753, PCM1754

NOTE: Qualified Version Definitions:

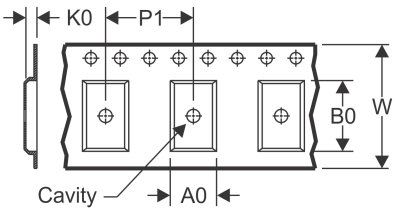
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

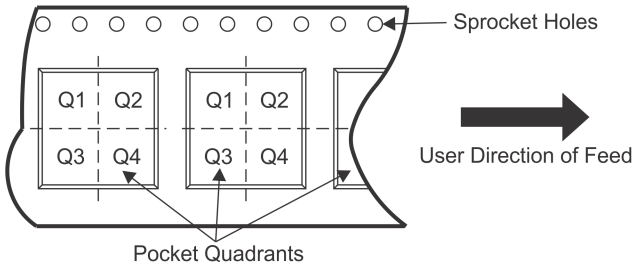


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

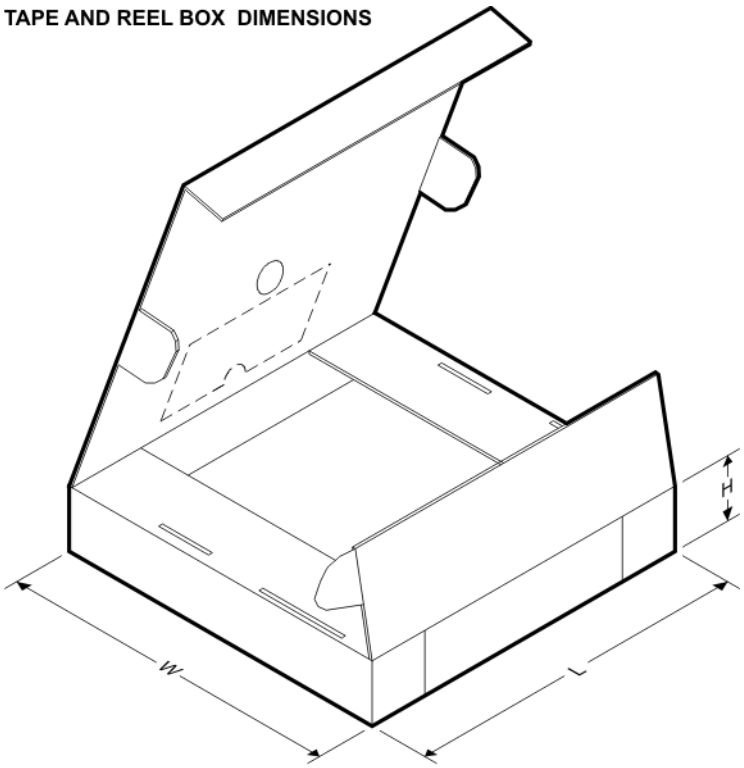
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1753TDBQRQ1	SSOP	DBQ	16	2000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
PCM1754TDBQRQ1	SSOP	DBQ	16	2000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



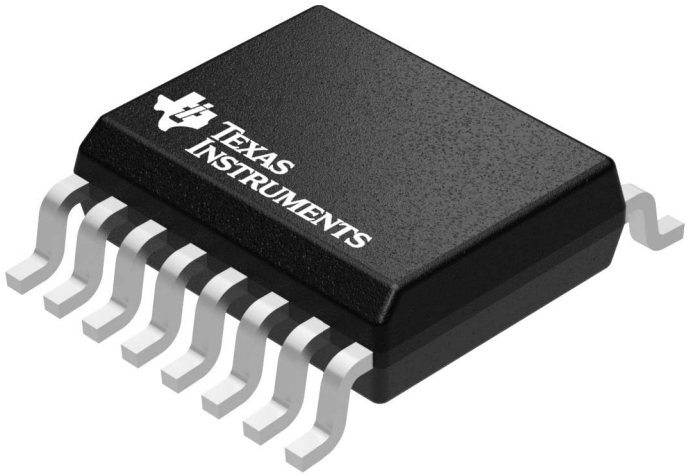
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1753TDBQRQ1	SSOP	DBQ	16	2000	367.0	367.0	35.0
PCM1754TDBQRQ1	SSOP	DBQ	16	2000	367.0	367.0	35.0

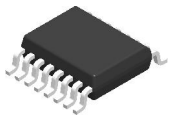
GENERIC PACKAGE VIEW

DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

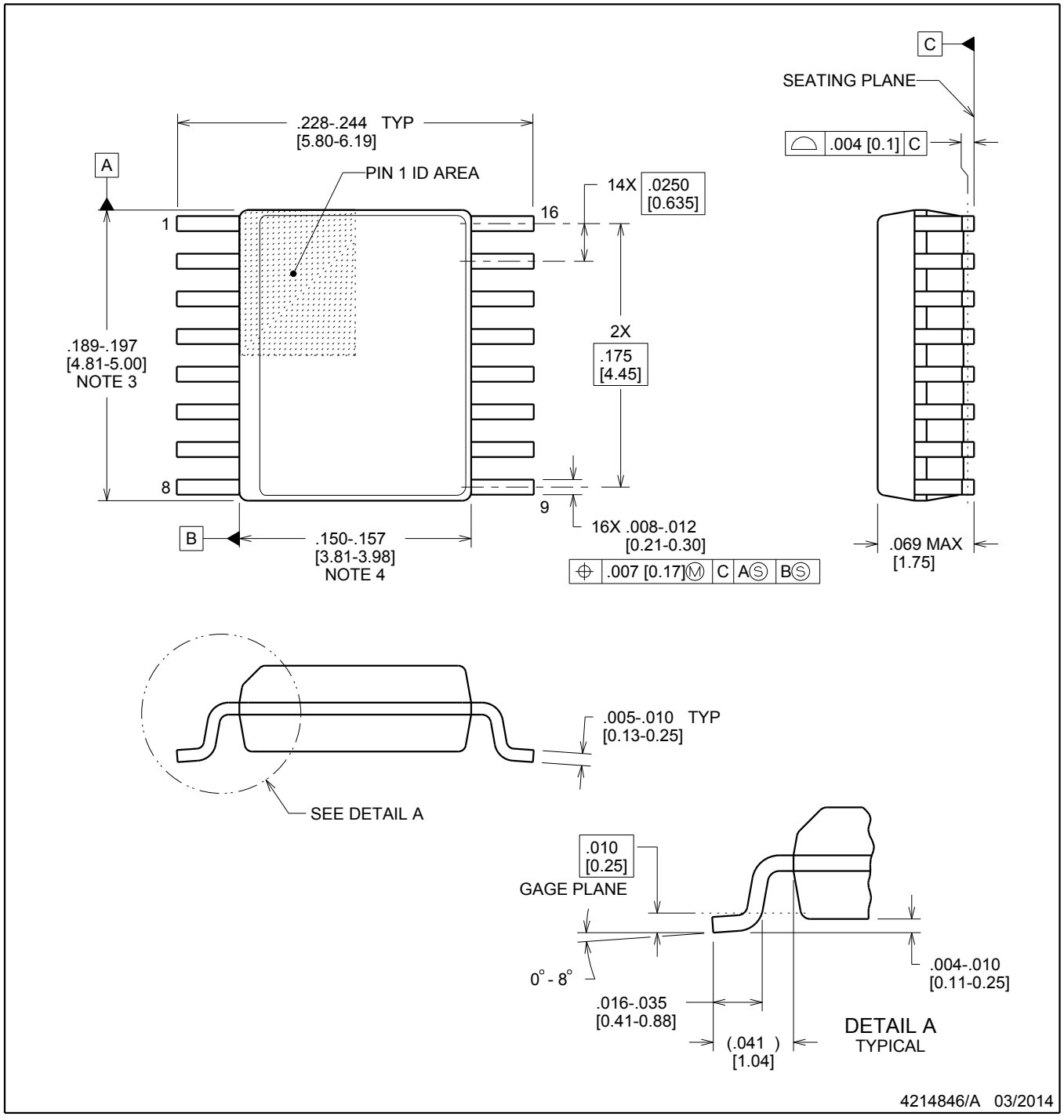


PACKAGE OUTLINE

DBQ0016A

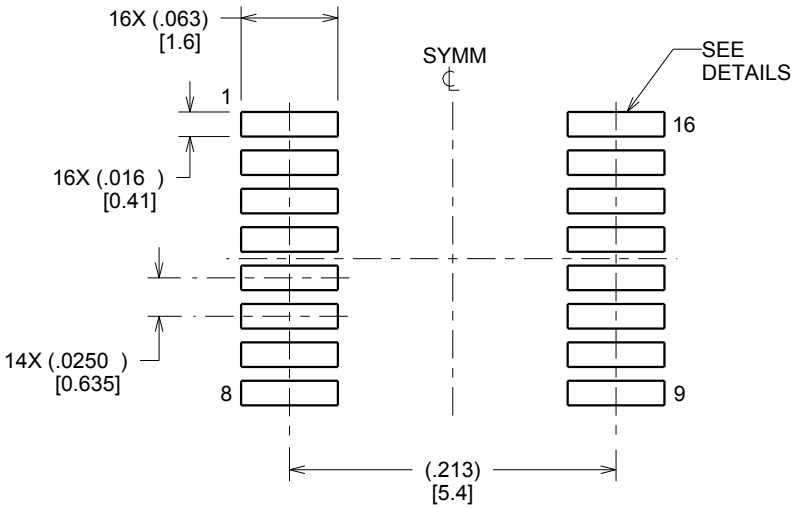
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

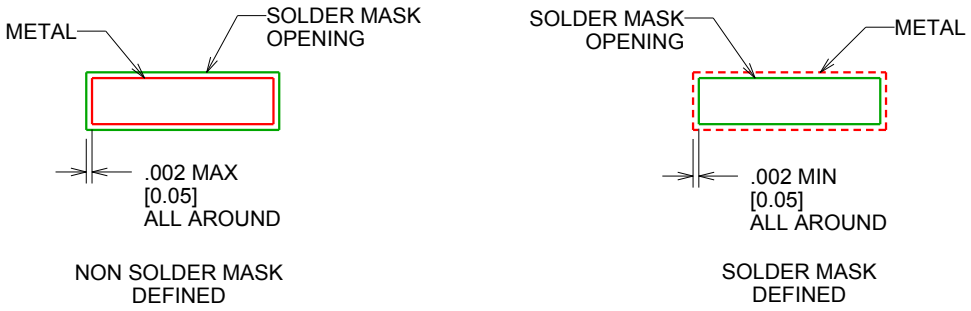


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

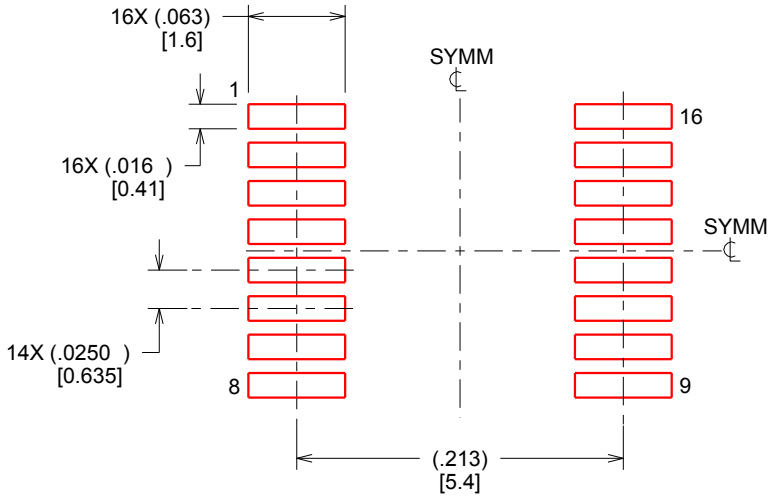
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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