



SD1728 (TH430)

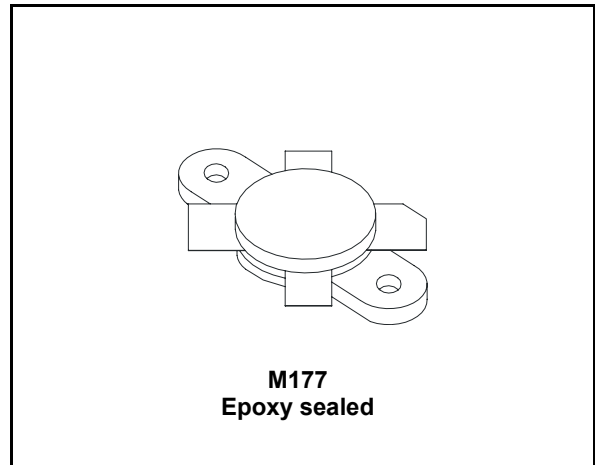
RF & Microwave transistors
HF SSB application

Features

- 13.56MHz
- 44V
- Gold metallization
- Common emitter
- $P_{OUT} = 200W$ with 15dB gain

Description

The SD1728 is a 50V epitaxial silicon NPN planar transistor designed primarily for SSB and Industrial HF applications. This device utilizes emitter ballasting for improved ruggedness and reliability.



Pin connection

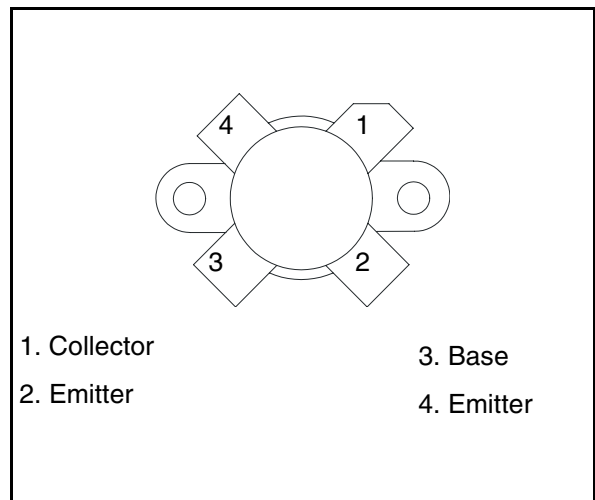


Table 1. Device summary

Part number	Package	Marking
SD1728	M177	TH430

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1 Electrical data

1.1 Maximum ratings

Table 2. Absolute maximum ratings ($T_{CASE} = 25^{\circ}C$)

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base voltage	110	V
V_{CEO}	Collector-emitter voltage	55	V
V_{EBO}	Emitter-base voltage	4.0	V
I_C	Device current	40	A
P_{DISS}	Power dissipation	330	W
T_J	Maximum operating junction temperature	200	$^{\circ}C$
T_{STG}	Storage temperature	-65 to +150	$^{\circ}C$

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.4	$^{\circ}C/W$

2 Electrical characteristics

$$T_{CASE} = +25\text{ }^{\circ}\text{C}$$

2.1 Static

Table 4. Static

Symbol	Test conditions	Values			Unit
		Min	Typ	Max	
BV_{CES}	$I_C = 200\text{mA}, V_{BE} = 0\text{V}$	110			V
BV_{CEO}	$I_C = 200\text{mA}, I_B = 0\text{mA}$	55			V
BV_{EBO}	$I_E = 20\text{mA}, I_C = 0\text{mA}$	4.0			V
I_{CEO}	$V_{CE} = 30\text{V}, I_E = 0\text{mA}$			500	μA
I_{CES}	$V_{CE} = 60\text{V}, I_E = 0\text{mA}$			500	μA
I_{EBO}	$V_{BE} = 4.2\text{V}$			500	μA
h_{FE}	$V_{CE} = 6\text{V}, I_C = 10\text{A}$	23		45	

Table 5. h_{FE} ranking ($V_{CE} = 6\text{V}; I_C = 10\text{A}$)

C	23 - 27
D	27 - 32
E	32 - 38
F	38 - 45

2.2 Dynamic

Table 6. Dynamic

Symbol	Test conditions	Values			Unit
		Min	Typ	Max	
P_{OUT}	$V_{CC} = 44\text{V}, f = 13.56\text{MHz}$	200	250		W
G_P	$V_{CC} = 44\text{V}, P_{OUT} = 200\text{W}$	15	17		dB
η_C	$V_{CC} = 44\text{V}, P_{OUT} = 200\text{W}$	56			%
C_{OB}	$V_{CB} = 50\text{V}, f = 1\text{MHz}$		250	360	pF

3 Typical performance (Class C)

Figure 1. Output power vs input power

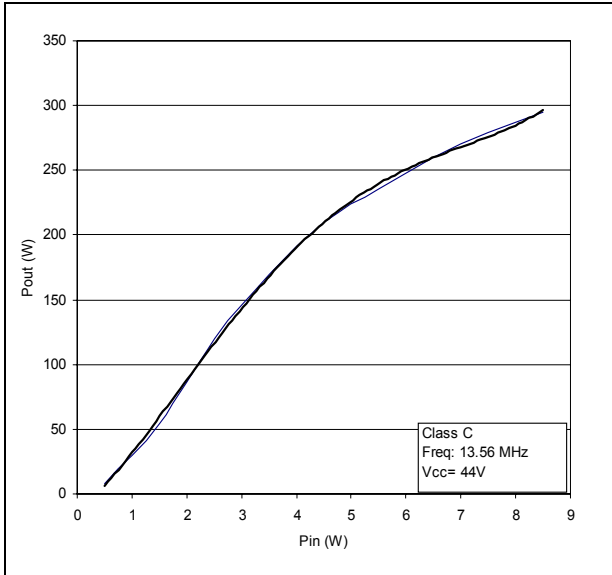


Figure 2. Collector base capacitance vs Collector base voltage (f = 1MHz)

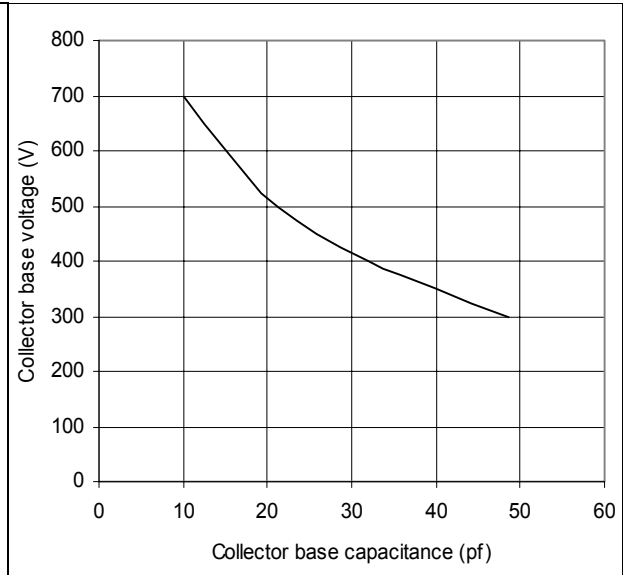


Figure 3. Power gain vs P_{OUT}

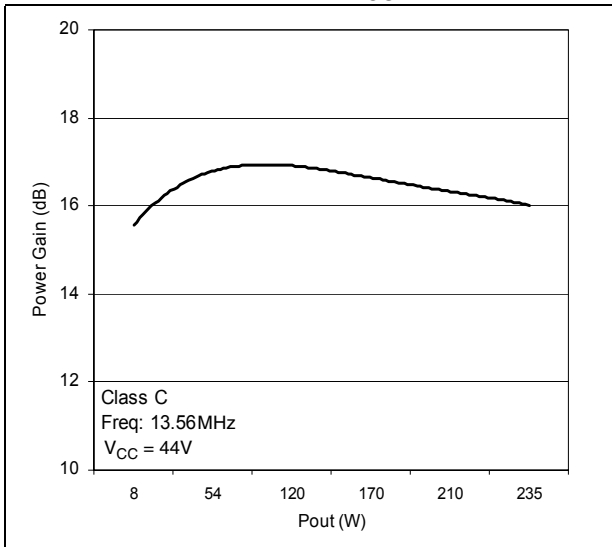
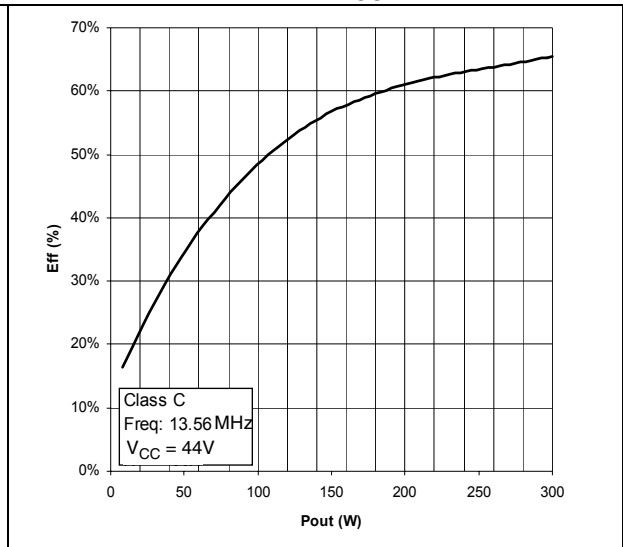


Figure 4. Efficiency vs P_{OUT}



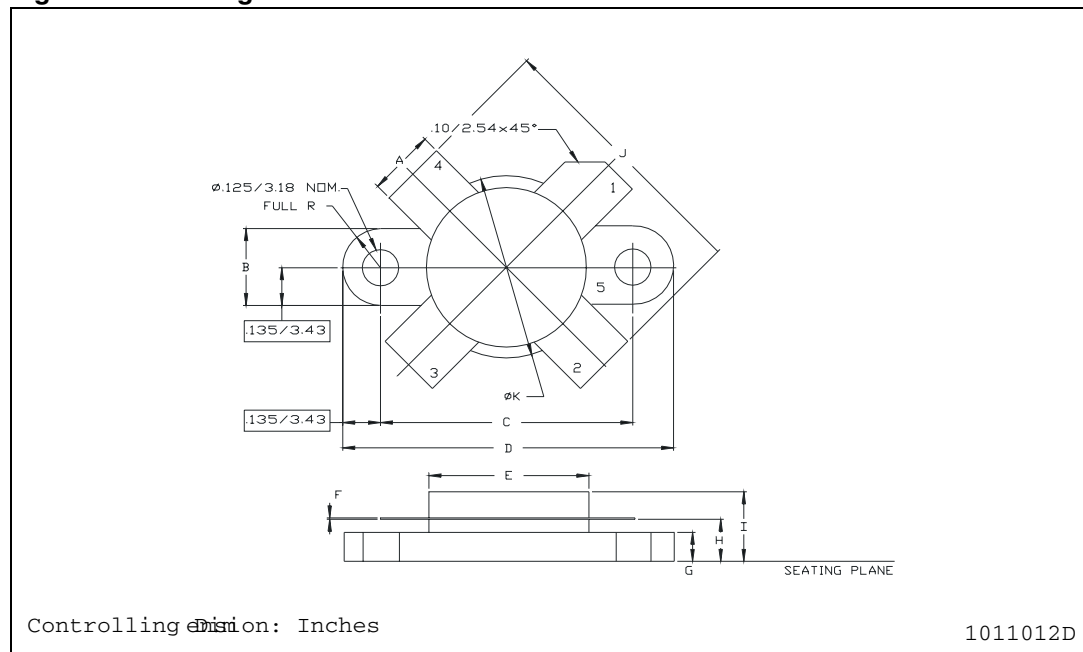
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 7. M177 (.550 DIA 4/L N/HERM W/FLG) mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	5.72		5.97	0.225		0.235
B	6.73		6.96	0.265		0.275
C	21.84		22.10	0.860		0.870
D	28.70		28.96	1.130		1.140
E	13.84		14.10	0.545		0.555
F	0.08		0.18	0.003		0.007
G	2.49		2.74	0.098		0.108
H	3.81		4.32	0.150		0.170
I			7.11			0.280
J	27.43		28.45	1.080		1.120
K	15.88		16.13	0.625		0.635

Figure 5. Package dimensions



5 Revision history

Table 8. Revision history

Date	Revision	Changes
1-Jul-2003	1	First release
24-Apr-2007	2	Document reformatted, updated Table 2 .

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