# TPS22951 Current-Limited 1-Ω Smart-Load Switch

## 1 Features

- 1-Ω P-Channel MOSFET
- 300-mA Continuous Source Current
- Thermal and Short-Circuit Protection
- 600-mA Current Limit
- Operating Range: $V_{CC}$ = 2.8 V to 5.3 V
- 41-µs Typical Rise Time
- 10-µA Maximum Standby Supply Current
- Ambient Temperature Range: –40°C to +85°C
- ESD Performance Tested Per JESD 22
  - 4000-V Human-Body Model (HBM)
  - 400-V Machine Model (MM)
  - 1000-V Charged-Device Model (CDM)

## 2 Applications

- Smart Phones
- Notebooks
- Digital Cameras
- Peripheral Ports

## 3 Description

The TPS22951 smart-load switch is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. This device incorporates a 1-Ω P-channel MOSFET power switch for power distribution. The switch is controlled by a logic enable (EN) input and an accessory detect ($\overline{DET}$) pin. The switch is active when EN is high and $\overline{DET}$ is low. The switch is disabled if EN is low or $\overline{DET}$ is high. A low power state is achieved by driving EN low.

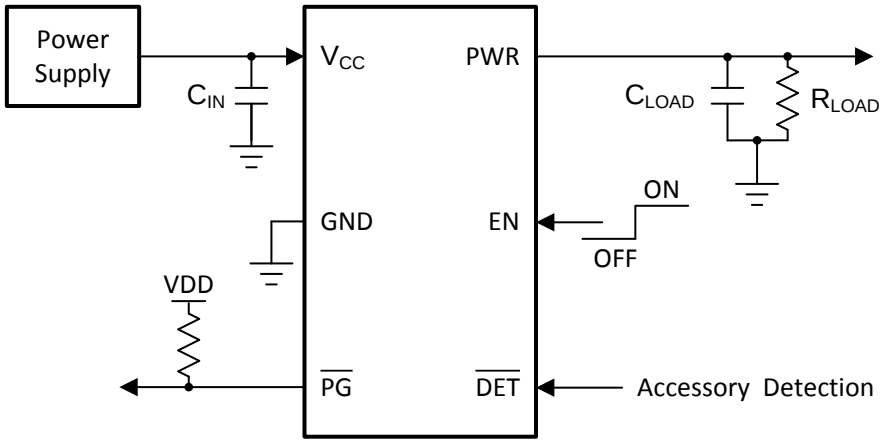
When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by increasing the on resistance of the power switch. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal-protection circuit shuts off the switch to prevent damage. The device recovers from a thermal shutdown once the device has cooled sufficiently, but the switch remains OFF until EN is toggled. This smart-load switch is designed to set current limit at 600 mA maximum.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS22951 | DSBGA (6) | 1.20 mm x 0.80 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Simplified Schematic**



## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision C (March 2015) to Revision D** — **Page**

- Changed all instances of "POK" to "PG" in the data sheet ... 1

**Changes from Revision B (November 2012) to Revision C** — **Page**

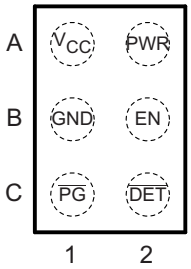
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

**Changes from Revision A (March 2009) to Revision B** — **Page**

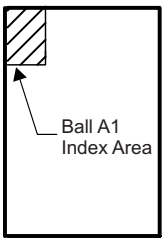
- Updated Top-Side Marking in the *Ordering Information* table. ... 3

# 5 Pin Configurations and Functions

**YFP Package**
**6-Pin DSBGA**
**Top-Through View**




**YFP Package**
**6-Pin DSBGA**
**Top View**




**Pin Functions**

| Pin | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| A1 | $V_{CC}$ | I | Supply voltage |
| A2 | PWR | O | Power switch output |
| B1 | GND | — | Ground |
| B2 | EN | I | Enable input (1) |
| C1 | $\overline{PG}$ | O | Power Good switch status open-drain output, active low |
| C2 | $\overline{DET}$ | I | Accessory detect, active low |

(1) $\overline{DET}$ must be low for a minimum of 2 μs before EN is pulled high (see the *Timing Requirements* section).

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ (2) | Supply voltage | –0.3 | 6 | V |
| $V_{O(PWR)}$ (2) | Output voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $V_{I(EN)}$, $V_{I(\overline{DET})}$ | Input voltage | –0.3 | 6 | V |
| $V_{O(\overline{PG})}$ | Voltage | –0.3 | 6 | V |
| $I_{O(PWR)}$ | Continuous output current | Internally limited | | |
| | Continuous total power dissipation | See the *Thermal Information* section | | |
| | Lead temperature soldering 1,6 mm (1/16 in) from case for 10 s | –0.3 | 6 | V |
| $T_J$ | Operating virtual junction temperature | –40 | 85 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | 4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | 1000 | |
| | | Machine model (MM) | 400 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.2 | 5.3 | V |
| $V_{I(EN)}$, $V_{I(\overline{DET})}$ | Input voltage | 0 | $V_{CC}$ | V |
| $I_{O(PWR)}$ | Continuous output current | 0 | –600 | mA |
| $T_J$ | Operating virtual junction temperature | –40 | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | TPS22951 YFP (DSBGA) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 125.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 1.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 26 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 26 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over operating –40°C ≤ $T_J$ ≤ +85°C range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | |
| $r_{DS(on)}$ | Static drain-source ON-state resistance, 3-V operation | $V_{CC}$ = 3 V, $I_O$ = 0.3 A | | | 1 | Ω |
| | Leakage current | PWR connected to GND, $V_{I(EN)}$ = 0 V | | 1 | | µA |
| **EN AND $\overline{DET}$** | | | | | | |
| $V_{IH}$ | High-level input voltage | 2.8 V ≤ $V_{CC}$ ≤ 5.3 V | 1.35 | | | V |
| $V_{IL}$ | Low-level input voltage | 2.8 V ≤ $V_{CC}$ ≤ 5.3 V | | | 0.45 | V |
| $I_I$ | Input current | $V_{I(EN)}$ or $V_{I(\overline{DET})}$ = 0 V or 5.3 V | | | 1 | µA |
| **CURRENT LIMIT** | | | | | | |
| $I_{OS}$ | Short-circuit output current | $V_{CC}$ = 2.8 V or 5.3 V, PWR connected to GND, Device enabled into short circuit | –0.3 | | –0.6 | A |
| **SUPPLY CURRENT** | | | | | | |
| | Supply current, enabled | No load on PWR, $V_{CC}$ = 5.3 V, $V_{I(EN)}$ = $V_{CC}$, $V_{I(\overline{DET})}$ = $V_{CC}$ or 0 V | | | 100 | µA |
| | Supply current, disabled | No load on PWR, $V_{CC}$ = 5.3 V, $V_{I(EN)}$ = 0 V, $V_{I(\overline{DET})}$ = $V_{CC}$ or 0 V | | | 10 | µA |
| **$\overline{PG}$** | | | | | | |
| $V_{OL(\overline{PG})}$ | Power Good output low voltage | $I_{(PG)}$ = 1 mA | | | 0.4 | V |
| | OFF-state current | $V_{(PG)}$ = 5.3 V | | | 1 | µA |
| **THERMAL SHUTDOWN** | | | | | | |
| | Thermal shutdown threshold (2) | | 135 | | | °C |
| | Recovery from thermal shutdown (2) | | 125 | | | °C |
| | Hysteresis (2) | | | 25 | | °C |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Not tested in production, specified by design

## 6.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{su}$ | Setup time, $\overline{DET}$ low before EN high | 2 | | µs |

## 6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | | |
| $t_r$ (1) | Rise time, output | $V_{CC}$ = 5.3 V | $C_L$ = 1 µF, $R_L$ = 20 Ω | $T_J$ = 25°C | | 41 | | µs |
| | | $V_{CC}$ = 2.8 V | | | | 6 | | |
| $t_f$ (1) | Fall time, output | $V_{CC}$ = 5.3 V | $C_L$ = 1 µF, $R_L$ = 20 Ω | $T_J$ = 25°C | | 43 | | µs |
| | | $V_{CC}$ = 2.8 V | | | | 43 | | |
| **EN AND DET** | | | | | | | | |
| $t_{on}$ (1) | Turnon time (EN to PWR) | $V_{CC}$ = 5.3 V | $C_L$ = 1 µF, $R_L$ = 20 Ω | | | 42 | | µs |
| | Turnon time (EN to $\overline{PG}$) | | $C_P$ = 15 pF, $R_P$ = 10 kΩ | | | 9.5 | | |
| $t_{off}$ (1) | Turnoff time (EN to PWR) | $V_{CC}$ = 5.3 V | $C_L$ = 1 µF, $R_L$ = 20 Ω | | | 48 | | µs |
| | Turnoff time (EN to $\overline{PG}$) | | $C_P$ = 15 pF, $R_P$ = 10 kΩ | | | 47 | | |

(1) Not tested in production, specified by design

## 6.8 Typical Characteristics

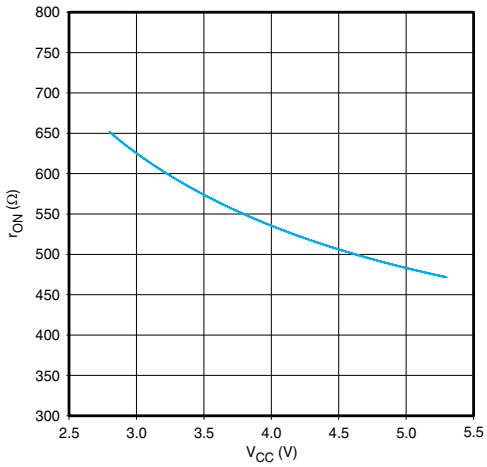



**Figure 1. ON-State Resistance vs $V_{CC}$**

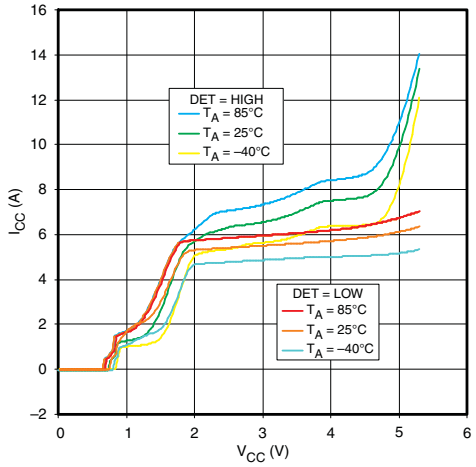



**Figure 2. $I_{CC}$ vs $V_{CC}$, EN = $V_{CC}$**

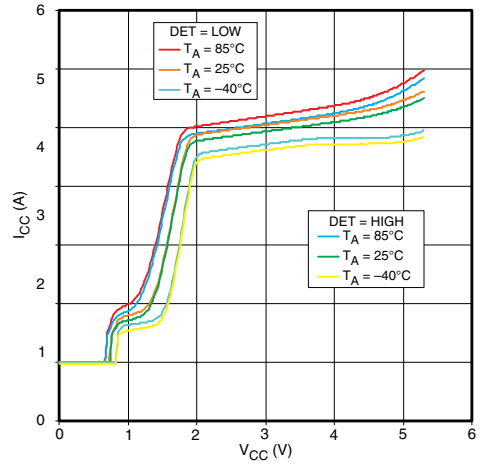



**Figure 3. $I_{CC}$ vs $V_{CC}$, EN = GND**

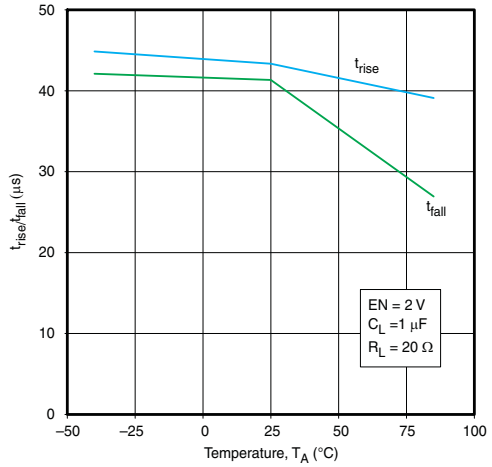



**Figure 4. $t_{rise}/t_{fall}$ vs Temperature, $V_{CC}$ = 5.3 V**

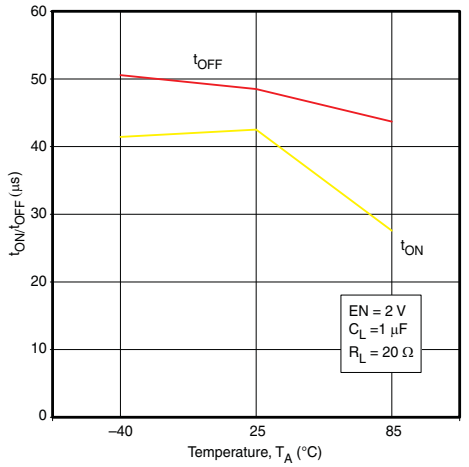



**Figure 5. $t_{ON}/t_{OFF}$ vs Temperature, $V_{CC}$ = 5.3 V**

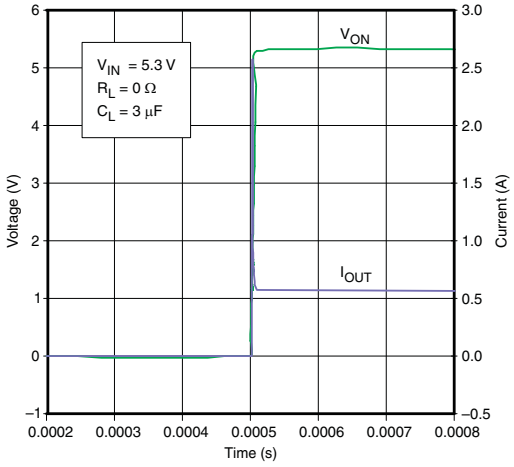



**Figure 6. Device Enabled into Short-Circuit**

## Typical Characteristics (continued)

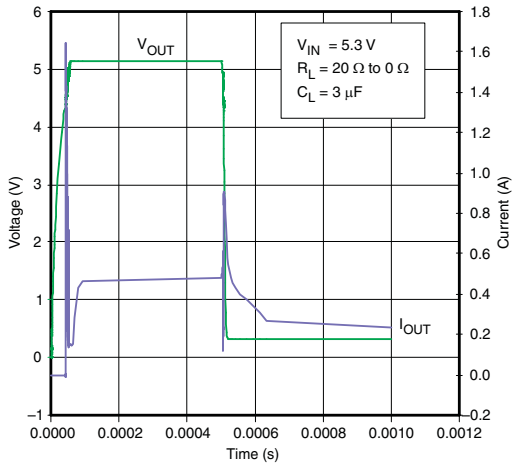



**Figure 7. Full-Load to Short-Circuit Transient Response**

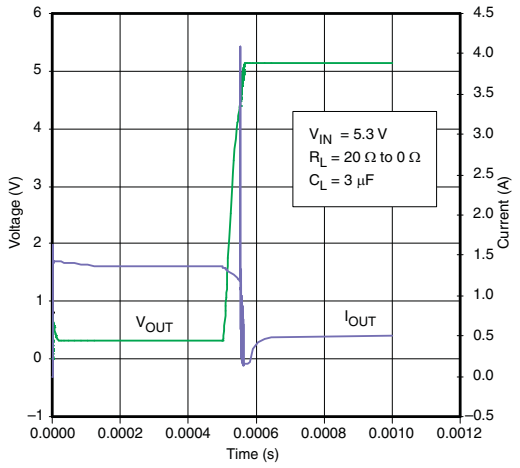



**Figure 8. Short-Circuit to Full-Load Recovery Response**

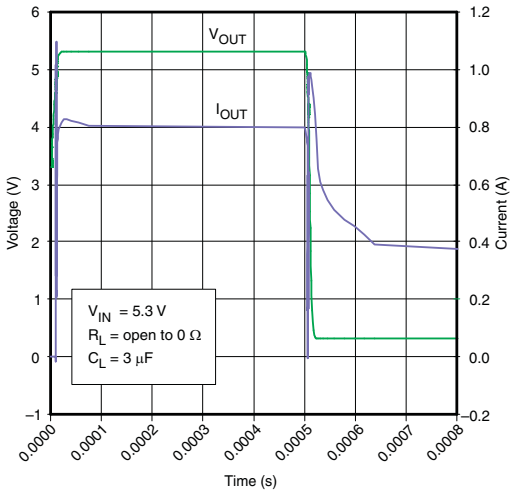



**Figure 9. No-Load to Short-Circuit Transient Response**

# 7 Parameter Measurement Information

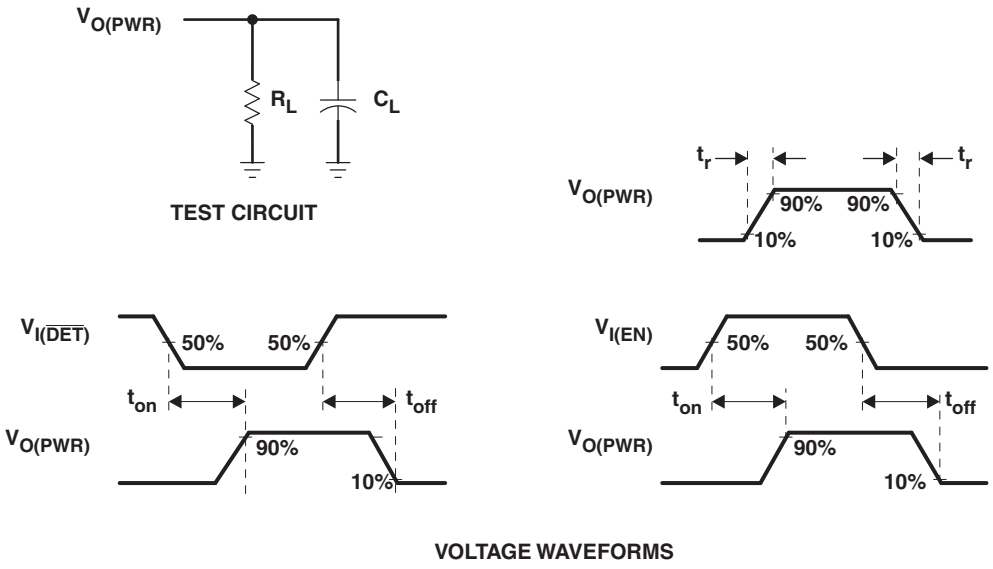



**Figure 10. Test Circuit and Voltage Waveforms**

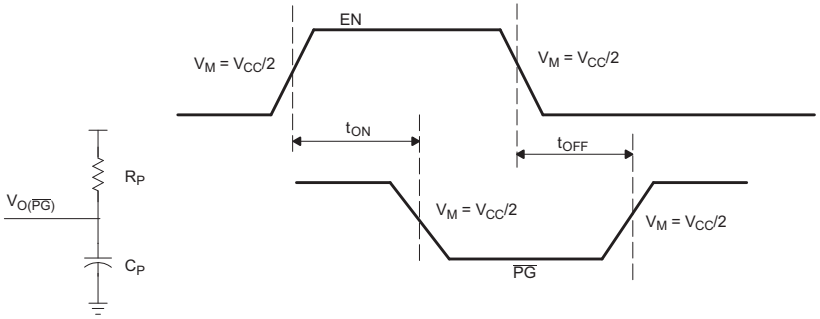



**Figure 11. EN to $\overline{PG}$ Test Point**

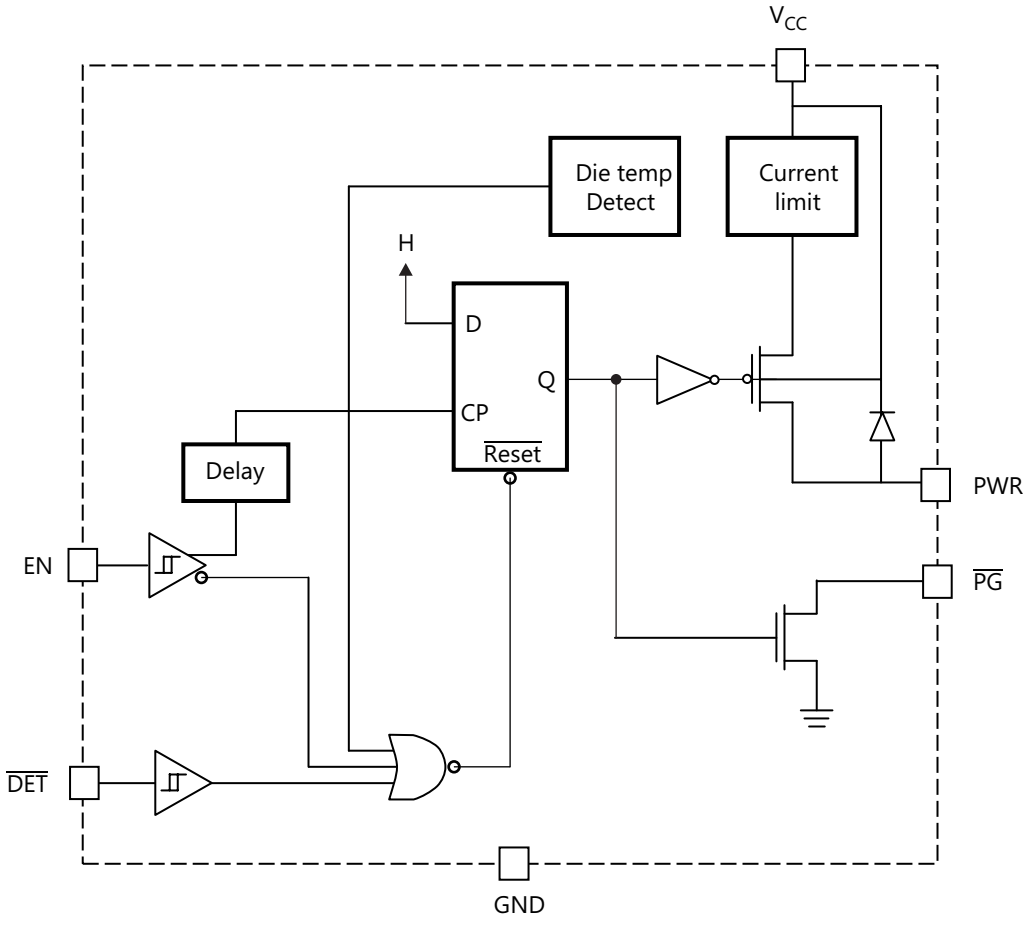
# 8 Detailed Description

## 8.1 Overview

The TPS22951 smart-load switch is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. This device incorporates a 1-Ω P-channel MOSFET power switch for power distribution. The switch is controlled by a logic enable (EN) input and an accessory detect ($\overline{\text{DET}}$) pin. The switch is active when EN is high and $\overline{\text{DET}}$ is low. The switch is disabled if EN is low or $\overline{\text{DET}}$ is high. A low power state is achieved by driving EN low.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by increasing the on resistance of the power switch. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal-protection circuit shuts off the switch to prevent damage. The device recovers from a thermal shutdown once the device has cooled sufficiently, but the switch remains OFF until EN is toggled. This smart-load switch is designed to set current limit at 600 mA maximum.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Current Limit

The TPS22951 includes a current-limiting feature. The current limit can help protect the system from high currents in the case of large capacitive loads and short circuits. When the load current exceeds the current limit threshold, the device limits the output current by increasing the on-resistance of the switch.

### 8.3.2 Power Good Indication

The TPS22951 includes an open-drain Power Good indication. This signal can be used to provide an indication to another component in the system. The signal behaves according to Table 1.

To use the signal, the PG pin must be connected to a pullup resistor. The PG pin has an absolute maximum rating of 6 V and must not be pulled up to any voltage beyond 6 V. The pullp resistor must be in the range of 10 kΩ to limit the current flowing into the PG pin when the switch is on and the PG signal is low.

### 8.3.3 EN and DET inputs

The switch is controlled by the EN and DET pins. To enable the switch, the EN pin must be high and the DET pin must be low.

### 8.3.4 Thermal Shutdown

The TPS22951 includes a thermal shutdown circuit. If the device reaches the thermal shutdown threshold, the switch is automatically be disabled. The switch retrys after the device temperature has decreased and the EN pin is toggled from H to L to H.

## 8.4 Device Functional Modes

Table 1 lists the functional modes of the TPS22951.

**Table 1. Function Table**

| EN | $\overline{\text{DET}}$ | CURRENT LIMIT | THERMAL LIMIT | POWER SWITCH ($V_{CC}$ TO PWR) | $\overline{\text{PG}}$ (OPEN-DRAIN) |
|---|---|---|---|---|---|
| 0 | X | Not exceeded | Not exceeded | OFF | Z |
| X | 1 | Not exceeded | Not exceeded | OFF | Z |
| 1 | 0 | Not exceeded | Not exceeded | ON | L |
| 1 | 0 | Exceeded | Not exceeded | ON – current-limited | L |
| X | X | X | Exceeded (1) | OFF | Z |

(1) To recover from a thermal event, the die temperature must first drop below the specified limit. EN must then be toggled to latch in the proper state of the flip-flop.

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The input to output voltage drop in the device is determined by the $R_{ON}$ of the device and the load current. The $R_{ON}$ of the device depends upon the $V_{CC}$ condition of the device. Refer to Figure 1 $r_{ON}$ vs $V_{CC}$ to determine the $r_{ON}$ of the device based upon the $V_{CC}$ condition. Use Equation 1 to calculate the input to output voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

where

- $\Delta V$ = voltage drop from $V_{CC}$ to PWR
- $I_{LOAD}$ = load current
- $R_{ON}$ = ON-Resistance of the device for a specific $V_{CC}$

## 9.2 Typical Application

This application demonstrates how the TPS22951 can be used to protect against a short-circuit event. In this application, the PWR node is accidentally shorted to ground.

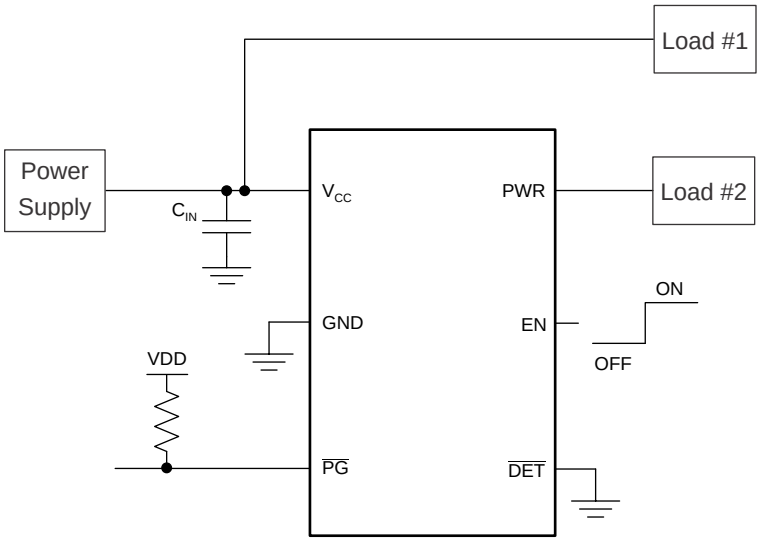



**Figure 12. Typical Application Circuit**

### 9.2.1 Design Requirements

For this design example, use the input parameters given in Table 2:

**Table 2. Design Parameters**

| DESIGN PARAMTER | EXAMPLE VALUE |
|---|---|
| Power Supply Maximum DC Output Current | 2 A |
| Load 1 Current Consumption | 1 A |

### 9.2.2 Detailed Design Procedure

The power supply provides power to multiple loads. In the event that Load 2 is shorted to ground, the power supply must continue providing power to Load 1. The power supply can provide 2-A continuous current. Load 1 consumes 1-A continuous current. The TPS22951 is used to ensure that Load 2 consumes less than 1-A continuous current. This ensures that the power supply can provide power to Load 1 even in the case that Load 2 is shorted to ground.

### 9.2.3 Application Curve

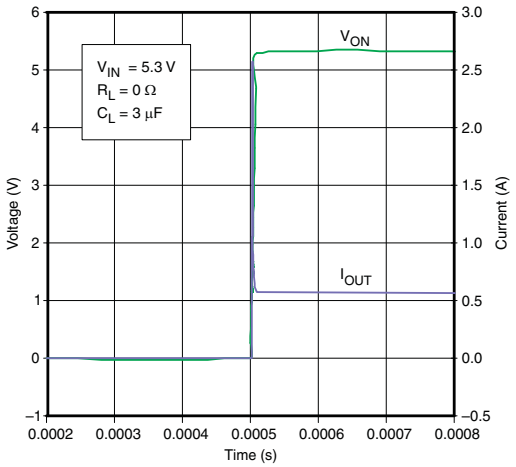



**Figure 13. Device Enabled into Short-Circuit**

## 10 Power Supply Recommendations

The device is designed to operate from a $V_{CC}$ range of 2.8 to 5.3 V. The $V_{CC}$ power supply must be well regulated and placed as close to the $V_{CC}$ terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using a small input capacitor is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

# 11 Layout

## 11.1 Layout Guidelines

- The $V_{CC}$ and PWR traces must be wide enough to carry the necessary load current (up to 600 mA).
- To handle transient load currents, a capacitor may be placed close to the $V_{CC}$ pin.
- To make use of the PG signal, it must be connected to a pullup resistor. The pullup source may be the $V_{CC}$ node. It is also possible to use a different source for the pullup resistor.

## 11.2 Layout Example

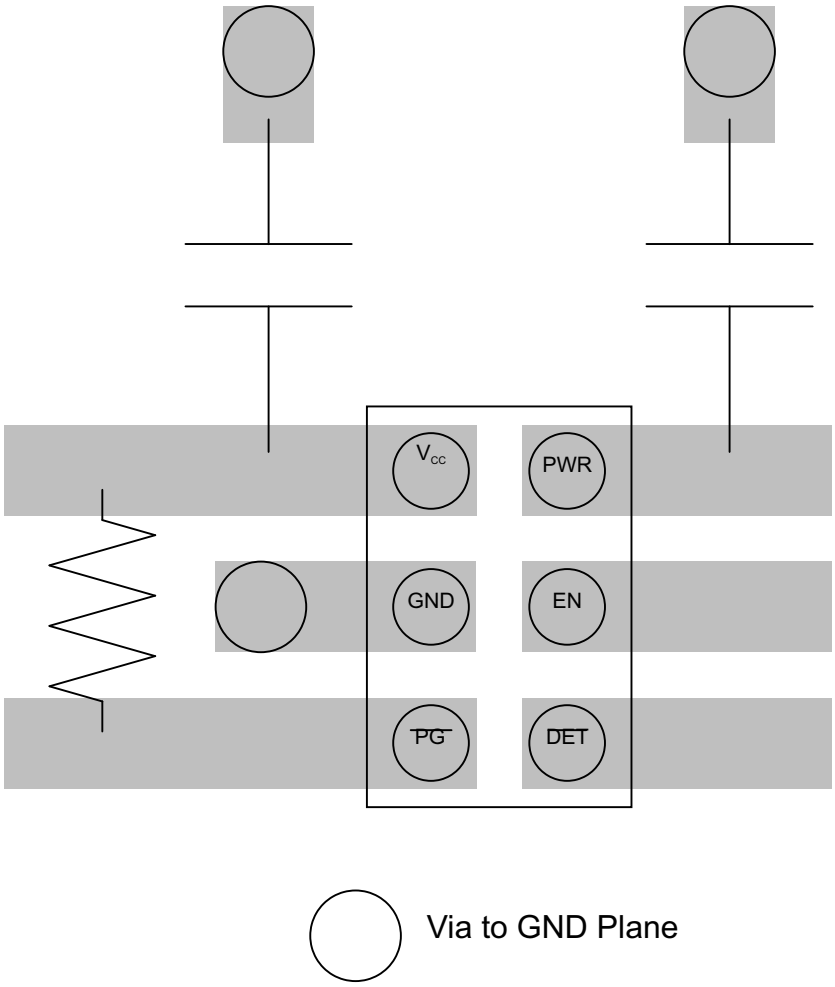



**Figure 14. Layout Example**

## 11.3 Thermal Considerations

The maximum IC junction temperature must be restricted to 85°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given ambient temperature, use Equation 2 and Equation 3.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}}$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (85°C for the TPS22951)

## Thermal Considerations (continued)

- $T_A$ = ambient temperature of the device
- $R_{\theta JA}$ = junction to air thermal impedance. See thermal metrics table. This parameter is highly dependent upon board layout.

(2)

$$P_D = I^2 \times R \quad (3)$$

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- *Basics of Load Switches*
- *Load Switch Thermal Considerations*

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS22951YFPR | ACTIVE | DSBGA | YFP | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (2W ~ 2W7) | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

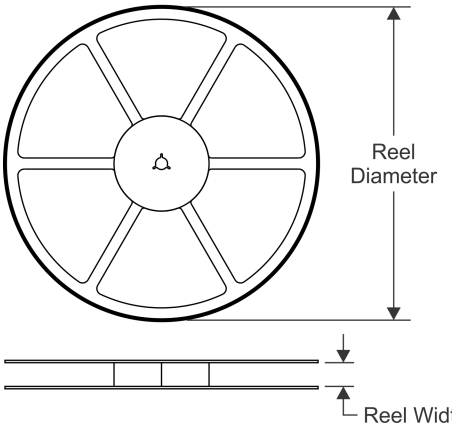
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

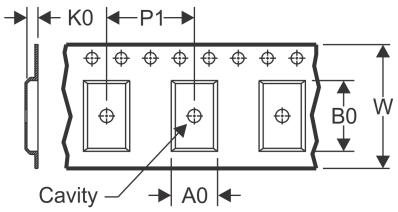
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

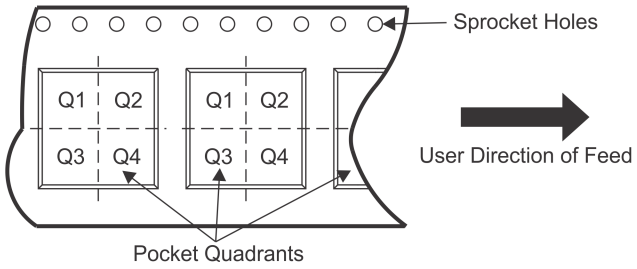



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

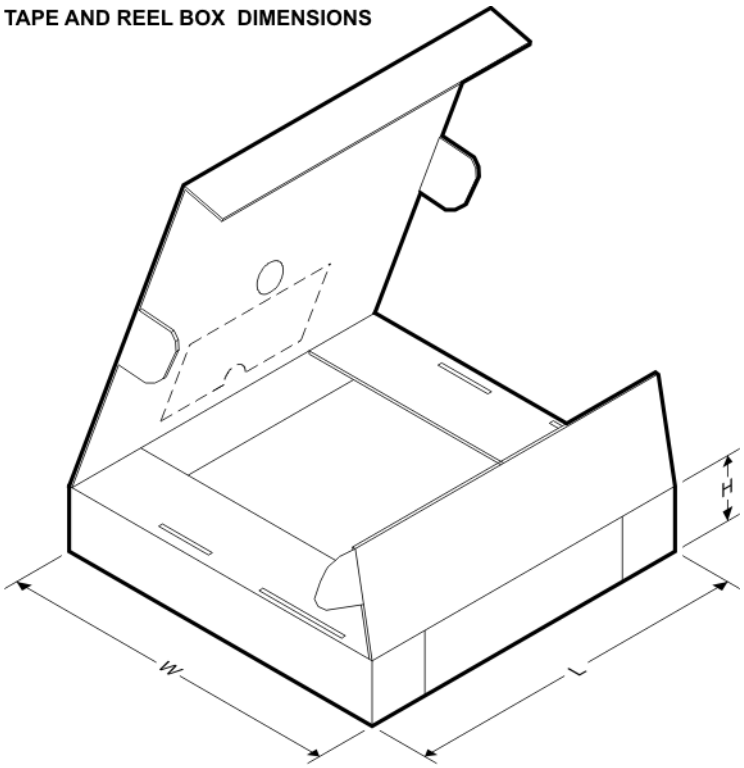
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS22951YFPR | DSBGA | YFP | 6 | 3000 | 180.0 | 8.4 | 0.9 | 1.3 | 0.6 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

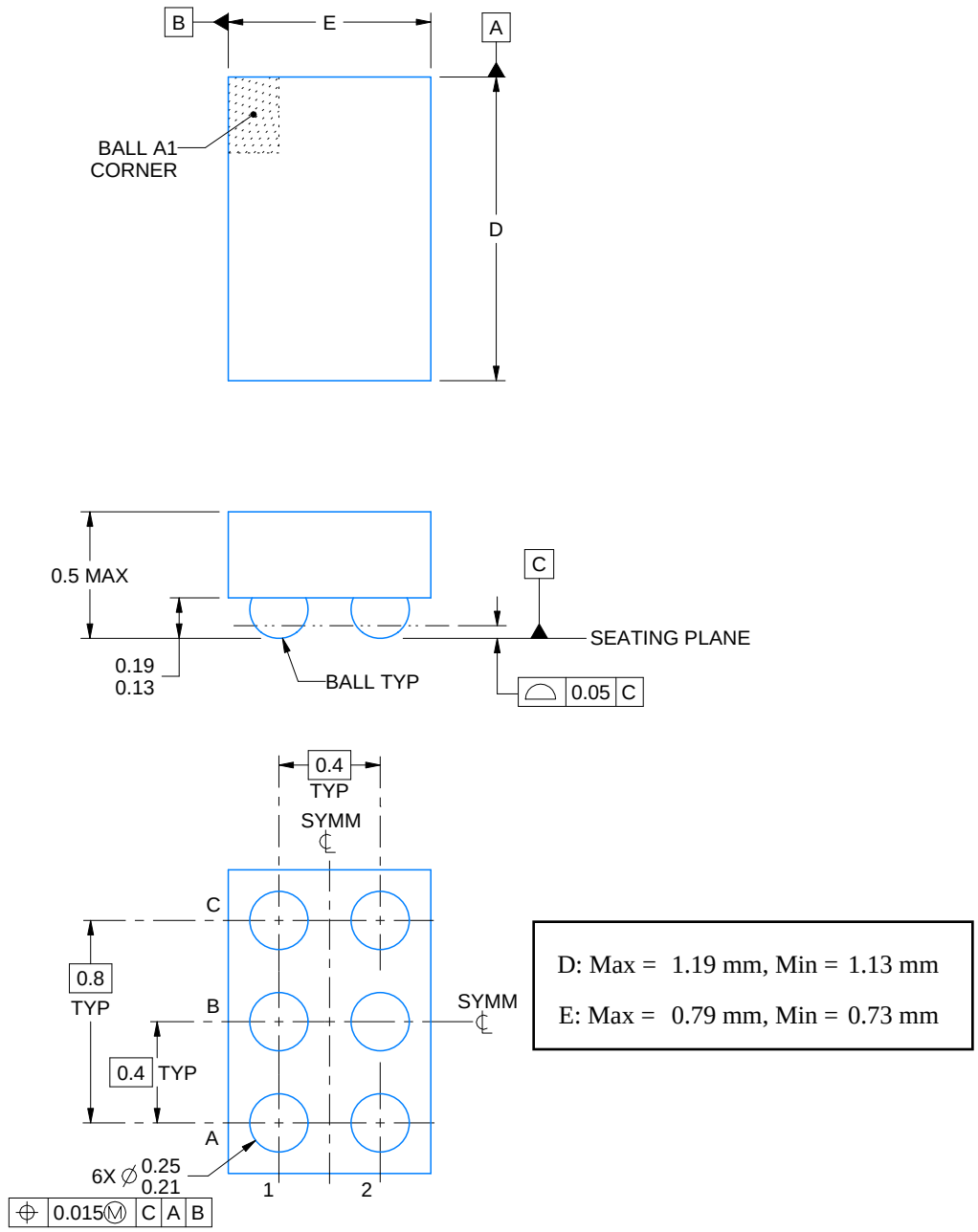
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS22951YFPR | DSBGA | YFP | 6 | 3000 | 220.0 | 220.0 | 34.0 |

# PACKAGE OUTLINE

## YFP0006

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

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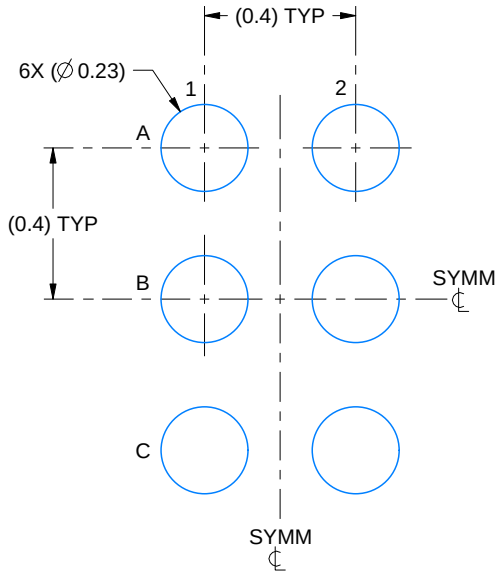
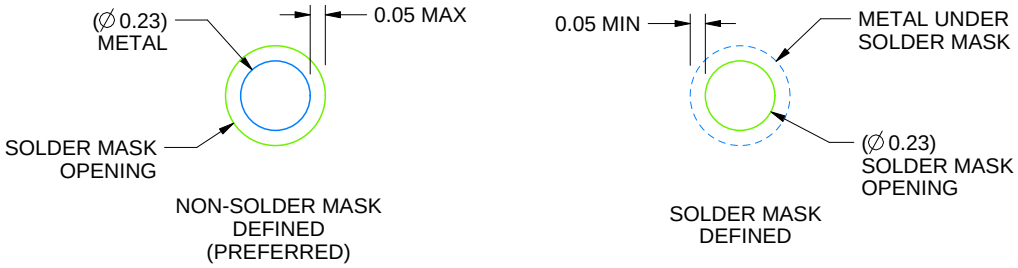
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:50X




SOLDER MASK DETAILS
NOT TO SCALE

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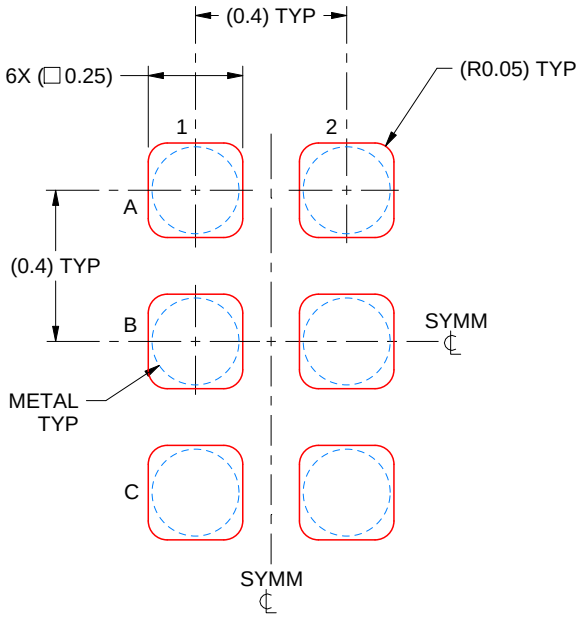
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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