19-5143; Rev 1; 1/12

EVALUATION KIT AVAILABLE

Low-Capacitance VGA 2:2 Dual-Graphics Crossover Switch

General Description

The MAX14885E integrates high-bandwidth analog switches, level-translating buffers, and level-translating FET switches. The device implements a complete 2:2 dual-graphics crossover solution for VGA signal switching. The MAX14885E provides 12 very high-frequency 700MHz (typ) SPST switches for RGB signals, four low-frequency clamping switches for display data channel (DDC) signals, two pairs of level-translating buffers for the HSYNC and VSYNC signals, and integrated extended ESD protection. The MAX14885E is used to select one of two sources to either of two destinations (see the *Typical Operating Circuit*) within a laptop computer.

Horizontal and vertical synchronization (SH_/SV_) inputs feature level-shifting buffers to support low-voltage controllers and standard 5V TTL-level monitors. DDC, consisting of SDA_ and SCL_, are FET switches that protect the low-voltage VGA source from potential damage from high-voltage presence on the monitor while reducing capacitive load.

All 14 output terminals of the MAX14885E feature high-ESD protection to ±15kV Human Body Model (HBM) and ±6kV IEC 61000-4-2 Contact Discharge (see the *Pin Description*). All other pins are protected to ±2kV HBM.

The MAX14885E is specified over the extended -40°C to +85°C temperature range, and is available in a 40-pin TQFN (5mm x 5mm) package.

Features

- **Low Quiescent Current ≤ 5µA (max)**
- **Low 5Ω (typ) On-Resistance (RGB Signals)**
- **High Bandwidth, 700MHz (typ), RGB**
- **DDC Level Shifting, Isolation with Internal Pullup Termination, and Protection**
- **Horizontal and Vertical Sync Level Shifting and Buffering**
- **Inputs Compatible with V_L, Outputs TTL Compatible**
- **Source/Sink ±10mA on Each SH_, SV_ Output**
- **Independent Selectable Logic Inputs for Switching**
- **High ESD Protection on Outputs**
  - **±15kV ESD HBM**
  - **±6kV IEC 61000-4-2 Contact Discharge**
- **Small, 40-Pin TQFN (5mm x 5mm) Package**

Applications

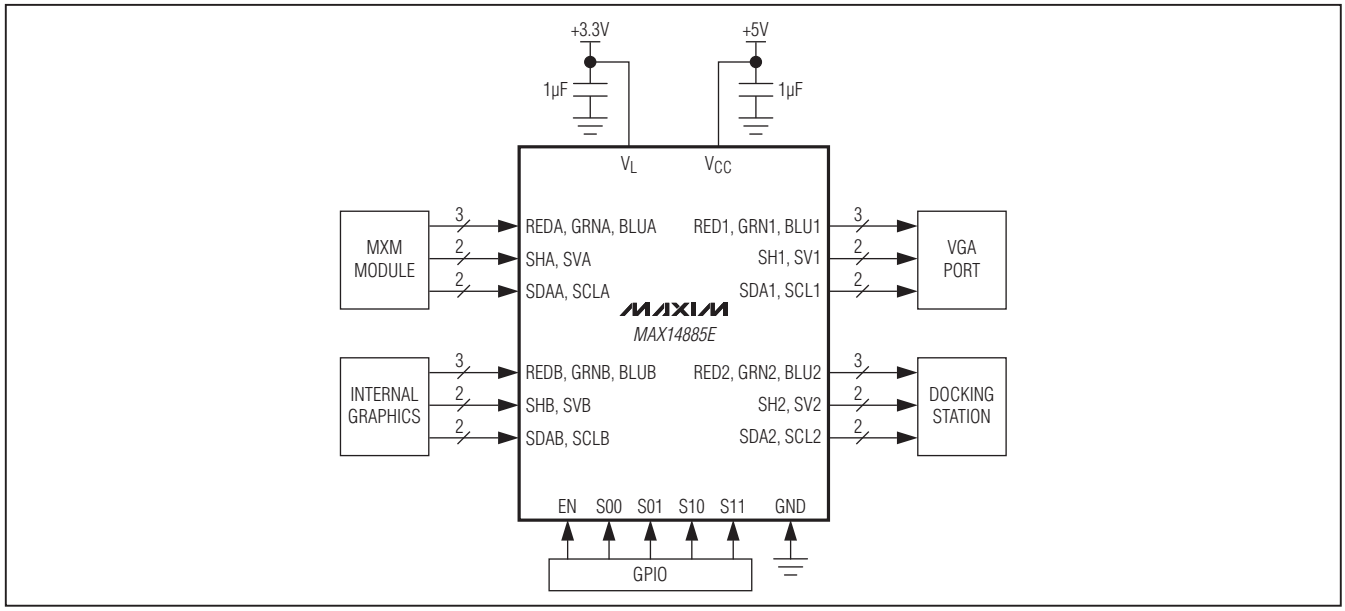
Notebook Computer—Switchable Graphics

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14885EETL+	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Application Circuit



Low-Capacitance VGA 2:2 Dual-Graphics Crossover Switch

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V_{CC} ..... -0.3V to +6V
V_L ..... -0.3V to +6V
RED_, GRN_, BLU_, SCL1, SCL2, SDA1, SDA2, SH1, SH2, SV1, SV2 ..... -0.3V to (V_{CC} + 0.3V)
SCLA, SCLB, SDAA, SDAB, SHA, SHB, SVA, SVB, S00, S01, S10, S11, EN ..... -0.3V to (V_L + 0.3V)
Continuous Current Through RED_, GRN_, BLU_ Switches ..... ±50mA
Continuous Current Through SDA_, SCL_ Switches ..... ±50mA
Peak Current Through All Switches (pulsed at 1ms, 10% duty cycle)..... ±100mA
Continuous Power Dissipation (Multilayer Board, T_A = +70°C):
40-Pin TQFN (derate 35.7mW/°C above +70°C).....2857mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature .....+150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....28°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, V_L = +2.3V to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5.0V, V_L = +3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}			4.5		5.5	V
Logic Supply Voltage	V_L	$V_L \le V_{CC}$		2.3	3.3	5.5	V
V_{CC} Supply Current	I_{CC}	V_{CC} = +5.5V, V_L = +3.6V, V_{EN} = 0V, V_{SHA}, V_{SHB}, V_{SVA}, V_{SVB} = 0V or V_L			0.2	5	µA
V_L Supply Current	I_L	V_{CC} = +5.5V, V_L = +3.6V, SCL_ and SDA_ unconnected	V_{EN}, V_{SHA}, V_{SHB}, V_{SVA}, V_{SVB} = 0V		0.2	5	µA
			V_{EN}, V_{SHA}, V_{SHB}, V_{SVA}, V_{SVB} = V_L		0.3	0.5	mA
On-Resistance (RED_, GRN_, BLU_)	RHF_{ON}	V_{IN} = +0.7V, I_{IN} = +10mA			5	8	Ω
On-Resistance Match (RED_, GRN_, BLU_)	ΔR_{ON}	0V ≤ V_{IN} ≤ +0.7V, I_{IN} = -10mA				1	Ω
On-Resistance Flatness (RED_, GRN_, BLU_)	$R_{FLAT(ON)}$	0V ≤ V_{IN} ≤ +0.7V, I_{IN} = -10mA			0.5	1	Ω
Leakage Current (RED_, GRN_, BLU_)	I_{LK}	V_{EN} = 0V		-1		+1	µA
On-Resistance (SDA_, SCL_)	$RDDC_{ON}$	V_{IN} = +0.7V, I_{IN} = ±10mA			25		Ω
V_{CC} Pullup Resistor (SDA1, SDA2, SCL1, SCL2)		Resistor to V_{CC}			20		kΩ
V_L Pullup Resistor (SDAA, SDAB, SCLA, SCLB)		Resistor to V_L			3		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V, V_L = +2.3V to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +5.0V, V_L = +3.3V and T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (EN, S00, S01, S10, S11, SHA, SHB, SVA, SVB)						
Input Threshold Low	V_{IL}	+2.3V ≤ V_L ≤ V_{CC}	0.25 x V_L			V
Input Threshold High	V_{IH}	+3.3V ≤ V_L ≤ V_{CC}			0.55 x V_L	V
		+2.3V ≤ V_L ≤ +3.3V			0.6 x V_L	
Input Hysteresis	V_{HYST}	+2.3V ≤ V_L ≤ V_{CC}		100		mV
V_L Pulldown Resistor		Resistor to V_L (EN, S00, S01, S10, S11, SHA, SHB, SVA, SVB)		100		kΩ
Enable Time	t_{EN}	R_L = 2.2kΩ, C_L = 10pF, Figure 1 (EN)		1		µs
Select Time	t_{SEL}	R_L = 2.2kΩ, C_L = 10pF, Figure 1 (S00, S01, S10, S11)		1		µs
DIGITAL OUTPUTS (SH1, SV1, SH2, SV2)						
Output-Voltage Low	V_{OL}	I_{OUT} = +10mA, V_{CC} = +4.5V			0.6	V
Output-Voltage High	V_{OH}	I_{OUT} = -10mA, V_{CC} = +4.5V	3			V
Rise/Fall Time	$t_{R/F}$	R_L = 2.2kΩ, C_L = 10pF, Figure 2 (Note 3)		2	4	ns
RGB AC PERFORMANCE						
Bandwidth	f_{BW}	R_S = R_L = 50Ω		700		MHz
On-Loss		f = 10MHz, R_S = R_L = 50Ω, 0V ≤ V_{BIAS} ≤ +0.7V, Figure 3		0.7		dB
Crosstalk (RED_, GRN_, BLU_)		R_S = R_L = 50Ω, f = 50MHz, Figure 3		-40		dB
Off-Capacitance	C_{OFF}	V_{EN} = 0V, RED_, GRN_, BLU_ to GND, f = 1MHz, REDA/REDB to RED1/RED2, GRNA/GRNB to GRN1/GRN2, BLUA/BLUB to BLU1/BLU2		3.5		pF
On-Capacitance	C_{ON}	f = 1MHz, REDA/REDB to RED1/RED2, GRNA/GRNB to GRN1/GRN2, BLUA/BLUB to BLU1/BLU2 (Note 3)		10	12	pF
ESD PROTECTION						
RED1, GRN1, BLU1, RED2, GRN2, BLU2, SDA1, SCL1, SDA2, SCL2, SH1, SV1, SH2, SV2		HBM (Note 4)		±15		kV
		IEC 61000-4-2 Contact Discharge (Note 4)		±6		
All Other Terminals		HBM		±2		kV

Note 2: The device is 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and not production tested.

Note 3: Guaranteed by design. Not production tested.

Note 4: Tested terminal to GND, 1µF bypass capacitors on V_{CC} and V_L.

Low-Capacitance VGA 2:2 Dual-Graphics Crossover Switch

Test Circuits/Timing Diagrams

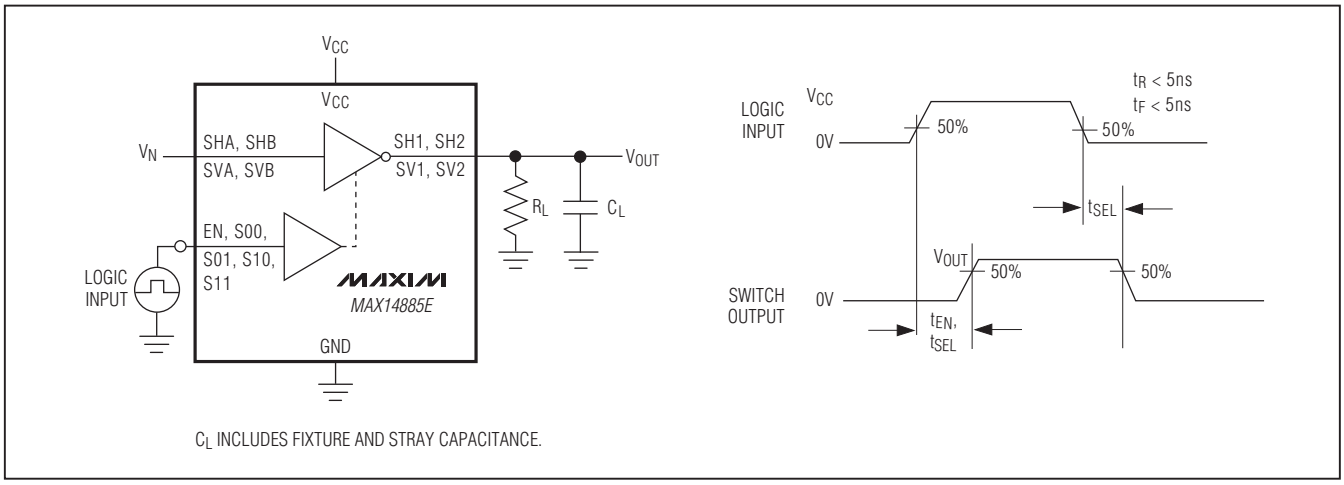


Figure 1. Enable/Select Time

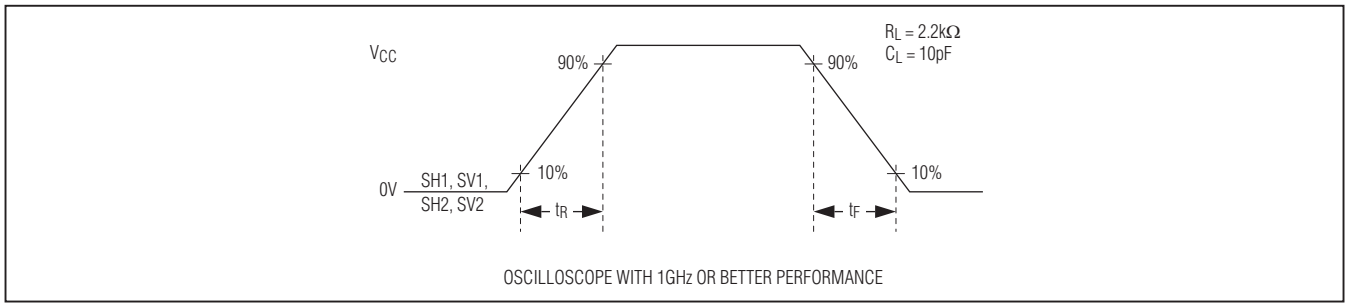


Figure 2. Rise/Fall Time

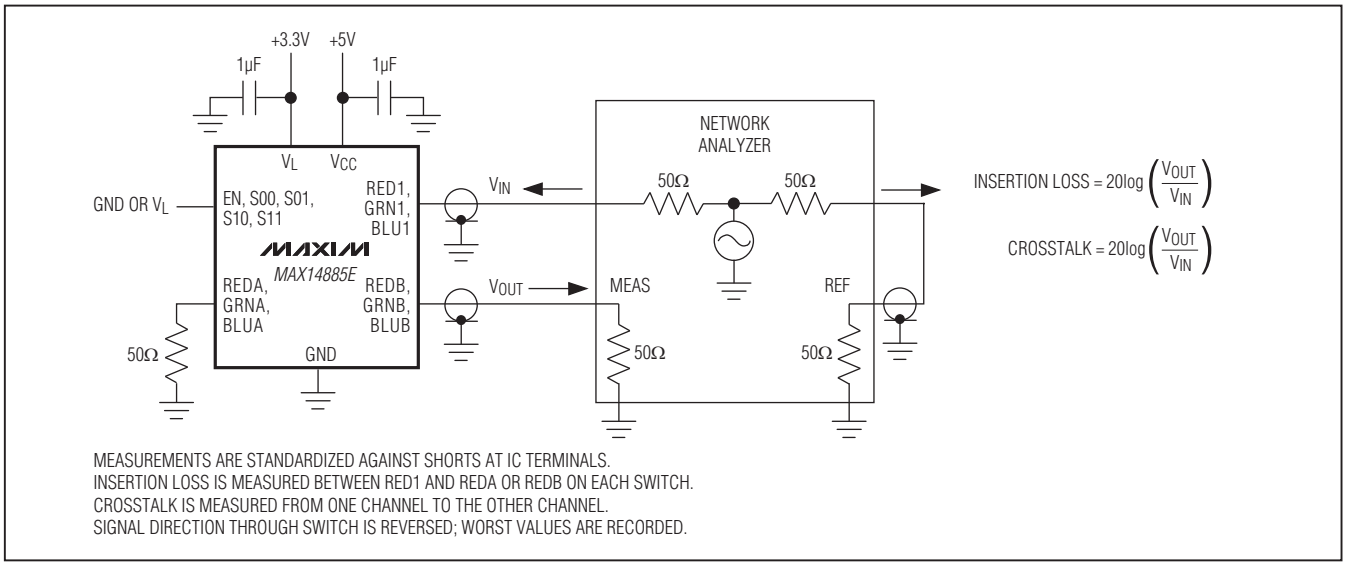
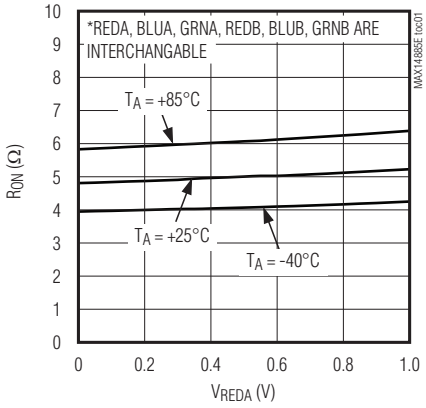


Figure 3. Insertion Loss and Crosstalk

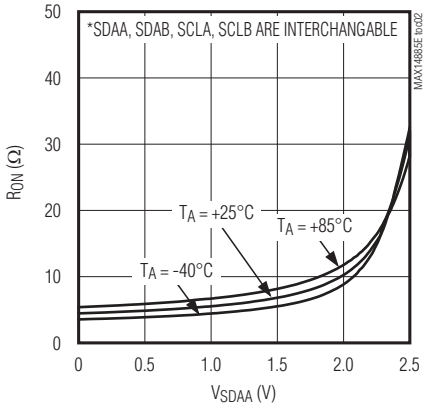
Typical Operating Characteristics

(V_{CC} = +5.0V, V_L = +3.3V, T_A = +25°C, unless otherwise noted.)

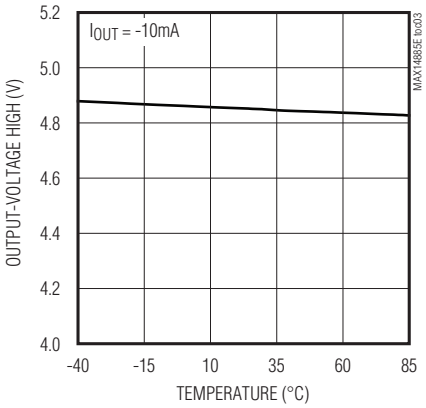
RON vs. VREDA* (RGB SWITCHES)



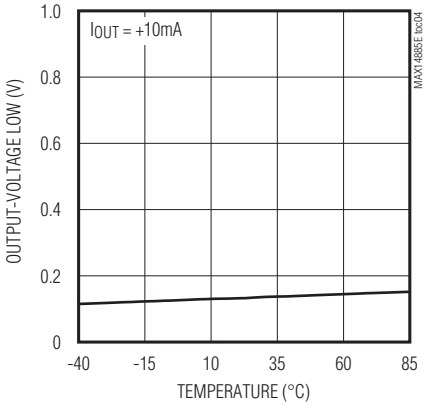
RON vs. VSDAA* (DDC SWITCHES)



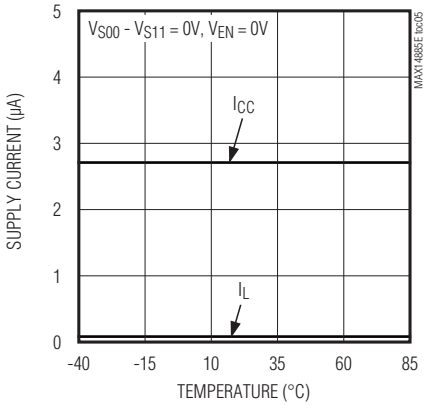
HV BUFFER OUTPUT-VOLTAGE HIGH vs. TEMPERATURE



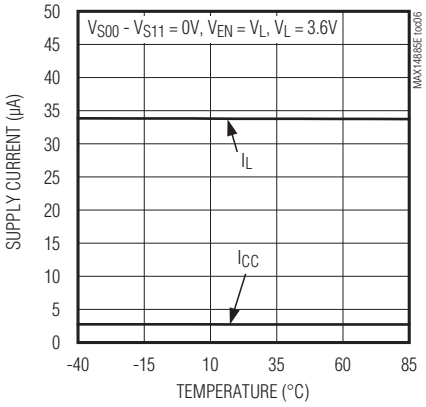
HV BUFFER OUTPUT-VOLTAGE LOW vs. TEMPERATURE



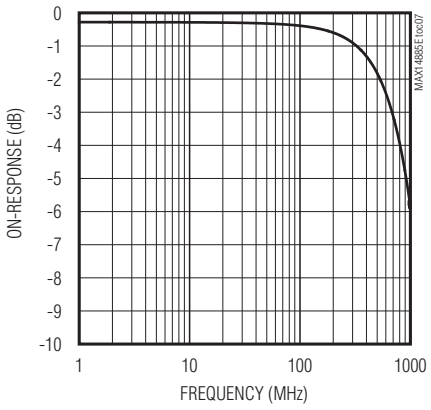
SUPPLY CURRENT vs. TEMPERATURE



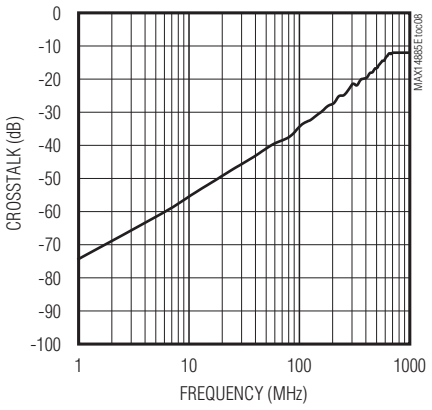
SUPPLY CURRENT vs. TEMPERATURE



ON-RESPONSE vs. FREQUENCY

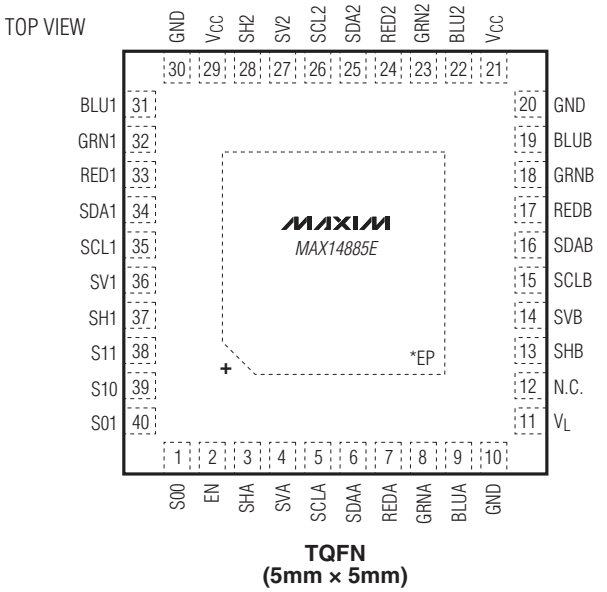


CROSSTALK vs. FREQUENCY



Low-Capacitance VGA 2:2 Dual-Graphics Crossover Switch

Pin Configuration



TQFN
(5mm × 5mm)

*CONNECT EP TO GND.

Pin Description

PIN	NAME	FUNCTION
1	S00	Select Input. S00 selects SDA_ and SCL_ signal path (see Table 1).
2	EN	Enable Input. Drive EN high for normal operation. Drive EN low to disable the device (all switch outputs in three-state and SH1, SH2, SV1, and SV2 are low).
3	SHA	Horizontal Sync Input 1
4	SVA	Vertical Sync Input 1
5	SCLA	DDC Clock Input 1
6	SDAA	DDC Data Input 1
7	REDA	RGB Red Input 1
8	GRNA	RGB Green Input 1
9	BLUA	RGB Blue Input 1
10, 20, 30	GND	Ground
11	V_L	Supply Voltage. $+2.3V \le V_L \le V_{CC}$. Bypass V_L to GND with a 1µF or larger ceramic capacitor as close to the device as possible.
12	N.C.	No Connection. Connect N.C. to GND or leave unconnected.
13	SHB	Horizontal Sync Input 2
14	SVB	Vertical Sync Input 2
15	SCLB	DDC Clock Input 2
16	SDAB	DDC Data Input 2

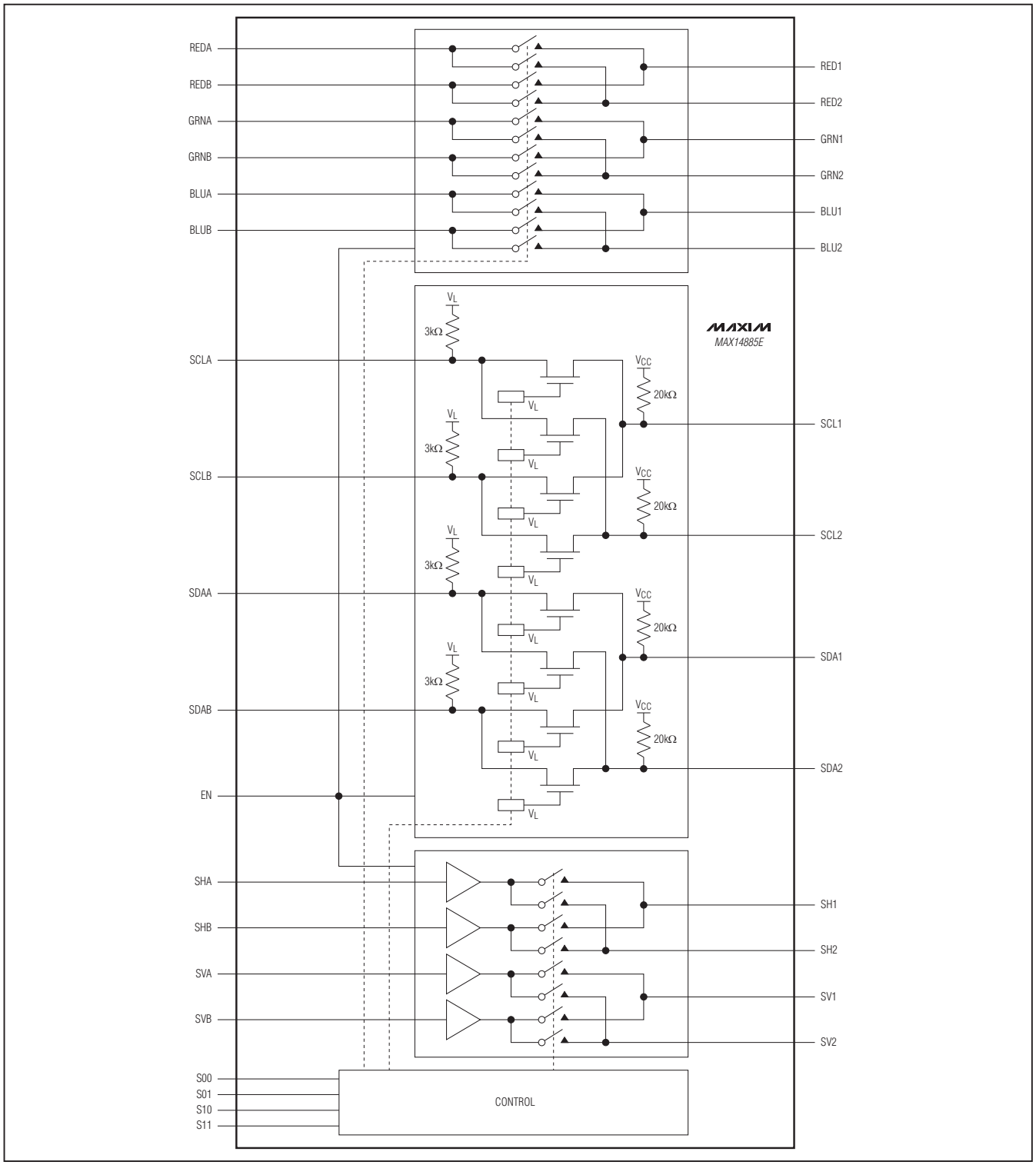
Pin Description (continued)

PIN	NAME	FUNCTION
17	REDB	RGB Red Input 2
18	GRNB	RGB Green Input 2
19	BLUB	RGB Blue Input 2
21, 29	V_{CC}	Supply Voltage. V_{CC} = +5.0V ±10%. Bypass V_{CC} to GND with a 1µF or larger ceramic capacitor as close to the device as possible.
22	BLU2	RGB Blue Output 2*
23	GRN2	RGB Green Output 2*
24	RED2	RGB Red Output 2*
25	SDA2	DDC Data Output 2*
26	SCL2	DDC Clock Output 2*
27	SV2	Vertical Sync Output 2*
28	SH2	Horizontal Sync Output 2*
31	BLU1	RGB Blue Output 1*
32	GRN1	RGB Green Output 1*
33	RED1	RGB Red Output 1*
34	SDA1	DDC Data Output 1*
35	SCL1	DDC Clock Output 1*
36	SV1	Vertical Sync Output 1*
37	SH1	Horizontal Sync Output 1*
38	S11	Select Input. S11 selects RED_, GRN_, BLU_, SH_ and SV_ signal path (see Table 2).
39	S10	Select Input. S10 selects RED_, GRN_, BLU_, SH_ and SV_ signal path (see Table 2).
40	S01	Select Input. S01 selects SDA_ and SCL_ signal path (see Table 1).
—	EP	Exposed Pad. Connect EP to GND. Do not use EP as a sole ground connection.

**Terminal with ±15kV Human Body Model (HBM) and ±6kV IEC 61000-4-2 Contact Discharge protection.*

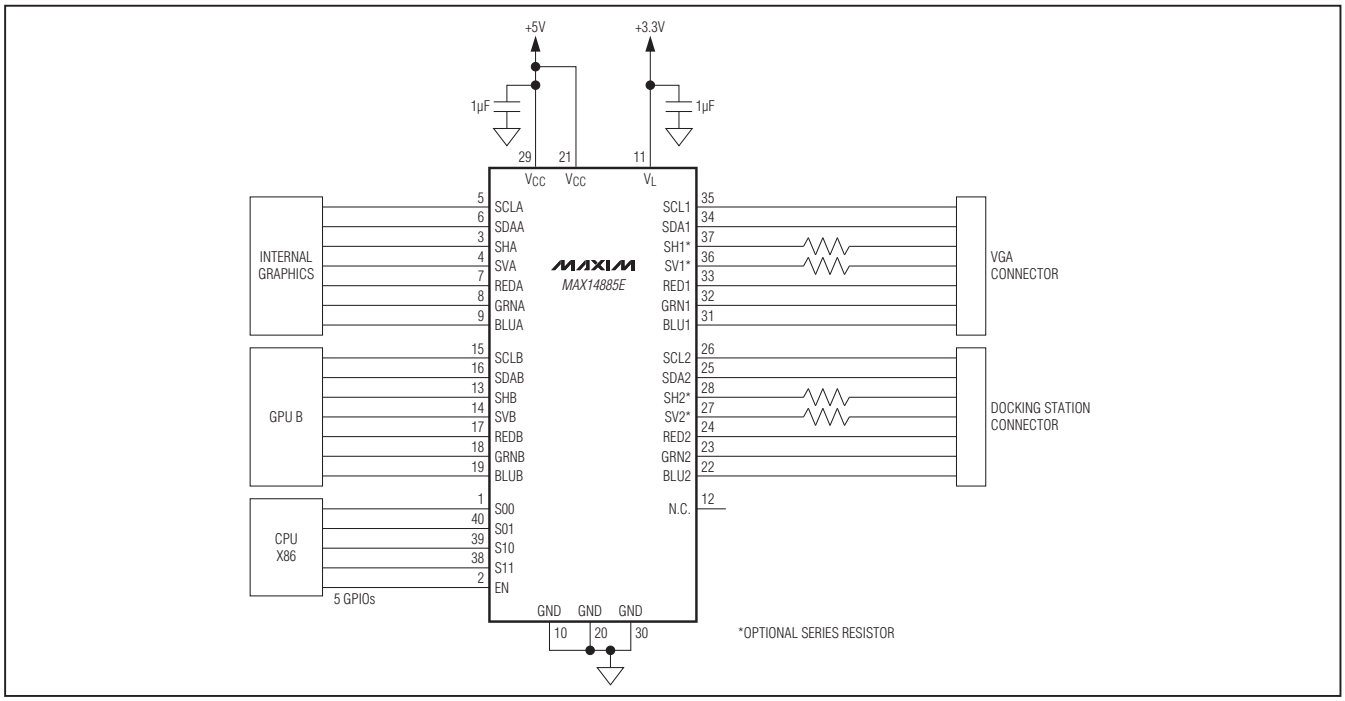
Low-Capacitance VGA 2:2 Dual-Graphics Crossover Switch

Functional Diagram



Low-Capacitance VGA 2:2 Dual-Graphics Crossover Switch

Typical Operating Circuit



Detailed Description

The MAX14885E integrates high-bandwidth analog switches and level-translating buffers to implement a complete 2:2 dual-graphics crossover function for VGA signals. The device provides switching for RGB, HSYNC, VSYNC, SDA, and SCL signals—all signals required in notebook VGA switching applications. The MAX14885E permits the system to select between internal standard graphics and add-in graphics (MXM or other) to be routed to either the VGA port on the laptop or to the connector on the docking station.

The HSYNC and VSYNC inputs feature level-shifting buffers to support 5V TTL output logic levels from low-voltage graphics controllers. These buffered switches can be driven from +2.3V up to V_L. RGB signals are routed with high-performance analog switches. SDA_ and SCL_ are DDC signals with pullups to their respective voltages. The MAX14885E translates the low-voltage SH_, SV_ signals to 5V TTL-level compatible signals, protecting the low voltage GPU from potentially harmful levels present in a monitor.

Drive EN logic-low to shut down the MAX14885E. In shutdown mode, all switches are high impedance, providing high signal rejection. Four select inputs are provided to individually select groups of switches. The RGB, HSYNC, and VSYNC signals are controlled by S11 and S10. The SDA and SCL signals are controlled by S01 and S00.

RGB Switches

The MAX14885E provides 12 SPST high-bandwidth switches to route standard VGA red, green, and blue signals (Table 2). The RED_, GRN_, and BLU_ analog switches are identical, and any of the three switches can be used to route red, green, or blue video signals. The RED1, RED2, GRN1, GRN2, BLU1, and BLU2 outputs are ESD protected to ±15kV HBM and ±6kV IEC 61000-4-2 Contact Discharge.

Horizontal/Vertical Sync Level Shifter

The SHA, SHB, SVA, and SVB inputs are buffered to provide level-shifting and drive capability for horizontal/vertical sync signals that meet the VESA specification. The SH_ and SV_ level shifters are identical, and each level shifter can be used for either horizontal or vertical signals. The SH1, SH2, SV1, and SV2 outputs are ESD protected to ±15kV HBM and ±6kV IEC 61000-4-2 Contact Discharge. Because of the high-speed nature of S and V buffers, users may add small series resistors (e.g., 25Ω). See the *Typical Operating Circuit*.

Low-Capacitance VGA 2:2 Dual-Graphics Crossover Switch

Display Data Channel Switches (DDC)

The MAX14885E provides four logic-level translating switches to route DDC signals (Table 1). V_L is normally set to +3.3V to provide logic shifting for VESA DDC (I^2C)-compatible signals. The MAX14885E protects the low-voltage graphics controller from +5V that presents itself in VESA-compatible monitors. The SDA_ and SCL_ switches are identical, and each switch can be used to route either SDA or SCL signals. The SDA1, SDA2, SCL1, and SCL2 outputs are ESD protected to ±15kV HBM and ±6kV IEC 61000-4-2 Contact Discharge. These outputs are pulled up to V_{CC} internally by 20kΩ resistors. Users can elect to parallel these resistors to achieve higher drive, if necessary.

Table 1. DDC Truth Table

EN	S01	S00	FUNCTION
0	X	X	All switches high impedance
1	0	0	SDAA to SDA1 SCLA to SCL1
1	0	1	SDAB to SDA1 SCLB to SCL1
1	1	0	SDAA to SDA2 SCLA to SCL2
1	1	1	SDAB to SDA2 SCLB to SCL2

X = Don't care.

Table 2. RGB/HSYNC, VSYNC Truth Table

EN	S11	S10	FUNCTION	
0	X	X	All switches high impedance and V_{SH1}, V_{SH2}, V_{SV1}, V_{SV2} = 0V	
1	0	0	REDA to RED1 GRNA to GRN1 BLUA to BLU1	SHA to SH1 SVA to SV1
1	0	1	REDB to RED1 GRNB to GRN1 BLUB to BLU1	SHB to SH1 SVB to SV1
1	1	0	REDA to RED2 GRNA to GRN2 BLUA to BLU2	SHA to SH2 SVA to SV2
1	1	1	REDB to RED2 GRNB to GRN2 BLUB to BLU2	SHB to SH2 SVB to SV2

X = Don't care.

ESD Protection

As with all Maxim devices, ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. Additionally, the RED1, RED2, GRN1, GRN2, BLU1, BLU2, SH1, SH2, SV1, SV2, SDA1, SDA2, SCL1, and SCL2 terminals of the MAX14885E are designed for protection to the following limits:

- ±15kV using the HBM
- ±6kV using the Contact Discharge Method specified in IEC 61000-4-2

For optimum ESD performance, bypass V_{CC} and V_L pins to ground with 1µF or larger ceramic capacitors as close as possible to these supply pins.

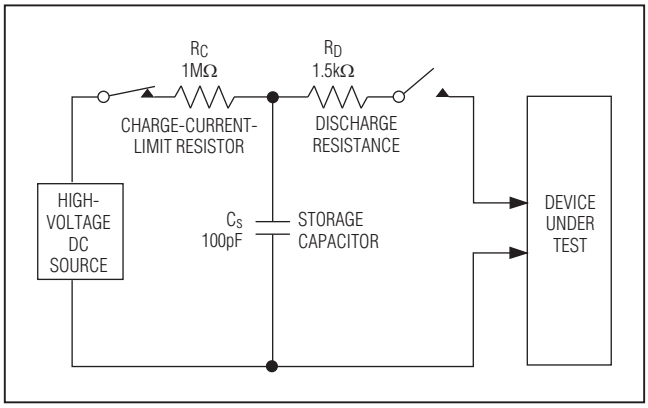


Figure 4. Human Body ESD Test Model

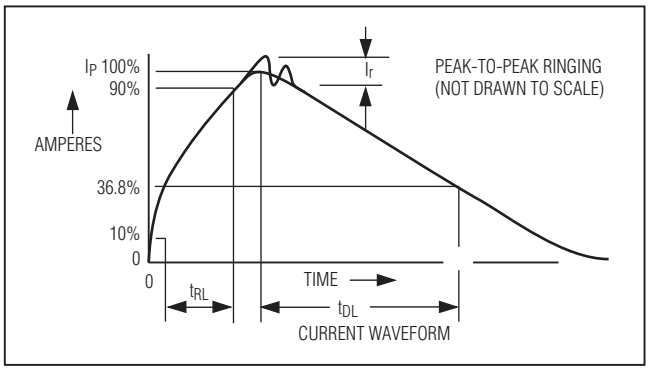


Figure 5. Human Body Current Waveform

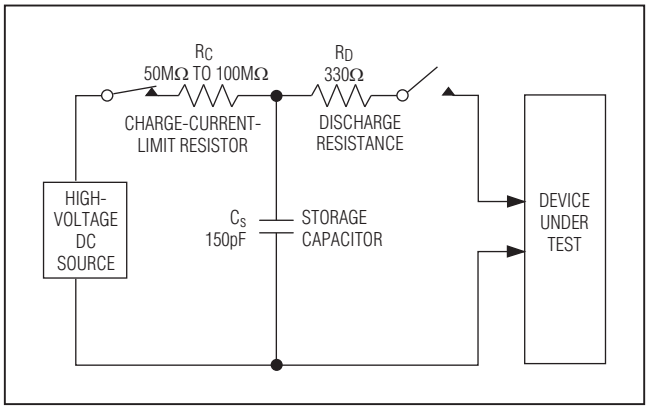


Figure 6. IEC 61000-4-2 ESD Test Model

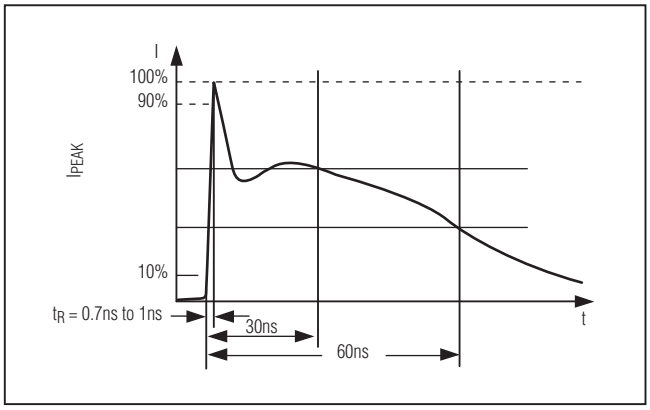


Figure 7. IEC 61000-4-2 ESD Generator Current Waveform

Human Body Model (HBM)

Figure 4 shows the HBM, and Figure 5 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. The MAX14885E helps users design equipment that meets Level 4 of IEC 61000-4-2. The main difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 6), the ESD-withstand voltage measured to this standard is generally lower than that measured using the HBM. Figure 7 shows the current waveform for the ±6kV IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge Method connects the probe to the device before the probe is energized.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report test setup, methodology, and results.

Applications Information

The MAX14885E provides the switching and level-shifting necessary to drive a standard VGA port from either an internal graphics controller or an add-in module (MXM or GPU). The RGB signals are switched through the 12 low-capacitance SPST switches, and internal buffers drive the HSYNC and VSYNC signals to VGA standard 5V TTL levels. The DDC switches provide level shifting. Connect V_L to +3.3V for normal operation. See the *Typical Application Circuit*.

Power-Supply Decoupling and Sequencing

Bypass each V_{CC} and V_L terminals to ground with a 1µF or larger ceramic capacitor as close as possible to the device. Refer to Application Note 5314: *Power Sequencing the MAX14885E VGA Crossover Switch* for guidance on power sequencing of the V_L and V_{CC} power rails.

PCB Layout

High-speed switches such as the MAX14885E require proper PCB layout for optimum performance. Ensure that impedance-controlled PCB traces for high-speed signals are matched in length and as short as possible. Connect the exposed pad to ground.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4055+1	21-0140	90-0016

Low-Capacitance VGA 2:2 Dual-Graphics Crossover Switch

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/10	Initial release	—
1	1/12	Updated *Power-Supply Decoupling and Sequencing* section to reference Application Note 5314	11

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