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### P-Channel 1.8V Specified PowerTrench<sup>®</sup> MOSFET

#### **General Description**

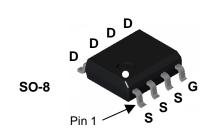
This P-Channel 1.8V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (1.8V - 8V).

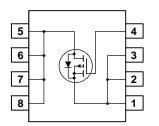
#### Applications

- Power management
- Load switch
- Battery protection

#### Features

- -13.5 A, -20 V.  $R_{DS(ON)} = 8.5 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$  $R_{DS(ON)} = 10.5 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$  $R_{DS(ON)} = 14 \text{ m}\Omega @ V_{GS} = -1.8 \text{ V}$
- Fast switching speed
- High performance trench technology for extremely low  $R_{\text{DS}(\text{ON})}$
- High current and power handling capability





#### Absolute Maximum Ratings TA=25°C unless otherwise noted

Symbol		Parameter		Ratings	Units	
V <sub>DSS</sub>	Drain-Source	ce Voltage		-20	V	
V <sub>GSS</sub>	Gate-Sourc	e Voltage		±8	V	
D	Drain Curre	nt – Continuous	(Note 1a)	-13.5	A	
		– Pulsed		-50		
P <sub>D</sub>	Power Dissipation for Single Operation		n (Note 1a)	2.5	W	
			(Note 1b)	1.5		
			(Note 1c)	1.2		
Г <sub>Ј</sub> , Т <sub>STG</sub>	Operating and Storage Junction Temperature Range		perature Range	-55 to +175	°C	
Therma	I Charac	teristics				
$R_{ ext{ hetaJA}}$	Thermal Resistance, Junction-to-Ambient		Dient (Note 1a)	50	°C/W	
R <sub>eja</sub>	Thermal Resistance, Junction-to-Ambient		Dient (Note 1c)	125	°C/W	
R <sup>θJC</sup>	Thermal Resistance, Junction-to-Case		e (Note 1)	25	°C/W	
	e Markin	g and Ordering I	Information			
Раскад						
•	Marking	Device	Reel Size	Tape width	Quantity	

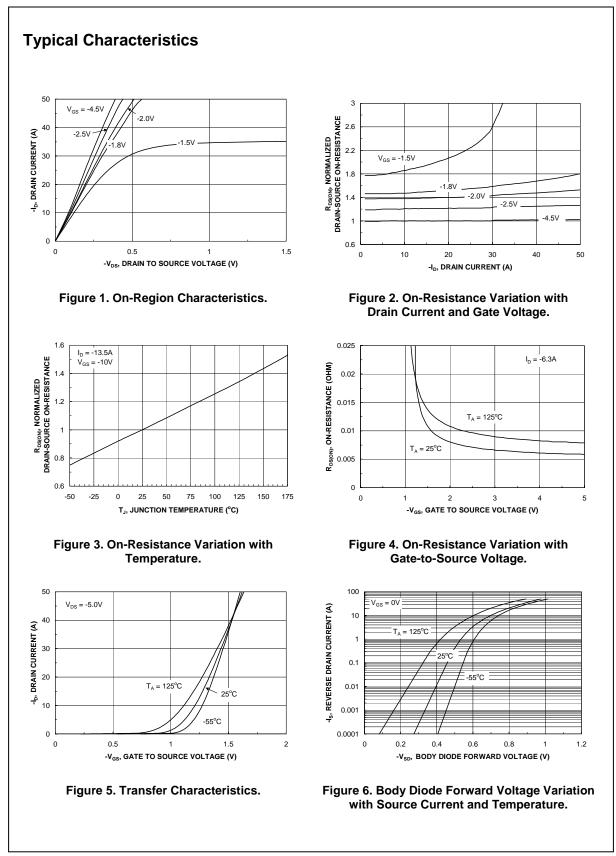
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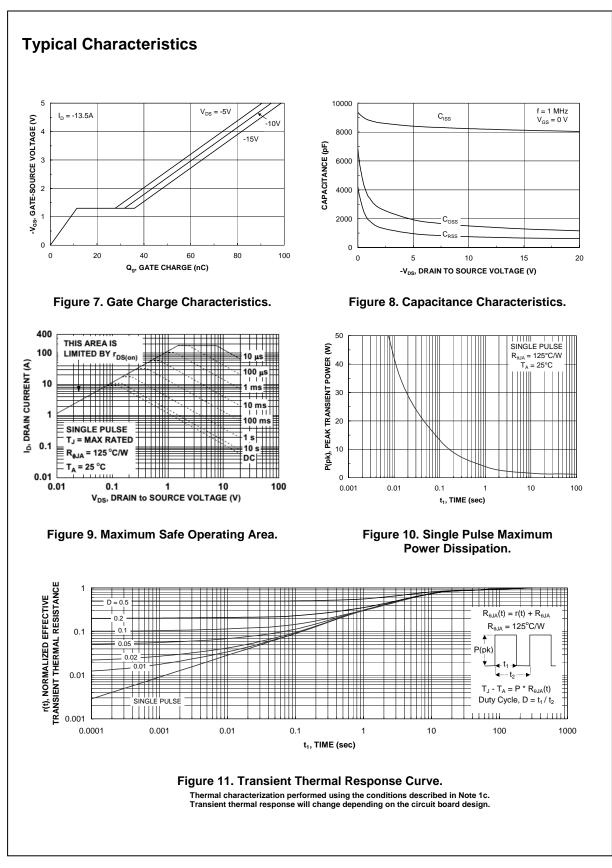
# FDS4465

September 2014

	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics				•	
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 V, I_D = -250 \mu A$	-20			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = -250 \ \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$		-12		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V},  V_{GS} = 0 \text{ V}$			-1	μA
I <sub>GSSF</sub>	Gate–Body Leakage, Forward	$V_{GS} = 8 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
I <sub>GSSR</sub>	Gate–Body Leakage, Reverse	$V_{GS} = -8 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	-0.4	-0.6	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \ \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$		3		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$ \begin{array}{l} V_{GS}=-4.5 \ V,  I_D=-13.5 \ A \\ V_{GS}=-2.5 \ V,  I_D=-12 \ A \\ V_{GS}=-1.8 \ V,  I_D=-10.5 \ A \\ V_{GS}=-4.5 \ V, \ I_D=-13.5A, \ T_J=125^\circ C \end{array} $		6.7 8.0 9.8 9.0	8.5 10.5 14 13	mΩ
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = -4.5 V$ , $V_{DS} = -5 V$	-50			Α
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5 V$ , $I_D = -13.5 A$		70		S
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -10 V$ , $V_{GS} = 0 V$ ,		8237		pF
Coss	Output Capacitance	f = 1.0  MHz		1497		, pF
C <sub>rss</sub>	Reverse Transfer Capacitance			750		pF
R <sub>g</sub>	Gate Resistance		0.1	3.0	6.0	Ω
-	g Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = -10V, \qquad I_D = -1 A,$		20	36	ns
t <sub>r</sub>	Turn–On Rise Time	$V_{\text{GS}} = -4.5 \text{ V}, \qquad R_{\text{GEN}} = 6 \Omega$		24	38	ns
t <sub>d(off)</sub>	Turn–Off Delay Time	-		300	480	ns
t <sub>f</sub>	Turn–Off Fall Time			140	224	ns
Qg	Total Gate Charge	$V_{DS} = -10 \text{ V}, \qquad I_D = -13.5 \text{ A},$		86	120	nC
Q <sub>qs</sub>	Gate–Source Charge	$V_{GS} = -4.5 V$		20	-	nC
Q <sub>gd</sub>	Gate–Drain Charge	1		11		nC
-	ource Diode Characteristics	and Maximum Patings	1	1	1	1
ls	Maximum Continuous Drain–Source				-2.1	А
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_S = -2.1 \text{ A}  (\text{Note 2})$		-0.6	-1.2	V

**2.** Pulse Test: Pulse Width < 300 $\mu$ s, Duty Cycle < 2.0%







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