FAIRCHILD™

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD

FDS4465

P-Channel 1.8V Specified PowerTrench® MOSFET

General Description

This P-Channel 1.8V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (1.8V – 8V).

Applications

- Power management
- Load switch
- Battery protection

Features

- −13.5 A, −20 V. $R_{DS(ON)}$ = 8.5 mΩ @ V_{GS} = −4.5 V
  $R_{DS(ON)}$ = 10.5 mΩ @ V_{GS} = −2.5 V
  $R_{DS(ON)}$ = 14 mΩ @ V_{GS} = −1.8 V

- Fast switching speed

- High performance trench technology for extremely low $R_{DS(ON)}$

- High current and power handling capability

SO-8

Pin 1
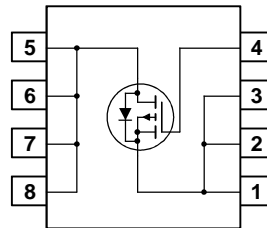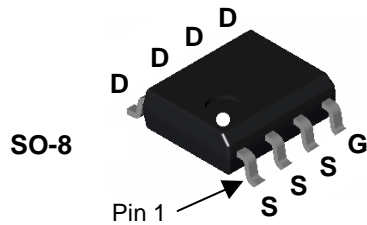
Absolute Maximum Ratings
T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		−20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current – Continuous	(Note 1a)	−13.5	A
	– Pulsed		−50	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.5	
		(Note 1c)	1.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +175	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	125	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS4465	FDS4465	13''	12mm	2500 units

Electrical Characteristics $T_A = 25°C$ unless otherwise noted

| Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = -250$ µA	−20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250$ µA, Referenced to 25°C		−12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16$ V, $V_{GS} = 0$ V			−1	µA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 8$ V, $V_{DS} = 0$ V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -8$ V, $V_{DS} = 0$ V			−100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250$ µA	−0.4	−0.6	−1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250$ µA, Referenced to 25°C		3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5$ V, $I_D = -13.5$ A		6.7	8.5	mΩ
		$V_{GS} = -2.5$ V, $I_D = -12$ A		8.0	10.5	
		$V_{GS} = -1.8$ V, $I_D = -10.5$ A		9.8	14	
		$V_{GS}=-4.5$ V, $I_D =-13.5$A, T_J=125°C		9.0	13	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5$ V, $V_{DS} = -5$ V	−50			A
g_{FS}	Forward Transconductance	$V_{DS} = -5$ V, $I_D = -13.5$ A		70		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -10$ V, $V_{GS} = 0$ V,		8237		pF
C_{oss}	Output Capacitance	f = 1.0 MHz		1497		pF
C_{rss}	Reverse Transfer Capacitance			750		pF
R_g	Gate Resistance		0.1	3.0	6.0	Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -10$V, $I_D = -1$ A,		20	36	ns
t_r	Turn–On Rise Time	$V_{GS} = -4.5$ V, $R_{GEN} = 6$ Ω		24	38	ns
$t_{d(off)}$	Turn–Off Delay Time			300	480	ns
t_f	Turn–Off Fall Time			140	224	ns
Q_g	Total Gate Charge	$V_{DS} = -10$ V, $I_D = -13.5$ A,		86	120	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = -4.5$ V		20		nC
Q_{gd}	Gate–Drain Charge			11		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				−2.1	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = -2.1$ A (Note 2)		−0.6	−1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
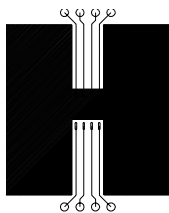
a) 50 °C/W when mounted on a 1in² pad of 2 oz copper
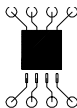
b) 105 °C/W when mounted on a .04 in² pad of 2 oz copper
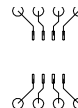
c) 125 °C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

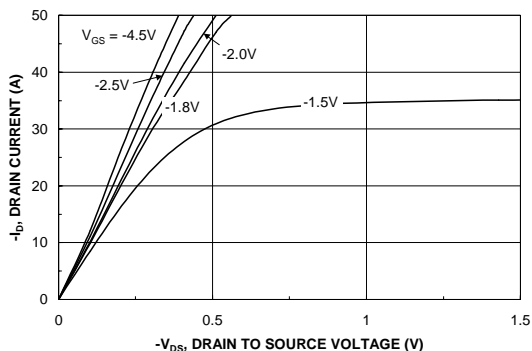## Typical Characteristics

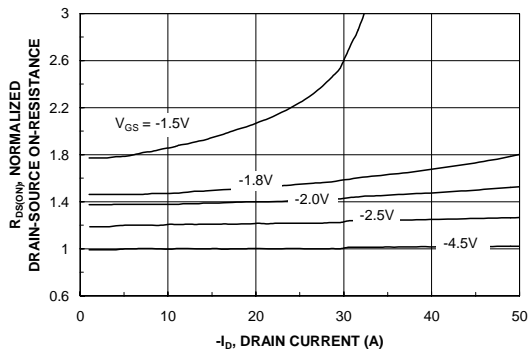**Figure 1. On-Region Characteristics.**

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.
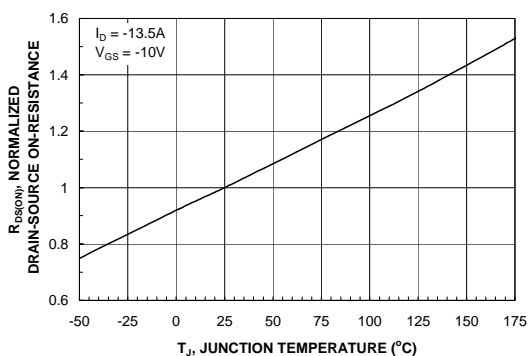

Figure 3. On-Resistance Variation with Temperature.
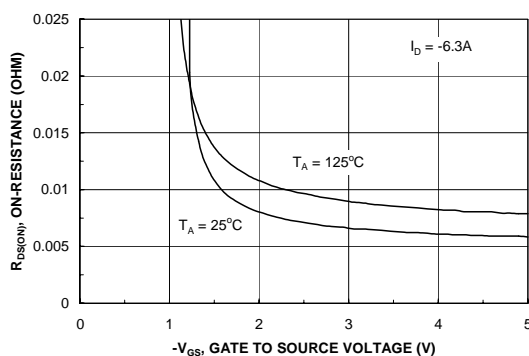

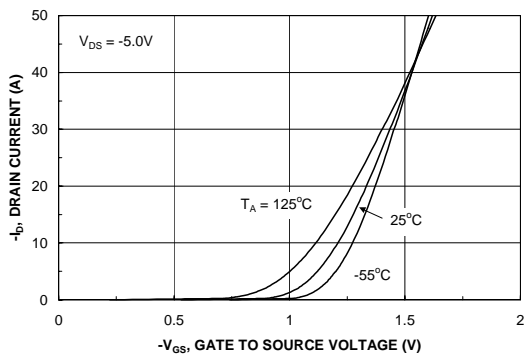**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**
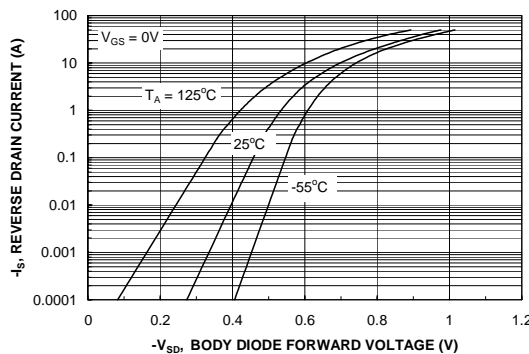

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.
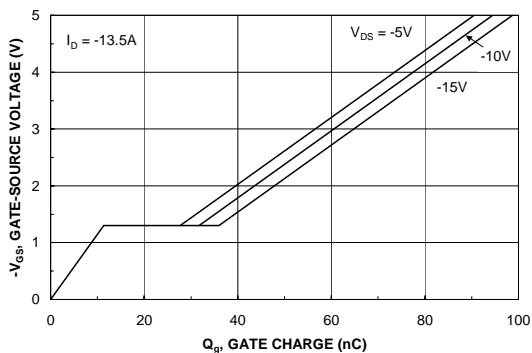
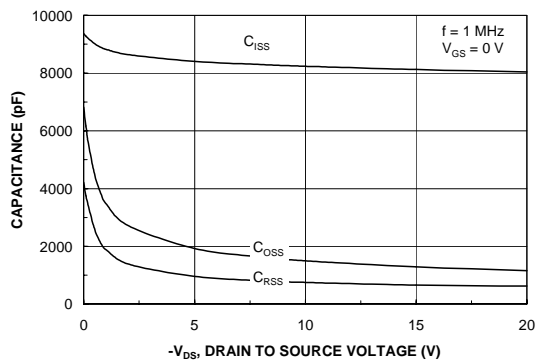## Typical Characteristics

Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.
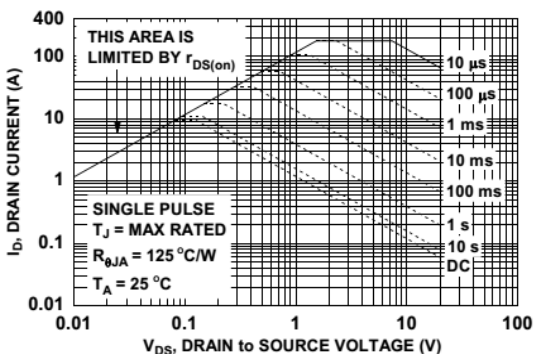
Figure 9. Maximum Safe Operating Area.
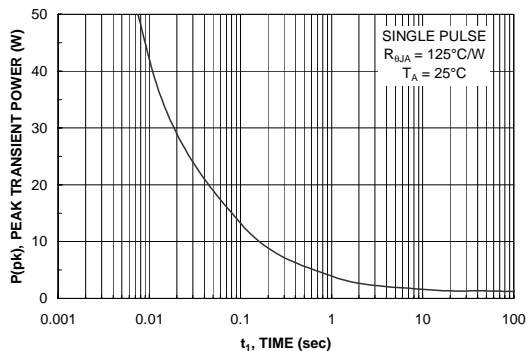
Figure 10. Single Pulse Maximum Power Dissipation.
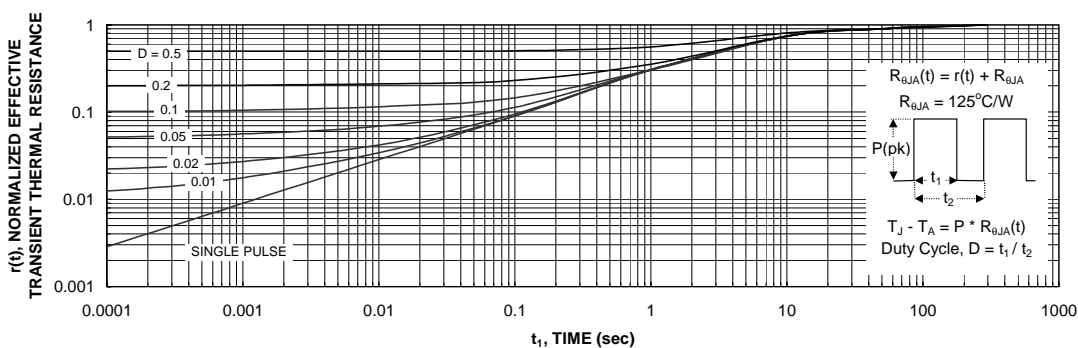
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in **Note 1c.**
Transient thermal response will change depending on the circuit board design.

4.90±0.10 | A

(0.635)

8 | 5 | B

6.00±0.20

3.90±0.10

PIN ONE
INDICATOR

1 | 4

1.27

⊕ | 0.25Ⓜ | C | B | A

0.65

1.75

5.60

1.27

LAND PATTERN RECOMMENDATION

0.175±0.075

1.75 MAX

0.42±0.09

⌒ | 0.10

SEE DETAIL A

0.22±0.03

OPTION A - BEVEL EDGE

OPTION B - NO BEVEL EDGE

(0.86) x 45°

R0.10

GAGE PLANE

R0.10

0.36

8°
0°

SEATING PLANE

0.65±0.25

(1.04)

DETAIL A
SCALE: 2:1
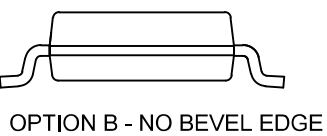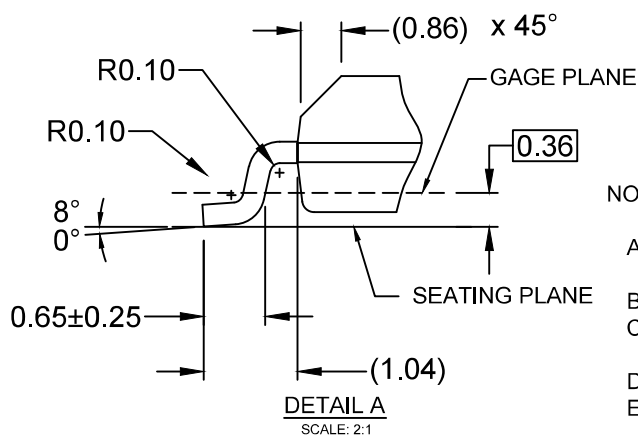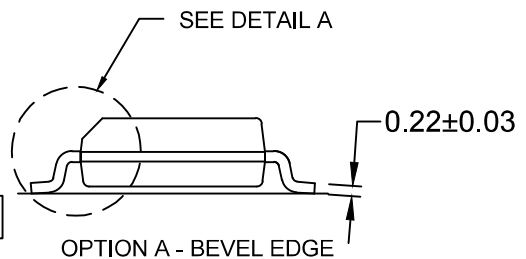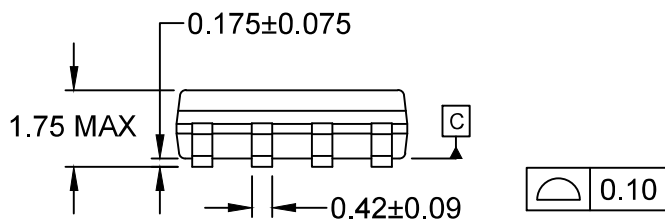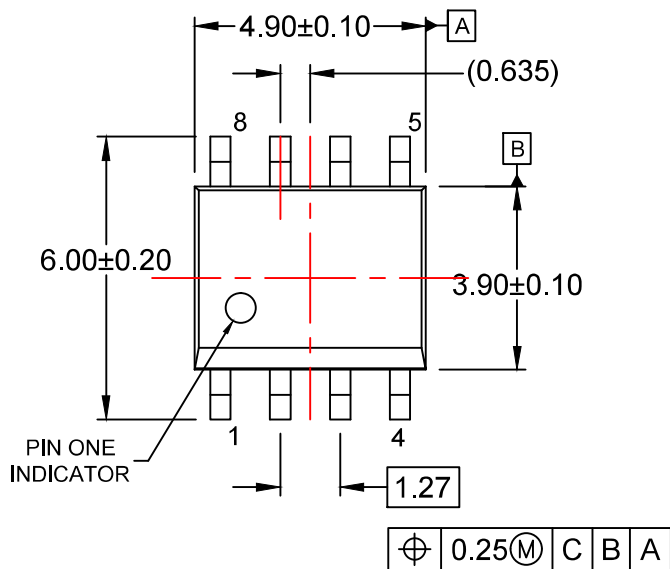
NOTES:

A) THIS PACKAGE CONFORMS TO JEDEC
   MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD
   FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M
E) DRAWING FILENAME: M08Arev16

FAIRCHILD.

PUBLICATION ORDERING INFORMATION

© Semiconductor Components Industries, LLC

www.onsemi.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#):
  [FDS4465](#)