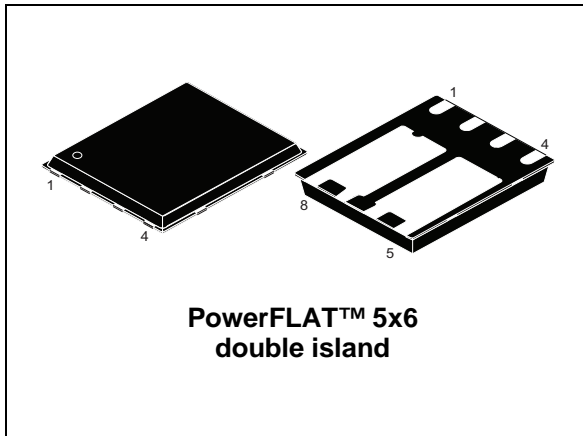
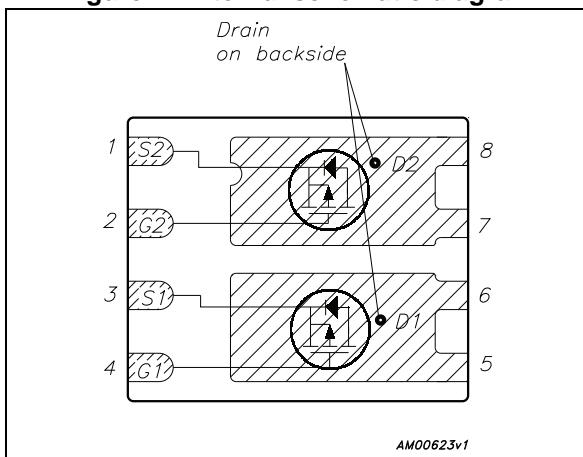


## Dual P-channel 100 V, 0.136 $\Omega$ typ., 3.3 A STripFET™ VI DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 double island

Datasheet - production data



**Figure 1. Internal schematic diagram**



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL13DP10F6	100 V	0.18 $\Omega$	3.3 A

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- High avalanche ruggedness
- Low gate drive power losses

### Applications

- Switching applications

### Description

This device is a dual P-channel Power MOSFET developed using the 6<sup>th</sup> generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages.

**Table 1. Device summary**

Order code	Marking	Packages	Packaging
STL13DP10F6	13DP10F6	PowerFLAT™ 5x6 double island	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	13	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	7.3	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25^\circ\text{C}$	3.3	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb}=100^\circ\text{C}$	2	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	13.2	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	62.5	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25^\circ\text{C}$	4	W
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according  $R_{thj-c}$
2. The value is rated according  $R_{thj-pcb}$
3. Pulse width limited by safe operating area

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	32	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec

*Note: For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.*

## 2 Electrical characteristics

( $T_{CASE}=25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS}=0, I_D=250\text{ }\mu\text{A}$	100			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS}=0, V_{DS}=100\text{ V}$			1	$\mu\text{A}$
		$V_{GS}=0, V_{DS}=100\text{ V}, T_C=125\text{ }^{\circ}\text{C}$			10	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS}=0, V_{GS}=\pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS}=10\text{ V}, I_D=1.7\text{ A}$		0.136	0.18	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS}=25\text{ V}, f=1\text{ MHz}, V_{GS}=0$	-	864	-	pF
$C_{oss}$	Output capacitance		-	45	-	pF
$C_{rss}$	Reverse transfer capacitance		-	25	-	pF
$Q_g$	Total gate charge	$V_{DD}=50\text{ V}, I_D=3.3\text{ A}$	-	16.5	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS}=10\text{ V}$	-	3.5	-	nC
$Q_{gd}$	Gate-drain charge	(see <a href="#">Figure 14</a> )	-	3.8	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=50\text{ V}, I_D=1.7\text{ A}, R_G=4.7\text{ }\Omega, V_{GS}=10\text{ V}$ (see <a href="#">Figure 13</a> )	-	10.5	-	ns
$t_r$	Rise time		-	4.8	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
$t_f$	Fall time		-	4.5	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		3.3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		13.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3.3 \text{ A}$ , $V_{GS} = 0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 3.3 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 80 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$	-	26.5		ns
$Q_{rr}$	Reverse recovery charge		-	36.5		nC
$I_{RRM}$	Reverse recovery current		-	2.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

*Note:* For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

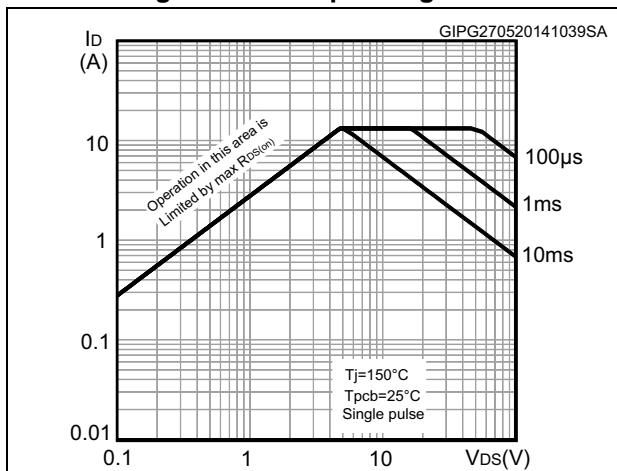


Figure 3. Thermal impedance

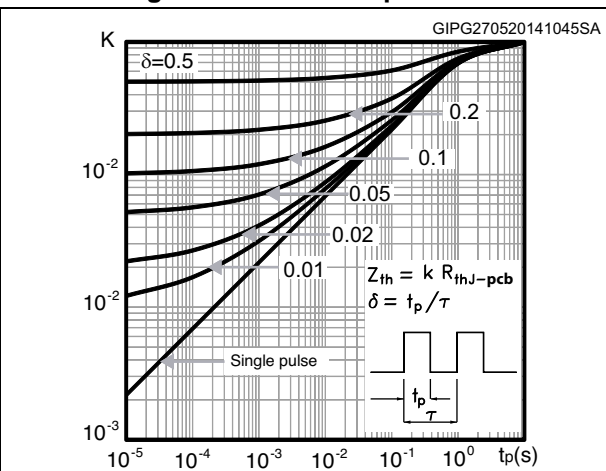


Figure 4. Output characteristics

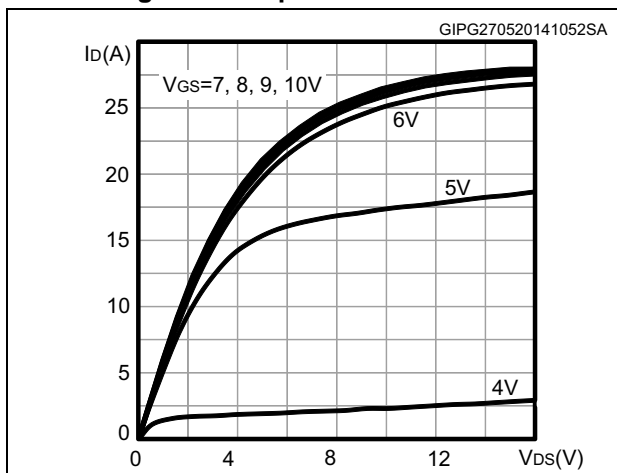


Figure 5. Transfer characteristics

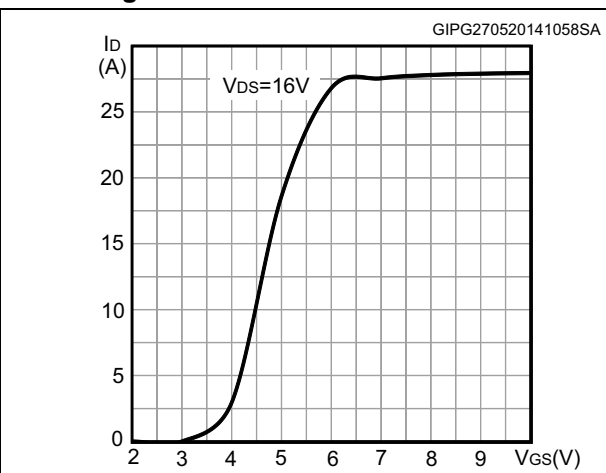


Figure 6. Gate charge vs gate-source voltage

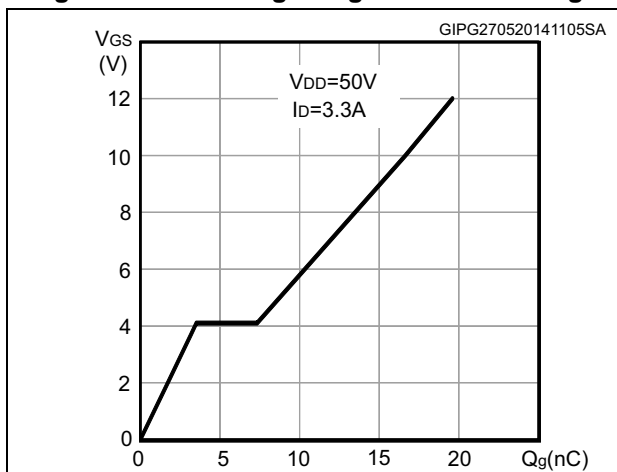


Figure 7. Static drain-source on-resistance

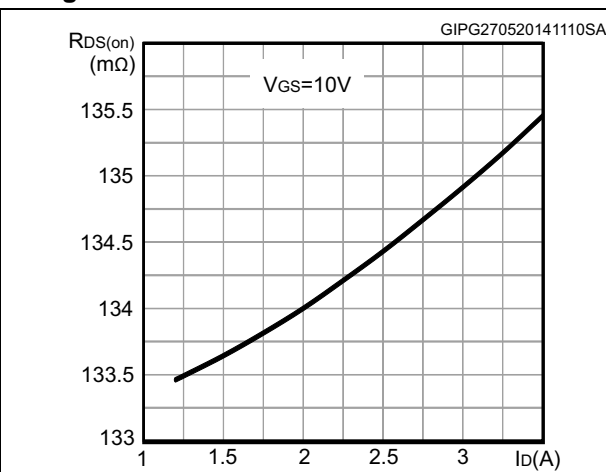


Figure 8. Capacitance variations

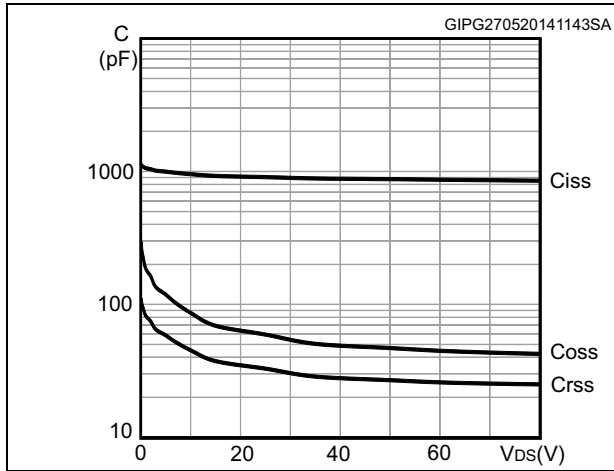


Figure 9. Normalized gate threshold voltage vs temperature

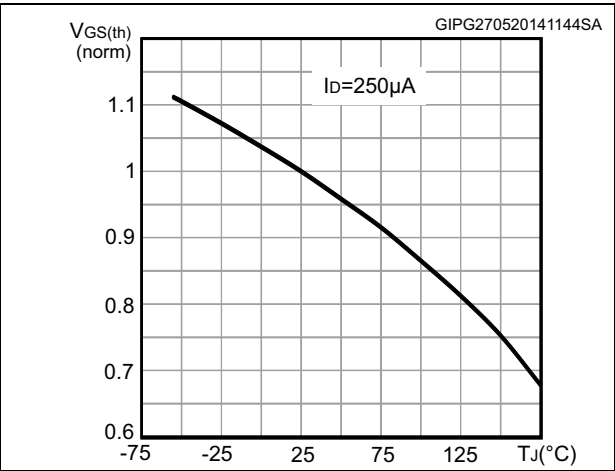


Figure 10. Normalized on-resistance vs temperature

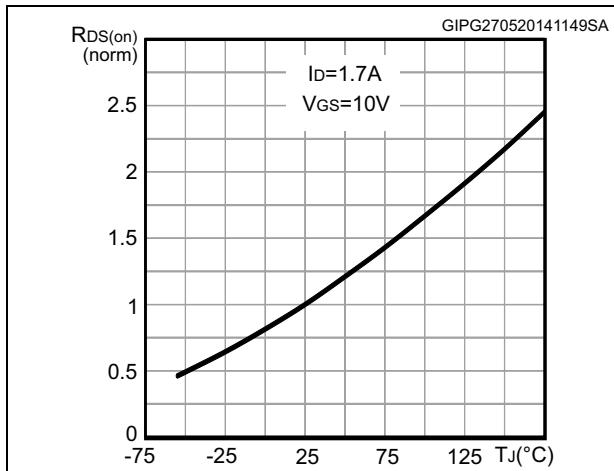


Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature

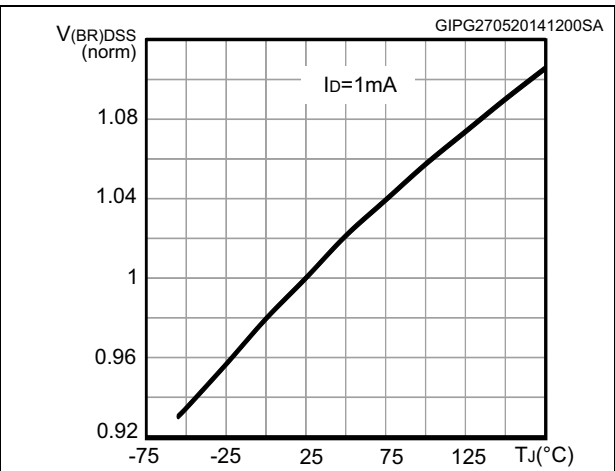
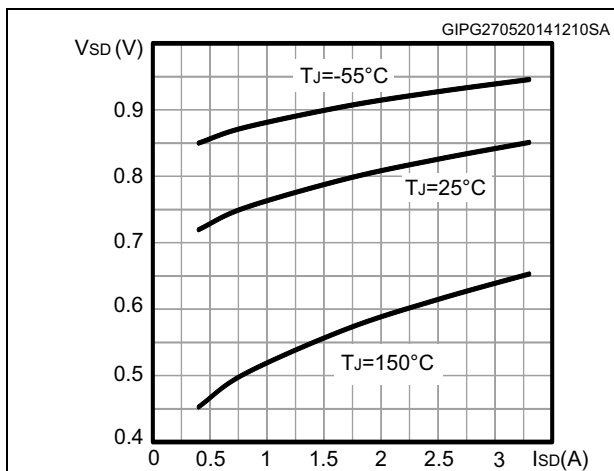
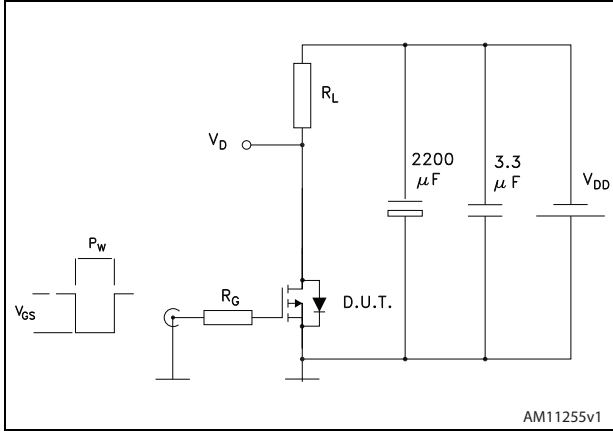


Figure 12. Source-drain diode forward characteristics

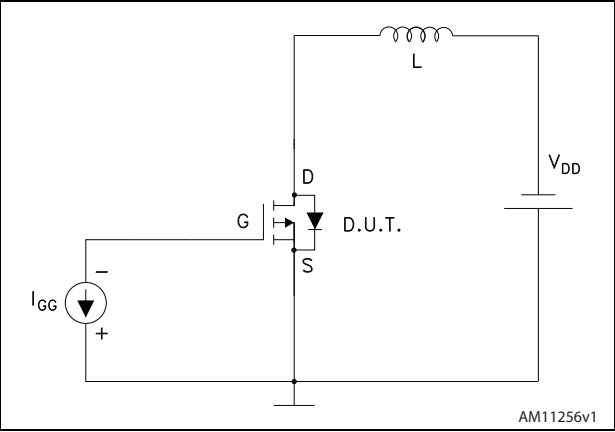


### 3 Test circuits

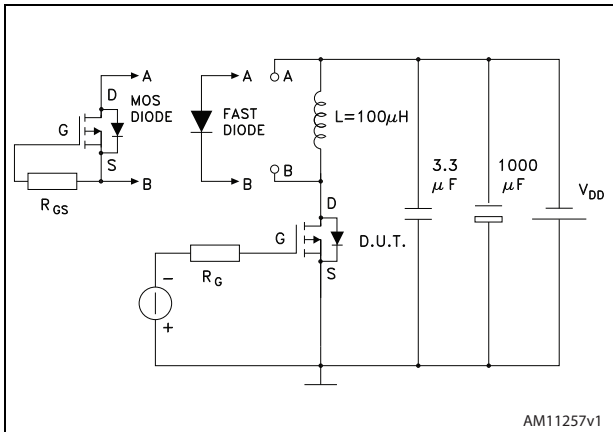
**Figure 13. Switching times test circuit for resistive load**



**Figure 14. Gate charge test circuit**



**Figure 15. Test circuit for inductive load switching and diode recovery times**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 16. PowerFLAT™ 5x6 double island type R-A drawing

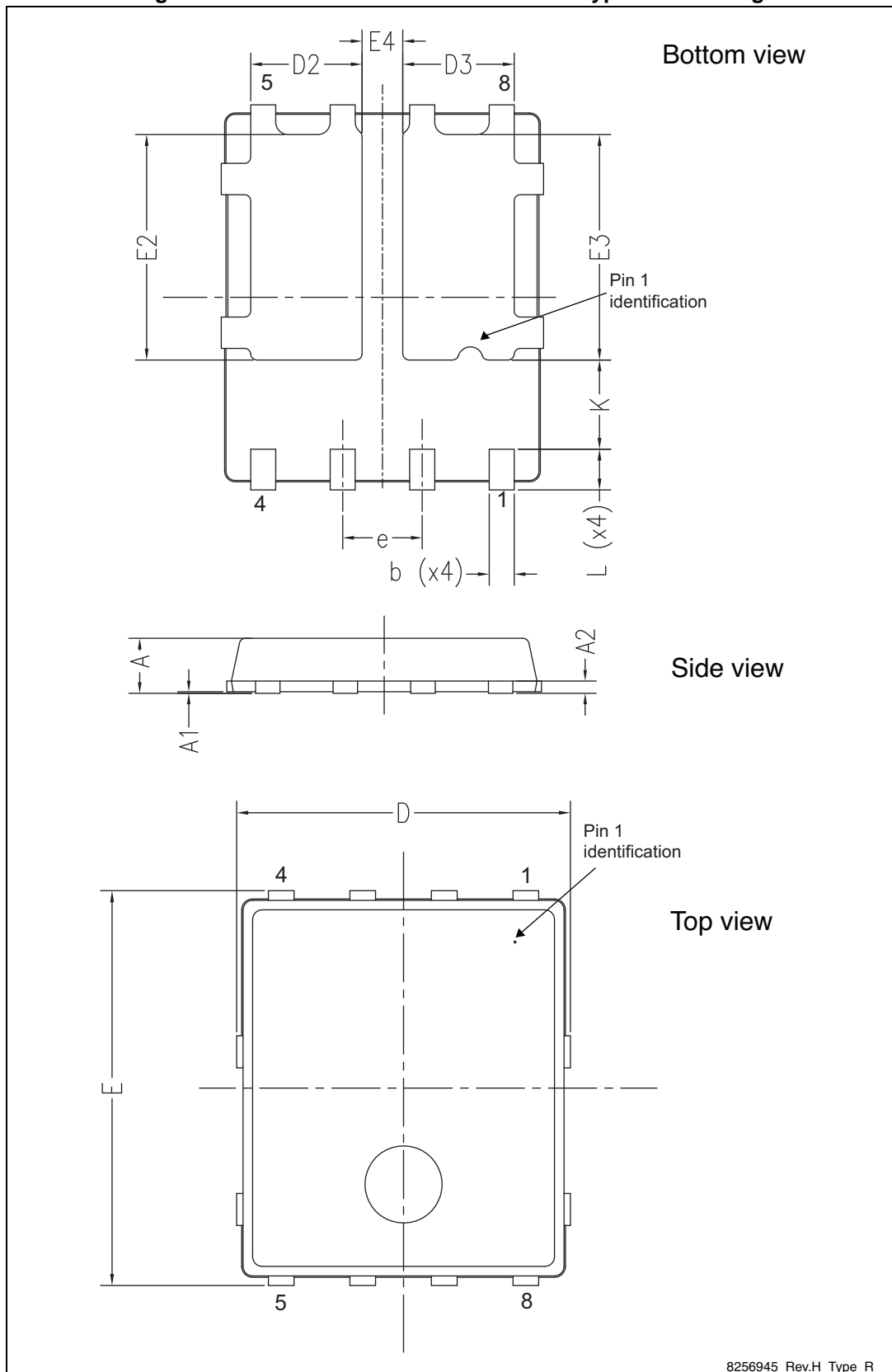
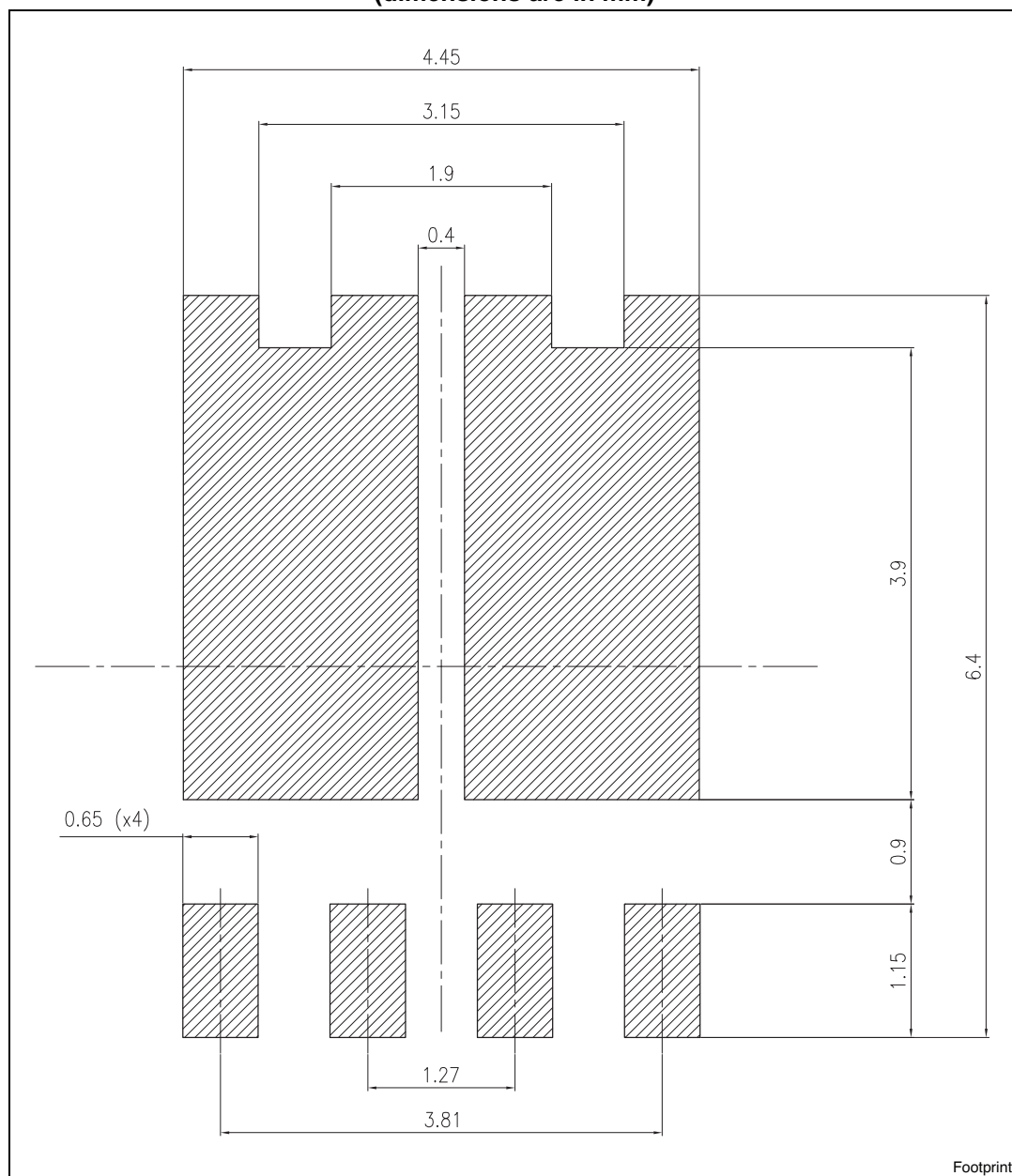


Table 8. PowerFLAT™ 5x6 double island type R-A mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.60		0.80
K	1.275		1.575

Figure 17. PowerFLAT™ 5x6 double island type R-A drawing recommended footprint (dimensions are in mm)



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
19-Nov-2012	1	First release.
30-May-2014	2	<ul style="list-style-type: none"><li>– Document status promoted from target to production data</li><li>– Modified: title</li><li>– Modified: <math>R_{DS(on)}</math> typical value in <a href="#">Table 4</a>, <a href="#">5</a>, <a href="#">6</a>, <a href="#">7</a> and <a href="#">8</a></li><li>– Added: <a href="#">Section 2.1: Electrical characteristics (curves)</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>

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