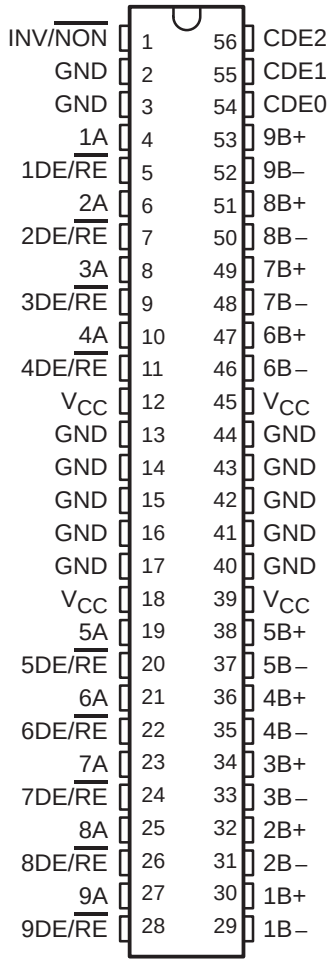
- **9 Channels for the Data and Control Paths of the Small Computer Systems Interface (SCSI)**
- **Supports Single-Ended and Low-Voltage Differential (LVD) SCSI**
- **CMOS Input Levels (’LVDM976) or TTL Input Levels (’LVDM977) Available**
- **Includes DIFFSENS Comparators on CDE0**
- **Single-Ended Receivers Include Noise Pulse Rejection Circuitry**
- **Packaged in Thin Shrink Small-Outline Package With 20-Mil Terminal Pitch**
- **Low Disabled Supply Current 7 mA Maximum**
- **Power-Up/Down Glitch Protection**
- **Bus is High-Impedance With V_{CC} = 1.5 V**
- **Pin-Compatible With the SN75976ADGG High-Voltage Differential Transceiver**

DGG PACKAGE
(TOP VIEW)



description

The SN75LVDM976 and SN75LVDM977 have nine transceivers for transmitting or receiving the signals to or from a SCSI data bus. They offer electrical compatibility to both the single-ended signaling of X3.277:1996–SCSI–3 Parallel Interface (Fast–20) and the new low-voltage differential signaling method of proposed standard 1142–D SCSI Parallel Interface – 2 (SPI–2).

The differential drivers are nonsymmetrical. The SCSI bus uses a dc bias on the line to allow terminated fail safe and wired-OR signaling. This bias can be as high as 125 mV and induces a difference in the high-to-low and low-to-high transition times of a symmetrical driver. In order to reduce pulse skew, an LVD SCSI driver’s output characteristics become nonsymmetrical. In other words, there is more assertion current than negation current to or from the driver. This allows the actual differential signal voltage on the bus to be symmetrical about 0 V. Even though the driver output characteristics are nonsymmetrical, the design of the ’LVDM976 drivers maintains balanced signaling. Balanced means that the current that flows in each signal line is nearly equal but opposite in direction and is one of the keys to the low-noise performance of a differential bus.

AVAILABLE OPTIONS

T_A	PACKAGE	
	TSSOP (DGG) CMOS INPUT LEVELS	TSSOP (DGG) TTL INPUTS LEVELS
0°C to 70°C	SN75LVDM976DGG SN75LVDM976DGGR†	SN75LVDM977DGG SN75LVDM977DGGR†

† The R suffix designates a taped and reeled package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

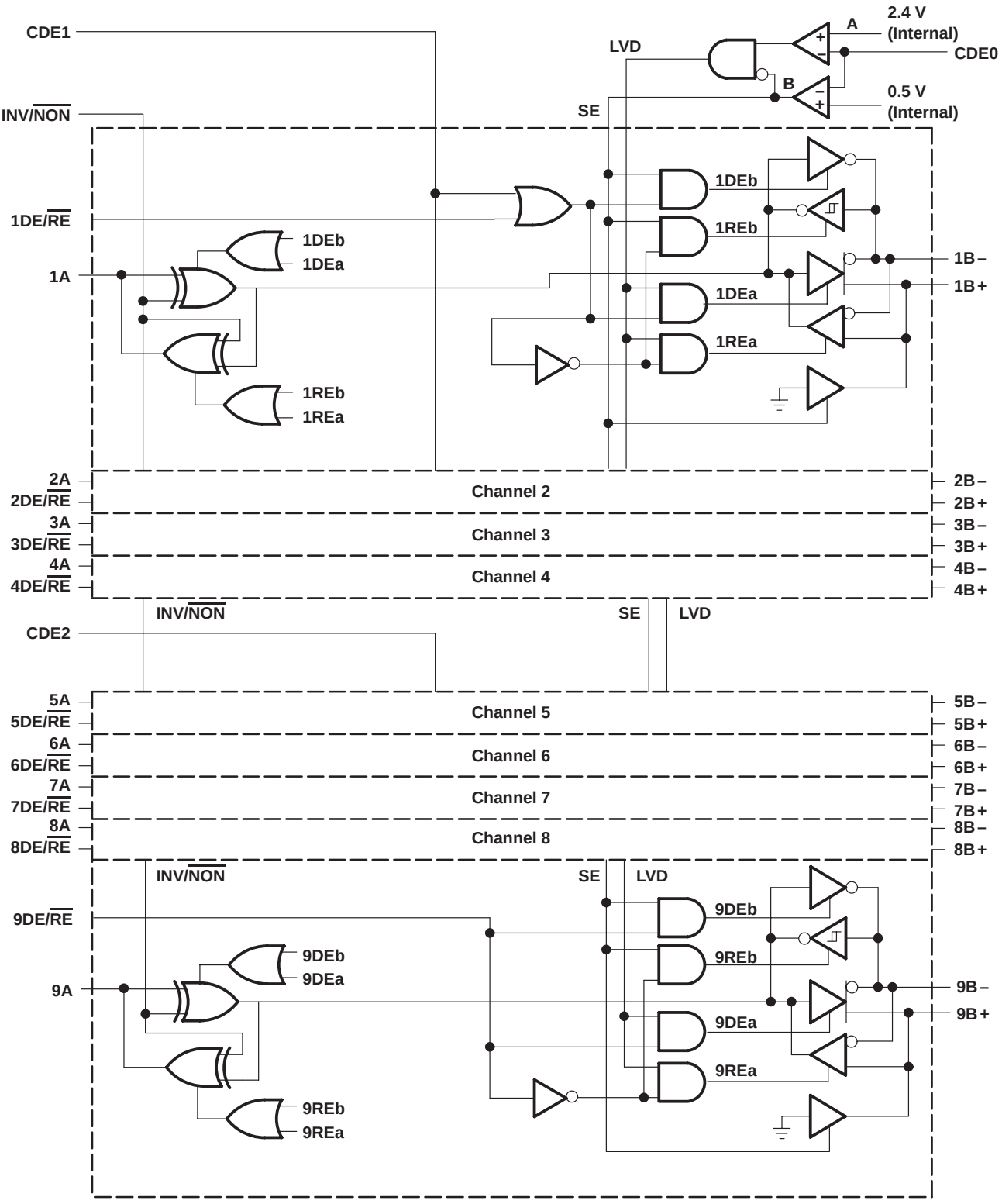
The signal symmetry requirements of the LVD-SCSI bus mean you can no longer obtain logical inversion of a signal by simply reversing the differential signal connections. This requires the ability to invert the logic convention through the INV/$\overline{\text{NON}}$ terminal. This input would be a low for SCSI controllers with active-high data and high for active-low data. In either case, the B+ signals of the transceiver must be connected to the SIGNAL+ line of the SCSI bus and the B– of the transceiver to the SIGNAL– line.

The CDE0 input incorporates a window comparator to detect the status of the DIFFSENS line of a SCSI bus. This line is below 0.5 V, if using single-ended signals, between 1.7 V and 1.9 V if low-voltage differential, and between 2.4 V and 5.5 V if high-voltage differential. The outputs assume the characteristics of single-ended or LVD accordingly or place the outputs into high-impedance, when HVD is detected. This, and the INV/$\overline{\text{NON}}$ input, are the only differences to the trade-standard function of the SN75976A HVD transceiver.

Two options are offered to minimize the signal noise margins on the interface between the communications controller and the transceiver. The SN75LVDM976 has logic input voltage thresholds of about 0.5 V_{CC}. The SN75LVDM977 has a fixed logic input voltage threshold of about 1.5 V. The input voltage threshold should be selected to be near the middle of the output voltage swing of the corresponding driver circuit.

The SN75LVDM976 and SN75LVDM977 are characterized for operation over an free-air temperature range of T_A = 0°C to 70°C.

logic diagram (positive logic)



logic diagrams and function tables

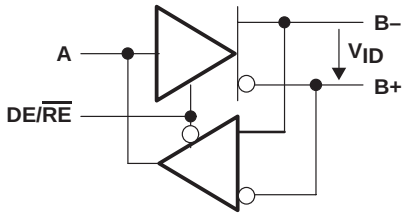


Figure 1. Inverting LVD Transceiver

FUNCTION TABLE

Inputs			Outputs		
(B+ – B–)	DE/$\overline{RE}$	A	B+	B –	A
$V_{ID} \geq 30$ mV	L	NA	Z	Z	L
-30 mV < $V_{ID} < 30$ mV	L	NA	Z	Z	?
$V_{ID} -30$ mV	L	NA	Z	Z	H
Open circuit	L	NA	Z	Z	?
NA	H	L	H	L	Z
NA	H	H	L	H	Z

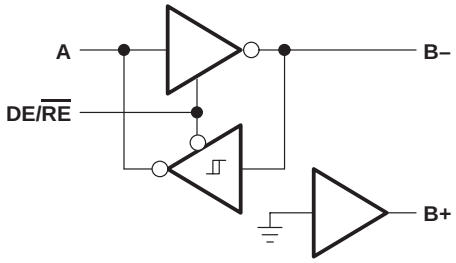


Figure 2. Inverting Single-Ended Transceiver

FUNCTION TABLE

Inputs			Outputs		
B–	DE/$\overline{RE}$	A	B+	B –	A
H	L	NA	L	Z	L
L	L	NA	L	Z	H
Open circuit	L	NA	L	Z	?
NA	H	L	L	H	Z
NA	H	H	L	L	Z

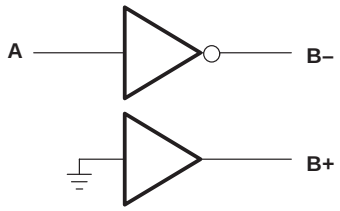


Figure 3. Inverting Single-Ended Driver

FUNCTION TABLE

Input	Outputs	
A	B+	B –
L	L	H
H	L	L

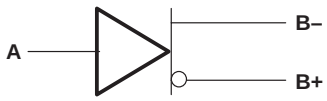


Figure 4. Inverting LVD Driver

FUNCTION TABLE

Input	Outputs	
A	B+	B –
L	H	L
H	L	H

logic diagrams and function tables (continued)

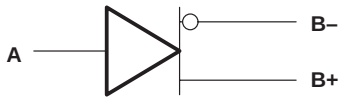


Figure 5. Noninverting LVD Driver

FUNCTION TABLE

Input	Outputs	
A	B+	B–
L	L	H
H	H	L

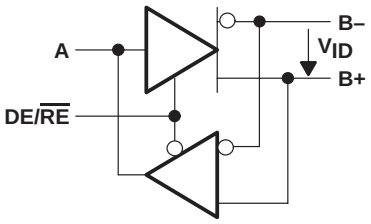


Figure 6. Noninverting LVD Transceiver

FUNCTION TABLE

Inputs			Outputs		
(B+ – B–)	DE/$\overline{RE}$	A	B+	B–	A
$V_{ID} \geq 30$ mV	L	NA	Z	Z	H
-30 mV $< V_{ID} < 30$ mV	L	NA	Z	Z	?
$V_{ID} \leq -30$ mV	L	NA	Z	Z	L
Open circuit	L	NA	Z	Z	?
NA	H	L	L	H	Z
NA	H	H	H	L	Z

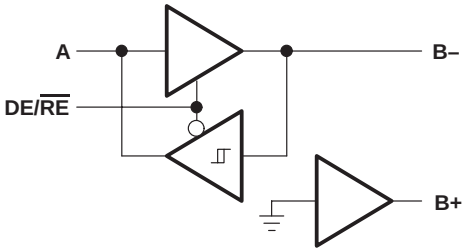


Figure 7. Noninverting Single-Ended Transceiver

FUNCTION TABLE

Inputs			Outputs		
B–	DE/$\overline{RE}$	A	B+	B–	A
H	L	NA	L	Z	H
L	L	NA	L	Z	L
Open Circuit	L	NA	L	Z	?
NA	H	L	L	L	Z
NA	H	H	L	H	Z

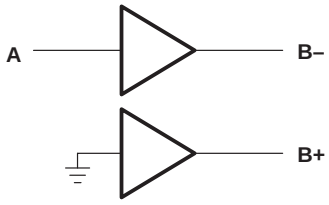
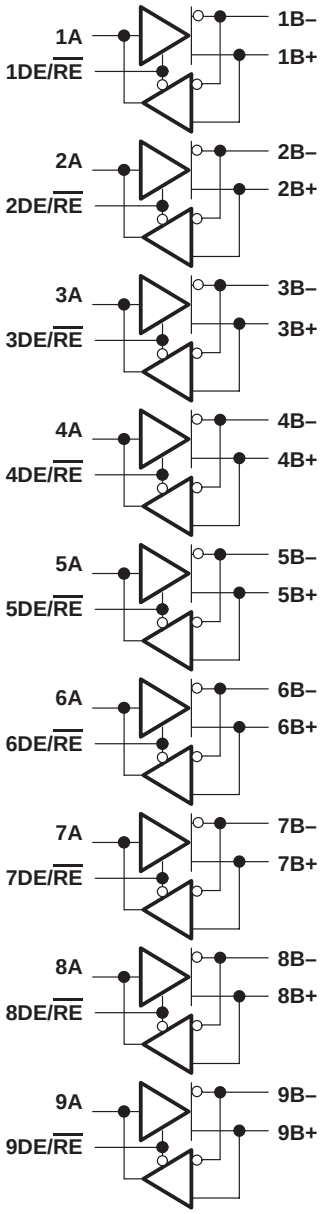


Figure 8. Noninverting Single-Ended Driver

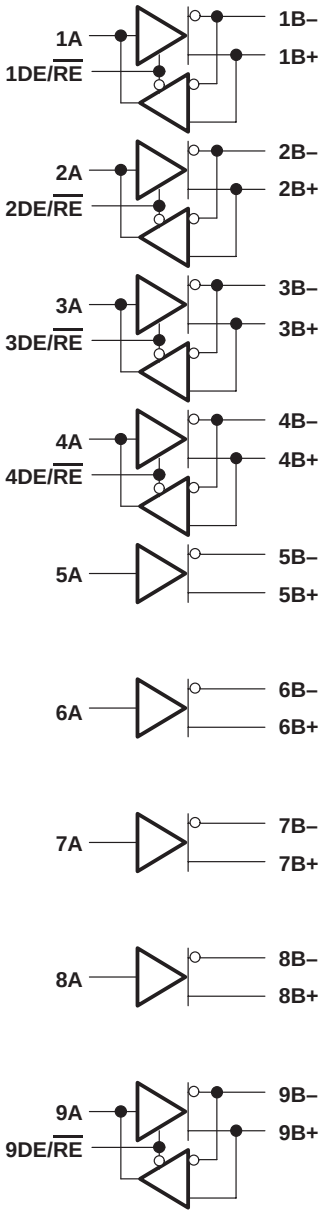
FUNCTION TABLE

Input	Outputs	
A	B+	B–
L	L	L
H	L	H



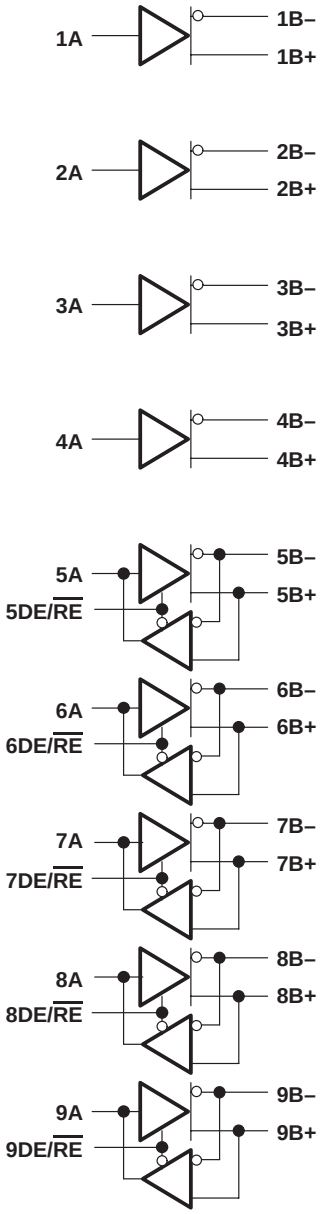
Control Inputs	
CDE0	0.7 V < V_I < 1.9 V
INV/NON	L
CDE1	L
CDE2	L

(a)



Control Inputs	
CDE0	0.7 V < V_I < 1.9 V
INV/NON	L
CDE1	L
CDE2	H

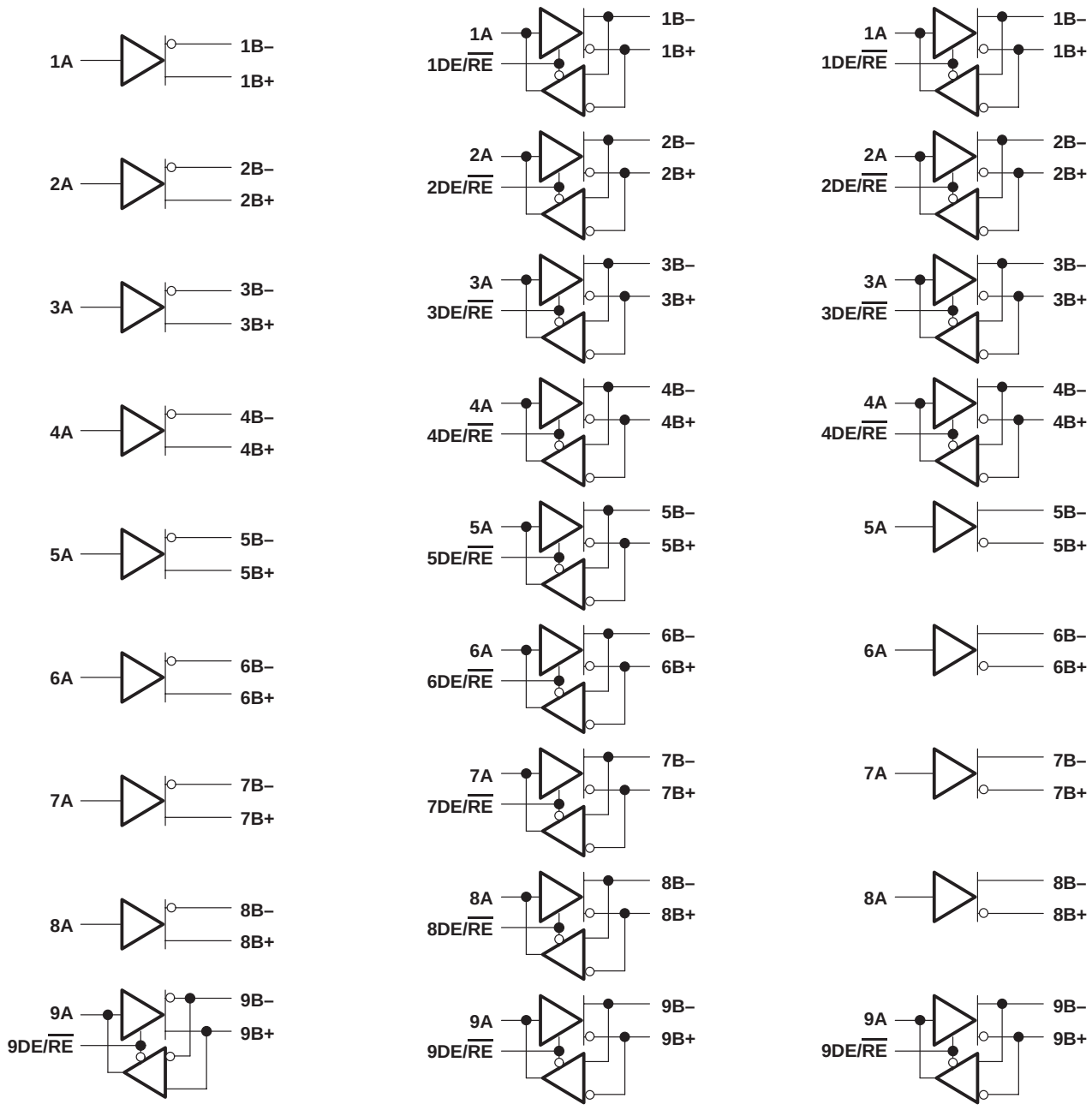
(b)



Control Inputs	
CDE0	0.7 V < V_I < 1.9 V
INV/NON	L
CDE1	H
CDE2	L

(c)

Figure 9. Logic Diagrams



Control Inputs	
CDE0	0.7 V < V_I < 1.9 V
INV/NON	L
CDE1	H
CDE2	H

(a)

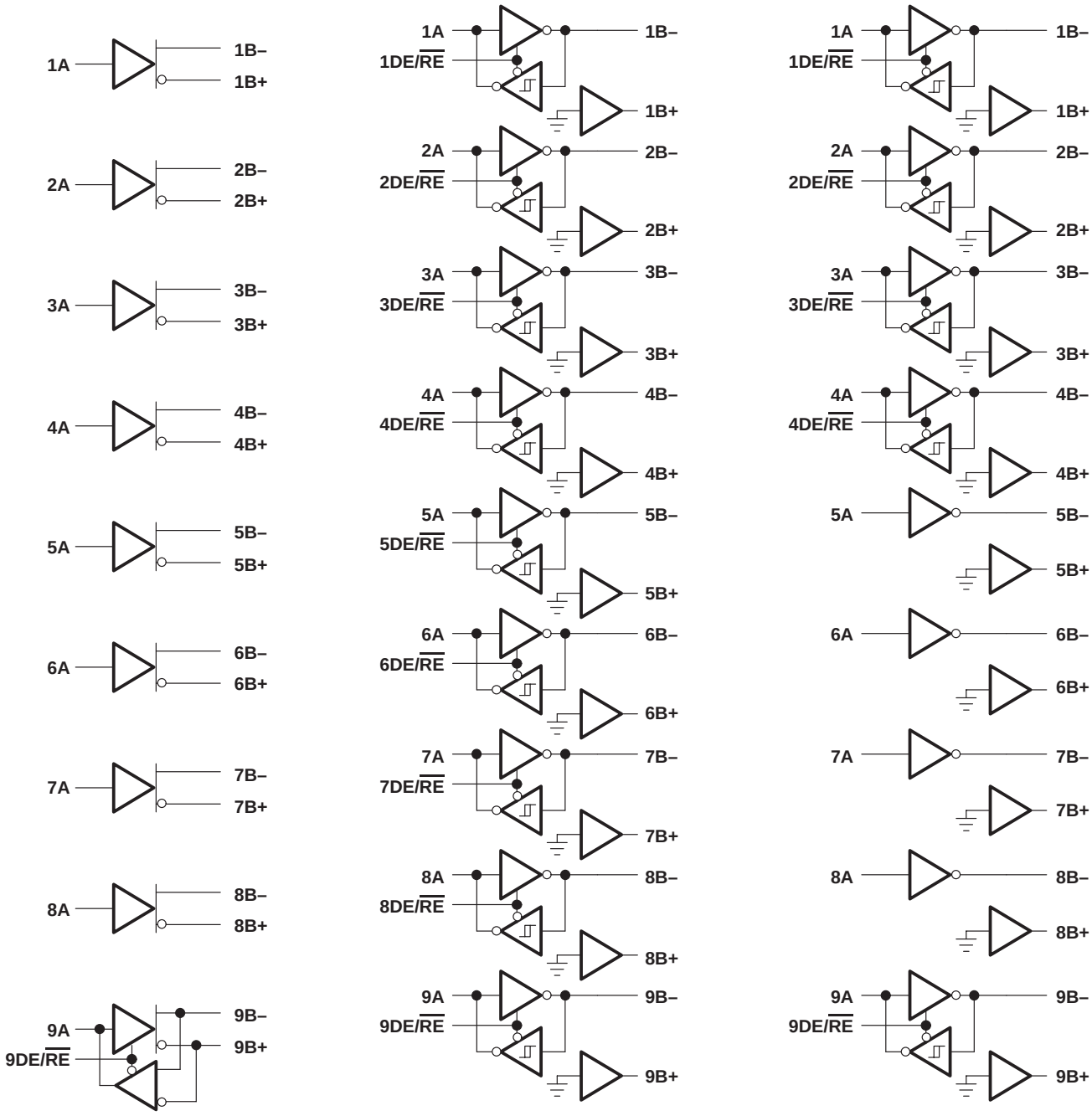
Control Inputs	
CDE0	0.7 V < V_I < 1.9 V
INV/NON	H
CDE1	L
CDE2	L

(b)

Control Inputs	
CDE0	0.7 V < V_I < 1.9 V
INV/NON	H
CDE1	L
CDE2	H

(C)

Figure 10. Logic Diagrams



Control Inputs

CDE0	0.7 V < V_I < 1.9 V
INV/$\overline{\text{NON}}$	H
CDE1	H
CDE2	H

(a)

Control Inputs

CDE0	V_I < 0.5 V
INV/$\overline{\text{NON}}$	L
CDE1	L
CDE2	L

(b)

Control Inputs

CDE0	V_I < 0.5 V
INV/$\overline{\text{NON}}$	L
CDE1	L
CDE2	H

(c)

Figure 11. Logic Diagrams

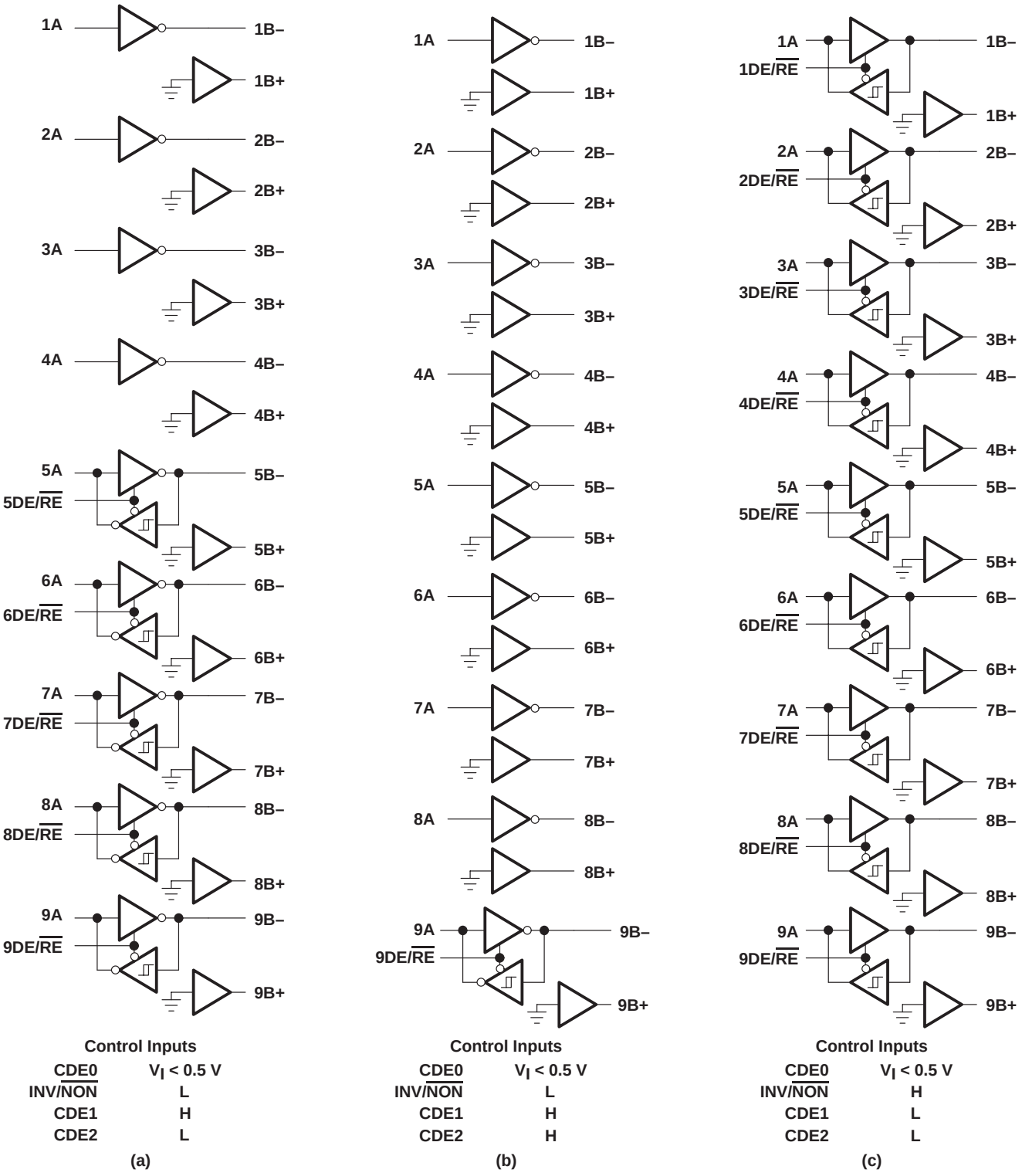
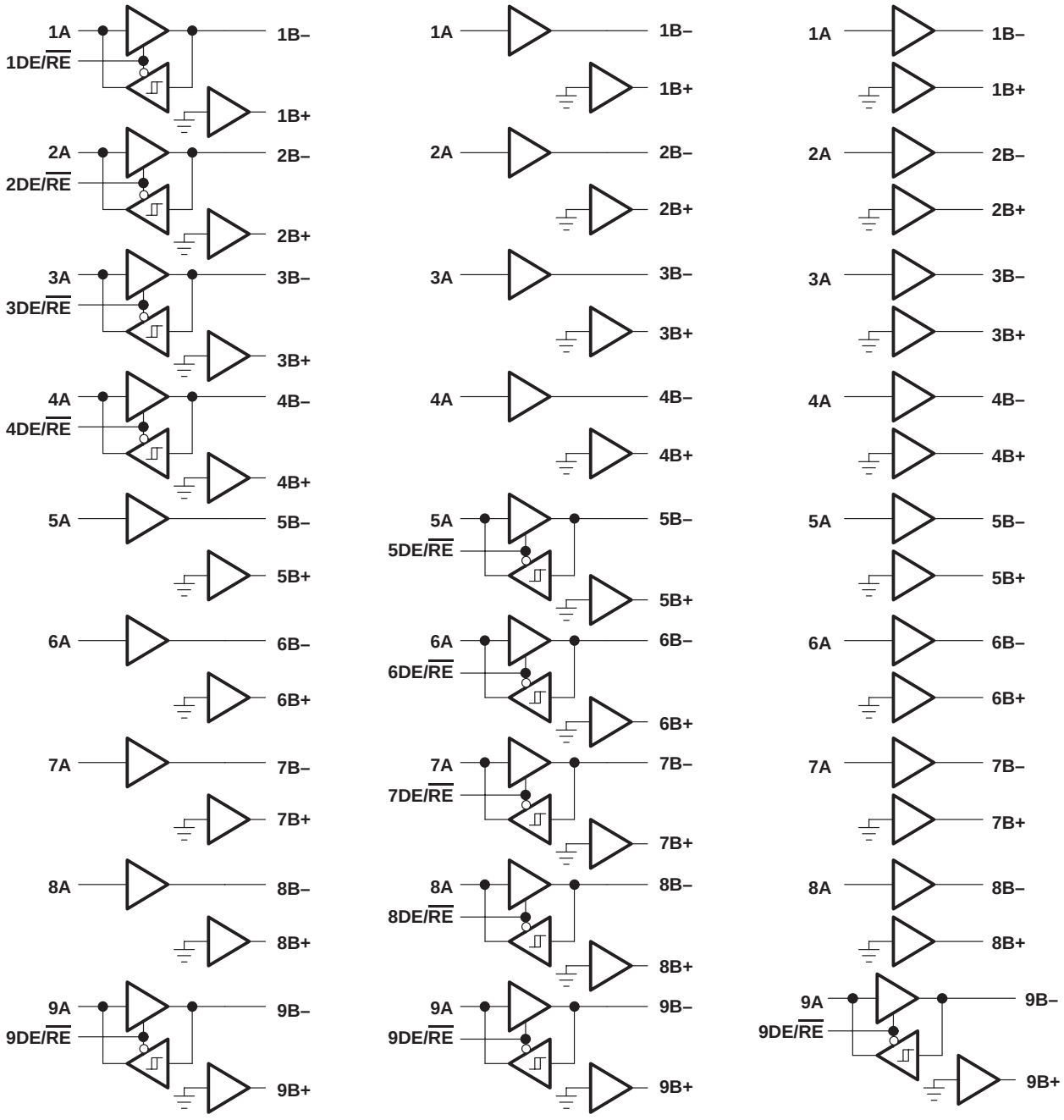


Figure 12. Logic Diagrams



Control Inputs

CDE0	V_I < 0.5 V
INV/NON	H
CDE1	L
CDE2	H

(a)

Control Inputs

CDE0	V_I < 0.5 V
INV/NON	H
CDE1	H
CDE2	L

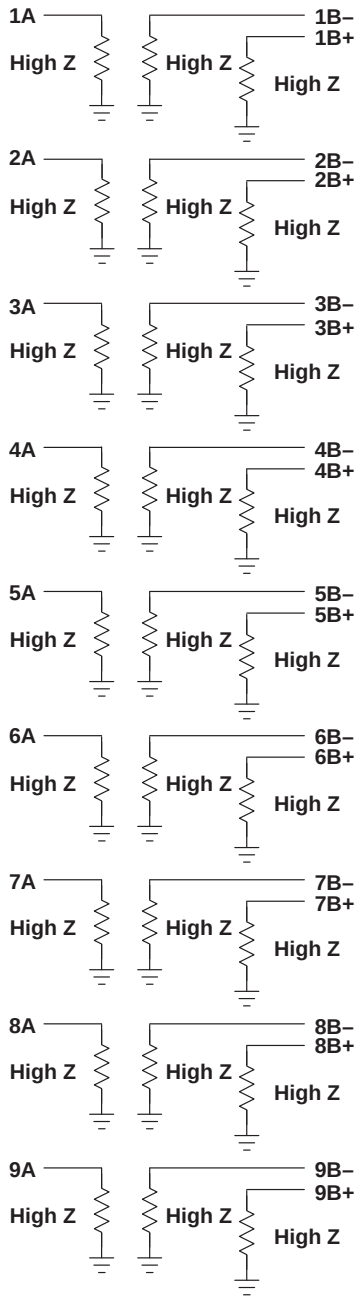
(b)

Control Inputs

CDE0	V_I < 0.5 V
INV/NON	H
CDE1	H
CDE2	H

(b)

Figure 13. Logic Diagrams

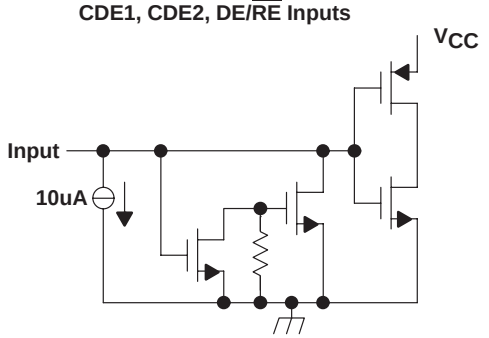


Control Inputs	
CDE0	V_I > 2.5 V
INV/NON	X
CDE1	X
CDE2	X

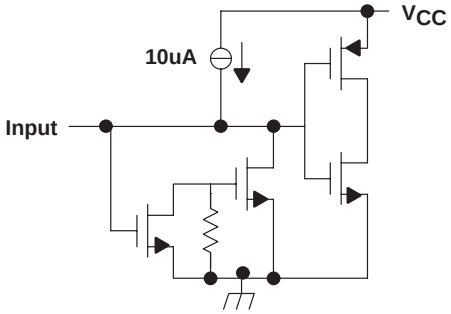
Figure 14. Logic Diagrams

input and output equivalent schematic diagrams

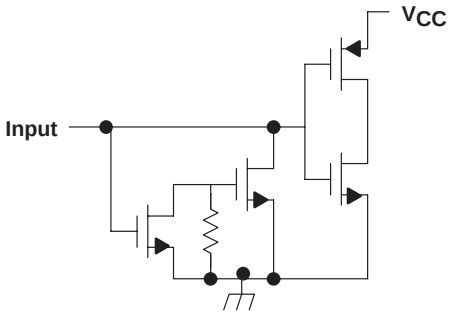
CDE1, CDE2, DE/$\overline{\text{RE}}$ Inputs



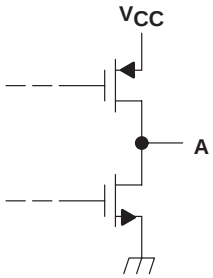
A and INV/$\overline{\text{NON}}$ Inputs



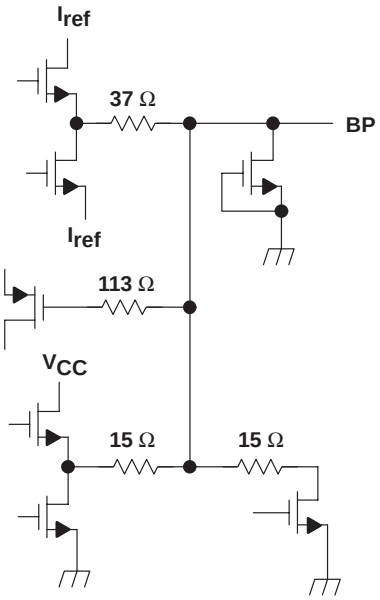
CDE0 Input



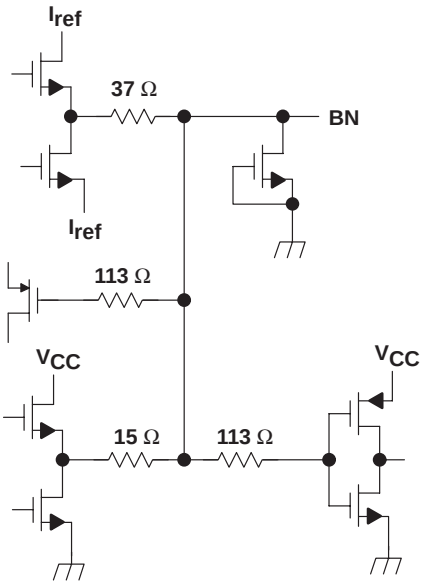
A Output



B+ Input



B– Input



Terminal Functions

TERMINAL NAME	TERMINAL NO.	'LVDM976 Logic Level	'LVDM977 Logic Level	I/O	Termination	DESCRIPTION
1A – 9A	4,6,8,10, 19,21,23, 25,27	CMOS	TTL	I/O	Pullup	1A – 9A carry data to and from the communication controller.
$1B^- – 9B^-$	29,31,33, 35,37,46, 48,50,52	LVD or TTL	LVD or TTL	I/O	None	1B– to 9B– are the signals to and from the data bus. When INV/$\overline{\text{NON}}$ is low, the logic sense is the opposite that of the A input (inverted). When INV/$\overline{\text{NON}}$ is high, the logic sense is the same as the A input (noninverted).
$1B^+ – 9B^+$	30,32,34, 36,38,47, 49,51,53	LVD or GND	LVD or GND	I/O	None	When in the LVD mode, 1B+ – 9B+ are signals to or from the data bus and follow the same logic sense as the A input when INV/$\overline{\text{NON}}$ is low (noninverted). The logic sense is opposite that of the A input (inverted) when INV/$\overline{\text{NON}}$ is high. When in single-ended mode, these terminals become a ground connection through a transistor and do not switch.
CDE0	54	Trinary	Trinary	Input	None	CDE0 is the common driver enable 0. With the driver enabled and the CDE0 input less than 0.5 V, the driver output is single-ended mode. With the driver enabled and the CDE0 input between 0.7 V and 1.9 V the driver output is LVD mode. All drivers are disabled when the input is greater than 2.4 V.
CDE1	55	CMOS	TTL	Input	Pulldown	CDE1 is the common driver enable 1. When CDE1 is high, drivers 1 – 4 are enabled
CDE2	56	CMOS	TTL	Input	Pulldown	CDE2 is the common driver enable 2. When CDE2 is high, drivers 5 to 8 are enabled.
1DE/$\overline{\text{RE}}$ – 9DE/$\overline{\text{RE}}$	5,7,9,11, 20,22,24, 26,28	CMOS	TTL	Input	Pulldown	1DE/$\overline{\text{RE}}$ – 9DE/$\overline{\text{RE}}$ are direction controls that transmit data to the bus when it is high and CDE0 is below 2.2 V. Data is received from the bus when 1DE/$\overline{\text{RE}}$ – 9DE/$\overline{\text{RE}}$, CDE1, and CDE2 are low.
GND	2,3,13,14, 15,16,17, 40,41,42, 43,44	NA	NA	Power	NA	GND is the circuit ground.
INV/$\overline{\text{NON}}$	1	CMOS	CMOS	Input	Pullup	A high-level input to INV/$\overline{\text{NON}}$ inverts the logic to and from the A terminals. (i.e., the voltage at A terminal and the corresponding B– terminal are in phase.)
V_{CC}	12,18,39, 45	NA	NA	Power	NA	Supply voltage

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
Input voltage range, V_I (A, INV/$\overline{NON}$) . . . . . –0.5 V to V_{CC} + 0.5 V
(DE/$\overline{RE}$, B+, B–, CDE0, CDE1, CDE2) . . . . . –0.5 V to 5.25 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DGG	978 mW	10.8 mW/°C	492 mW

recommended operating conditions (see Figure 15)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	SN75LVDM976	0.7 V_{CC}			V
	SN75LVDM977	2			
Low-level input voltage, V_{IL}	SN75LVDM976			0.3 V_{CC}	V
	SN75LVDM977			0.8	
Differential input voltage, $\|V_{ID}\|$	Differential receiver	0.03		3.6	V
Common-mode input voltage, V_{IC}		0.7		1.8	V
Differential output voltage bias, $V_{OD(bias)}$	Differential	–100		–125	mV
High-level output current, I_{OH}	Single-ended driver			–7	mA
	Receiver			–2	
Low-level output current, I_{OL}	Single-ended driver			48	mA
	Receiver			2	
Differential load impedance, Z_L		40		65	Ω
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{IH}	High-level input current	CDE1 and CDE2				50	µA
		INV/$\overline{NON}$				–50	
I_{IL}	Low-level input current	CDE1 and CDE2				50	µA
		INV/$\overline{NON}$				–50	
I_{CC}	Supply current		Disabled			7	mA
			LVD drivers enabled, No load			26	
			Single-ended drivers enabled, No load			10	
			LVD receivers enabled, No load			26	
			Singled-ended receivers enabled, No load			7	
C_I	Input capacitance	Bus terminal	V_I = 0.2 sin (2 π (1E06)t) + 0.5 ± 0.01 V		9.5		pF
ΔC_I	Difference in input capacitance between B+ and B–					0.2	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

DIFFSENS (CDE0) receiver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT1}	Input threshold voltage		0.5	0.6	0.7	V
V_{IT2}	Input threshold voltage		1.9	2.1	2.4	
I_I	Input current	0 V ≤ V_I ≤ 2.7 V			±1	µA
$I_{I(OFF)}$	Power-off input current	V_{CC} = 0, 0 V ≤ V_I ≤ 2.7 V			±1	µA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

LVD driver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OD(H)}$	Driver differential high-level output voltage		$V_{I(1)}$ = 0.96 V, $V_{I(2)}$ = 0.53 V, See Figure 16	270	460	780	mV
				0.69|$V_{OD(L)}$|+ 50		1.45|$V_{OD(L)}$|– 65	
			$V_{I(1)}$ = 1.96 V, $V_{I(2)}$ = 1.53 V, See Figure 16	270	500	780	
				0.69|$V_{OD(L)}$|+ 50		1.45|$V_{OD(L)}$|– 65	
$V_{OD(L)}$	Driver differential low-level output voltage		$V_{I(1)}$ = 0.96 V, $V_{I(2)}$ = 0.53 V, See Figure 16	–260	–400	–640	mV
			$V_{I(1)}$ = 1.96 V, $V_{I(2)}$ = 1.53 V, See Figure 16	–260	–400	–640	
$V_{OC(SS)}$	Steady-state common-mode output voltage		$V_{I(1)}$ = 1.41 V, $V_{I(2)}$ = 0.99 V, See Figure 17	1.1	1.2	1.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				±50	±120	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				80	150	mV
I_{IH}	High-level input current	A	V_{IH} = 3.3 V ('976) V_{IH} = 2 V ('977)	–7			µA
		$\overline{DE}$/RE				50	
I_{IL}	Low-level input current	A	V_{IL} = 1.6 V ('976) V_{IL} = 0.8 V ('977)			–30	µA
		$\overline{DE}$/RE		8			
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0, 0 V ≤ V_O ≤ 2.5 V			±1	µA
I_{OS}	Short-circuit output current		0 V ≤ V_O ≤ 2.5 V			±24	mA
I_{OZ}	High-impedance output current		V_O = 0 or 2.5 V			±1	µA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

LVD driver switching characteristics over recommended operating conditions (unless otherwise noted) (See Figure 16)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	V_{CC} = 5 V, V_{I1} = 1.41 V, V_{I2} = 0.99 V, T_A = 25°C	2.9		8.8	ns
t_{PHL}	Propagation delay time, high-to-low level output		2.9		8.8	ns
t_r	Differential output signal rise time		1	3	6	ns
t_f	Differential output signal fall time		1	3	6	ns
$t_{sk(p)}$	Pulse skew (|t_{PHL} – t_{PLH}|)				3.7	ns
$t_{sk(lim)}$	Skew limit‡				5.9	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output	V_{I1} = 1.41 V, V_{I2} = 0.99 V, See Figure 18			50	ns
t_{en}	Enable time, receiver to driver				33	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

single-ended driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	B– output	I_{OH} = –7 mA, See Figure 19	2		3.24	V
			I_{OH} = 0 mA			3.7	V
V_{OL}	Low-level output voltage	B– output	V_{CC} = 5 V, I_{OL} = 48 mA			0.5	V
		B+	I_{OL} = –25 mA			–0.5	V
			I_{OL} = 25 mA			0.5	
I_{IH}	High-level input current	A	V_{IH} = 3.3 V ('976), V_{IH} = 2 V ('977)	–7			µA
		DE/$\overline{RE}$				50	
I_{IL}	Low-level input current	A	V_{IL} = 1.6 V ('976), V_{IL} = 0.8 V ('977)			–30	µA
		DE/$\overline{RE}$		8			
$I_{O(OFF)}$	Power-off output current	B–	V_{CC} = 0, 0 V ≤ V_O ≤ 5.25 V			±1	µA
I_{OZ}	High-impedance output current		V_O = 0 or V_{CC}			±1	µA

single-ended driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	V_{CC} = 5 V, T_A = 25°C, See Figure 19	2.7		8.2	ns
t_{PHL}	Propagation delay time, high-to-low level output		2.7		8.2	ns
t_r	Differential output signal rise time		0.5		4	ns
t_f	Differential output signal fall time		0.5		4	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				3.4	ns
$t_{sk(lim)}$	Skew limit‡				5.5	ns
t_{en}	Enable time, receiver to driver	See Figure 20			50	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output				30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

LVD receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 21			30	mV
$V_{IT–}$	Negative-going differential input voltage threshold				–30	mV
V_{OH}	High-level output voltage	I_{OH} = –2 mA	3.7			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.5	V
I_I	Input current, B+ or B–	V_I = 0 V to 2.5 V			±1	µA
$I_{I(OFF)}$	Power-off Input current, B+ or B–	V_{CC} = 0, V_I = 0 V to 2.5 V			±1	µA
I_{IH}	High-level input current, DE/$\overline{RE}$	V_{IH} = 3.3 V ('976), V_{IH} = 2 V ('977)			50	µA
I_{IL}	Low-level input current, DE/$\overline{RE}$	V_{IL} = 1.6 V ('976), V_{IL} = 0.8 V ('977)	8			µA
I_{OZ}	High-impedance output current	V_O = 0 or V_{CC}			±30	µA

LVD receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	V_{CC} = 5 V, T_A = 25°C, See Figure 21	4.5		10	ns
t_{PHL}	Propagation delay time, high-to-low level output		4.5		10	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				3	ns
t_r	Output signal rise time				8	ns
t_f	Output signal fall time				8	ns
$t_{sk(lim)}$	Skew limit‡				5.5	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output	See Figure 18			42	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output				20	ns
t_{en}	Enable time, driver to receiver				26	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

single-ended receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input voltage threshold	B–			1.6	1.9	V
V_{IT-}	Negative-going input voltage threshold	B–		1	1.1		V
V_{OH}	High-level output voltage		I_{OH} = –2 mA	3.7	4.6		V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA		0.3	0.5	V
I_I	Input current	B–	V_I = 0 to V_{CC}			±1	µA
$I_{I(OFF)}$	Power-off Input current	B–	V_{CC} = 0 V, V_I = 0 to 5.25 V			±1	µA
I_{IH}	High-level input current	DE/$\overline{RE}$	V_{IH} = 3.3 V ('976), V_{IH} = 2 V ('977)			50	µA
I_{IL}	Low-level input current	DE/$\overline{RE}$	V_{IL} = 1.6 V ('976), V_{IL} = 0.8 V ('977)	8			µA
I_{OZ}	High-impedance output current		V_O = 0 or V_{CC}			–30	µA

single-ended receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	V_{CC} = 5 V, T_A = 25°C, See Figure 22	7		12.5	ns
t_{PHL}	Propagation delay time, high-to-low level output		7		12.5	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				3.5	ns
t_r	Output signal rise time				8	ns
t_f	Output signal fall time				8	ns
$t_{sk(lim)}$	Skew limit†				5.5	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output	See Figure 20			20	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output				30	ns
t_{en}	Enable time, driver to receiver				48	ns

† $t_{sk(lim)}$ is the maximum delay time difference between any two drivers on any two devices operating at the same supply voltage and the same ambient temperature.

PARAMETER MEASUREMENT INFORMATION

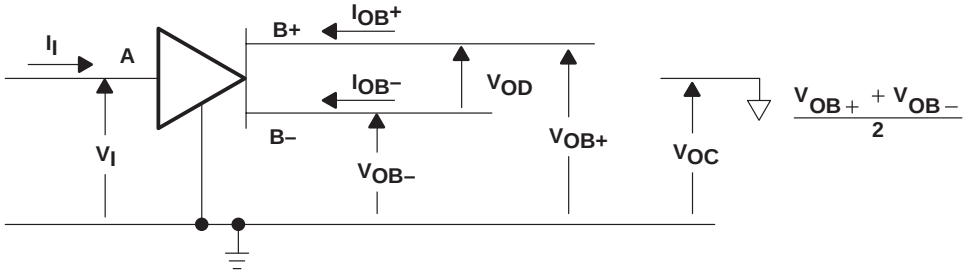
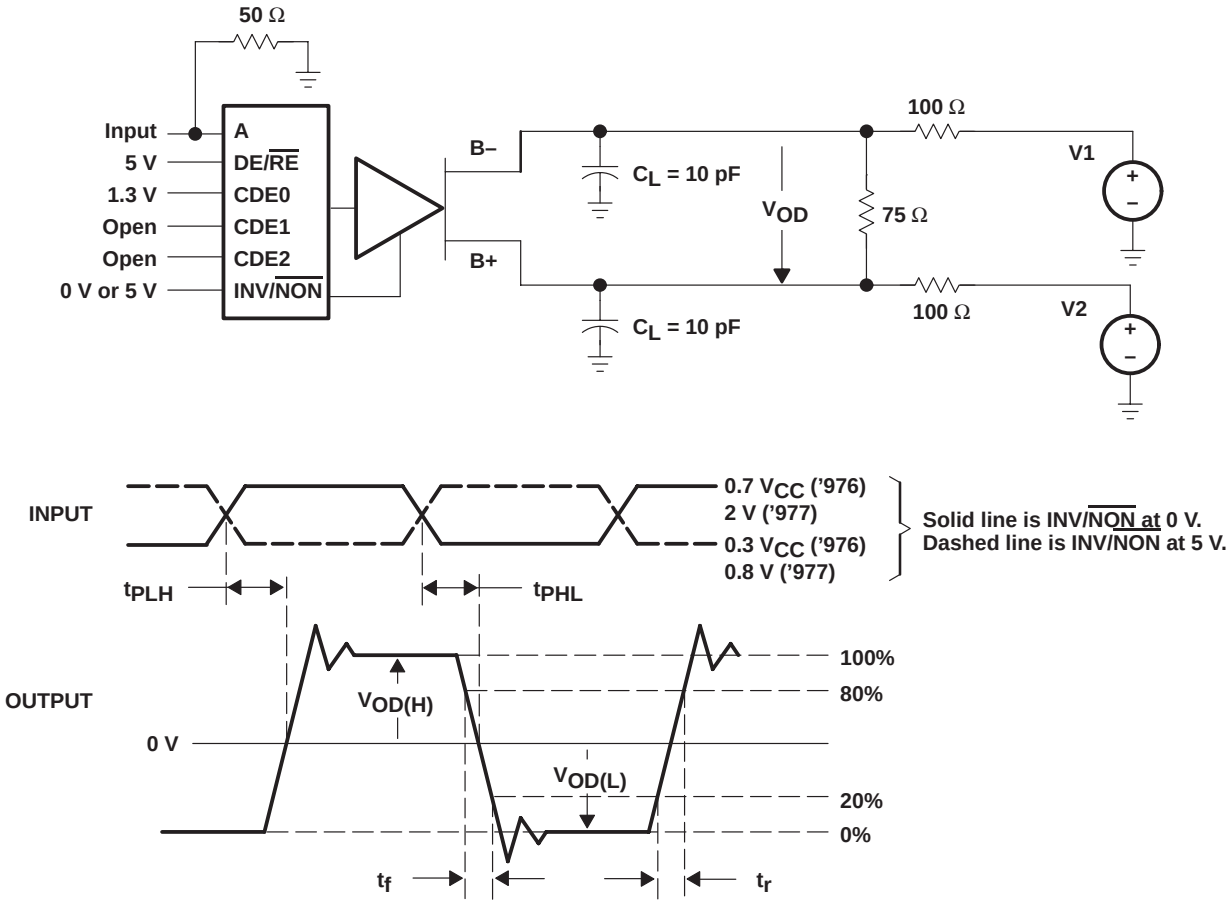


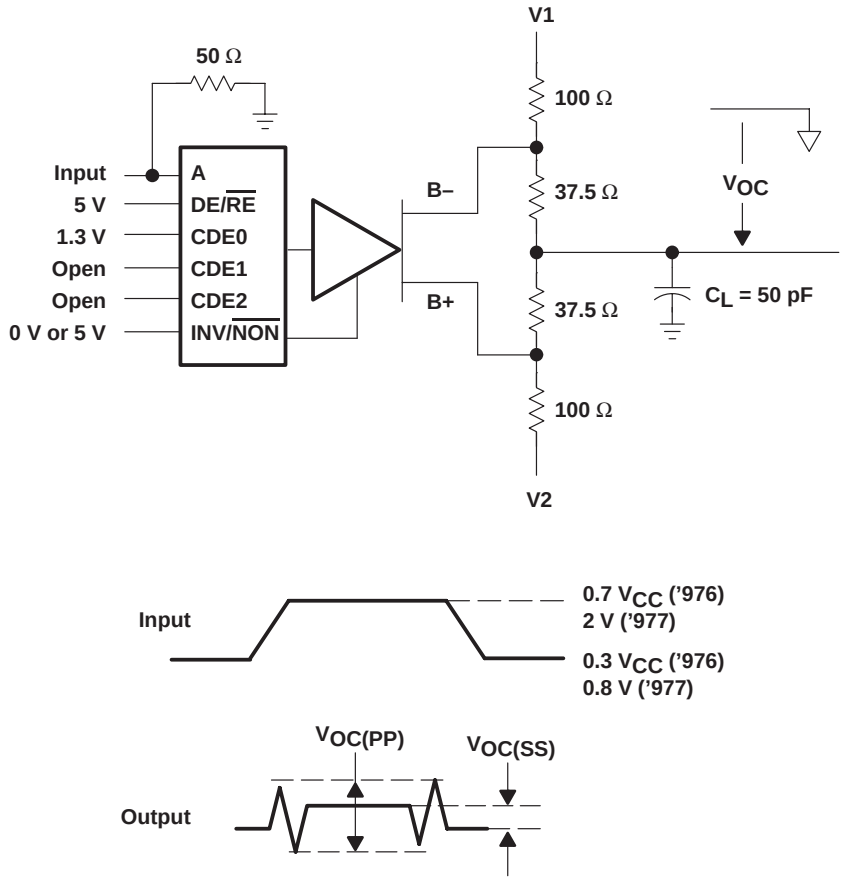
Figure 15. Voltage and Current Definitions



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ±5 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 16. Differential Output Signal Test Circuit, Timing, and Voltage Definitions

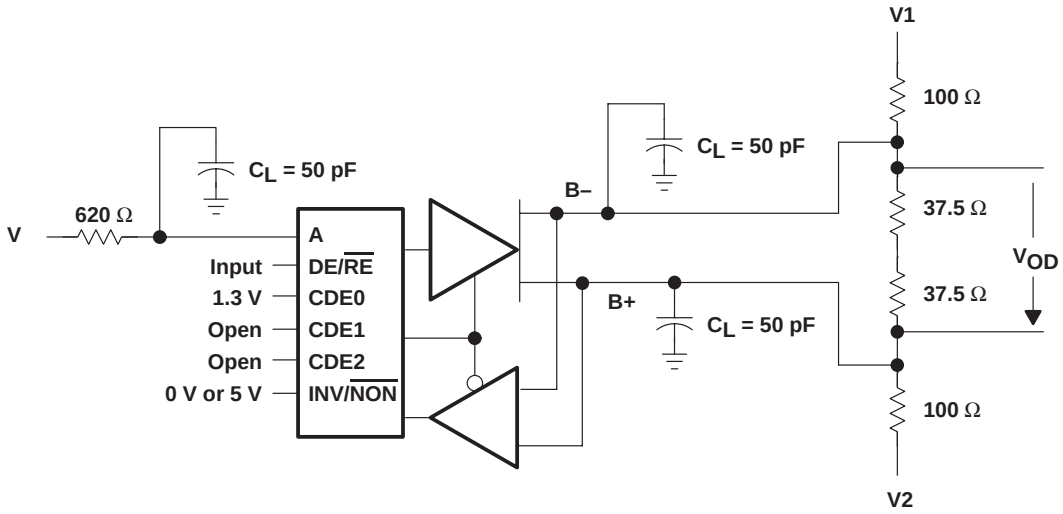
PARAMETER MEASUREMENT INFORMATION



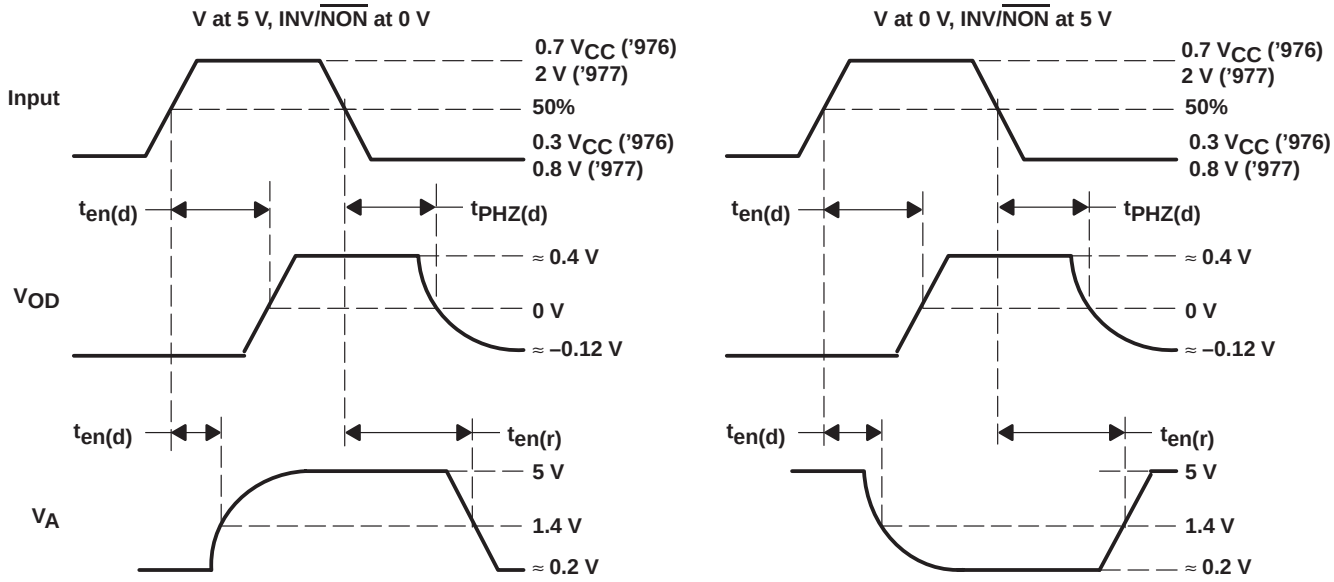
NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ±5 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.
C. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 17. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

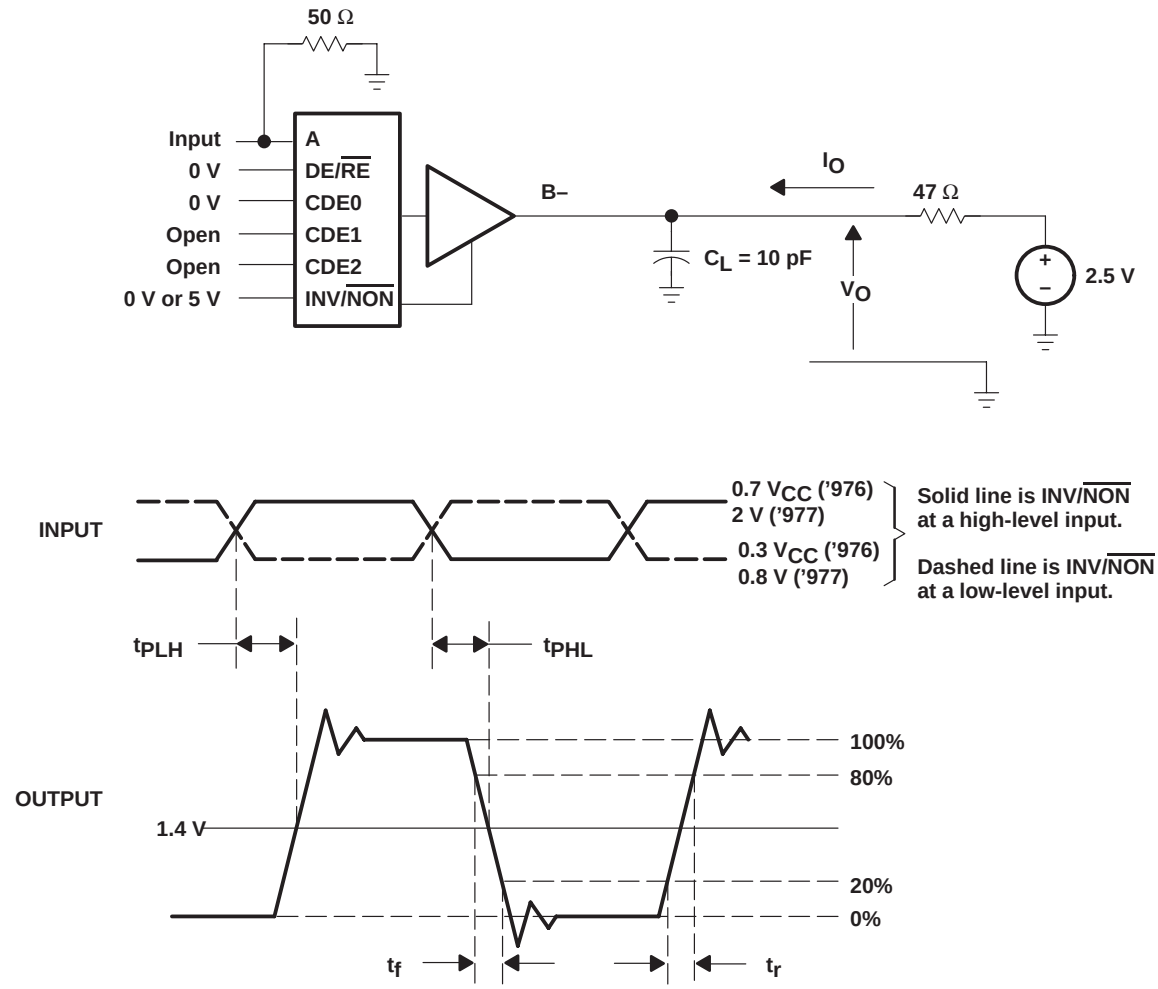


VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulsewidth = 500 ns ±50 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 18. LVD Transceiver Enable and Disable Time Test Circuit and Definitions

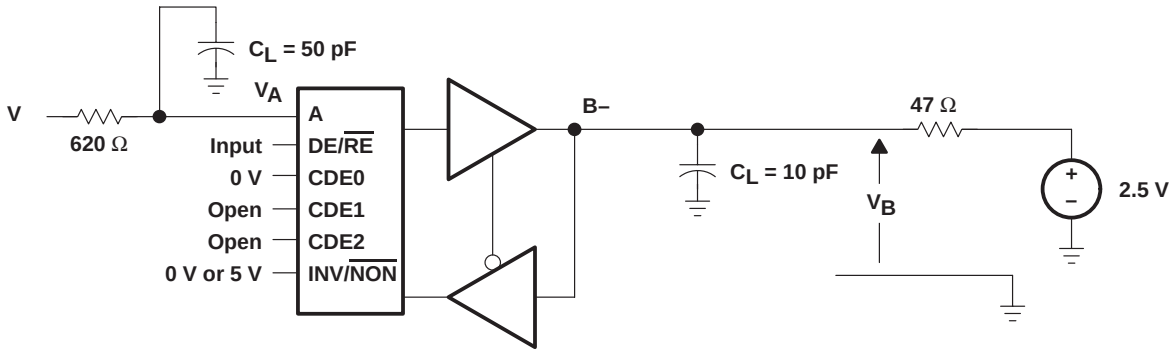
PARAMETER MEASUREMENT INFORMATION



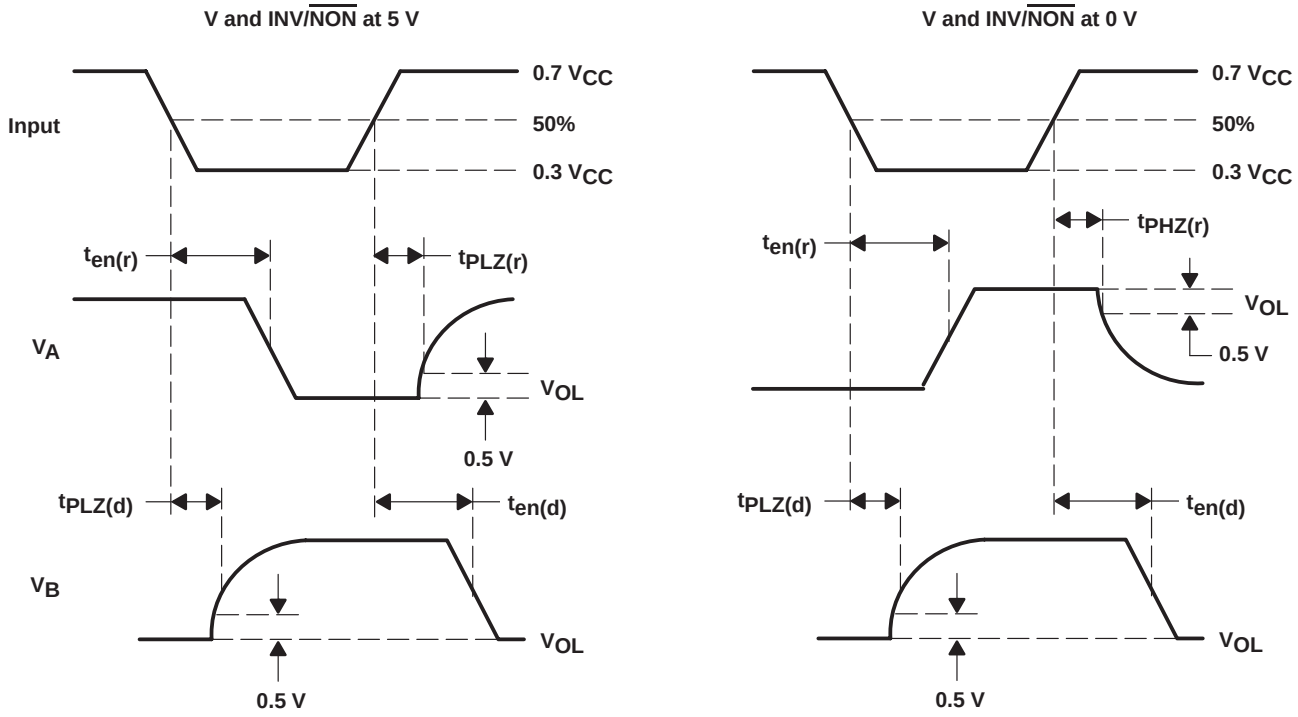
NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ±5 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 19. Single-Ended Driver Switching Test Circuit

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

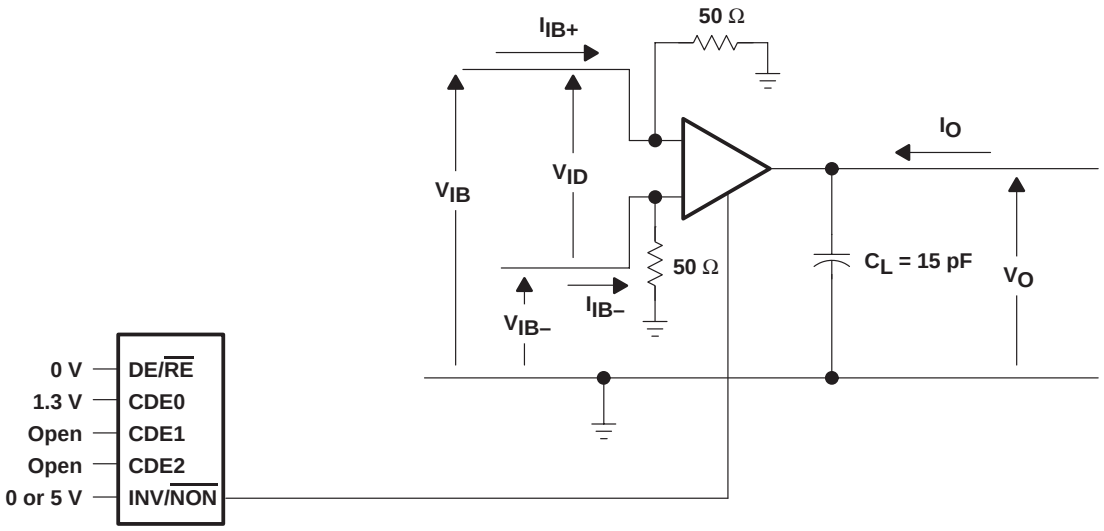


VOLTAGE WAVEFORMS

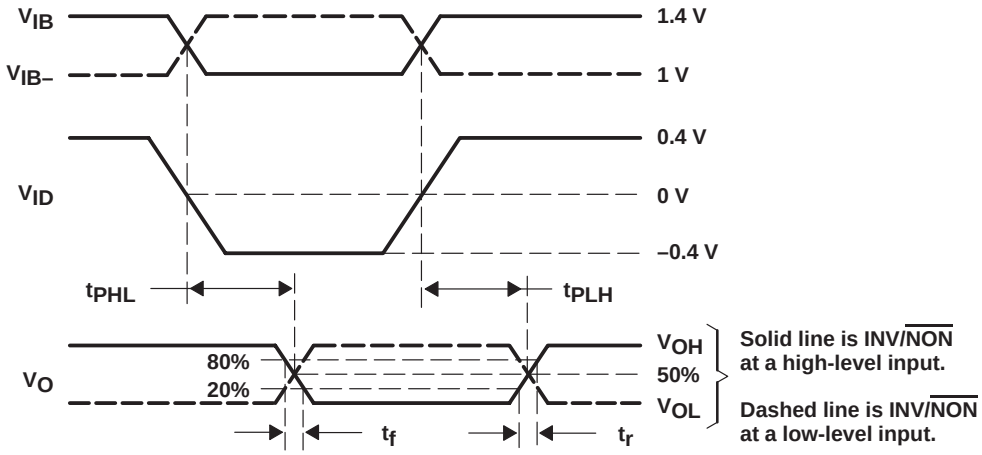
NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 1 Mpps, pulsewidth = 500 ns ±50 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 20. Single-Ended Transceiver Enable and Disable Timing Measurements

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

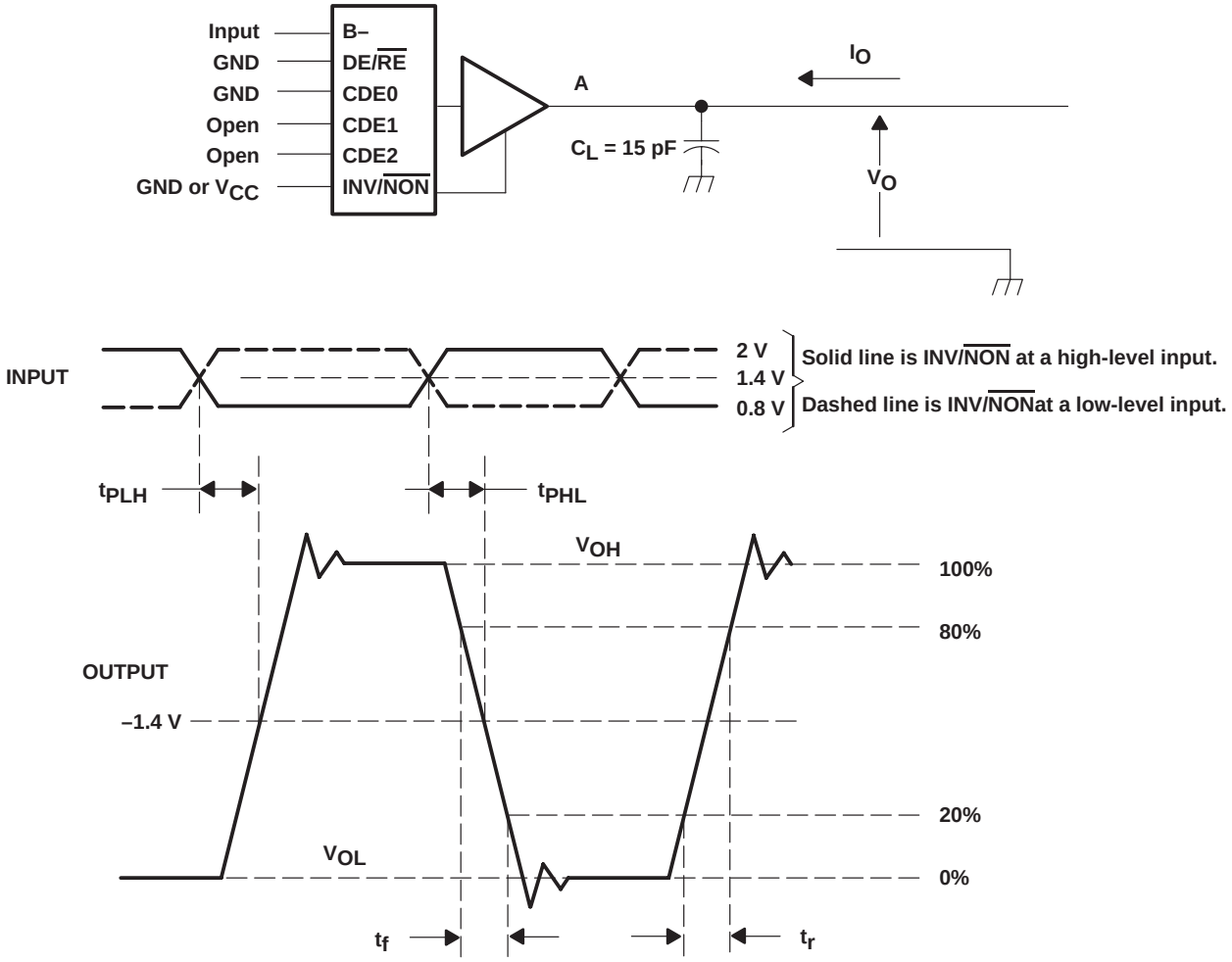


VOLTAGE WAVEFORMS

NOTES: A. Note: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \le 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ±5 ns, Z_O = 50 Ω.
B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 21. LVD Receiver Switching Characteristic Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 10 Mpps, pulsewidth = 50 ns ±5 ns.
B. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 22. Single-Ended Receiver Timing Test Circuit

APPLICATION INFORMATION

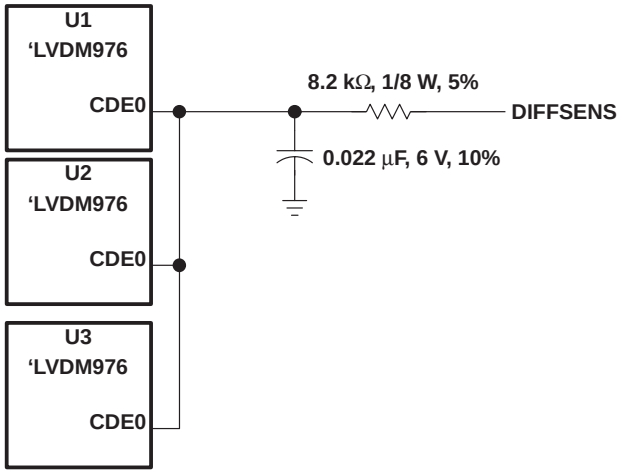
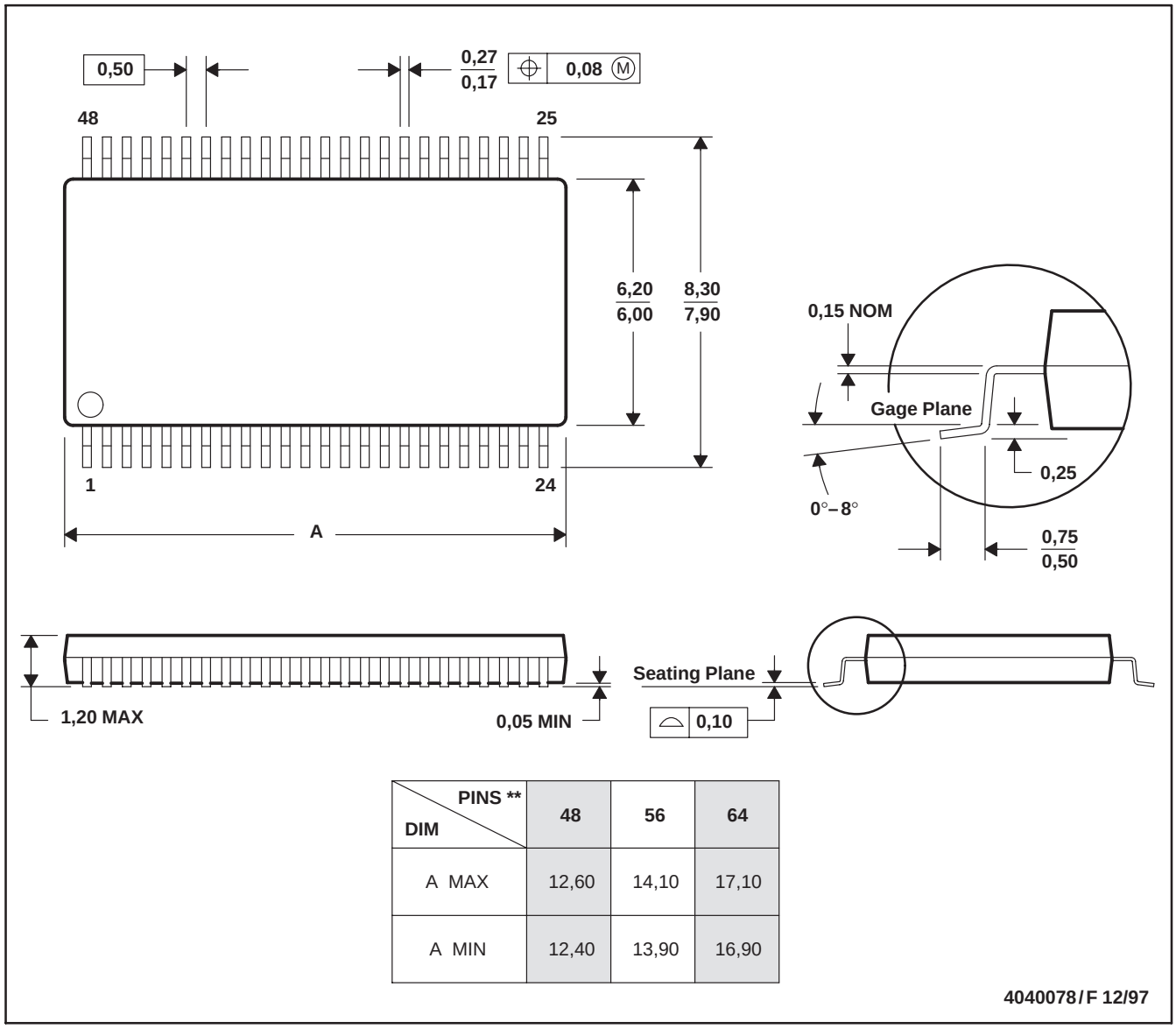


Figure 23. Low-Pass Filter for Connecting DIFFSENS to CDE0

MECHANICAL INFORMATION

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PIN SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75LVDM976DGG	ACTIVE	TSSOP	DGG	56	35	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDM976DGGR	ACTIVE	TSSOP	DGG	56	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDM976DL	ACTIVE	SSOP	DL	56	20	None	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDM976DLR	ACTIVE	SSOP	DL	56	1000	None	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDM977DGG	ACTIVE	TSSOP	DGG	56	35	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDM977DGGR	ACTIVE	TSSOP	DGG	56	2000	None	CU NIPDAU	Level-1-220C-UNLIM
SN75LVDM977DL	ACTIVE	SSOP	DL	56	20	None	CU NIPDAU	Level-2-220C-1 YEAR
SN75LVDM977DLR	ACTIVE	SSOP	DL	56	1000	None	CU NIPDAU	Level-2-220C-1 YEAR

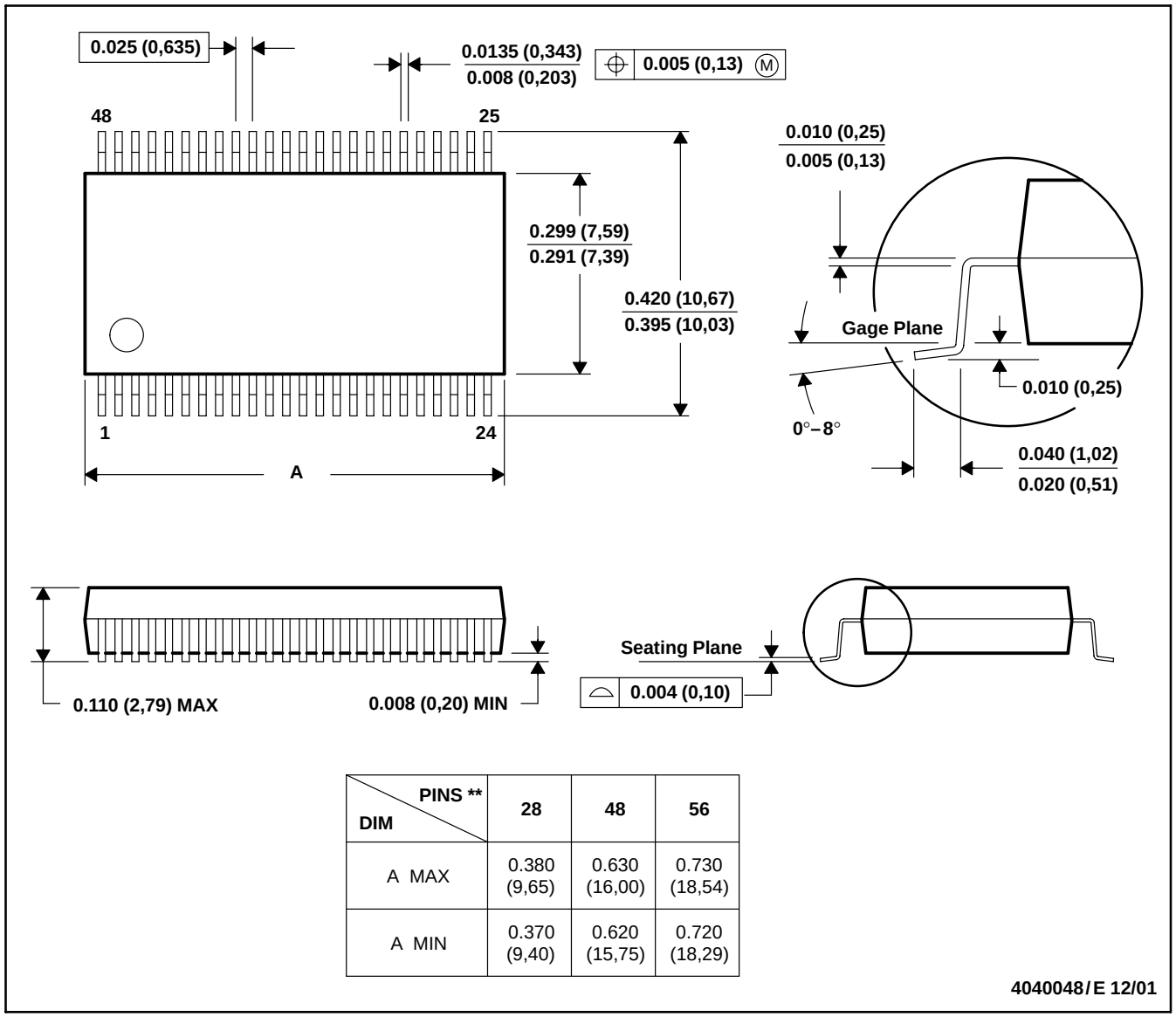
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



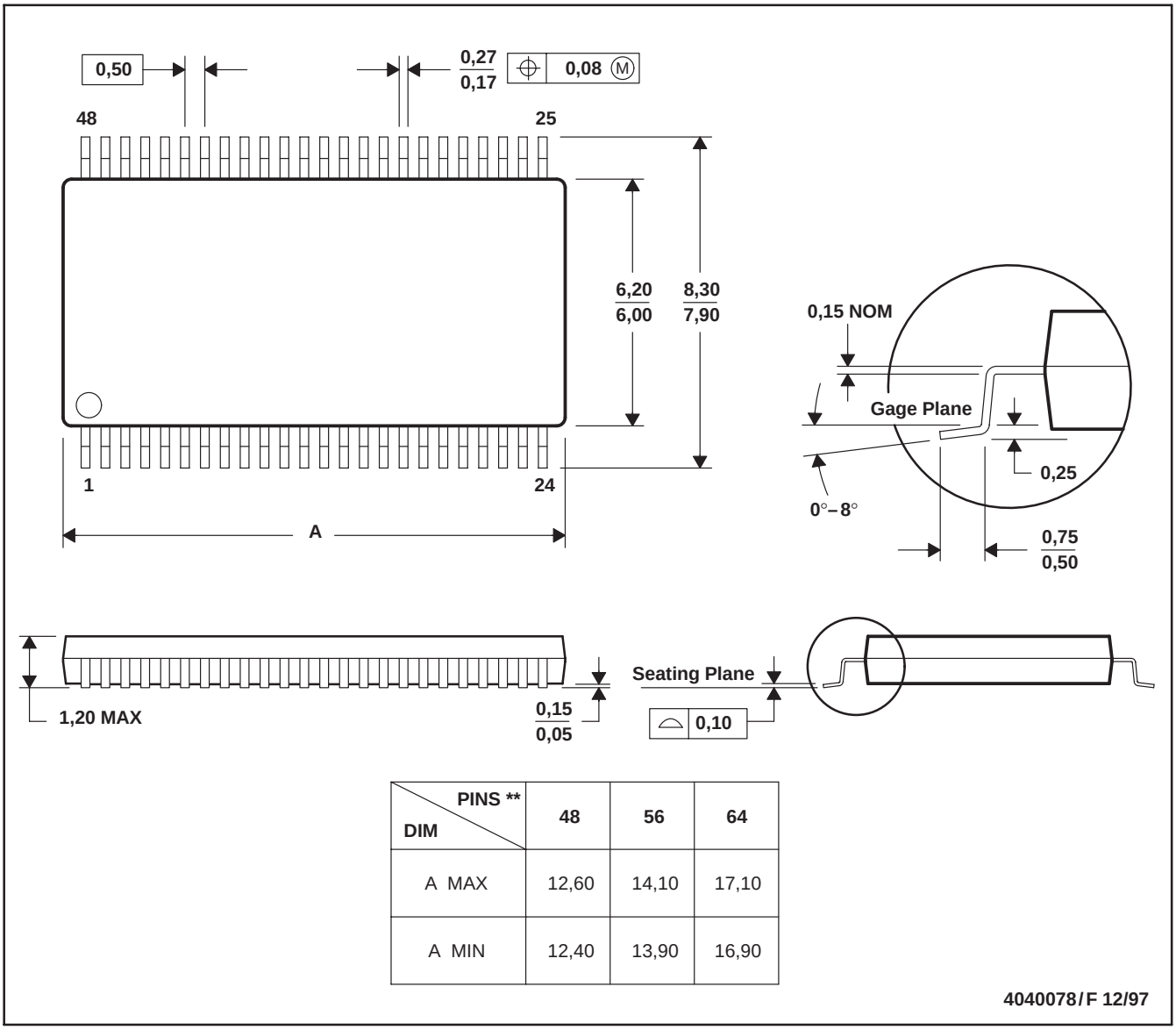
DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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