

74AHC1G125; 74AHCT1G125

Bus buffer/line driver; 3-state

Rev. 10 — 23 August 2012

Product data sheet

1. General description

74AHC1G125 and 74AHCT1G125 are high-speed Si-gate CMOS devices. They provide one non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (\overline{OE}). A HIGH at \overline{OE} causes the output to assume a high-impedance OFF-state.

The AHC device has CMOS input switching levels and supply voltage range 2 V to 5.5 V.

The AHCT device has TTL input switching levels and supply voltage range 4.5 V to 5.5 V.

2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- ESD protection:
 - ◆ HBM JESD22-A114F: exceeds 2000 V
 - ◆ MM JESD22-A115-A: exceeds 200 V
 - ◆ CDM JESD22-C101E: exceeds 1000 V
- Specified from -40°C to $+125^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74AHC1G125GW	-40°C to $+125^{\circ}\text{C}$	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm		SOT353-1
74AHCT1G125GW					
74AHC1G125GV	-40°C to $+125^{\circ}\text{C}$	SC-74A	plastic surface-mounted package; 5 leads		SOT753
74AHCT1G125GV					
74AHC1G125GM	-40°C to $+125^{\circ}\text{C}$	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1.45 \times 0.5$ mm		SOT886
74AHCT1G125GM					
74AHC1G125GF	-40°C to $+125^{\circ}\text{C}$	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1 \times 0.5$ mm		SOT891
74AHCT1G125GF					



4. Marking

Table 2. Marking codes

Type number	Marking ^[1]
74AHC1G125GW	AM
74AHCT1G125GW	CM
74AHC1G125GV	A25
74AHCT1G125GV	C25
74AHC1G125GM	AM
74AHCT1G125GM	CM
74AHC1G125GF	AM
74AHCT1G125GF	CM

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

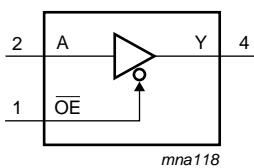


Fig 1. Logic symbol

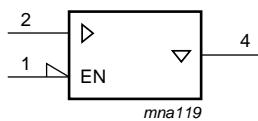


Fig 2. IEC logic symbol

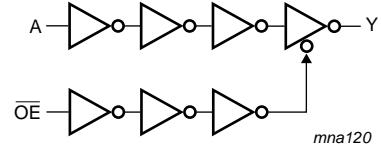


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

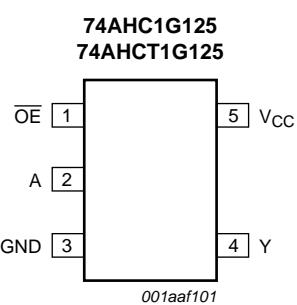


Fig 4. Pin configuration SOT353-1 and SOT753

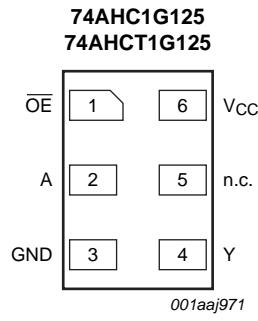


Fig 5. Pin configuration SOT886

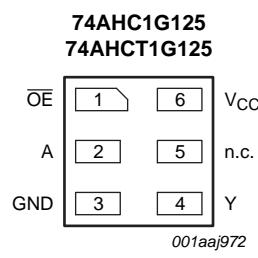


Fig 6. Pin configuration SOT891

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT353-1/SOT753	SOT886/SOT891	
OE	1	1	output enable input
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

Inputs		Output
OE	A	Y
L	L	L
L	H	H
H	X	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V	[1]	-20	- mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1]	-	±20 mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	250 mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

For XSON6 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC1G125			74AHCT1G125			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V _{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC1G125										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = −50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = −8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _{OZ}	OFF-state output current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	0.25	-	2.5	-	10	μA
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	1.0	-	10	-	40	μA

Table 7. Static characteristics ...continued
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	1.5	10	-	10	-	10	pF
74AHCT1G125										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
V_{OL}	LOW-level output voltage	$I_O = -8.0 \text{ mA}$	3.94	-	-	3.8	-	3.70	-	V
		$I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
I_{OZ}	OFF-state output current	$V_I = V_{CC} \text{ or GND}; V_{CC} = 5.5 \text{ V}$	-	-	0.25	-	2.5	-	10	μA
I_I	input leakage current	$V_I = 5.5 \text{ V or GND}; V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = 3.4 \text{ V};$ other inputs at V_{CC} or GND; $I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC1G125										
t_{pd}	propagation delay	A to Y; see Figure 7	[1]							
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2]							
		$C_L = 15 \text{ pF}$	-	4.7	8.0	1.0	9.5	1.0	11.5	ns
		$C_L = 50 \text{ pF}$	-	6.6	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50 \text{ pF}$	-	4.8	7.5	1.0	8.5	1.0	9.5	ns

Table 8. Dynamic characteristics ...continued
GND = 0 V; For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{en}	enable time	\overline{OE} to Y; see Figure 8	[1]							
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2]							
		$C_L = 15 \text{ pF}$	-	5.0	8.0	1.0	9.5	1.0	11.5	ns
		$C_L = 50 \text{ pF}$	-	6.9	11.5	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	3.6	5.1	1.0	6.0	1.0	6.5	ns
t_{dis}	disable time	\overline{OE} to Y; see Figure 8	[1]							
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2]							
		$C_L = 15 \text{ pF}$	-	6.0	9.7	1.0	11.5	1.0	12.5	ns
		$C_L = 50 \text{ pF}$	-	8.3	13.2	1.0	15.0	1.0	16.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	4.1	6.8	1.0	8.0	1.0	8.5	ns
C_{PD}	power dissipation capacitance	per buffer; $C_L = 50 \text{ pF}$; $f = 1 \text{ MHz}$; $V_I = \text{GND to } V_{CC}$	[4]	-	9	-	-	-	-	pF

74AHCT1G125

t_{pd}	propagation delay	A to Y; see Figure 7	[1]							
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	3.4	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50 \text{ pF}$	-	4.8	7.5	1.0	8.5	1.0	9.5	ns
t_{en}	enable time	\overline{OE} to Y; see Figure 8	[1]							
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	3.9	5.1	1.0	6.0	1.0	6.5	ns
		$C_L = 50 \text{ pF}$	-	5.1	7.5	1.0	8.5	1.0	9.5	ns
t_{dis}	disable time	\overline{OE} to Y; see Figure 8	[1]							
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	4.5	6.8	1.0	8.0	1.0	8.5	ns
		$C_L = 50 \text{ pF}$	-	6.1	8.8	1.0	10.0	1.0	11.0	ns

Table 8. Dynamic characteristics ...continued
GND = 0 V; For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation per buffer; capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	[4]	-	11	-	-	-	-	pF

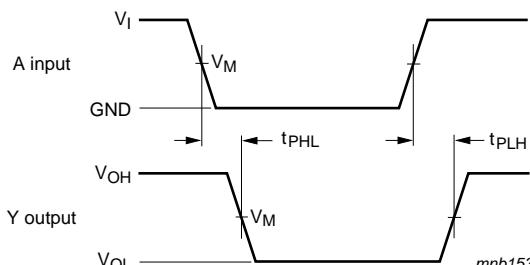
[1] t_{pd} is the same as t_{PLH} and t_{PHL} .
 t_{en} is the same as t_{PZL} and t_{PZH} .
 t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[2] Typical values are measured at $V_{CC} = 3.3 \text{ V}$.

[3] Typical values are measured at $V_{CC} = 5.0 \text{ V}$.

[4] C_{PD} is used to determine the dynamic power dissipation P_D (μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in Volts.

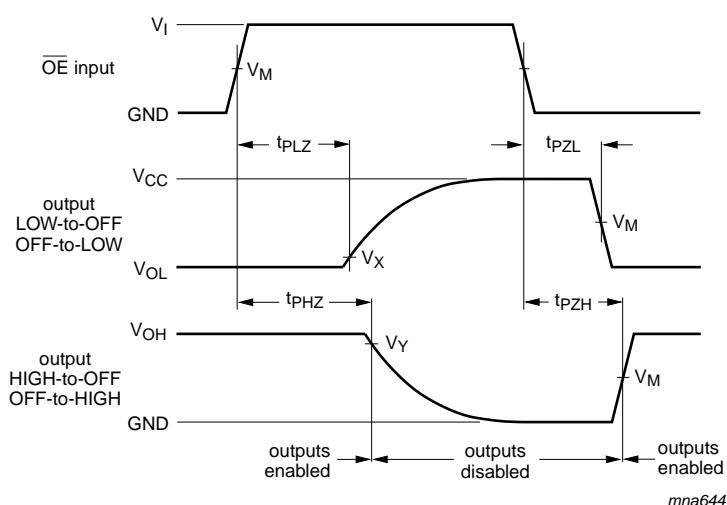
12. Waveforms



Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. Input (A) to output (Y) propagation delays



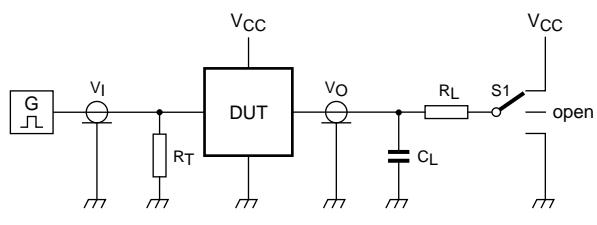
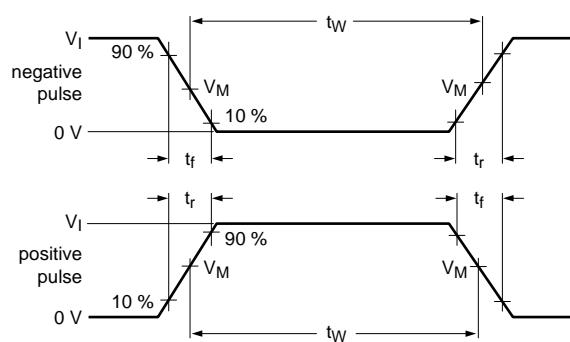
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. Enable and disable times

Table 9. Measurement point

Type	Inputs		Output		
	V_I	V_M	V_M	V_X	V_Y
74AHC1G125	GND to V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V
74AHCT1G125	GND to 3.0 V	1.5 V	$0.5V_{CC}$	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V



001aad983

Test data is given in [Table 10](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

$S1$ = Test selection switch.

Fig 9. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC1G125	V_{CC}	≤ 3 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}
74AHCT1G125	3 V	≤ 3 ns	15 pF, 50 pF	1 k Ω	open	GND	V_{CC}

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

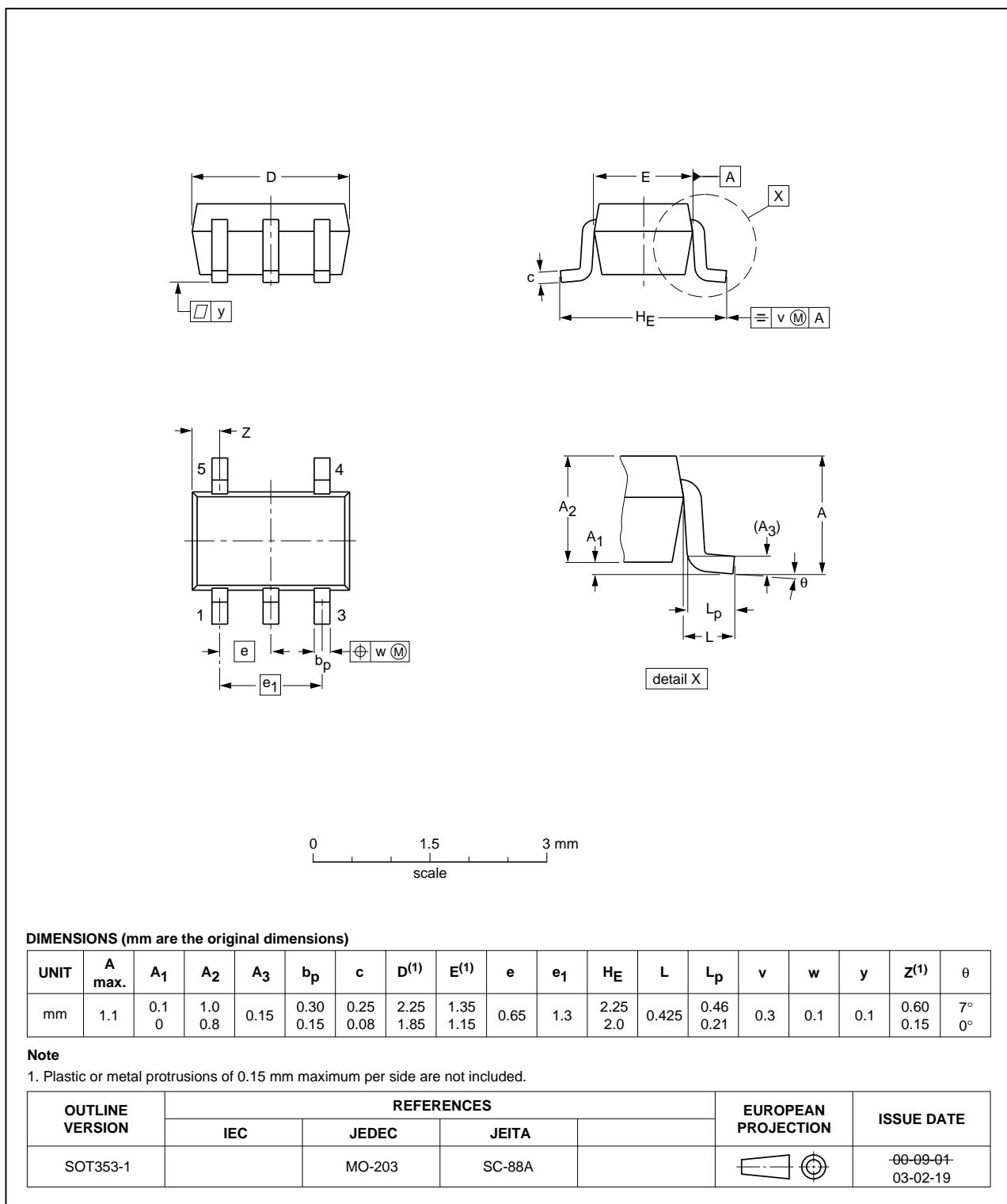


Fig 10. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

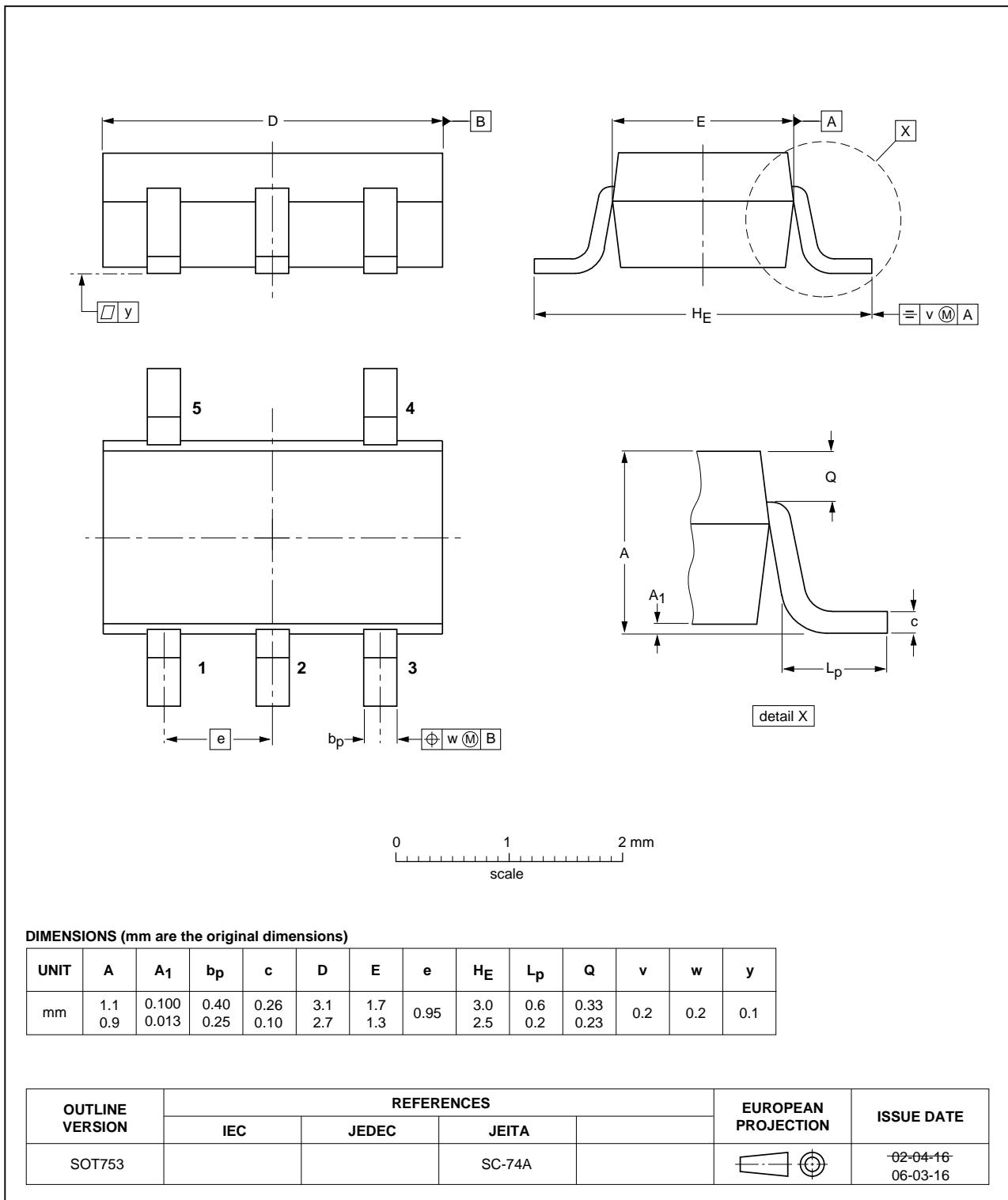


Fig 11. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body $1 \times 1.45 \times 0.5$ mm

SOT886

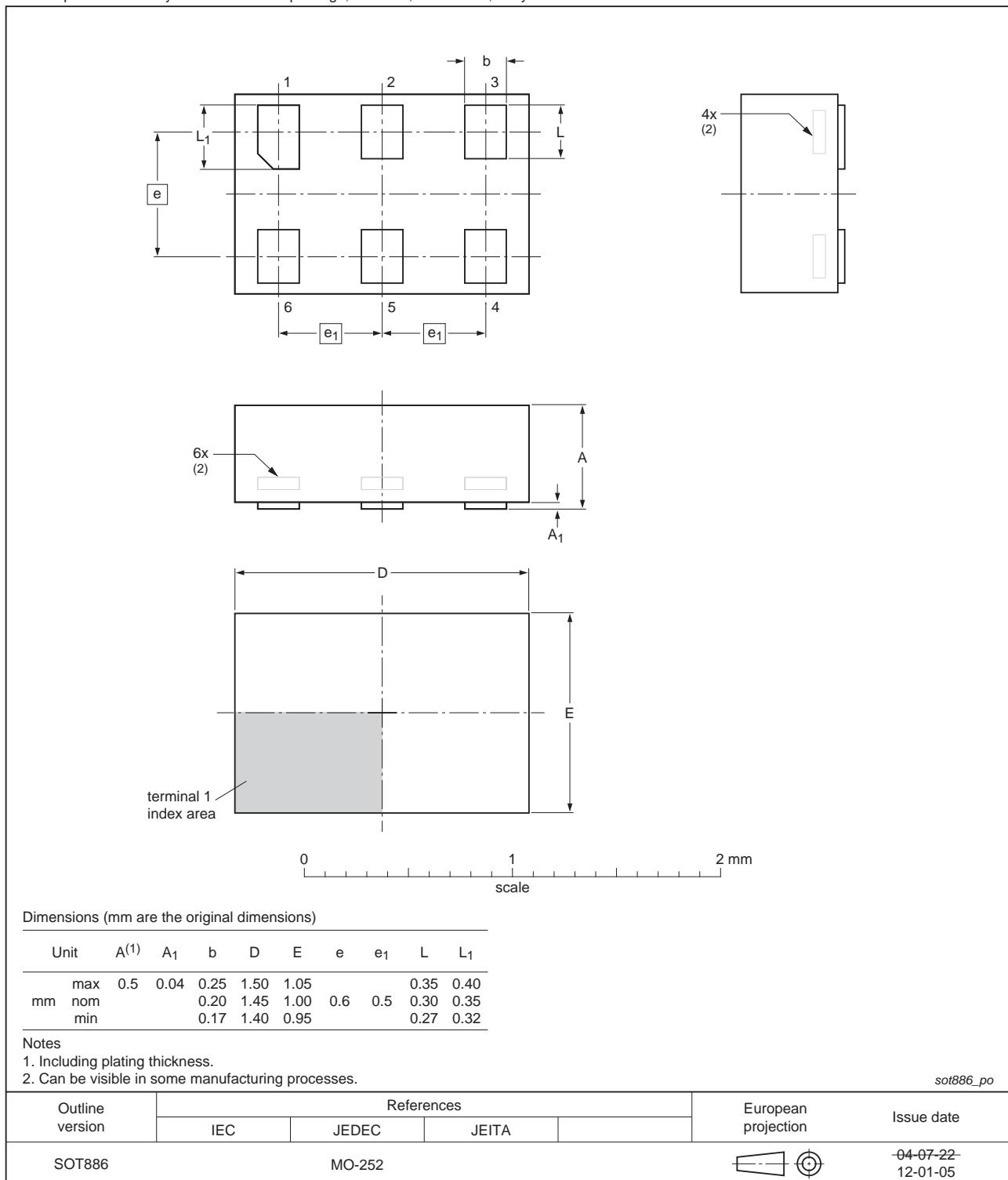
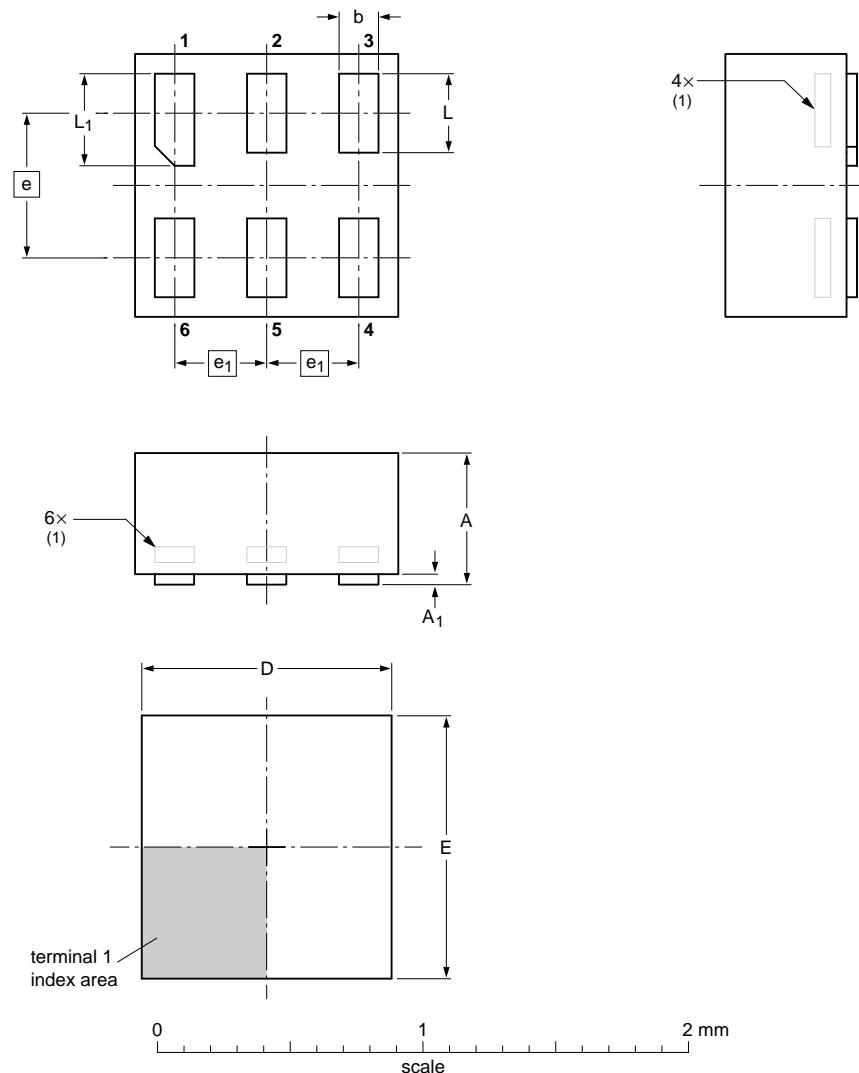


Fig 12. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max}	A _{1max}	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.20 0.12	1.05 0.95	1.05 0.95	0.55	0.35	0.35 0.27	0.40 0.32

Note

1. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT891						05-04-06 07-05-15

Fig 13. Package outline SOT891 (XSON6)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G125 v10	20120823	Product data sheet	-	74AHC_AHCT1G125 v.9
Modifications:		• Package outline drawing of SOT886 (Figure 12) modified.		
74AHC_AHCT1G125 v.9	20090622	Product data sheet	-	74AHC_AHCT1G125 v.8
74AHC_AHCT1G125 v.8	20090409	Product data sheet	-	74AHC_AHCT1G125 v.7
74AHC_AHCT1G125 v.7	20070707	Product data sheet	-	74AHC_AHCT1G125 v.6
74AHC_AHCT1G125 v.6	20020606	Product specification	-	74AHC_AHCT1G125 v.5
74AHC_AHCT1G125 v.5	20020322	Product specification	-	74AHC_AHCT1G125 v.4
74AHC_AHCT1G125 v.4	20010222	Product specification	-	74AHC_AHCT1G125 v.3
74AHC_AHCT1G125 v.3	19990615	Product specification	-	74AHC_AHCT1G125_N v.2
74AHC_AHCT1G125_N v.2	19981207	Preliminary specification	-	74AHC_AHCT1G125_N v.1
74AHC_AHCT1G125_N v.1	19981125	Preliminary specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

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