# ISL8216M

Complete High Voltage 80V, 4A DC/DC Power Module

FN8607
Rev 2.00
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The ISL8216M is a simple and easy to use, high voltage DC/DC module and is ideal for a wide variety of applications. It eliminates design and manufacturing risks while dramatically improving time to market.

The simplicity is in the "Off-The-Shelf" unassisted implementation. All you need is the ISL8216M, input and output capacitors, and one resistor to program the output voltage and you have a complete high voltage power design ready for the market.

The ISL8216M is packaged in a thermally enhanced, compact (15mm×15mm×3.6mm) over-molded High-Density Array (HDA) Package, which permits full load operation without heat sink or fans. The package is suitable for automated assembly by standard surface mount equipment. The small amount of external components reduce the PCB to a component layer and a simple ground layer.

## Related Literature

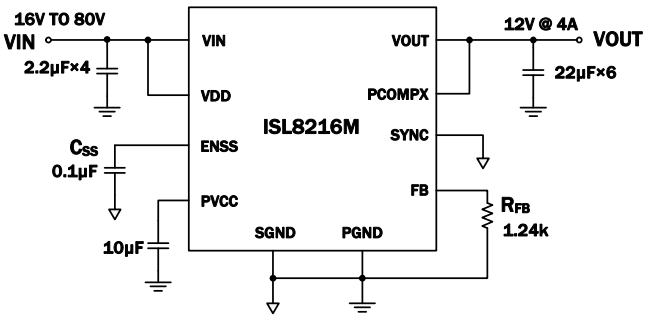
- AN1907 "ISL8216MEVAL1Z Evaluation Board User's Guide"

## Features

- Complete switch mode power supply in one package
- Wide input voltage range: 10V to 80V
- Output current 4A
- Programmable soft-start
- Compliant with EN 55022 Class B (see AN1907)
- SYNC and adjustable frequency 200kHz to 600kHz
- Single resistor sets $V_{OUT}$ +2.5V up to +30V
- Setpoint accuracy ±1.5%
- Programmable overcurrent protection
- RoHS compliant with exemption
- Small footprint, low profile (15mm×15mm×3.6mm)

## Applications

- Servers
- 48V telecom and datacom applications
- 12V and 42V automotive and industrial equipment
- Distributed power converters and point-of-load (POL) regulation
- General purpose step-down DC/DC




NOTE: ALL PINS NOT SHOWN ARE FLOATING

FIGURE 1. TYPICAL APPLICATION CIRCUIT

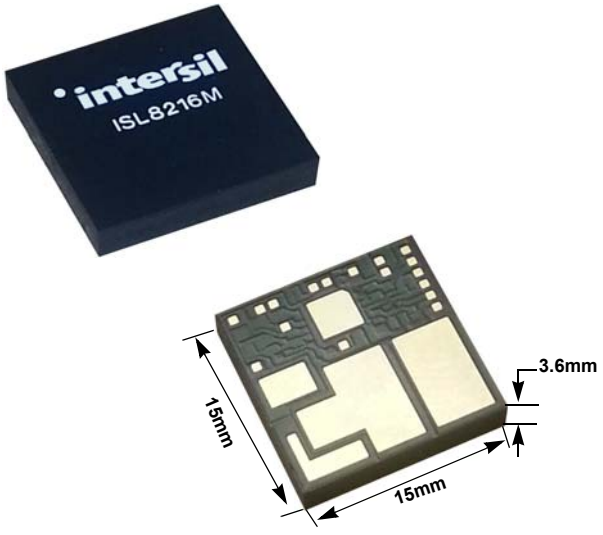



FIGURE 2. SMALL FOOTPRINT PACKAGE WITH LOW PROFILE (3.6mm)

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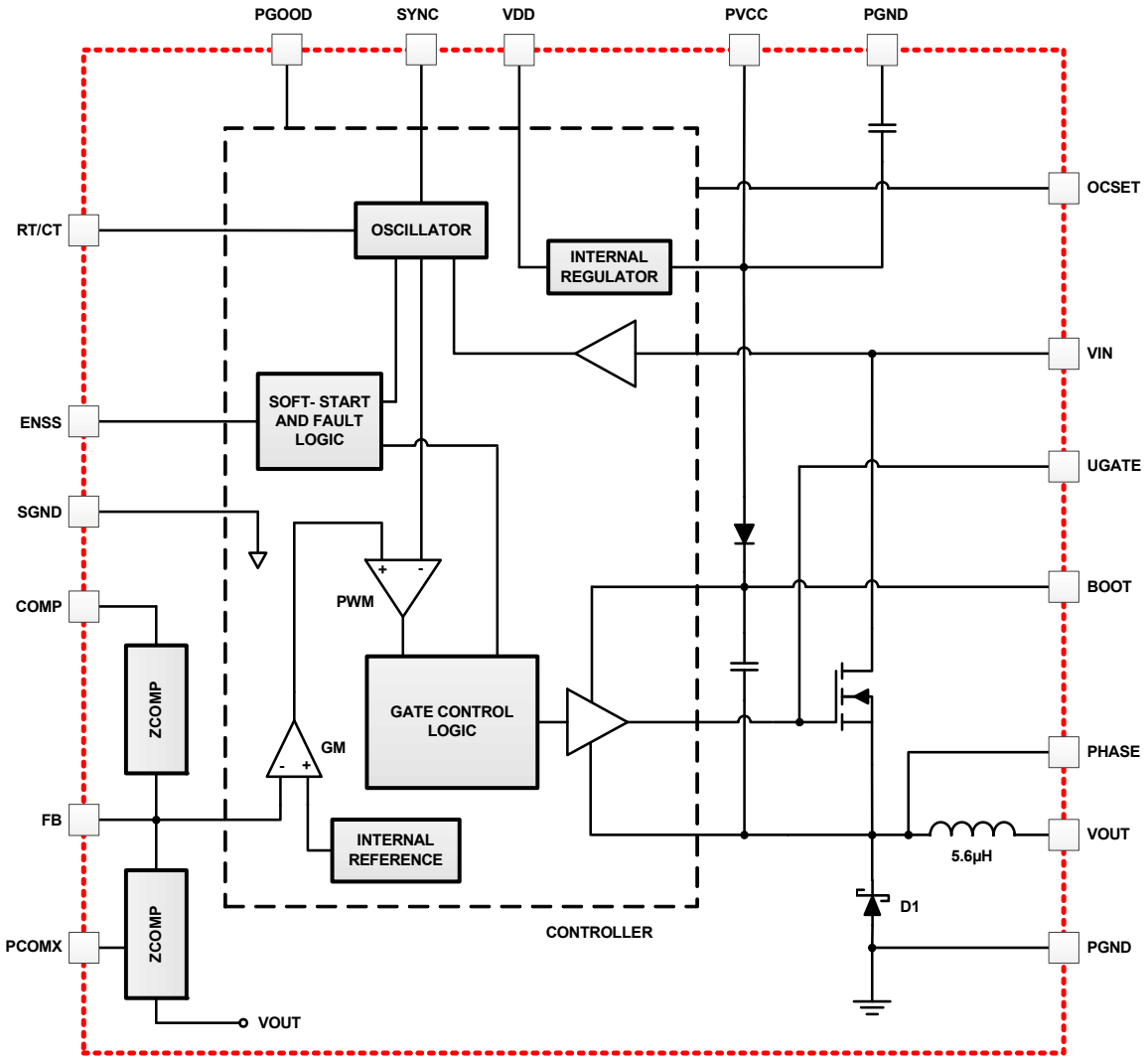
# Internal Block Diagram




# Ordering Information

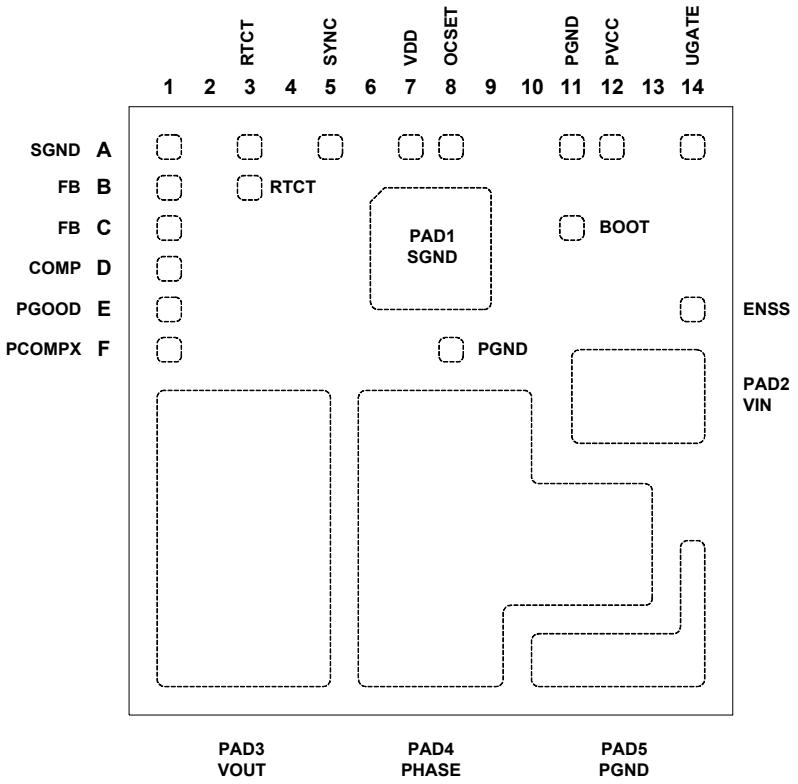
| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP RANGE (°C) | PACKAGE (RoHS Compliant) | PKG. DWG. # |
|---|---|---|---|---|
| ISL8216MIRZ | ISL8216M | -40 to +85 | 22 Ld HDA | Y22.15x15 |
| ISL8216MEVAL1Z | Evaluation Board | | | |

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant by EU exemption 7C-I and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL8216M. For more information on MSL, please see tech brief TB363

# Pin Configuration

ISL8216M
(22 LD HDA)
TOP VIEW



# Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | PIN DESCRIPTION |
|---|---|---|---|
| A1 | SGND | PWR | **Control signal ground**. All voltage levels are measured with respect to this pin. |
| A3, B3 | RTCT | I | **Frequency setting pin**. This pin sets the frequency of the sawtooth oscillator. The module has a resistor and a capacitor internally, which set the default frequency to 300kHz. Connect an external resistor to VIN and an external capacitor to SGND to change the frequency of the sawtooth oscillator. See "Oscillator and Frequency Synchronization" on page 12. Range: 0V to $V_{IN}$. |
| A5 | SYNC | I | **Signal synchronization**. The switching frequency can be synchronized to an external clock through this pin. When the sync function is not used, this pin must be tied to ground. If the sync function is used, the RTCT natural frequency must be set to a frequency lower than the sync input frequency. See "Oscillator and Frequency Synchronization" on page 12. Range: 0V to 5V. |
| A7 | VDD | PWR | **Power connection for the internal controller**. Tie to VIN directly. A decoupling ceramic capacitor between this pin and signal ground (SGND) is optional. |
| A8 | OCSET | I | **Current limit sensing pin**. The current limit can be reduced by placing a resistor, $R_{OCSET\_EX}$, between this pin and VIN. See "Overcurrent Protection" on page 13. Range: 0V to $V_{IN}$. |
| A11, F8 | PGND | PWR | **Power ground**. These pins provides the power ground to the internal controller IC. Tie these pins to the power ground plane through the lowest impedance connection. These pins are not internally connected to PAD5. |
| A12 | PVCC | PWR | **Internal linear regulator output**. Typical: 11V. |
| A14 | UGATE | - | **Test pin**. This pin must be floating. Avoid routing any trace close to this pin, as voltage on this pin can be as high as 100V. |
| B1, C1 | FB | I | **Feedback pin**. Output voltage is set by an external resistor between FB to SGND. Refer to Equation 1 and Table 1 on page 10. Typical: 1.2V |
| C11 | BOOT | PWR | **Floating bootstrap supply pin for the MOSFET gate driver**. The module has a bootstrap diode and a bootstrap capacitor internally. This pin can be used to provide an additional current path for charging the internal bootstrap capacitor; the charging current is derived from VIN through a resistor. See Figure 23, on page 14. Range: 0V to 92V. |
| D1 | COMP | I/O | **Error amplifier output**. This pin is connected to the output of the transconductance error amplifier and may be used to compensate the feedback loop. Range: 0V to 12V. |
| E1 | PGOOD | O | **Power good**. Provides a power good status. An open drain output is asserted when the voltage at the FB pins is within ±14% of the reference voltage. See "Power-Good" on page 14. Range: 0V to 12V. |
| E14 | ENSS | I/O | **Enable and soft-start pin**. This pin provides enable/disable functionality and soft-start timing functionality for the PWM output. Connect a capacitor to SGND to set the soft-start time. See "Enable/Soft-Start" on page 11. The module is disabled when this pin is held below 0.5V. To use this pin as an enable control pin, connect to a device with open drain output, or alternatively to an external enable control circuit, as shown in Figure 18. Range: 0V to 5V. |
| F1 | PCOMPX | I | **Compensation adjustment pin**. Short this pin to VOUT if the output capacitors are all ceramic capacitors. Connect a lower than 1kΩ resistor to VOUT if the output capacitors are tantalum capacitors, polymer capacitors, or aluminum electrolytic capacitors. Range: 1.2V to 30V. |
| PAD1 | SGND | PWR | **Signal ground of the internal controller**. All voltage levels are measured with respect to this pad. This pad is electrically isolated. Connect this pad to the signal ground plane using multiple vias for a robust thermal conduction path. |
| PAD2 | VIN | PWR | **Power input pin.** Apply input voltage between VIN and PGND (PAD5). It is recommended to place an input decoupling capacitor directly between VIN pin and PGND. The input capacitor should be placed as closely as possible to the module. Range: 10V to 80V. |
| PAD3 | VOUT | PWR | **Power output pin**. Apply output load between VOUT and PGND (PAD5). Place a high frequency output decoupling capacitor directly between VOUT and PGND (PAD5). The output capacitor should be placed as closely to the module as possible. Range: 1.2V to 30V. |
| PAD4 | PHASE | PWR | **Phase node**. The PHASE pin should be floating. To achieve better thermal performance, the phase planes can also be used for heat removal with thermal vias connected to large inner layers. |
| PAD5 | PGND | PWR | **Power Ground**. Power ground pins for both input and output returns. Connect to power ground plane immediately below the module to maximize heat dissipation and to minimize the effect of switching noise and power loss due to the impedance of the copper traces. |

## Absolute Maximum Ratings

Input Voltage (VIN,VDD) . . . . . 100V
BOOT . . . . . 105V
ENSS pin . . . . . 6V
FB, COMP, SYNC pins . . . . . 8V
PHASE (Note 4) . . . . . 100V
ESD Rating
Human Body Model (Tested per JESD22-A114E) . . . . . 2kV
Machine Model (Tested per JESD22-A115-A) . . . . . 200V
Charge Device Model (Tested per JESD22-C101C) . . . . . 750V
Latch Up (Tested per JESD-78B; Class 2, Level A) . . . . . 100mA

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 22 Ld HDA (Notes 5, 6) | 13 | 2.6 |

Storage Temperature Range, ($T_{STG}$) . . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

## Recommended Operating Ratings

Input Supply Voltage ($V_{IN}$) . . . . . +10V to +80V
VDD . . . . . +10V or +80V
Output Voltage ($V_{OUT}$) . . . . . +2.5V to +30V
Ambient Temperature Range ($T_A$) . . . . . -40°C to +85°C
Junction Temperature Range, ($T_J$) . . . . . -40°C to +125°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $V_{AC}$ (Anode to Cathode) specification for internal power diode.
5. $\theta_{JA}$ is tested in free air with device mounted on a four-layer FR-4 test board (76.2x76.2x1.6mm) with 80% coverage, 2oz Cu on top and bottom layers, plus two, buried, 1oz Cu layers with coverage across the entire test board area. Multiple vias were used, with via diameter = 0.3mm on 1.2mm pitch.
6. For $\theta_{JC}$, the “case” temperature is measured at the center of the package underside.

## Electrical Specifications

$T_A$ = +25°C. $V_{IN}$ = 24V, $V_{OUT}$ = 12V, $f_{SW}$ = 300kHz, $C_{IN}$ = 1x100µF ALUM and 2x2.2µF Ceramic, $C_{OUT}$ = 6x22µF Ceremic, unless otherwise noted.

| PARAMETER | SYMBOL | CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **$V_{DD}$ SUPPLY** | | | | | | |
| Bias Voltage Range | | | 10 | - | 80 | V |
| Bias Supply Current | $I_{VIN}$ | $V_{IN}$ = $V_{DD}$ = 24V, $V_{OUT}$ = 12V, $I_{OUT}$ = 0A | - | 14 | - | mA |
| $V_{DD}$ Shutdown Current | $I_{VIN\_SD}$ | $V_{IN}$ = $V_{DD}$ = 24V, ENSS = 0V | - | 20 | - | µA |
| **INTERNAL LINEAR REGULATOR (PVCC)** (Note 9) | | | | | | |
| Output Voltage | PVCC | $V_{DD}$ = 15V to 80V, Load = 3mA to 20mA | - | 10 | - | V |
| Maximum Output Current | | | 20 | - | - | mA |
| Short Current Protection | | | - | 60 | - | mA |
| **POWER-ON RESET** (Note 9) | | | | | | |
| Rising $V_{DD}$ Threshold | | | 6.8 | 7.8 | 8.5 | V |
| Falling $V_{DD}$ Threshold | | | - | 220 | - | mV |
| **OSCILLATOR** (Note 9) | | | | | | |
| Total Variation on Set Frequency | | $f_{SW}$ = 300kHz | - | ±10 | - | % |
| Frequency Range | | Set by $R_T$ and $C_T$. $R_T$ range = 20k to 100k, $C_T$ range = 470pF to 1200pF | 200 | - | 600 | kHz |
| SYNC Frequency Range | | above $R_T$ and $C_T$ natural frequency | 200 | - | 600 | kHz |
| Ramp Amplitude | $\Delta V_{OSC}$ | $V_{DD}$ varied from 9.0V to 75V | - | 0.11*$V_{IN}$ | - | $V_{P-P}$ |
| Min OFF Time | | | - | 190 | 300 | ns |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output Continuous Current Range | $IOUT_{(DC)}$ | | 0 | - | 4 | A |
| Line Regulation Accuracy | $\Delta V_{OUT}/\Delta V_{IN}$ | $V_{OUT}$ = 12V, $I_{OUT}$ = 0A, $V_{IN}$ = 15V - 75V | - | 0.005 | - | % |
| | | $V_{OUT}$ = 12V, $I_{OUT}$ = 4A, $V_{IN}$ = 15V - 75V | - | 0.005 | - | % |
| Load Regulation Accuracy | $\Delta V_{OUT}/\Delta I_{OUT}$ | $V_{IN}$ = 80V, $C_{IN}$ = 2x100µF ALUM, 3x4.7µF ceramic capacitor, $V_{OUT}$ = 12V, $C_{OUT}$ = 2x100µF ALUM, 2x10µF ceramic capacitor, $I_{OUT}$ = 0A to 4A, $f_{SW}$ = 300kHz". | - | - | 0.15 | % |

**Electrical Specifications** $T_A$ = +25°C. $V_{IN}$ = 24V, $V_{OUT}$ = 12V, $f_{SW}$ = 300kHz, $C_{IN}$ = 1x100µF ALUM and 2x2.2µF Ceramic, $C_{OUT}$ = 6x22µF Ceremic, unless otherwise noted. **(Continued)**

| PARAMETER | SYMBOL | CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| Output Ripple Voltage | $\Delta V_{OUT}$ | $I_{OUT}$ = 4A, $V_{OUT}$ = 12V, $V_{IN}$ = 24V, $f_{SW}$ = 400kHz | - | 40 | - | $mV_{P-P}$ |
| | | $I_{OUT}$ = 0A, $V_{OUT}$ = 12V, $V_{IN}$ = 24V, $f_{SW}$ = 400kHz | - | 10 | - | $mV_{P-P}$ |
| | | $I_{OUT}$ = 4A, $V_{OUT}$ = 12V, $V_{IN}$ = 80V, $f_{SW}$ = 400kHz | - | 60 | - | $mV_{P-P}$ |
| | | $I_{OUT}$ = 0A, $V_{OUT}$ = 12V, $V_{IN}$ = 80V, $f_{SW}$ = 400kHz | - | 20 | - | $mV_{P-P}$ |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Voltage Change For Positive Load Step | $\Delta V_{OUT-DP}$ | $I_{OUT}$ = 1A to 4A. Current slew rate = 2.5A/µs, $V_{IN}$ = 24V, $V_{OUT}$ = 12V | - | 220 | - | $mV_{P-P}$ |
| Voltage Change For Negative Load Step | $\Delta V_{OUT-DN}$ | $I_{OUT}$ = 4A to 1A. Current slew rate = 2.5A/µs, $V_{IN}$ = 24V, $V_{OUT}$ = 12V | - | 180 | - | $mV_{P-P}$ |
| **REFERENCE VOLTAGE** (Note 9) | | | | | | |
| Feedback Voltage | $V_{FB}$ | | - | 1.192 | - | V |
| Accuracy | | | -1.0 | - | +1.0 | % |
| **ENABLE/SS** (Note 9) | | | | | | |
| Soft-Start Current | $I_{SS}$ | VENSS = 0V | - | 2 | - | µA |
| | | VENSS = 1.3V | 22 | 33 | 43 | µA |
| Enable Threshold | $V_{EN}$ | Voltage level where soft-start current changes from low-to-high | 0.5 | 0.77 | 1.0 | V |
| Maximum Disable Voltage | $V_{DISEN}$ | | - | - | 0.5 | V |
| **ERROR AMPLIFIER** (Note 9) | | | | | | |
| Transconductance | | | 4.2 | 5.7 | 7.2 | mS |
| Gain-Bandwidth Product (Note 10) | GBW | | - | 15 | - | MHz |
| Slew Rate (Note 10) | SR | | - | 6 | - | V/µs |
| COMP Pin Drive (Note 10) | $I_{COMP}$ | | - | ±300 | - | µA |
| **POWER GOOD (OPEN DRAIN)** (Note 9) | | | | | | |
| Power-Good Lower Threshold | $V_{PG-}$ | Percentage of Nominal VFB; ~ 3µs noise filter | 84 | - | 88 | % |
| Power-Good Higher Threshold | $V_{PG+}$ | Percentage of Nominal VFB; ~ 3µs noise filter | 112 | - | 116 | % |
| PGOOD Leakage Current | $I_{PGLKG}$ | $V_{PULLUP}$ = 5.5V | - | - | 1 | µA |
| PGOOD Voltage Low | | $I_{PGOOD}$ = 4mA | - | - | 0.5 | V |
| **OVERCURRENT PROTECTION** (Note 9) | | | | | | |
| Dynamic Current Limit OFF-time | $t_{OCOFF}$ | | - | 4 | - | SS cycle |
| OCP (OCSET) Current Source | $I_{OCSET}$ | | 89 | 104 | 119 | µA |

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. Parameters with TYP limits are not production tested unless otherwise specified.
9. Parameters with MIN and/or MAX limits are 100% tested for internal IC prior to module assembly, unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. Limits should be considered typical and are not production tested.

# Typical Performance Characteristics

## Efficiency Performance

$T_A$ = +25°C. The efficiency equation is as follows:

$$\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{P_{OUT}}{P_{IN}} = \frac{(V_{OUT} x I_{OUT})}{(V_{IN} x I_{IN})}$$

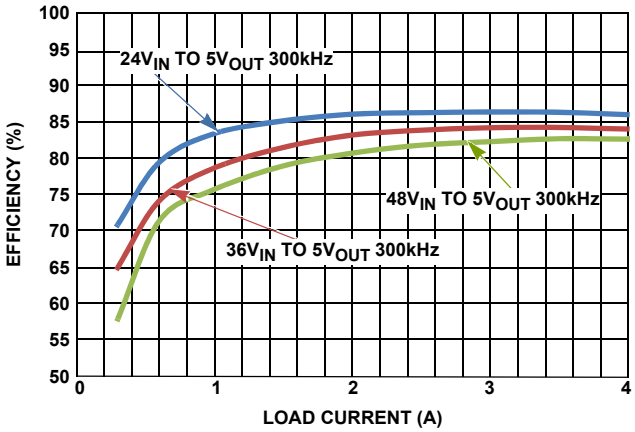



FIGURE 3. EFFICIENCY vs LOAD CURRENT ($5V_{OUT}$ AT 300kHz)

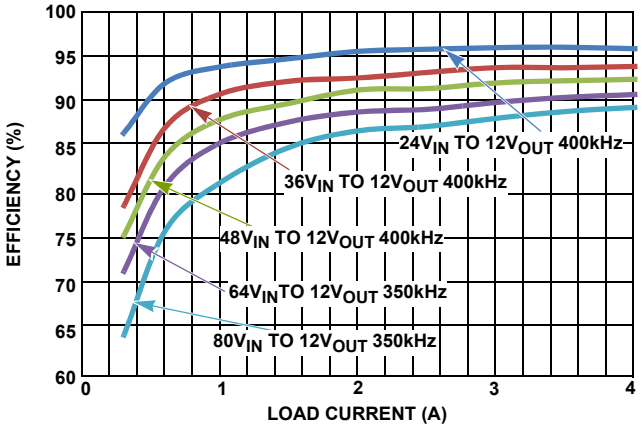



FIGURE 4. EFFICIENCY vs LOAD CURRENT ($12V_{OUT}$)

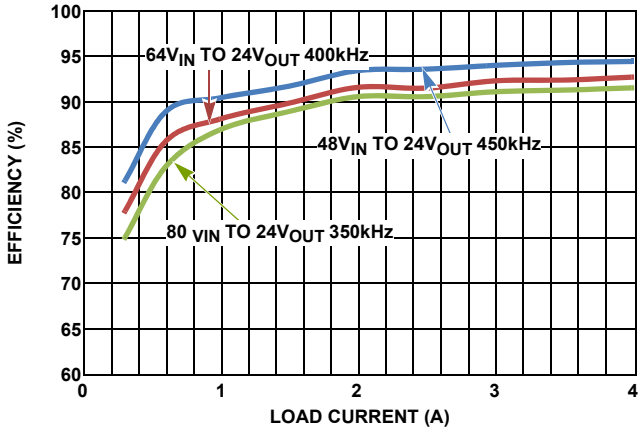



FIGURE 5. EFFICIENCY vs LOAD CURRENT ($24V_{OUT}$)

# Typical Performance Characteristics

## Transient Response Performance

$C_{OUT}$ = 6x22µF ceramic capacitors, $I_{OUT}$ = 1A to 4A, current slew rate = 2.5A/µs. $T_A$ = +25°C.

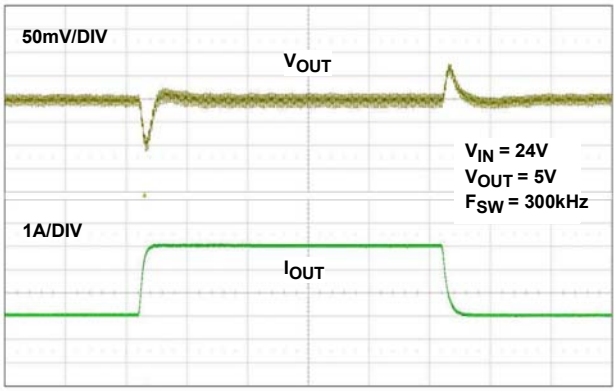



FIGURE 6. $5V_{OUT}$ TRANSIENT RESPONSE

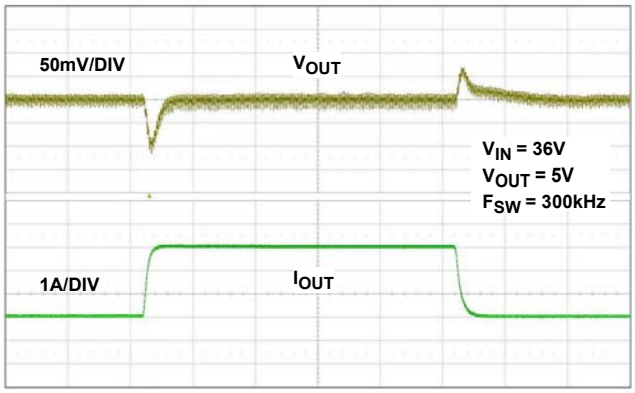



FIGURE 7. $5V_{OUT}$ TRANSIENT RESPONSE

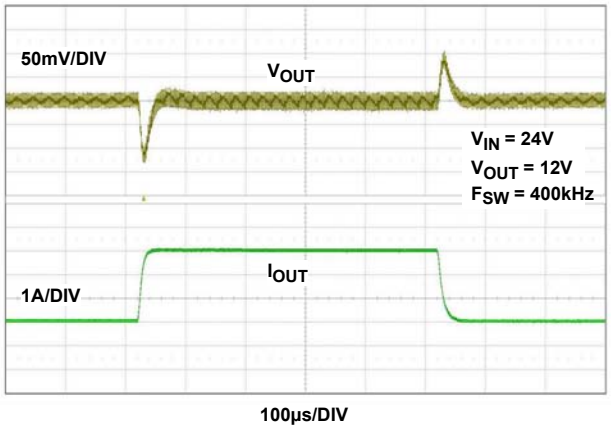



FIGURE 8. $12V_{OUT}$ TRANSIENT RESPONSE

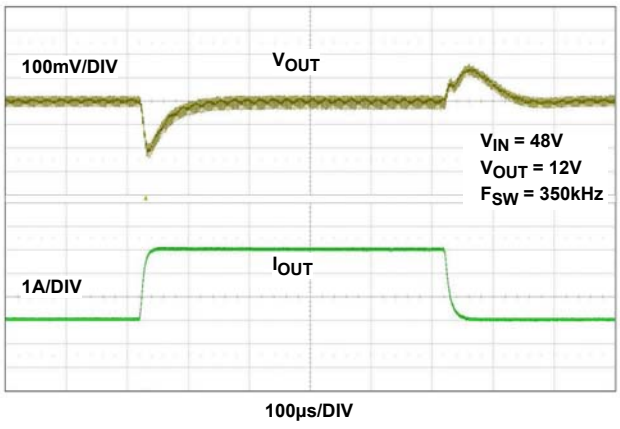



FIGURE 9. $12V_{OUT}$ TRANSIENT RESPONSE

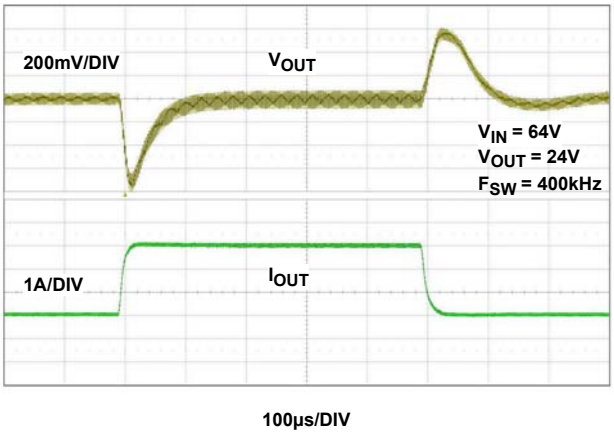



FIGURE 10. $24V_{OUT}$ TRANSIENT RESPONSE

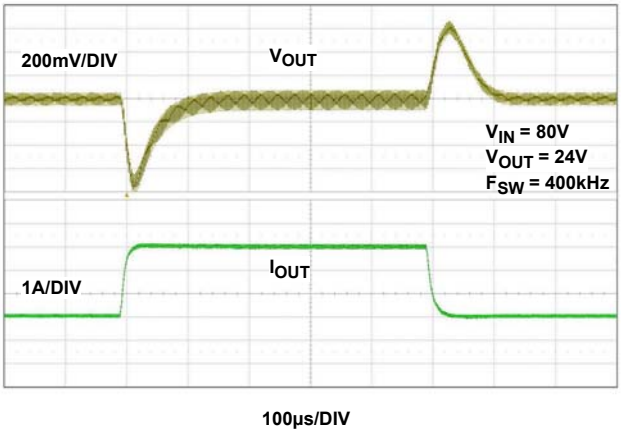



FIGURE 11. $24V_{OUT}$ TRANSIENT RESPONSE

## Start-Up Performance

$T_A$ = +25°C, $V_{IN}$ = 36V, $V_{OUT}$ = 12V, $C_{IN}$ = 100µF ALUM, 4x2.2µF ceramic capacitors, $C_{OUT}$ = 6x22µF ceramic capacitors, CSS = 0.047µF, $I_{OUT}$ = 0A, 4A

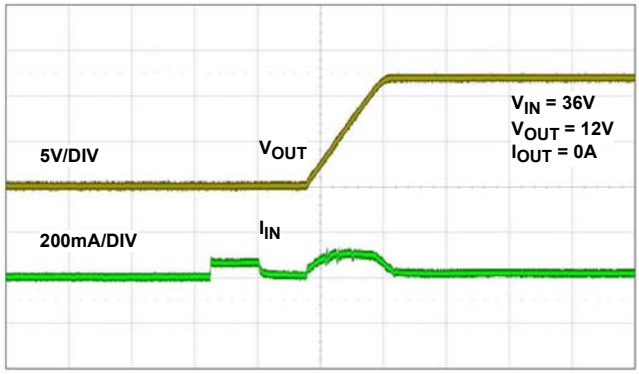



FIGURE 12. START-UP AT 0A

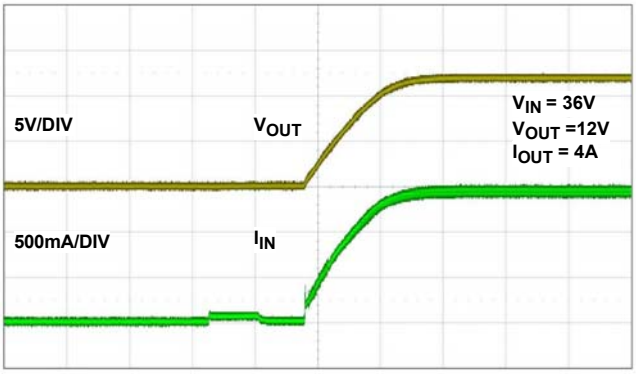



FIGURE 13. START-UP AT 4A

## Short Circuit Performance

$T_A$ = +25°C, $V_{IN}$ = 36V, $V_{OUT}$ = 12V, $C_{IN}$ = 100µF ALUM, 4x2.2µF ceramic capacitors, $C_{OUT}$ = 6x22µF ceramic capacitors, $I_{OUT}$ = 0A, 4A

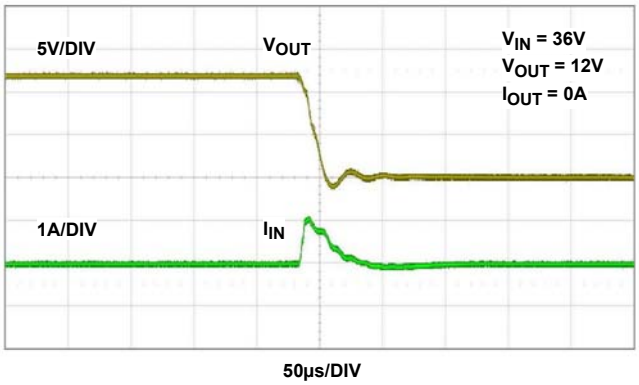



FIGURE 14. SHORT CIRCUIT AT 0A

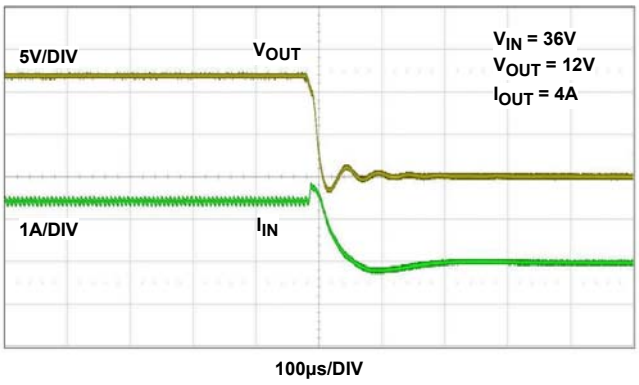



FIGURE 15. SHORT CIRCUIT AT 4A

# Application Information

## Programming the Output Voltage

The ISL8216M has an internal 1.192V ±1% reference voltage. Programming the output voltage requires a resistor, $R_{FB}$, between FB and SGND. Please note that the output voltage accuracy is also dependent on the resistance accuracy. The customer should select a high accuracy resistor (i.e. 0.5%) in order to achieve the overall output accuracy. The output voltage can be calculated as shown in Equation 1.

$$V_{OUT} = \left(1 + \frac{11.3k\Omega}{R_{FB}}\right) \cdot 1.192V \quad \text{(EQ. 1)}$$

The value of $R_{FB}$ for selecting different typical output voltages is shown in Table 1.

**TABLE 1. VALUE OF RFB FOR DIFFERENT OUTPUT VOLTAGES**

| $R_{FB}$ (Ω) | TYPICAL $V_{OUT}$ (V) |
|---|---|
| 3.48k | 5 |
| 1.24k | 12 |
| 715 | 20 |
| 590 | 24 |
| 464 | 30 |

## Enable/Soft-Start

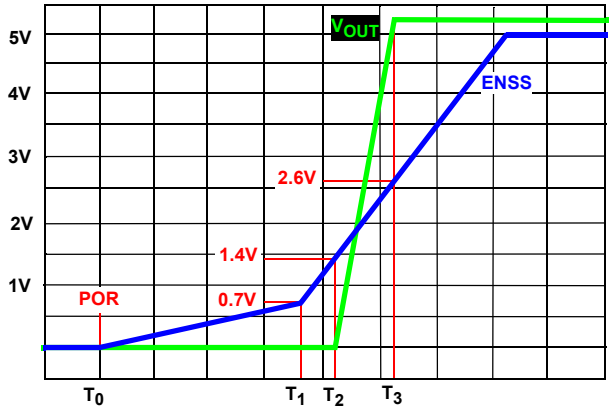



**FIGURE 16. TYPICAL SOFT-START DIAGRAM**

Figure 16 illustrates the start-up scheme of the ISL8216M. The Power-On Reset (POR) function continually monitors the bias voltage at $V_{DD}$ and $V_{IN}$. When the voltage at $V_{DD}$ and $V_{IN}$ exceed their rising POR thresholds ($T_0$), the ISL8216M initially provides 2µA to charge the soft-start capacitor, $C_{SS}$, connected to the ENSS pin. If the voltage at this pin is allowed to rise, it will ramp-up with at a slope determined by the 2µA current and the value of the soft-start capacitor. When the voltage at ENSS reaches 0.77V (Typ) at $T_1$, the oscillator circuit is active, causing the voltage at the RTCT pin to drop from $V_{IN}$ and generate a sawtooth waveform. At the same time, the soft-start current is increased to 33µA; as a result, the ENSS voltage then ramps up at a faster rate. The UGATE starts switching when the ENSS voltage reaches 1.4V (Typ). The delay from POR ($t_0$) to the time the IC starts switching ($t_2$) can be approximated by using Equation 2:

$$t_{delay,\,switching} = 3.712 \times 10^{5} \cdot C_{SS} \quad \text{(EQ. 2)}$$

The output voltage soft-start time is determined by the rise time of ENSS voltage from 1.4V to 2.6V ($t_3$ - $t_2$). The output voltage ramp time can be calculated from:

$$t_{SS} = \frac{1.2}{33 \times 10^{-6}} \cdot C_{SS} \quad \text{(EQ. 3)}$$

The soft-start capacitor $C_{SS}$ is continuously charged up linearly and clamped at 5V. Note that any leakage current on the ENSS node will extend the start-up period. Figure 17 shows the typical soft-start waveforms.

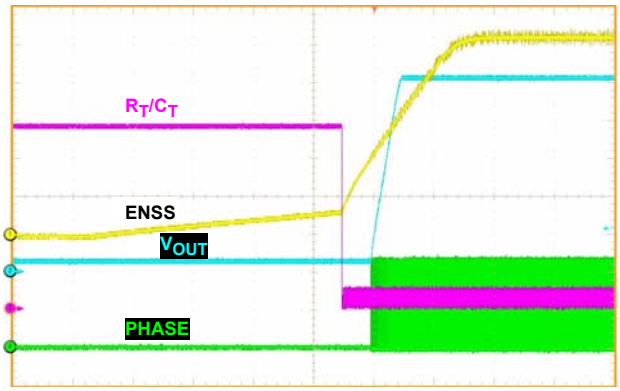



**FIGURE 17. TYPICAL SOFT-START WAVEFORM**

The module can be enabled by an external signal by using an open-drain output device, or by adding an external circuit, as shown in Figure 18. For such circuit, a bias voltage of approximately 5.1V is recommended, which can be generated from $V_{IN}$ simply through a resistor in series with a zener diode that has a nominal working voltage of 5.1V. When the external control signal is low, ENSS is pulled to ground. When the external control signal is high, ENSS is released to allow the soft-start function.

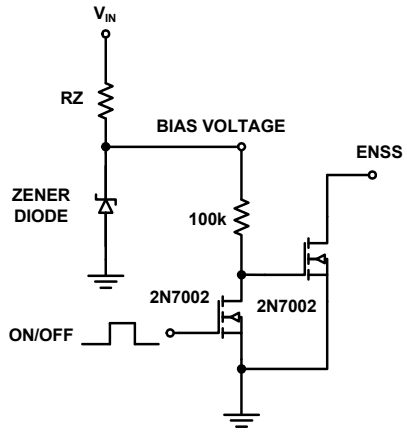



**FIGURE 18. EXTERNAL ENABLE CIRCUIT**

The selection of the resistor in series with the zener diode can be calculated as:

$$R_Z = \frac{V_{IN} - V_Z}{I_Z} \quad \text{(EQ. 4)}$$

Where:

- $V_Z$ is the zener diode's working voltage, nominal 5.1V.
- $I_Z$ is the zener diode's working reverse current, typically about 5mA.

Power dissipation rating should be taken into consideration when selecting $R_Z$.

## Oscillator and Frequency Synchronization

The ISL8216M has an internally set fixed frequency of 300kHz. By adding an external resistor ($R_T$) between $V_{IN}$ and RTCT pin and a capacitor ($C_T$) between RTCT pin and SGND, the ISL8216M can provide adjustable frequency from 200kHz to 600kHz. The time constant of $R_T/C_T$ determines the oscillator frequency. The frequency setting curve is shown in Figure 20. Note that any parasitic capacitance present on the RTCT pin adds to the equivalent $C_T$ value and thus decreases the switching frequency.

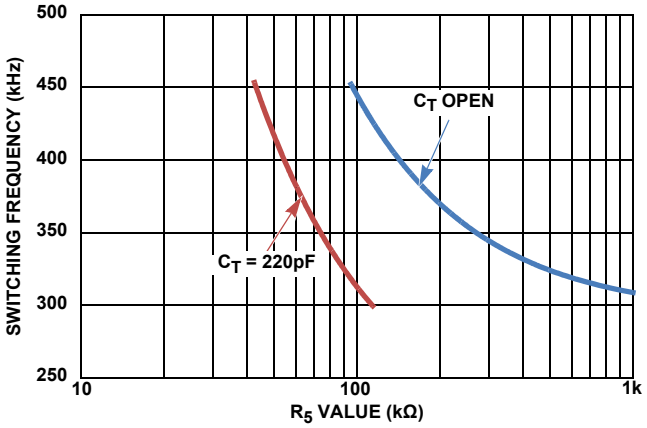



FIGURE 19. $R_T$ AND $C_T$ vs SWITCHING FREQUENCY

Table 2 provides frequency selection for optimum efficiency at typical $V_{IN}$ and $V_{OUT}$ conditions and corresponding $R_T$ and $C_T$ values.

TABLE 2. SWITCHING FREQUENCY FOR OPTIMUM EFFICIENCY FOR DIFFERENT INPUT AND OUTPUT VOLTAGES

| $V_{IN}$ (V) | $V_{OUT}$ (V) | SWITCHING FREQUENCY (kHz) | $R_T$ | $C_T$ |
|---|---|---|---|---|
| 24 | 5 | 300 | open | open |
| 36 | 5 | 300 | open | open |
| 48 | 5 | 300 | open | open |
| 24 | 12 | 400 | 143kΩ | open |
| | | | 54.9kΩ | 220pF |
| 36 | 12 | 400 | 143kΩ | open |
| | | | 54.9kΩ | 220pF |

TABLE 2. SWITCHING FREQUENCY FOR OPTIMUM EFFICIENCY FOR DIFFERENT INPUT AND OUTPUT VOLTAGES (Continued)

| $V_{IN}$ (V) | $V_{OUT}$ (V) | SWITCHING FREQUENCY (kHz) | $R_T$ | $C_T$ |
|---|---|---|---|---|
| 48 | 12 | 400 | 143kΩ | open |
| | | | 54.9kΩ | 220pF |
| 64 | 12 | 400 | 143kΩ | open |
| | | | 54.9kΩ | 220pF |
| 80 | 12 | 350 | 267kΩ | open |
| | | | 73.2kΩ | 220pF |
| 48 | 24 | 450 | 95.3kΩ | open |
| | | | 43.2kΩ | 220pF |
| 64 | 24 | 400 | 143kΩ | open |
| | | | 54.9kΩ | 220pF |
| 80 | 24 | 350 | 267kΩ | open |
| | | | 73.2kΩ | 220pF |

Note that when the controller is disabled, the voltage at RTCT pin rises up to the input voltage. Hence, the voltage rating of the $C_T$ capacitor must be sufficient to support the maximum input voltage.

The SYNC pin provides the function to synchronize the ISL8216M's switching frequency to an external source. When frequency synchronization is used, the time constant of $R_T/C_T$ must be set longer than the period of the sync signal. When the external sync feature is not used, the customer should tie the SYNC pin to SGND.

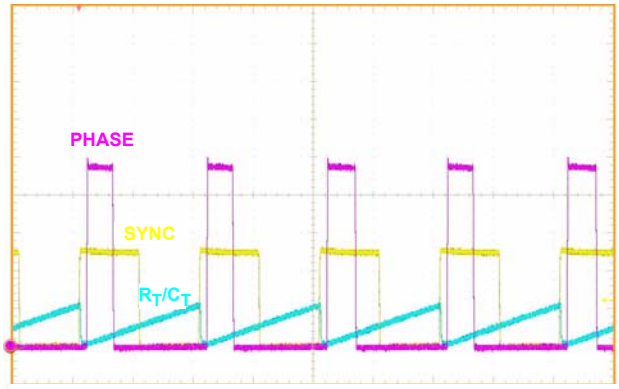



FIGURE 20. SYNCHRONIZATION OPERATION

### MINIMUM ON-TIME

The ISL8216M requires the internal MOSFET to be turned on to a minimum of 200ns (Typ). This minimum gate pulse width is required to ensure proper samplings of the overcurrent protection circuit.

For low duty cycle applications, the switching frequency must be selected to satisfy the condition shown in Equation 5:

$$F_{OSC} < \frac{V_{OUT}}{\eta \cdot V_{IN}} \cdot \frac{1}{t_{on(min)}} \quad \text{(EQ. 5)}$$

Where $\eta$ is converter efficiency.

### MINIMUM OFF-TIME

At the termination of the oscillator's ramp, there is a 190ns time interval before the next ramp starts. This time interval creates the minimum-off time of the PWM. This period ensures that the boot capacitor charge is refreshed. Equation 6 can be used to calculate the switching frequency to meet the condition:

$$F_{OSC} < \left(1 - \frac{V_{OUT}}{\eta \cdot V_{IN}}\right) \cdot \frac{1}{t_{off(min)}} \quad \text{(EQ. 6)}$$

## Overcurrent Protection

The overcurrent protection function protects the module from overcurrent conditions by monitoring the current flowing through the MOSFET. OCP (Overcurrent protection) is implemented via a resistor ($R_{OCSET}$) and a capacitor ($C_{OCSET}$) connected between the OCSET pin and the drain of the MOSFET. An internal 104µA current source develops a voltage across $R_{OCSET}$, which is then compared with the drain-to-source voltage developed across the MOSFET measured with regard to the PHASE node. When the drain-to-source voltage across the MOSFET exceeds the voltage drop across the resistor $R_{OCSET}$, an OCP event occurs. $C_{OCSET}$ is placed in parallel with $R_{OCSET}$ to smooth the voltage across $R_{OCSET}$ in the presence of switching noise on the input bus. The module has an internal resistor of 2kΩ; an external $R_{OCSET\_EX}$ can be added in between OCSET and VIN, and thus in parallel with the internal 2kΩ, to further reduce the overcurrent limit.

A 200ns blanking period is used to reduce the current sampling error due to leading-edge switching noise.

The OCP trip point varies mainly due to MOSFET $r_{DS(ON)}$ variations and layout noise concerns. To avoid overcurrent tripping in the normal operating load range, find the $R_{OCSET\_EX}$ resistor from the Equation 7 with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum $I_{OCSET}$, 89µA.

Determine the overcurrent limit greater than the inductor peak current at the maximum output continuous current.

$$R_{OCSET} = \frac{R_{OCSET-EX} \cdot 2k\Omega}{R_{OCSET-EX} + 2k\Omega} = \frac{\left(I_{OC} + \frac{\Delta I_L}{2}\right) \cdot r_{DS(ON)}}{I_{OCSET}} \quad \text{(EQ. 7)}$$

$$\Delta I_L = \left(\frac{V_{IN} - V_{OUT}}{f_{SW} \cdot L} \cdot \frac{V_{OUT}}{V_{IN}}\right)$$

Where:

- $R_{OCSET\_EX}$ is the external resistor between OCSET and $V_{IN}$
- $f_{SW}$ is the switching frequency
- Internal inductor L = 5.6µH nominal

If overcurrent is detected, the output immediately shuts off, it cycles the soft-start function in a hiccup mode (4 dummy soft-start time-outs, then up to one real one) to provide fault protection. If the shorted condition is not removed, this cycle will continue indefinitely. Figures 21 and 22 illustrate typical waveforms during overcurrent protection.

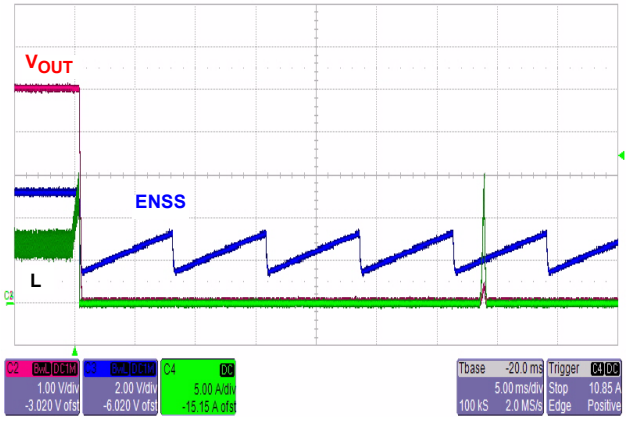



FIGURE 21. TYPICAL OVERCURRENT PROTECTION

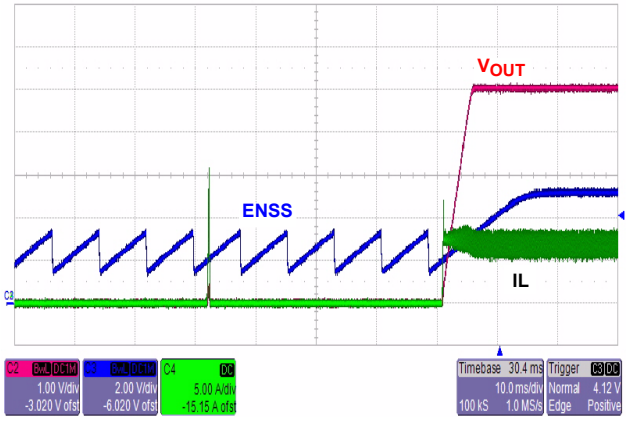



FIGURE 22. TYPICAL HICCUP RECOVER

## Resistor Between BOOT and $V_{IN}$ for Charging The Bootstrap Capacitor

The internal bootstrap diode connected to the PVCC pin provides charge for the internal bootstrap capacitor. For above $12V_{OUT}$ applications, a resistor connecting between BOOT pin and VIN pin is recommended for certain conditions. Refer to Table 3. This resistor provides additional bootstrap charge introduced from $V_{IN}$, which can ensure the gate drive circuit functions properly at very light load. See Figure 23 for the recommended external resistor values at $20V_{OUT}$, $24V_{OUT}$, $27V_{OUT}$, and $30V_{OUT}$ conditions. A minimum 0.25W power rating is recommended for this resistor.

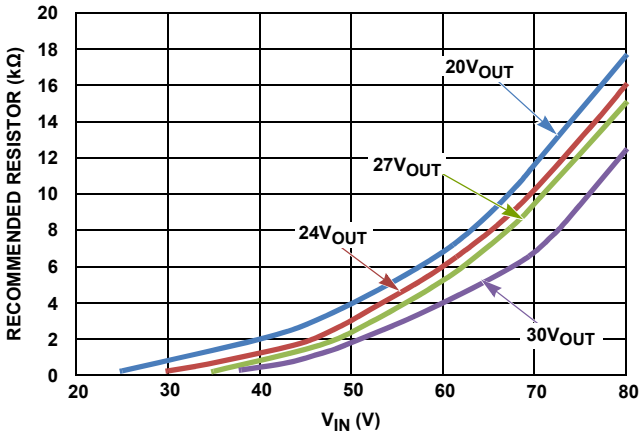



FIGURE 23. RECOMMENDED EXTERNAL RESISTOR VALUE FROM BOOT TO PVIN

If such a resistor is used while an external control signal is used to enable the module, an external circuit is required to pull ENSS and $V_{OUT}$ to ground when the external control signal is low, as shown in Figure 24. The bias voltage in this circuit can be the same bias voltage as shown in Figure 18. Without such a circuit, a residual voltage can be generated on $V_{OUT}$ through the path of $V_{IN}$, resistor, bootstrap diode, bootstrap capacitor, inductor and $V_{OUT}$.

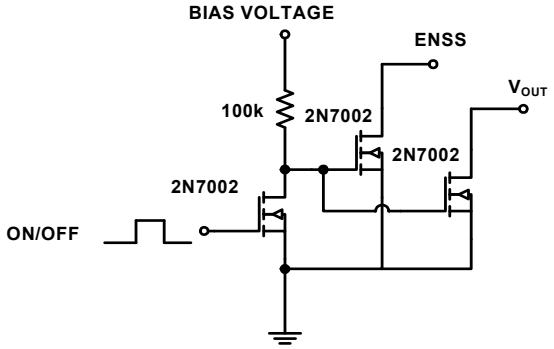



FIGURE 24. EXTERNAL ENABLE CIRCUIT WHILE $V_{IN}$-BOOT RESISTOR IS USED

## Power-Good

The PGOOD comparator monitors the voltage on the FB pin. PGOOD is asserted (open drain) when the FB pin voltage is within 14% of the reference voltage. The turn-on response of the PGOOD circuit has a typical 3µs delay. The PGOOD is de-asserted under disable, overcurrent event, or over-temperature event.

For $>12V_{OUT}$ applications where $V_{IN}$ power-up/down (module self enable/disable) is required and PGOOD signal is utilized, a PGOOD delay circuit and a 1kΩ, 1W rating dummy load resistor are recommended. The PGOOD delay circuit is shown in Figure 25. Note when the dummy load resistor is used, the resistor between $V_{IN}$ and BOOT (Figure 23) is no longer required. During $V_{IN}$ power-up (module self enable) for $>12V_{OUT}$ applications at very light load current, without such a delay circuit, $V_{OUT}$ may have a drop after initially reaching the target due to the lack of bootstrap charge. With such a delay circuit, the PGOOD signal can be delayed for 250ms. For applications of $\leq 12V_{OUT}$, the PGOOD delay circuit is not required.

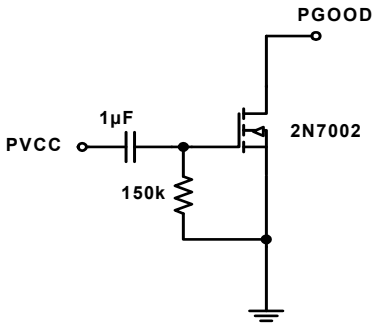



FIGURE 25. PGOOD DELAY CIRCUIT

## Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The output capacitor can be a low ESR tantalum capacitor, a low ESR polymer capacitor, a low ESR aluminum electrolytic capacitor, or all ceramic capacitors. Internally optimized loop compensation provides sufficient stability margins for applications using different types of capacitors. A minimum total output capacitance of 120µF with low ESR is recommended to meet the output voltage ripple and load transient requirements.

Use only specialized low-ESR capacitors intended for switching regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

A high frequency ceramic decoupling capacitor can be placed between module's $V_{OUT}$ and PGND, as close to the module as possible, in order to decouple high frequency switching noise. High frequency ceramic decoupling capacitors should also be placed as close to the power pins of the load as possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

## Input Capacitor Selection

A combination of bulk capacitors and low Equivalent Series Resistance (ESR) ceramic capacitors are recommended as input capacitors. A bulk input capacitor(s) is needed to supply the current during output load transient conditions. The minimum required input bulk capacitance can be calculated as shown in Equation 8.

$$C_{MIN(BULK)} = \frac{1.21 \bullet \Delta I_{IN}^2 \bullet L_{TRACE}}{\Delta V_{DROP}} \quad \text{(EQ. 8)}$$

$$\Delta I_{IN} = \frac{V_{OUT}}{\eta \bullet V_{IN}} \bullet \Delta I_O$$

Where:

- $\Delta V_{DROP}$ is the maximum allowable drop on the input voltage during output peak load transient.
- $C_{MIN(BULK)}$ is the minimum required bulk capacitance (µF).
- $\Delta I_{IN}$ is the input transient current reflected from the output load transient current (A).
- $L_{TRACE}$ is the parasitic inductance of the trace connected to input supply due to PCB layout. Typically 50nH.
- $\Delta I_O$ is the output load transient current (A).
- $\eta$ is the efficiency of the converter (%).

Other important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. The capacitor voltage rating should be at least 1.25x greater than the maximum input voltage. A voltage rating of 1.5x greater is a conservative guideline. The RMS current rating requirement for the total input capacitance is calculated approximately as shown in Equation 9.

$$I_{CIN(RMS)} = I_O\sqrt{D(1-D)} \qquad D = \frac{V_O}{V_{IN}} \quad \text{(EQ. 9)}$$

In addition to the bulk capacitance, low ESR ceramic capacitance is recommended in order to reduce input voltage ripple and decouple between the VIN and GND of the module. This capacitance reduces voltage ringing created by the switching current across parasitic circuit elements. The ceramic capacitors should be placed as closely as possible to the module pins. The minimum required input ceramic capacitors can be calculated as shown in Equation 10.

$$C_{MIN(CER)} = \frac{I_O \bullet D(1-D)}{f_{SW} \bullet V_{IN(P-P)}} \quad \text{(EQ. 10)}$$

Where:

- $C_{MIN(CER)}$ is the minimum required ceramic capacitance (µF)
- $I_O$ is the output current (A)
- D is the duty cycle, $D = V_{OUT}/V_{IN}$
- $f_{SW}$ is the switching frequency (kHz)
- $V_{IN(P-P)}$ is the allowable peak-to-peak input voltage ripple (V)

The higher the ceramic capacitance, the less RMS current the bulk capacitance is subject to, since the bulk capacitance typically has much higher ESR than the ceramic capacitance. By increasing the ceramic capacitance, the RMS current requirement for the bulk input capacitors can be reduced. A typical 4x2.2µF ceramic capacitance is recommended.

For a through-hole design, several electrolytic capacitors in parallel may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up.

## Thermal Protection

If the ISL8216M's junction temperature reaches a nominal temperature of +150°C, the controller will be disabled. The ISL8216M will not be re-enabled until the junction temperature drops below +110°C.

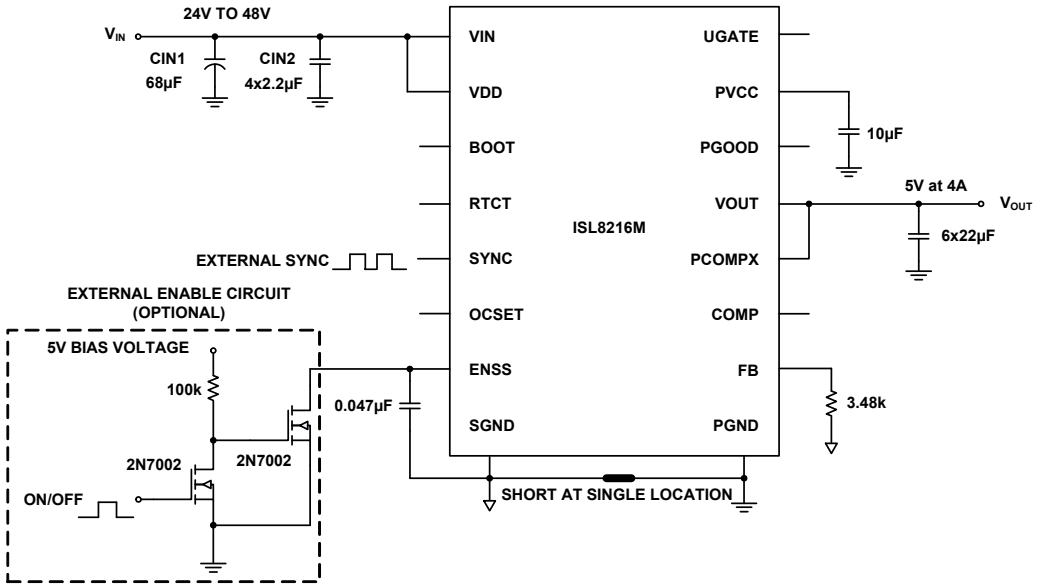
## Thermal Considerations and Current Derating

Experimental power loss curves (Figures 30 through 32), along with $\theta_{JA}$ from thermal modeling analysis, can be used as a guide for thermal consideration for the module. The derating curves (Figures 33 through 42) are derived from the maximum power allowed while maintaining temperature below the maximum junction temperature of +115°C. The maximum +115°C junction temperature is considered for the module to load the current consistently and it provides 10°C margin of safety from the rated junction temperature of +125°C. If necessary, customers can adjust the margin of safety according to the real applications. In the actual application, other heat sources and design margins should be considered.

# Typical Application Circuits

TABLE 3. EXTERNAL CIRCUITS REQUIREMENT BASED ON APPLICATION CONDITIONS

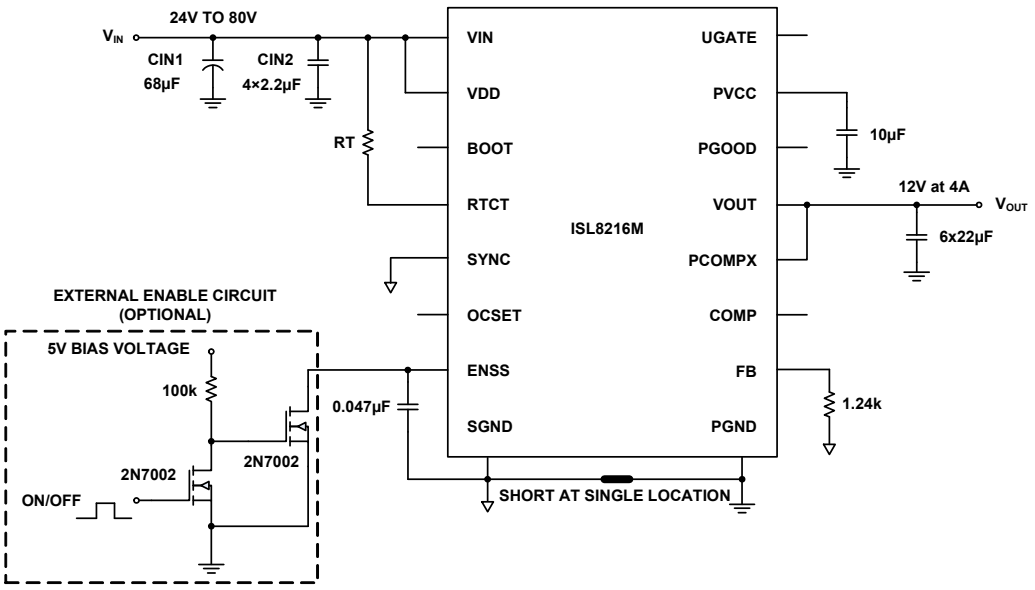
| CONDITIONS | | | EXTERNAL CIRCUITS REQUIREMENTS | | | FIGURES |
|---|---|---|---|---|---|---|
| $V_{OUT}$ | Use PGOOD Signal | Enable Method | PGOOD Delay Circuit | 1kΩ Dummy Load Resistor | $V_{IN}$-BOOT Resistor | - |
| ≤12V | No | Self or External Enable Control | No | No | No | Figures 26 and 27 |
| ≤12V | Yes | Self or External Enable Control | No | No | No | Figures 26 and 27 |
| >12V | No | Self or External Enable Control | No | No | Yes | Figure 28 |
| >12V | Yes | External Enable Control | No | No | Yes | Figure 28 |
| >12V | Yes | Self Enable | Yes | Yes | No | Figure 29 |




NOTE:

- If module is to be enabled by an external signal, an open drain device or an external enable circuit is required. Refer to "Enable/Soft-Start" on page 11.

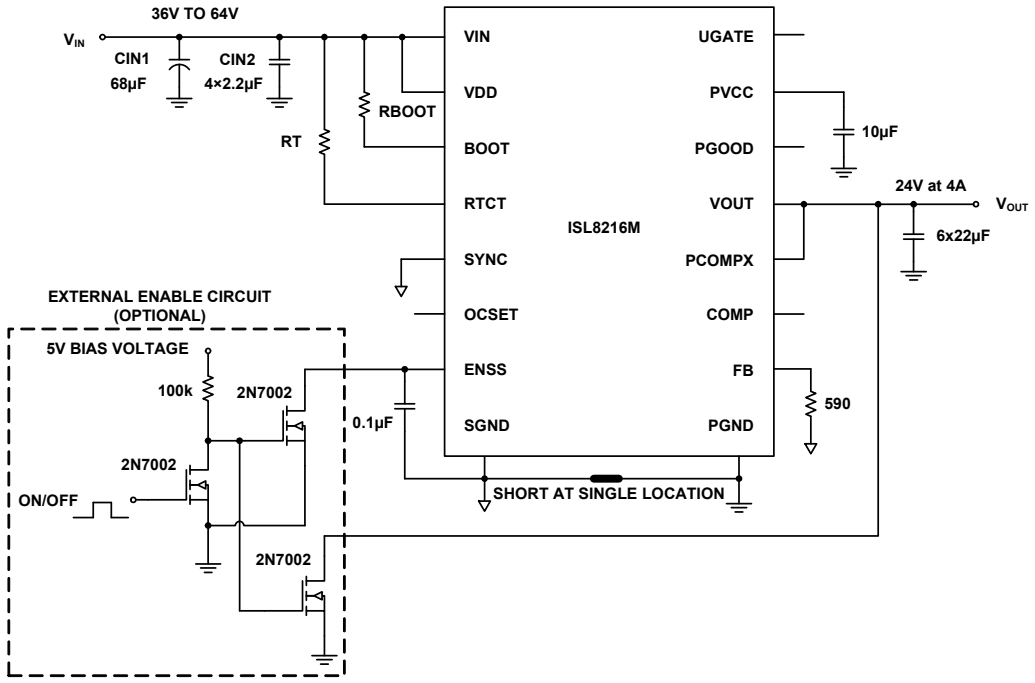
FIGURE 26. $24V_{IN}$ TO $48_{VIN}$ $5V_{OUT}$, 4A, 300kHz




NOTES:

- If module is to be enabled by an external signal, an open drain device or an external enable circuit is required. Refer to "Enable/Soft-Start" on page 11.
- Refer to Figure 19 and Table 2 for optimum switching frequency and $R_T$ and/or $C_T$ values.

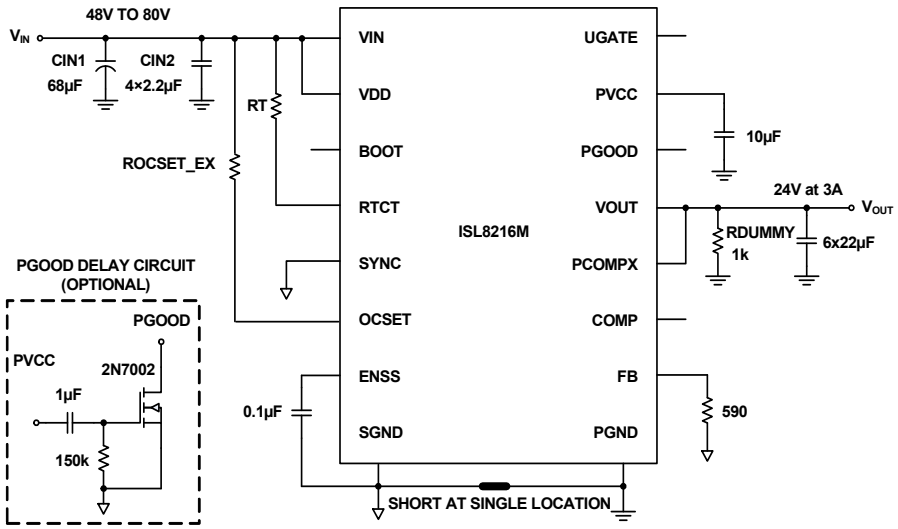
**FIGURE 27. $24_{VIN}$ TO $80_{VIN}$, $12V_{OUT}$, 4A**




NOTES:

- If module is to be enabled by an external signal, an open drain device or an external enable circuit is required. Refer to "Enable/Soft-Start" on page 11.
- Refer to Figure 19 and Table 2 for optimum switching frequency and $R_T$ and/or $C_T$ values.
- Refer to Figure 23 for VIN-BOOT resistor ($R_{BOOT}$) value.

**FIGURE 28. $36_{VIN}$ TO $64_{VIN}$, $24V_{OUT}$, 4A, 400kHz**




NOTES:

- For this condition (module self-enable, >12VOUT, using PGOOD), a PGOOD delay circuit, a 1kΩ, 1W rating dummy load resistor, as well as a soft-start capacitor of at least 0.1µF are required. Refer to "Power-Good" on page 14. The $V_{IN}$-BOOT resistor ($R_{BOOT}$) is not required when 1kΩ dummy load resistor is present.
- Refer to "Overcurrent Protection" on page 13 for the external OCSET resistor selection.
- Refer to Figure 19 and Table 2 for optimum switching frequency and $R_T$ and/or $C_T$ values.

**FIGURE 29. 80$V_{IN}$ 24$V_{OUT}$, 3A, 350kHz, SELF ENABLE, USING PGOOD SIGNAL**

## Power Loss Curves

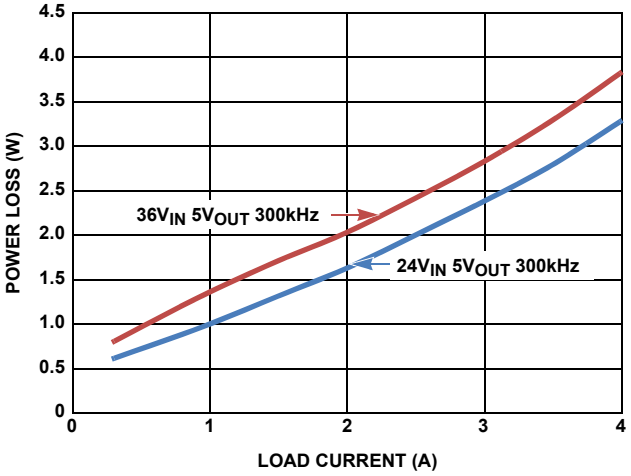



FIGURE 30. POWER LOSS vs LOAD CURRENT ($5V_{OUT}$) FOR VARIOUS INPUT VOLTAGES

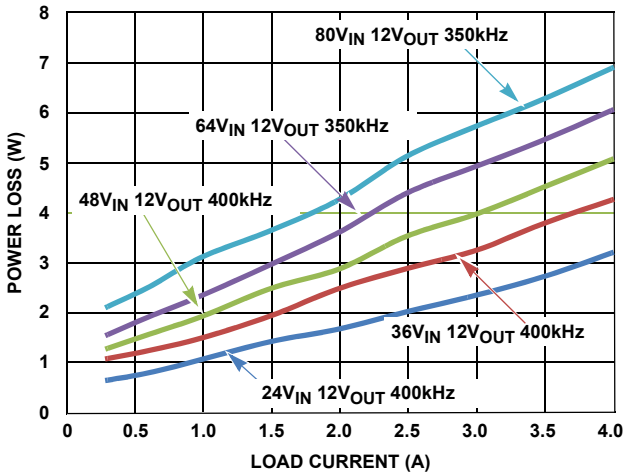



FIGURE 31. POWER LOSS vs LOAD CURRENT ($12V_{OUT}$) FOR VARIOUS INPUT VOLTAGE

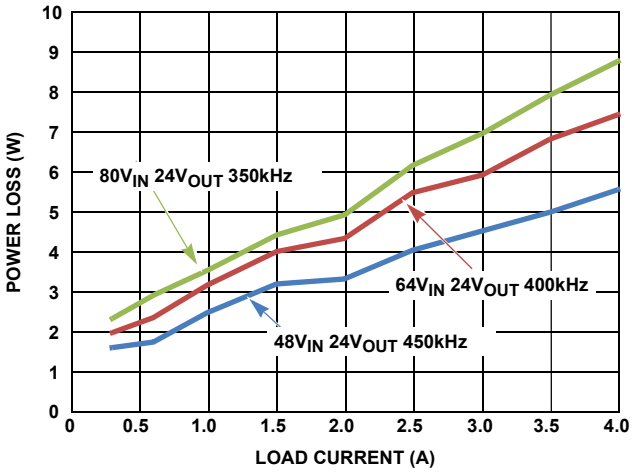



FIGURE 32. POWER LOSS vs LOAD CURRENT ($24V_{OUT}$) FOR VARIOUS INPUT VOLTAGE

## Derating Curves

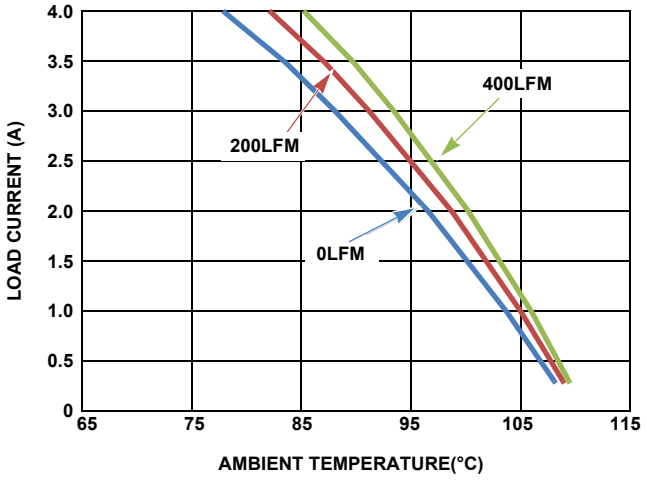



FIGURE 33. DERATING CURVE $24V_{IN}$ TO $5V_{OUT}$

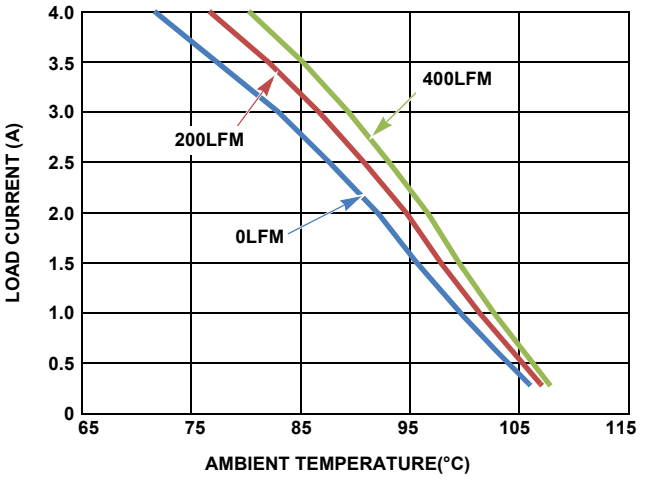



FIGURE 34. DERATING CURVE $36V_{IN}$ TO $5V_{OUT}$

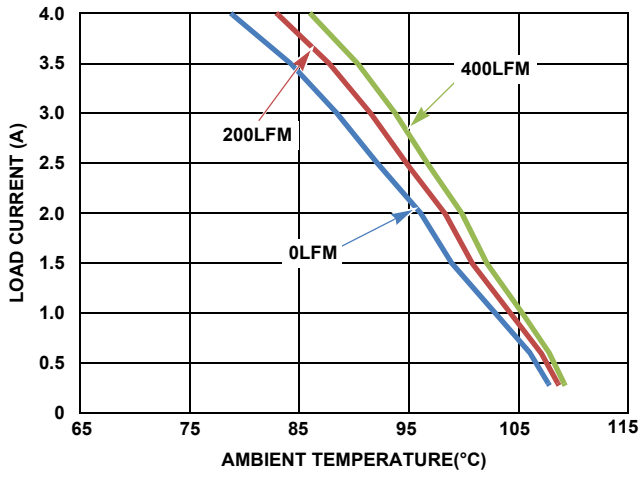



FIGURE 35. DERATING CURVE $24V_{IN}$ TO $12V_{OUT}$

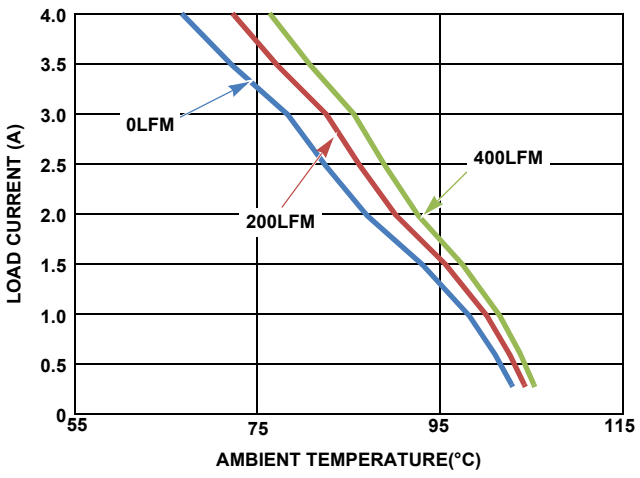



FIGURE 36. DERATING CURVE $36V_{IN}$ TO $12V_{OUT}$

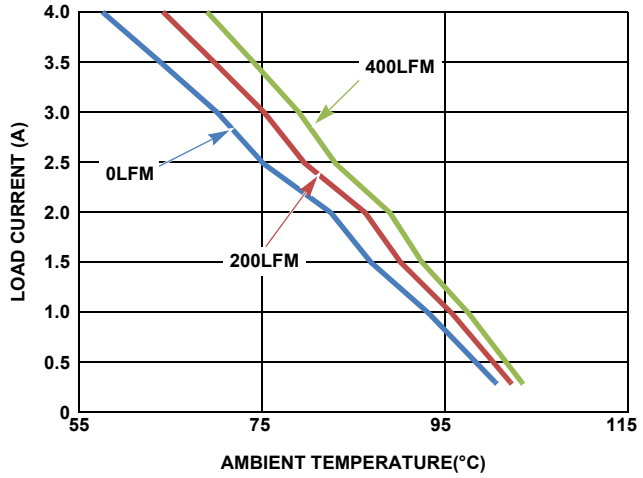



FIGURE 37. DERATING CURVE $48V_{IN}$ TO $12V_{OUT}$

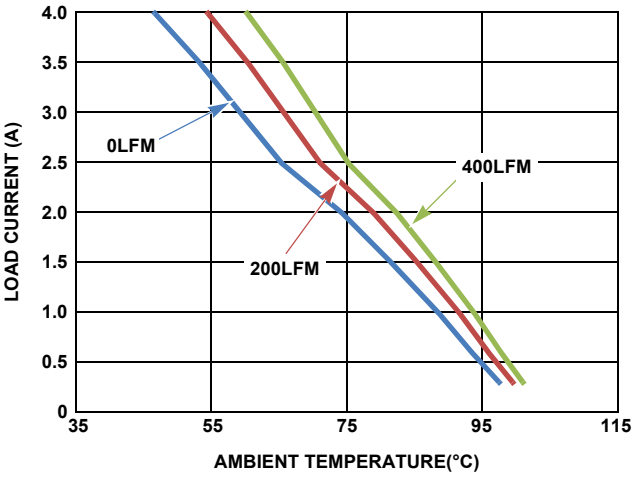



FIGURE 38. DERATING CURVE $64V_{IN}$ TO $12V_{OUT}$

## Derating Curves (Continued)

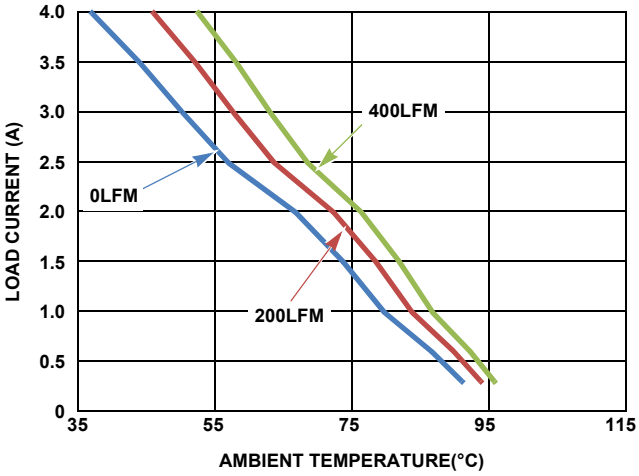



FIGURE 39. DERATING CURVE 80$V_{IN}$ TO 12$V_{OUT}$

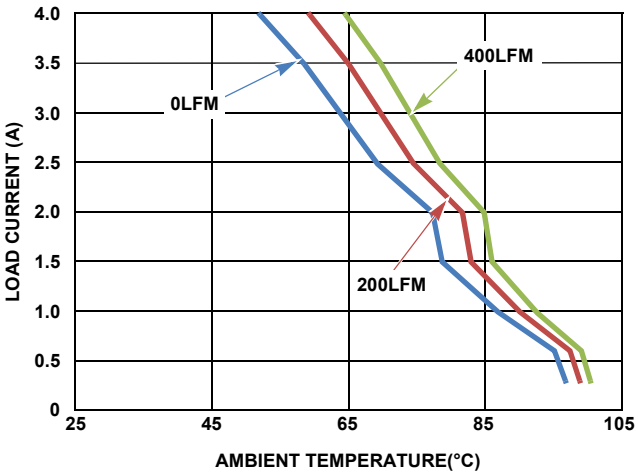



FIGURE 40. DERATING CURVE 48$V_{IN}$ TO 24$V_{OUT}$

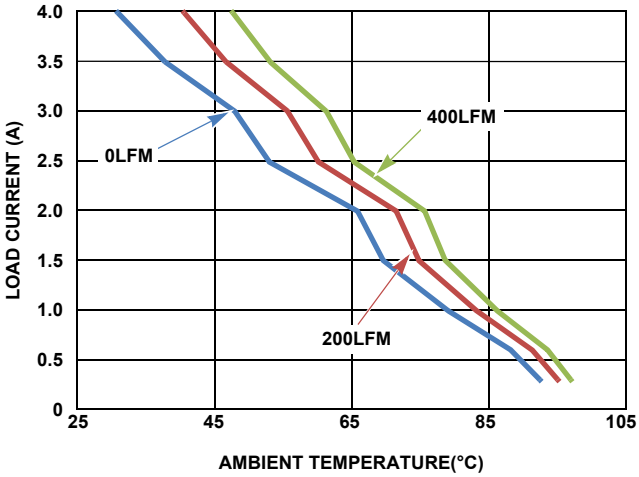



FIGURE 41. DERATING CURVE 64$V_{IN}$ TO 24$V_{OUT}$

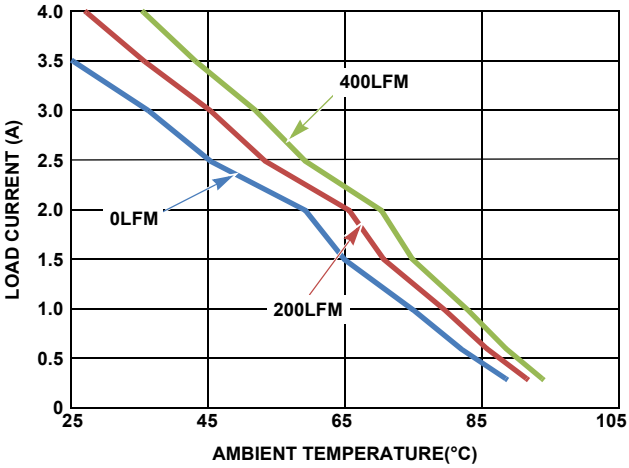



FIGURE 42. DERATING CURVE 80$V_{IN}$ TO 24$V_{OUT}$

# Layout Guide

To achieve stable operation, low losses and good thermal performance, some layout considerations are necessary.

- VOUT, VIN, PHASE, and GND should have large copper areas for power path to minimize conduction loss and thermal stress. Place enough thermal vias to connect the power planes in different layers under or around the module.
- Establish a separate ground plane for SGND (pin A1 and PAD 1) and PGND (pin F8, A11, and PAD 5) and connect them at a single point as shown in Figure 43. This will help block the high frequency noise from entering the controller via SGND.
- Place at least one high frequency ceramic capacitor between (1) VIN and PGND, (2) VOUT and PGND, and (3) PVCC and GND, as closely to the module as possible in order to minimize high-frequency noise.
- Avoid routing any sensitive signal traces, such as VOUT and FB near the PHASE pad.
- PHASE pad is a switching node that generates switching noise. Keep the pad under the module. For noise-sensitive applications, it is recommended to keep phase pad only on the top and inner layers of the PCB. Also, do not place phase pads exposed to the outside on the bottom layer of the PCB.

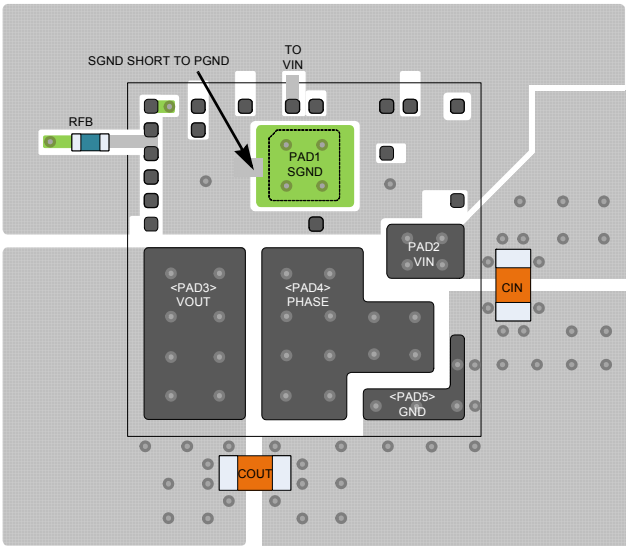



FIGURE 43. RECOMMENDED LAYOUT

# Package Description

The structure of ISL8216M belongs to the High Density Array (HDA) package. This kind of package has advantages, such as good thermal and electrical conductivity, low weight and small size. The HDA package is applicable for surface mounting technology. The ISL8216M contains several types of devices, including resistors, capacitors, inductors and control ICs. The ISL8216M is a copper lead-frame based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multi-component assembly is over-molded with polymer mold compound to protect these devices.

The package outline, typical PCB layout pattern design, and typical stencil pattern design are shown in the "Package Outline Drawing" on page 25. The module has a small size of 15mmx15mmx3.6mm. Figure 44 shows typical reflow profile parameters. These guidelines are general design rules. Users can modify parameters according to their application.

# PCB Layout Pattern Design

The bottom of the ISL8216M is a lead-frame footprint, which is attached to the PCB by surface mounting process. The PCB layout pattern is shown in the Package Outline Drawing on page 29. The PCB layout pattern is essentially 1:1 with the HDA exposed pad and I/O termination dimensions. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

## Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and your board design rules allow.

## Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mils to 3mils) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. Stencil aperture size to land size ratio should typically be 1:1. The aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands. To reduce solder paste volume on the larger thermal lands, it is recommended that an array of smaller apertures be used instead of one large aperture. It is recommended that the stencil printing area cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown in the Package Outline Drawing on page 28. The gap width between pad to pad is 0.6mm. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing "smooths" the aperture walls resulting in reduced surface friction and better paste release which reduces voids. Using a trapezoidal section aperture (TSA) also promotes paste release and forms a "brick like" paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) HDA.

## Reflow Parameters

Due to the low mount height of the HDA, "No Clean" Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in Figure 44 is provided as a guideline, to be customized for varying manufacturing practices and applications.

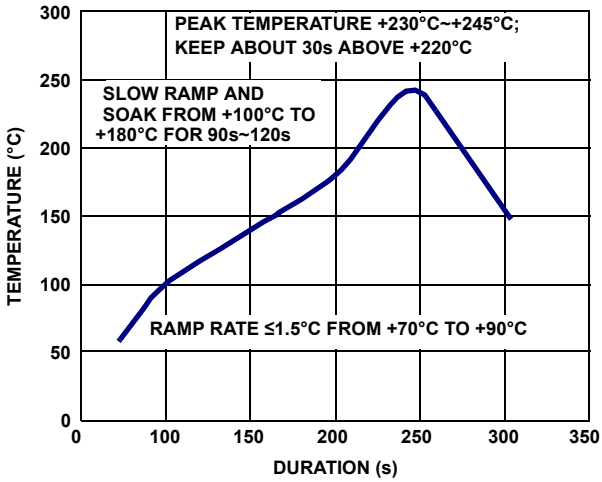



FIGURE 44. TYPICAL REFLOW PROFILE

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| May 9, 2014 | FN8607.2 | Page 1: Added “Compliant with “EN55022 Class B (see AN1907)” bullet to Features section.<br>Page 3: Removed redundant line that was on the “Internal Block Diagram”. |
| March 14, 2014 | FN8607.1 | Updated the following in the “Electrical Specifications” on page 6, OSCILLATOR section:<br>Frequency Range, MIN from 100 to 200<br>SYNC Frequency Range, MIN from 100 to 200 |
| February 10, 2014 | FN8607.0 | Initial Release |

# About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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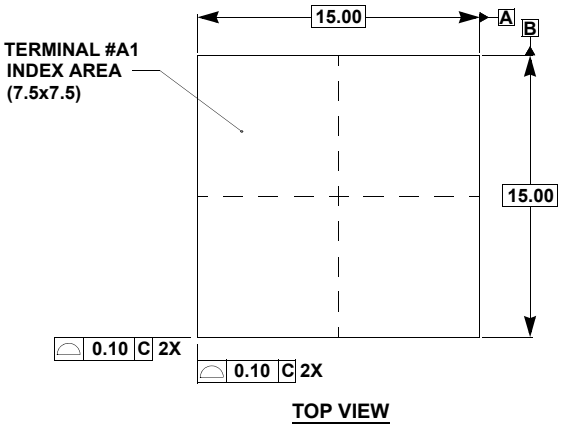
# Package Outline Drawing

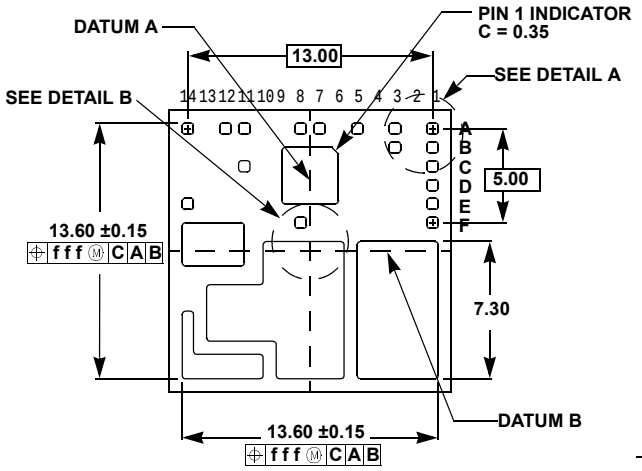
## Y22.15x15

**22 I/O 15mmx15mmx3.6mm CUSTOM HDA MODULE**

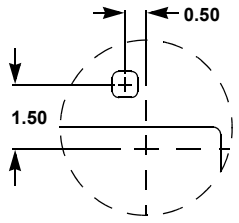
**Rev 2, 9/13**



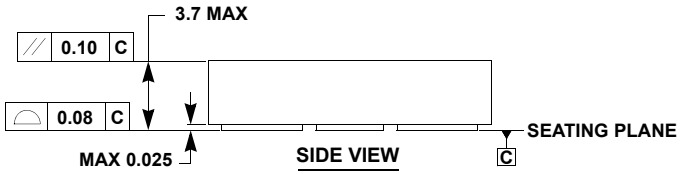

TOP VIEW



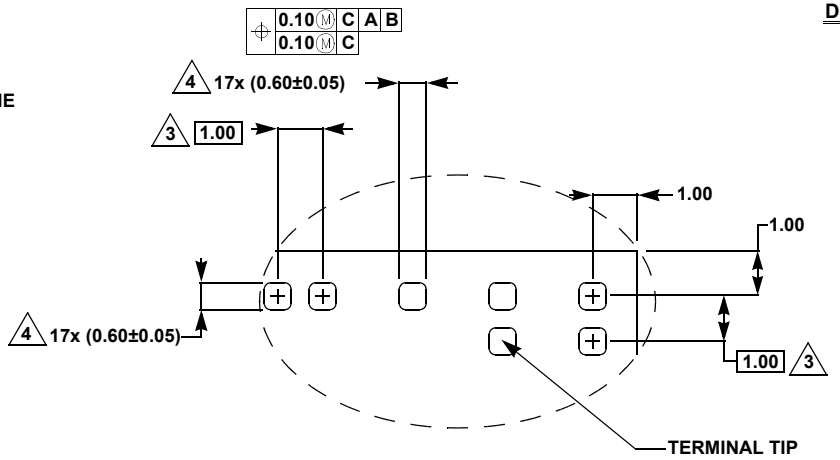

BOTTOM VIEW




DETAIL B



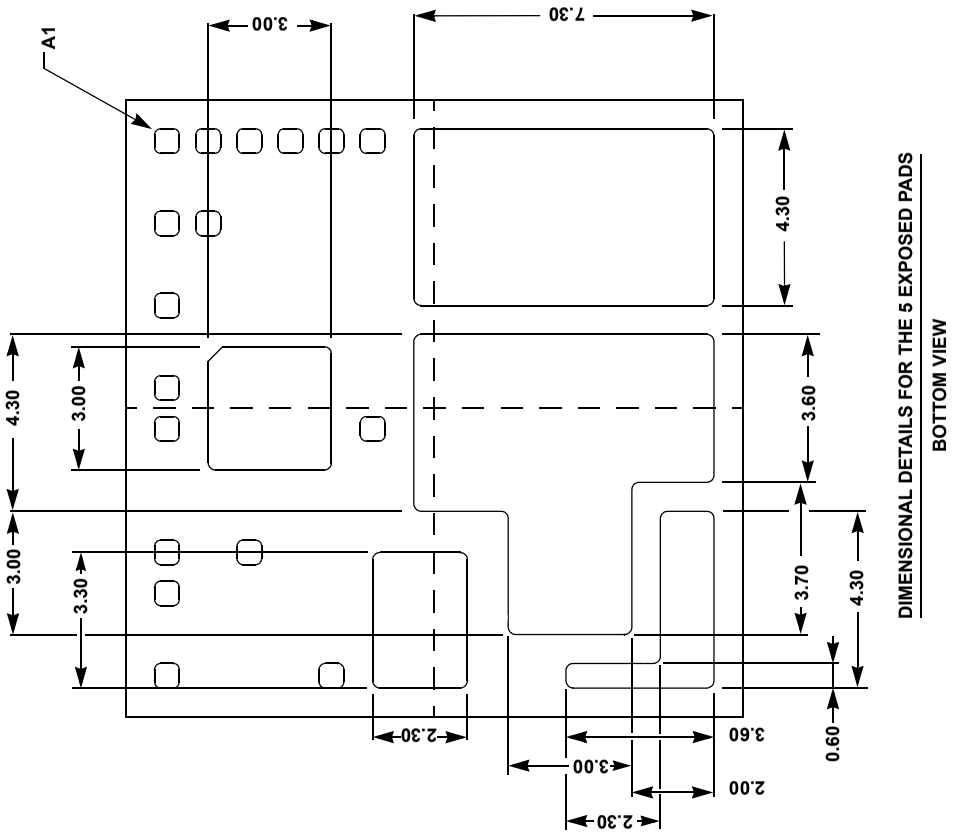

SIDE VIEW



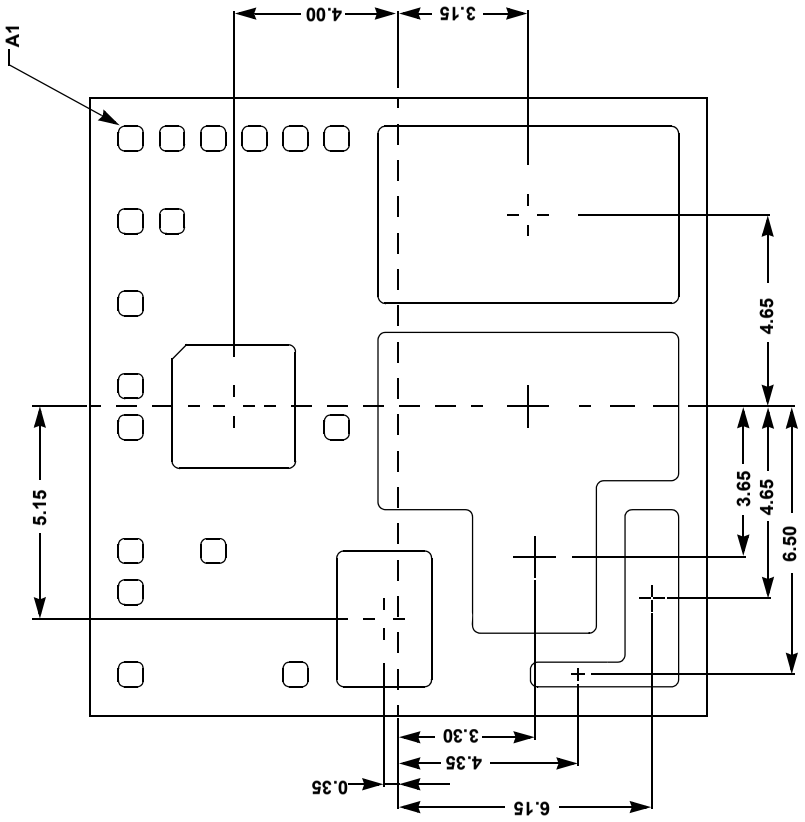

DETAIL A

**NOTES:**

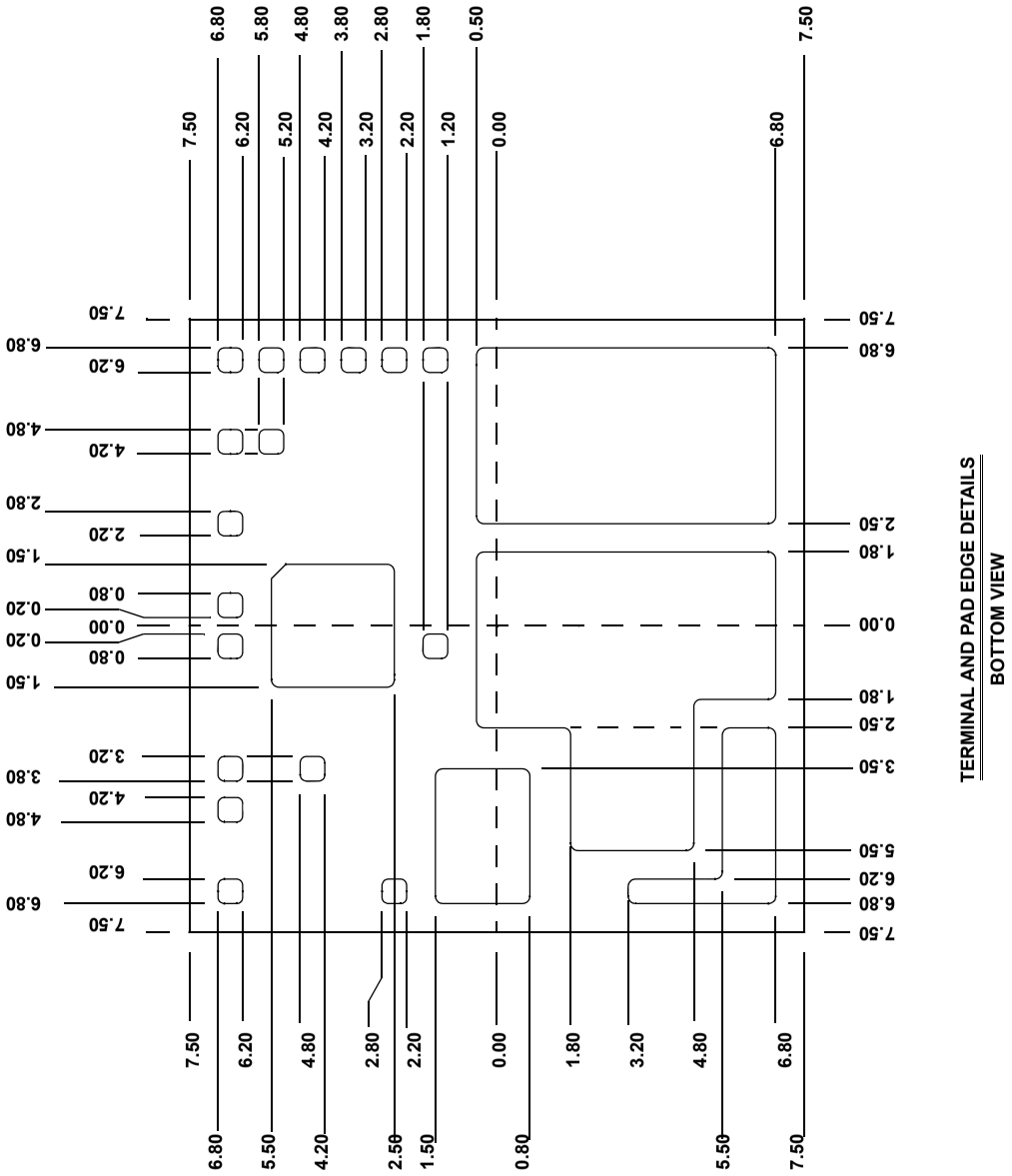
1. All dimensions are in millimeters.
2. All tolerances ± 0.10mm, unless otherwise noted.
3. Represents the basic land grid pitch.
4. The total number of smaller I/O pads is 17. All 17 I/O's are centered in a fixed row and column matrix at 1.0mm pitch BSC.
5. Dimensioning and tolerancing per ASME Y14.5M-1994.
6. Tolerance for exposed DAP edge location dimension.

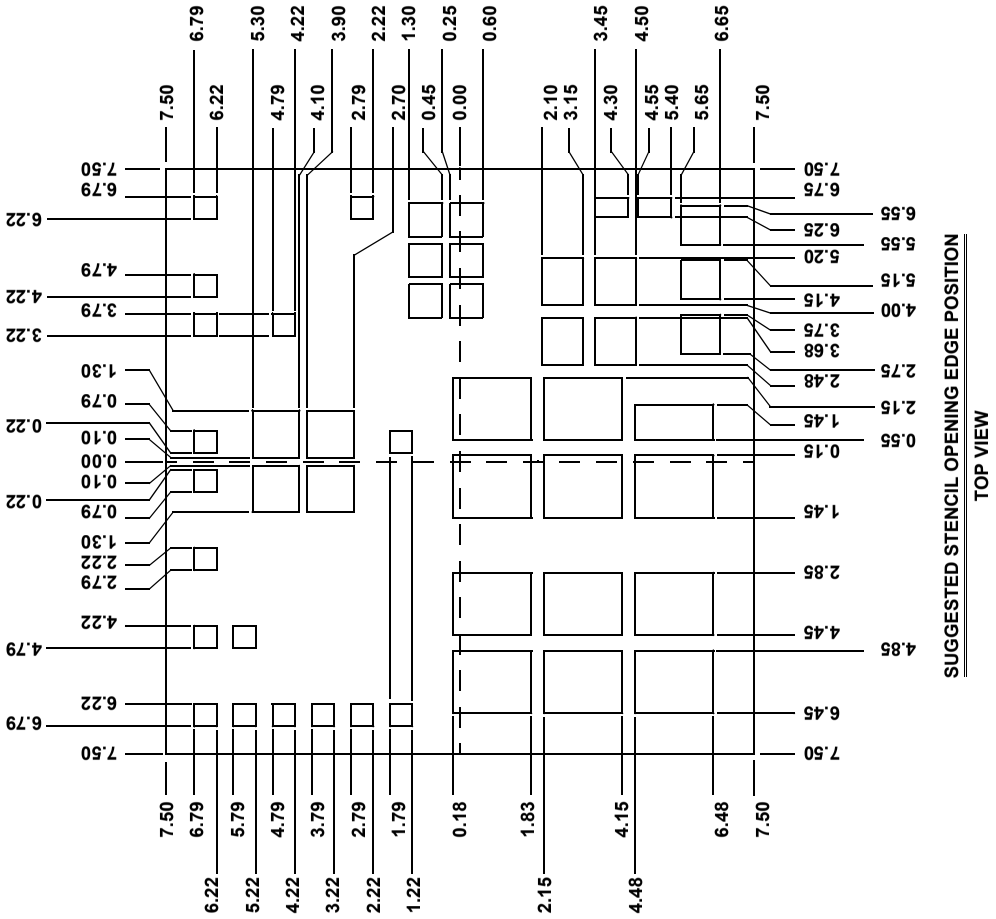


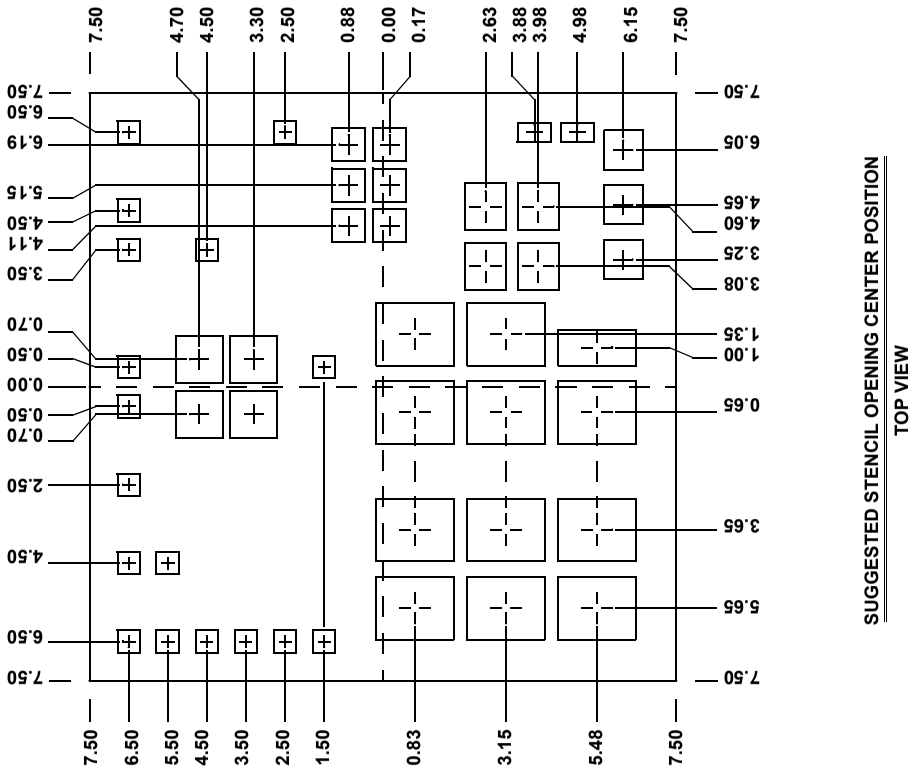

DIMENSIONAL DETAILS FOR THE 5 EXPOSED PADS
BOTTOM VIEW

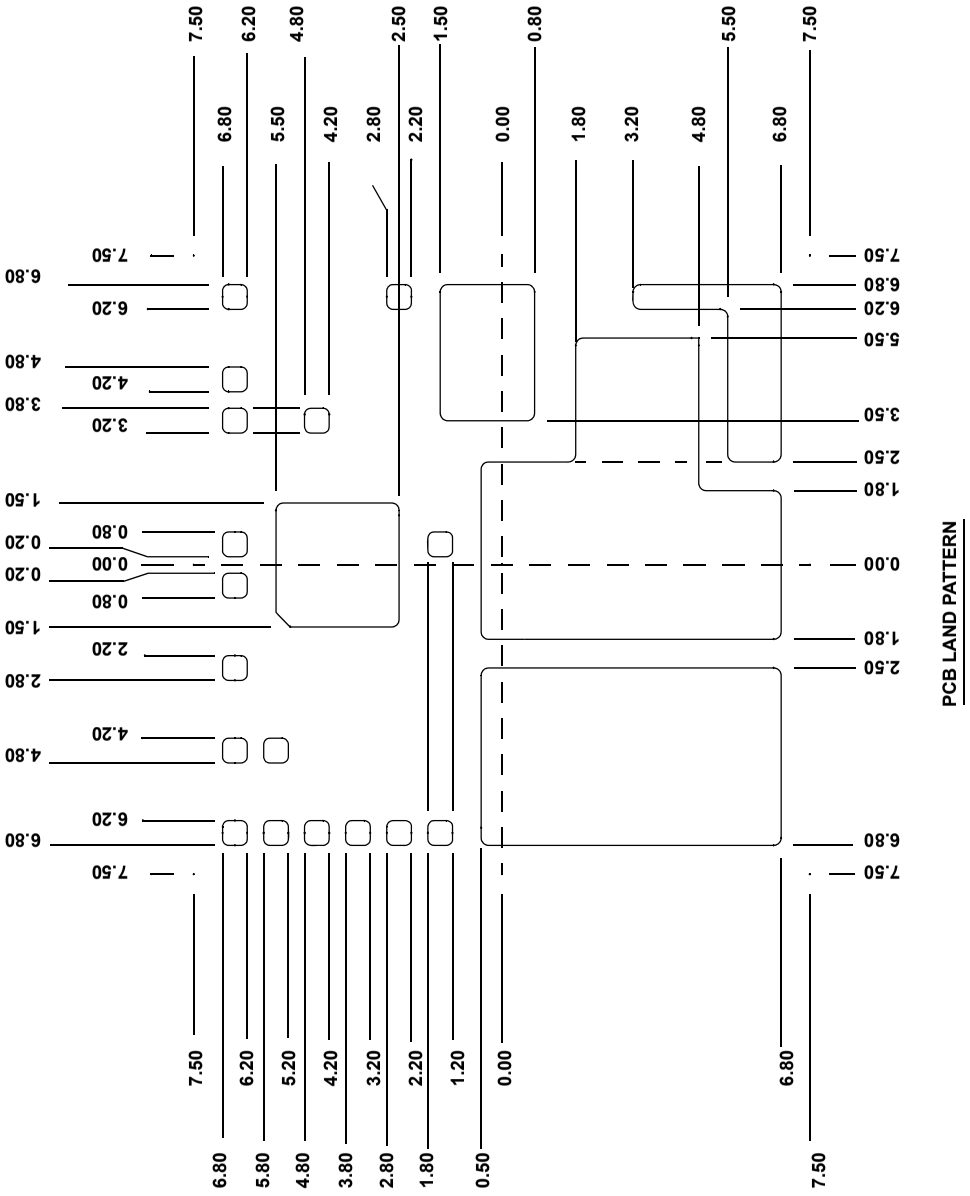



CENTERLINE POSITION DETAILS FOR THE 5 EXPOSED DAPS
BOTTOM VIEW


TERMINAL AND PAD EDGE DETAILS
BOTTOM VIEW


SUGGESTED STENCIL OPENING EDGE POSITION
TOP VIEW


SUGGESTED STENCIL OPENING CENTER POSITION
TOP VIEW


PCB LAND PATTERN

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