

3-A, 3.3/5-V INPUT, ADJUSTABLE SWITCHING REGULATOR WITH AUTO-TRACK™ SEQUENCING



FEATURES

- Up to 3-A Output Current at 85°C
- 3.3-V / 5-V Input Voltage
- Wide-Output Voltage Adjust (0.9 V to 3.6 V)
- Efficiencies Up To 94%
- On/Off Inhibit
- Undervoltage Lockout (UVLO)
- Output Overcurrent Protection (Nonlatching, Auto-Reset)
- Overtemperature Protection
- Ambient Temperature Range: -40°C to 85°C

- Point-of-Load Alliance (POLA™) Compatible
- Surface Mount Package
- Safety Agency Approvals:
 UL/IEC/CSA-22.2 60950-1

APPLICATIONS

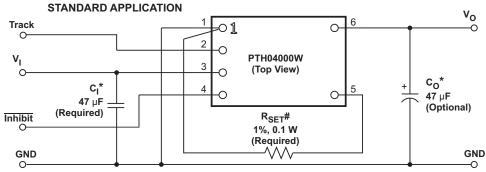
Telecommunications, Instrumentation, and General-Purpose Circuits



DESCRIPTION

The PTH04000W is a highly integrated, low-cost switching regulator module that delivers up to 3 A of output current. Occupying a small PCB area, the PTH04000W provides output current at a high efficiency and with minimal power dissipation, thereby eliminating the need for a heat sink. Their small size (0.75 inch \times 0.5 inch), high efficiency, and low cost makes these modules practical for a variety of applications.

The input voltage range of the PTH04000W is from 3 V to 5.5 V, allowing operation from either a 3.3-V or 5-V input bus. Using state-of-the-art switched-mode power-conversion technology, the PTH04000W can step down to voltages as low as 0.9 V from a 5-V input bus, with typically less than 1 W of power dissipation. The output voltage can be adjusted to any voltage over the range, 0.9 V to 3.6 V, using a single external resistor. This series includes Auto-Track™ sequencing. This feature simplifies the task of supply voltage sequencing in a power system by enabling modules to track each other, or any external voltage, during power up and power down. Other operating features include an undervoltage lockout (UVLO), on/off inhibit, output overcurrent protection, and overtemperature protection. Target applications include telecommunications, test and measurement applications, and high-end consumer products. The modules are available in both through-hole and surface-mount package options, including tape and reel. The PTH04000W is also compatible with TI's roadmap for RoHS and lead-free compliance.



- * See the Application Information section for capacitor recommendations.
- # See the Application Information section for R_{SET} values.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

POLA, Auto-Track, TMS320 are trademarks of Texas Instruments.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			PTH04000W	UNIT
T _A	Operating free-air temperature	Over V _I range	-40 to 85	°C
	Lead temperature (H suffix)	5 seconds	260	
	Solder reflow temperature (S suffix)	Surface temperature of module body or pins	235	°C
	Solder reflow temperature (Z suffix) ⁽²⁾	Surface temperature of module body or pins	260 ⁽²⁾	
T _{stg}	Storage temperature		-55 to 125	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
VI	Input voltage	3	5.5	V
T _A	Operating free-air temperature	-40	85	°C

PACKAGE SPECIFICATIONS

PTH04000Wx (Suffix AH, AS and AZ)								
Weight	1.5 grams							
Flammability								
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 msec, sine, mounted	500 G ⁽¹⁾						
Mechanical vibration								

(1) Qualification limit.

Submit Documentation Feedback

Copyright © 2005–2007, Texas Instruments Incorporated

⁽²⁾ Moisture Sensitivity Level (MSL) Rating Level-3-260C-168HR



ELECTRICAL CHARACTERISTICS

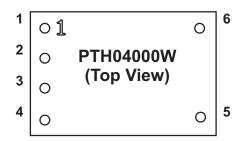
at 25°C free-air temperature, $V_I = 5 \text{ V}$, $V_O = 3.3 \text{ V}$, $I_O = I_O(\text{Max})$, $C_I = 47 \mu\text{F}$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Io	Output current	T _A = 25°C, natural convection	0		3 (1)	Α
VI	Input voltage range	Over I _O range	3 (2)		5.5	V
V _{O(TOL)}	Set-point voltage tolerance	T _A = 25°C			±2 ⁽³⁾	%V _O
	Temperature variation	-40°C ≤ T _A ≤ 85°C		±0.5		%V _O
	Line regulation	Over V _I range		±1		mV
	Load regulation	Over I _O range		±5		mV
	Total output voltage variation	Includes set-point, line, load, -40°C ≤ T _A ≤ 85°C			±3 ⁽³⁾	%V _O
V	Output valtage adjust range	V _I ≥ 4.5 V	0.9		3.6	V
$V_{O(ADJ)}$	Output voltage adjust range	V _I < 4.5 V	0.9		$V_1 - 1.1^{(2)}$	V
		T _A = 25C, I _O = 2 A				
		R_{SET} = 475 Ω , V_O = 3.3 $V^{(2)}$		92%		
		$R_{SET} = 2.32 \text{ k}\Omega, V_O = 2.5 \text{ V}^{(2)}$		89%		
η	Efficiency	$R_{SET} = 6.65 \text{ k}\Omega, V_{O} = 1.8 \text{ V}$		86%		
		$R_{SET} = 11.5 \text{ k}\Omega, V_{O} = 1.5 \text{ V}$		84%		
		$R_{SET} = 26.1 \text{ k}\Omega, V_{O} = 1.2 \text{ V}$		82%		
		$R_{SET} = 84.5 \text{ k}\Omega, V_O = 1 \text{ V}$		78%		
	Output voltage ripple	20 MHz bandwith		10		mV_{PP}
	Overcurrent threshold	Reset, followed by autorecovery		7		Α
		1 A/s load step from 50% to 100% I_{O} max, C_{O} = 47 μ F				
	Transient response	Recovery time		70		μs
		V _O over/undershoot		100		mV
I _{IL} track	Track Input Current (pin 2)	Pin to GND			-130	μΑ
dV _{track} /dt	Track Slew Rate Capability	$C_O \le C_O(max)$			1	V/ms
10/10		V _I = increasing		2.95	3	
UVLO	Undervoltage lockout	V _I = decreasing	2.7	2.8		V
		Input high voltage (V _{IH})	V _I - 0.5		Open (4)	
	Inhibit control (pin 4)	Input low voltage (V _{IL})	-0.2		0.6	V
		Input low current (I _{IL})		10		μA
I _{I (STBY)}	Input standby current	Inhibit (pin 4) to GND, Track (pin 2) open			1	mA
Fs	Switching frequency	Over V _I and I _O ranges		700		kHz
	External input capacitance	Ceramic type (C1)	47 (5)			μF
		Ceramic type (C2) 0 (6)			150	
	External output capacitance (6)	Nonceramic type (C3)		47 (6)	560 ⁽⁷⁾	μF
		Equivalent series resistance (nonceramic)	4 (8)			mΩ
MTBF	Calculated reliability	Per Telcordia SR-332, 50% stress, T _A = 40C, ground benign	15			10 ⁶ Hr

- (1) See SOA temperature derating curves to identify maximum output current at higher ambient temperatures.
- (2) The minimum input voltage is 3 V or (V_O + 1.1) V, whichever is greater. A 5-V input bus is recommended for output voltages higher than 2 V.
- (3) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
- (4) This control pin has an internal pullup to the input voltage V₁. Do not tie the inhibit pin to V₁ or to another module's inhibit pin. If it is left open circuit, the module operates when input power is applied. A small low-leakage (< 100 nA) MOSFET is recommended for control. See the application section for further guidance.</p>
- (5) An external 47-μF ceramic capacitor is required across the input (V_I and GND) for proper operation. Locate the capacitor close to the module.
- 6) An external output capacitor is not required for basic operation. Additional capacitance at the load improves the transient response.
- (7) This is the calculated maximum capacitance. The minimum ESR limitation often results in a lower value. See the capacitor application information for further guidance.
- (8) This is the minimum ESR for all the electrolytic (nonceramic) capacitance. Use 7 mΩ as the minimum when calculating the total equivalent series resistance (ESR) using the max-ESR values specified by the capacitor manufacturer.



PIN ASSIGNMENT



TERMINAL FUNCTIONS

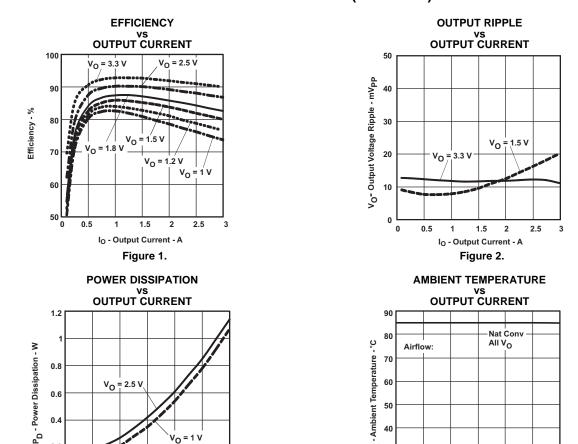
TERMI	NAL	1/0	DECODIDATION				
NAME	NO.	1/0	DESCRIPTION				
GND	1		This is the common ground connection for the V_I and V_O power connections. It is also the 0 V_{dc} reference for the <i>Inhibit</i> , the V_O <i>Adjust</i> , and the <i>Track</i> control inputs.				
Track	2	ı	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the output voltage follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V _I .				
			NOTE: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, see the related application report (SLTA054).				
VI	3	- 1	The positive input voltage power node to the module, which is referenced to common GND.				
Inhibit	4	ı	The Inhibit pin is an open-collector/drain-negative logic input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output voltage whenever a valid input source is applied.				
V _O Adjust	5	I	A 1% resistor must be connected between this pin and GND (pin 1) to set the output voltage of the module higher than 0.9 V. If left open-circuit, the output voltage defaults to this value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is from 0.9 V to 3.6 V. The electrical specification table gives the standard resistor value for a number of common output voltages. See the application information for further guidance.				
Vo	6	0	The regulated positive power output with respect to the GND node.				

Submit Documentation Feedback

Copyright © 2005–2007, Texas Instruments Incorporated



TYPICAL CHARACTERISTICS (5-V INPUT)(1)(2)



The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the

2.5

1.5 IO - Output Current - A

Figure 3.

converter. Applies to Figure 1, Figure 2, and Figure 3.

The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Applies to Figure 4.

30

20

0.5

2

IO - Output Current - A

Figure 4.

2.5

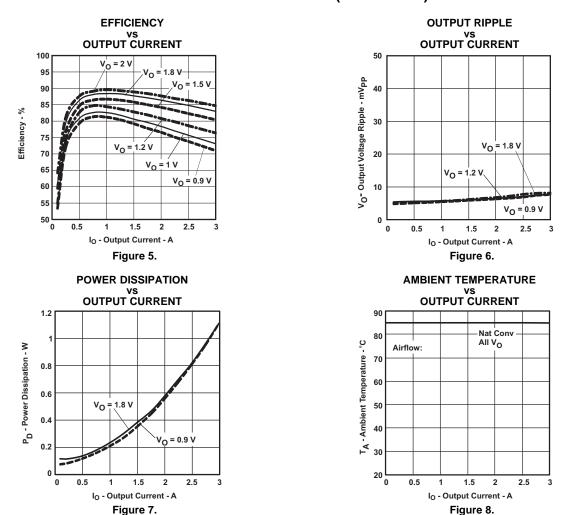
0.2

0

0.5



TYPICAL CHARACTERISTICS (3.3-V INPUT)(1)(2)



- The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the
- converter. Applies to Figure 5, Figure 6, and Figure 7.

 The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Applies to Figure 8.



APPLICATION INFORMATION

Adjusting the Output Voltage of the PTH04000W Wide-Output Adjust Power Modules

The $V_{\rm O}$ Adjust control (pin 5) sets the output voltage of the PTH04000W product. The adjustment range is from 0.9 V to 3.6 V. The adjustment method requires the addition of a single external resistor, $R_{\rm SET}$, that must be connected directly between the $V_{\rm O}$ Adjust and GND pin 1. Table 1 gives the standard external resistor for a number of common bus voltages, along with the actual voltage the resistance produces.

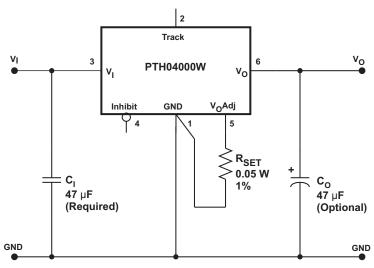
For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 2. Figure 9 shows the placement of the required resistor.

$$R_{SET} = 10 \text{ k}\Omega \text{ x } \frac{0.891 \text{ V}}{\text{V}_{\Omega} - 0.9 \text{ V}} - 3.24 \text{ k}\Omega$$

Table 1. Standard Values of R_{set} for Common Output Voltages

	_	
V _O (Required)	R _{SET} (Standard Value)	V _O (Actual)
3.3 V ⁽¹⁾	475 Ω	3.298 V
2.5 V ⁽¹⁾	2.32 kΩ	2.502 V
2 V	4.87 kΩ	1.999 V
1.8 V	6.65 kΩ	1.801 V
1.5 V	11.5 kΩ	1.504 V
1.2 V	26.1 kΩ	1.204 V
1 V	84.5 kΩ	1.001 V
0.9 V	Open	0.9 V

 The minimum input voltage is 3 V or (V_O + 1.1) V, whichever is greater.



- (1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 1 using dedicated PCB traces.
- (2) Never connect capacitors from V_O Adjust to either GND or V_O . Any capacitance added to the V_O Adjust pin affects the stability of the regulator.

Figure 9. Vo Adjust Resistor Placement



Table 2. Calculated Set-Point Resistor Values

V _O Required	R _{SET}	V _O Required	R _{SET}	V _O Required	R _{SET}
0.900	Open	1.475	12.3 kΩ	2.55	2.16 kΩ
0.925	353 kΩ	1.50	11.6 kΩ	2.60	2.00 kΩ
0.950	175 kΩ	1.55	10.5 kΩ	2.65	1.85 kΩ
0.975	116 kΩ	1.60	9.49 kΩ	2.70	1.71 kΩ
1.000	85.9 kΩ	1.65	8.64 kΩ	2.75	1.58 kΩ
1.025	68.0 kΩ	1.70	7.90 kΩ	2.80	1.45 kΩ
1.050	56.2 kΩ	1.75	7.24 kΩ	2.85	1.33 kΩ
1.075	47.7 kΩ	1.80	6.66 kΩ	2.90	1.22 kΩ
1.100	41.3 kΩ	1.85	6.14 kΩ	2.95	1.11 kΩ
1.125	36.4 kΩ	1.90	5.67 kΩ	3.00	1.00 kΩ
1.150	32.4 kΩ	1.95	5.25 kΩ	3.05	904 Ω
1.175	29.2 kΩ	2.00	4.86 kΩ	3.10	810 Ω
1.200	26.5 kΩ	2.05	4.51 kΩ	3.15	720 Ω
1.225	24.2 kΩ	2.10	4.19 kΩ	3.20	634 Ω
1.250	22.2 kΩ	2.15	3.89 kΩ	3.25	551 Ω
1.275	20.5 kΩ	2.20	3.61 kΩ	3.30	473 Ω
1.300	19.0 kΩ	2.25	3.36 kΩ	3.35	397 Ω
1.325	17.7 kΩ	2.30	3.12 kΩ	3.40	324 Ω
1.350	16.6 kΩ	2.35	2.90 kΩ	3.45	254 Ω
1.375	15.5 kΩ	2.40	2.70 kΩ	3.50	187 Ω
1.400	14.6 kΩ	2.45	2.51 kΩ	3.55	122 Ω
1.425	13.7 kΩ	2.50	2.33 kΩ	3.60	60 Ω
1.450	13.0 kΩ				



CAPACITOR RECOMMENDATIONS for the PTH04000W WIDE-OUTPUT ADJUST POWER MODULES

Input Capacitor

The minimum required input capacitor(s) is 47-µF of ceramic capacitance, in either an X5R or X7R temperature tolerance. The ceramic capacitors should be located within 0.5 inch (1,27 cm) of the regulator's input pins. Electrolytic capacitors can also be used at the input, but only in addition to the required ceramic capacitance. The minimum ripple current rating for nonceramic capacitors should be at least 200 mA rms. The ripple current rating of electrolytic capacitors is a major consideration when they are used at the input.

When specifying regular tantalum capacitors for use at the input, a minimum voltage rating of $2 \times$ (maximum dc voltage + ac ripple) is highly recommended. This is standard practice to ensure reliability. Polymer-tantalum capacitors are not affected by this requirement.

For improved ripple reduction on the input bus, additional ceramic capacitors can be used to complement the minimum requirement.

Output Capacitors (Optional)

For applications with load transients (sudden changes in load current), the regulator response benefits from additional external output capacitance. The recommended output capacitance of 47 μ F allows the module to meet its transient response specification. A high-quality computer-grade electrolytic capacitor should be adequate.

Electrolytic capacitors should be located close to the load circuit. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz. Aluminum electrolytic capacitors are suitable for ambient temperatures above 0°C. For operation below 0°C, tantalum or OS-CON type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 4 m Ω (7 m Ω using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR type capacitors are identified in Table 3.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors becomes less effective. To further improve the reflected input ripple current, or the output transient response, multilayer ceramic capacitors must be added. Ceramic capacitors have low ESR and their resonant frequency is higher than the bandwidth of the regulator. When placed at the output, their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 150 μ F. Also, to prevent the formation of local resonances, do not exceed the maximum number of capacitors specified in the capacitor table.

Tantalum Capacitors

Additional tantalum type capacitors can be used at both the input and output, and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595, and Kemet T495/T510/T520 capacitors series are suggested over many other tantalum types due to their rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR and lower ripple current capability. These capacitors are also less reliable as they have lower power dissipation capability and surge current ratings. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications. When specifying OS-CON and polymer-tantalum capacitors for the output, the minimum ESR limit is encountered well before the maximum capacitance value is reached.

Capacitor Table

The capacitor table, Table 3, identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type. This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The rms rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.



Designing for Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/s. The typical voltage deviation for this load transient is given in the data sheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases, special attention must be paid to the type, value, and ESR of the capacitors selected.

If the transient performance requirements exceed those specified in the data sheet, the selection of output capacitors becomes more important. Review the minimum ESR in the characteristic data sheet for details on the capacitance maximum.

Table 3. Recommended Input/Output Capacitors (1)

		CAPA	ACITOR CHARACT	ERISTICS		QU	ANTITY	
CAPACITOR VENDOR/ COMPONENT SERIES	WORKING VOLTAGE	VALUE (F)	EQUIVALENT SERIES RESISTANCE (ESR)	85C MAXIMUM RIPPLE CURRENT (I _{rms})	PHYSICAL SIZE (mm)	INPUT BUS ⁽²⁾	OUTPUT BUS	VENDOR NUMBER
Panasonic WA (SMT) FC (SMT)	10 V 25 V	120 47	0.035 Ω 0.400 Ω	2800 mA 230 mA	8 × 6,9 8 × 6,2	1 1	$\leq 4^{(2)}$ $1^{(2)}$	EEFWA1A121P ⁽³⁾ EEVFC1E470P ⁽³⁾
Panasonic SL SP-cap(SMT)	6.3 V 6.3 V	47 56	0.018 Ω 0.009 Ω	2500 mA 3000 mA	7,3 ×4,3 7,3 × 4,3	1 1	≤ 2 ≤ 1	EEFCD0J470R EEFSL0J560R
United Chemi-con PXA (SMT) FS LXZ MVZ (SMT)	10 V 10 V 16 V 16 V	47 100 100 100	0.031 Ω 0.040 Ω 0.250 Ω 0.440 Ω	2250 mA 2100 mA 290 mA 230 mA	6,3 × 5,7 6,3 × 9,8 6,3 × 11,5 6,3 × 5,7	1 1 1	1 ≤3 1 1	PXA10VC470MF60TP 10FS100M LXZ16VB101M6X11LL MVZ16VC101MF60TP
Nichicon UWG (SMT) F559(Tantalum) PM	16 V 10 V 10 V	100 100 100	0.400 Ω 0.055 Ω 0.550 Ω	230 mA 2000 mA 210 mA	8 × 6,2 7,7 × 4,3 6 × 11	1 1 1	1 ≤3 1	UWG1C101MCR1GS F551A107MN UPM1A101MEH
Sanyo Os-con\ POS-Cap SVP (SMT) SP	10 V 6.3 V 10 V	68 47 56	0.025 Ω 0.074 Ω 0.045 Ω	2400 mA 1110 mA 1710 mA	7,3 × 4,3 5 × 6 6,3 × 5	1 1 1	≤ 3 ≤ 3 ≤ 3	10TPE68M 6SVP47M 10SP56M
AVX Tantalum TPS (SMD)	10 V 10 V	47 47	0.100 Ω 0.060 Ω	1100 mA > 412 mA	7,3L × 4,3W × 4,1H	1 1	≤ 3 ≤ 53	TPSD476M010R0100 TPSB476M010R0500
Kemet T520 (SMD) AO-CAP	10 V 6.3 V	68 47	0.060 Ω 0.028 Ω	>1200 mA >1100 mA	7,3L × 5,7W × 4H	1 1	≤ 3 ≤ 3	T520V686M010ASE060 A700V476M006AT
Vishay/Sprague 594D/595D (SMD)	10 V 10 V	68 68	0.100 Ω 0.240 Ω	>1000 mA 680 mA	7,3L × 6W × 4,1H	1 1	≤ 3 ≤ 3	594D686X0010C2T 595D686X0010C2T
94SL	16 V	47	0.070 Ω	1550 mA	8×5	1	≤ 3	94SL476X0016EBP
TDK Ceramic X5R (Leaded)	10 V	47	0.005 Ω	>1400 mA	7,5L × 4,0W × 8,0H	≥ 1	≤ 2	FK22X5R1A476M
TDK Ceramic X5R Murata Ceramic X5R Kemet	6.3 V 6.3 V 6.3 V	22 22 22	0.002 Ω 0.002 Ω 0.002 Ω	>1400 mA >1000 mA >1000 mA	1210 case 3225 mm	≥ 2 ⁽⁴⁾ ≥ 2 ⁽⁴⁾ ≥ 2 ⁽⁴⁾	≤3 ≤3 ≤3	C3225X5R0J226KT/MT GRM32ER61J223M C1210C226K9PAC
TDK Ceramic X5R Murata Ceramic X5R Kemet	6.3 V 6.3 V 6.3 V	47 47 47	0.002 Ω 0.002 Ω 0.002 Ω	>1400 mA >1000 mA >1000 mA	1210 case 3225 mm	≥ 1 ≥ 1 ≥ 1	≤ 2 ≤ 2 ≤ 2	C3225X5R0J476KT/MT GRM32ER60J476M/6.3 C1210C476K9PAC

- (1) Check with capacitor manufacturers for availability and lead-free status.
- (2) A ceramic capacitor is required on the input. An electrolytic capacitor can be added to the output for improved transient response.
- (3) An optional through-hole capacitor available.
- (4) A total capacitance of 44 μF is an acceptable replacement for a single 47-μF capacitor.

Submit Documentation Feedback



Features of the PTH/PTV Family of Nonisolated, Wide-Output Adjust Power Modules

POLA™ Compatibility

The PTH/PTV family of nonisolated, wide-output adjustable power modules from Texas Instruments are optimized for applications that require a flexible, high-performance module that is small in size. Each of these products are POLA™ compatible. POLA-compatible products are produced by a number of manufacturers, and offer customers advanced, nonisolated modules with the same footprint and form factor. POLA parts are also ensured to be interoperable, thereby providing customers with true second-source availability.

Soft-Start Power Up

The Auto-Track feature allows the power up of multiple PTH/PTV modules to be directly controlled from the Track pin. However, in a stand-alone configuration, or when the Auto-Track feature is not being used, the *Track* pin should be directly connected to the input voltage, V_I (see Figure 10).

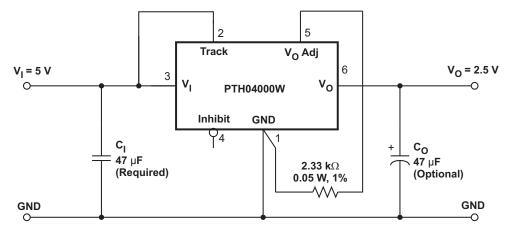


Figure 10. Power-Up Application Circuit

When the *Track* pin is connected to the input voltage, the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

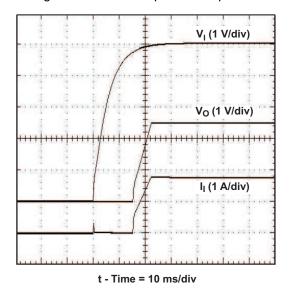


Figure 11. Power-Up Waveform



From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically less than 5 ms) before allowing the output voltage to rise. The output then progressively rises to the module set-point voltage. Figure 11 shows the soft-start power-up characteristic of the PTH04000W, operating from a 5-V input bus and configured for a 2.5-V output. The waveforms were measured with a 3-A resistive load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power up is complete within 25 ms.

Current Limit Protection

The PTH04000W modules protect against load faults with a continuous current limit characteristic. Under a load fault condition, the output current cannot exceed the current limit value. Attempting to draw current that exceeds the current limit value causes the output voltage to be progressively reduced. Current is continuously supplied to the fault until it is removed. On removal of the fault, the output voltage promptly recovers.

Thermal Shutdown

Thermal shutdown protects the module internal circuitry against excessively high temperatures. A rise in temperature may be the result of a drop in airflow, a high ambient temperature, or a sustained current limit condition. If the junction temperature of the internal components exceeds 150C, the module shuts down. This reduces the output voltage to zero. The module starts up automatically, by initiating a soft-start power up when the sensed temperature decreases 10C below the thermal shutdown trip point.

Output On/Off Inhibit

For applications requiring output voltage on/off control, the PTH04000W power module incorporates an output on/off Inhibit control (pin 4). The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power module functions normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to Vin with respect to GND.

Figure 12 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit control has its own internal pullup to V_I potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the *Inhibit* control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 20 ms. Figure 13 shows the typical rise in the output voltage, following the turn off of Q1. The turn off of Q1 corresponds to the rise in the waveform, V_(INH). The waveforms were measured with a 2-A resistive load.

2 Submit Documentation Feedback



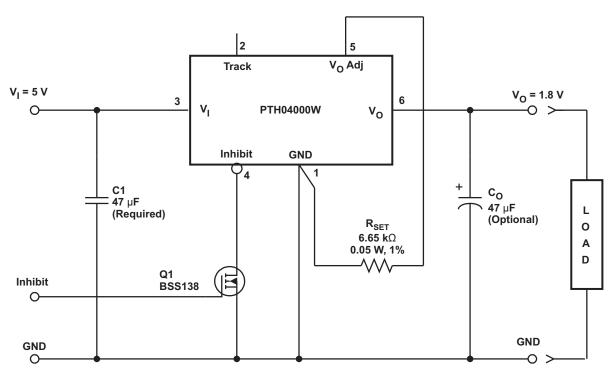


Figure 12. On/Off Inhibit Control Circuit

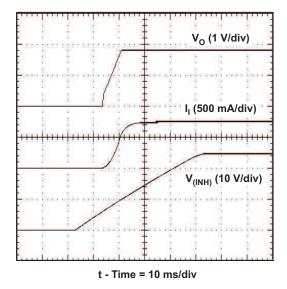


Figure 13. Power Up Response From Inhibit Control



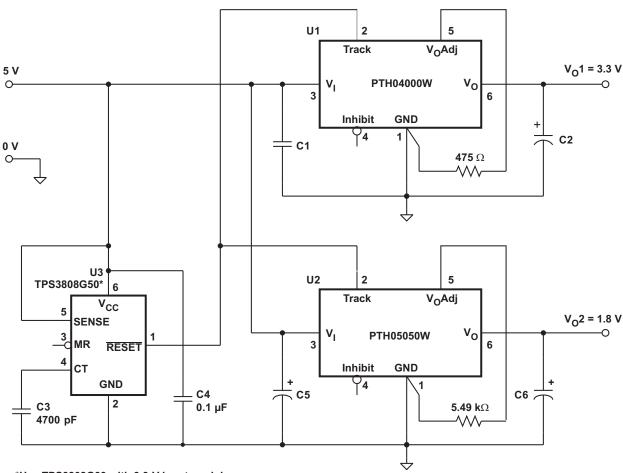
Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI ICs such as the TMS320™ DSP family, microprocessors, and ASICs.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin ⁽¹⁾. This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module output remains at its set-point ⁽²⁾. As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output is 1 V. If the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

Under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit ⁽³⁾. For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.



*Use TPS3808G33 with 3.3-V input modules.

Figure 14. Auto-Track Circuit



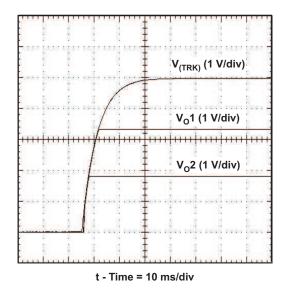


Figure 15. Simultaneous Power-Up With Auto-Track Control

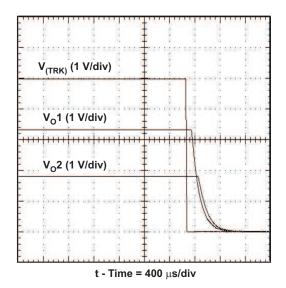


Figure 16. Simultaneous Power-Down With Auto-Track Control

Typical Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common track control signal. This can be an open-collector (or open drain) device, such as a power-up reset voltage supervisor IC. See U3 in Figure 14.

To coordinate a power-up sequence, the Track control must first be pulled to ground potential. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 20 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization ⁽⁴⁾, enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes a built-in time delay, is an ideal component for automatically controlling the track inputs at power up.

Figure 14 shows how the TPS3808G50 supply voltage supervisor IC (U3) can be used to coordinate the sequenced power-up of two 5-V input Auto-Track modules. The output of the TPS3808G50 supervisor becomes active above an input voltage of 0.8 V, enabling it to assert a ground signal to the common track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 27 ms after the input voltage has risen above U3's voltage threshold, which is 4.65 V. The 27-ms time period is controlled by the capacitor C3. The value of 4700 pF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the track control voltage is allowed to rise. When U3 removes the ground signal, the track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

Figure 15 shows the output voltage waveforms from the circuit of Figure 14 after input voltage is applied to the circuit. The waveforms, V_01 and V_02 represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. V_01 and V_02 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is reapplied to the common track control. This pulls the track inputs to zero volts, forcing the output of each module to follow. See Figure 16. Power-down is normally complete before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that an input voltage is no longer present, their outputs can no longer follow the voltage applied at their track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the Auto-Track slew rate capability.



Notes on Use of Auto-Track™

- 1. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
- 2. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
- 3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage V_I.
- 4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 20 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
- 5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises at a quicker and more linear rate after input power has been applied.

Submit Documentation Feedback

Copyright © 2005–2007, Texas Instruments Incorporated



PACKAGE OPTION ADDENDUM

4-Apr-2020

PACKAGING INFORMATION

www.ti.com

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
PTH04000WAH	ACTIVE	Through- Hole Module	EUS	6	56	RoHS Exempt & Green	SN	N / A for Pkg Type	-40 to 85		Samples
PTH04000WAS	ACTIVE	Surface Mount Module	EUT	6	49	Non-RoHS & Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH04000WAST	ACTIVE	Surface Mount Module	EUT	6	250	Non-RoHS & Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH04000WAZ	ACTIVE	Surface Mount Module	EUT	6	49	RoHS Exempt & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH04000WAZT	ACTIVE	Surface Mount Module	EUT	6	250	RoHS Exempt & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

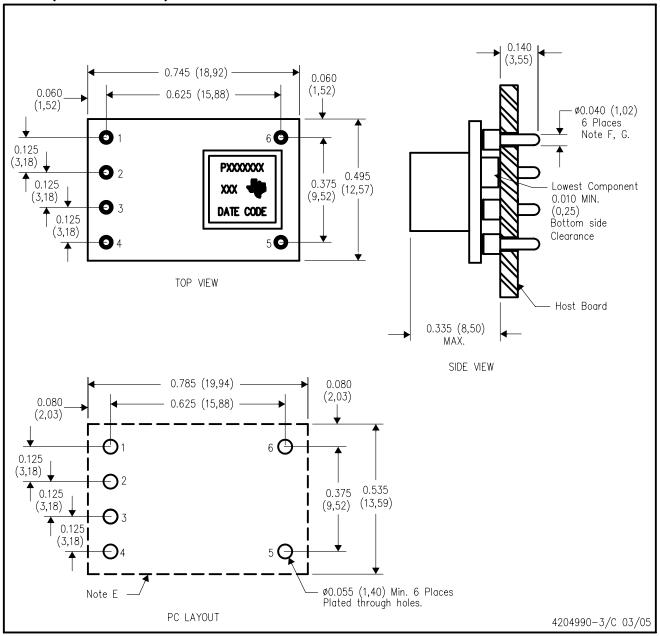
4-Apr-2020

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

EUS (R-PDSS-T6)

DOUBLE SIDED MODULE



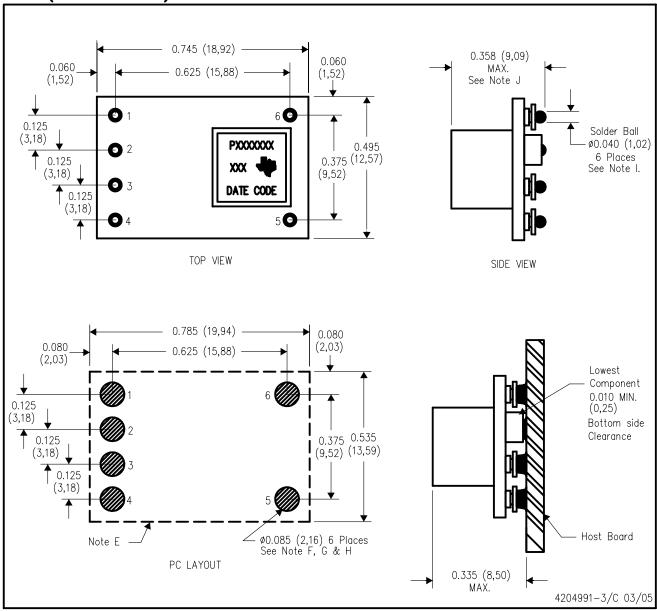
NOTES:

- All linear dimensions are in inches (mm).
- B. This drawing is subject to change without notice.
- C. 2 place decimals are ± 0.030 (± 0.76 mm). D. 3 place decimals are ± 0.010 (± 0.25 mm).
- E. Recommended keep out area for user components.
- F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
- G. All pins: Material Copper Alloy Finish - Tin (100%) over Nickel plate



EUT (R-PDSS-B6)

DOUBLE SIDED MODULE



NOTES: All linear dimensions are in inches (mm).

- This drawing is subject to change without notice.
- 2 place decimals are ± 0.030 (± 0.76 mm).
- D. 3 place decimals are ± 0.010 (± 0.25 mm).
- Recommended keep out area for user components.
- Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
- Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
- H. Pad type: Solder mask defined.
- I. All pins: Material Copper Alloy Finish - Tin (100%) over Nickel plate Solder Ball — See product data sheet.
- J. Dimension prior to reflow solder.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

Tl's products are provided subject to Tl's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such Tl products. Tl's provision of these resources does not expand or otherwise alter Tl's applicable warranties or warranty disclaimers for Tl products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2020, Texas Instruments Incorporated