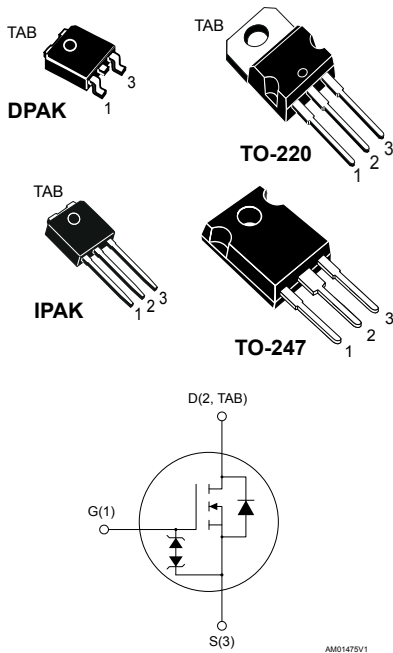


## N-channel 950 V, 1 $\Omega$ typ., 9 A MDmesh™ K5 Power MOSFETs in DPAK, TO-220, IPAK and TO-247 packages



### Features

Order codes	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STD6N95K5	950 V	1.25 $\Omega$	9 A	90 W
STP6N95K5				
STU6N95K5				
STW6N95K5				

- DPAK 950 V worldwide best  $R_{DS(on)}$
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

#### Product status link

[STD6N95K5](#)

[STP6N95K5](#)

[STU6N95K5](#)

[STW6N95K5](#)

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	9	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	90	W
$I_{AR}^{(2)}$	Max current during repetitive or single pulse avalanche	3	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	90	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_J$	Operating junction temperature range	- 55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

1. Pulse width limited by safe operating area.
2. Pulse width limited by  $T_{Jmax}$ .
3.  $I_{SD} \leq 9\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} \leq V_{(BR)DSS}$
4.  $V_{DS} \leq 760\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value			Unit
		TO-220, IPAK	DPAK	TO-247	
$R_{thj-case}$	Thermal resistance junction-case	1.39			$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb	62.5		50	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb		50		$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz Cu

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	950			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 950\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 950\text{ V}, T_c = 125\text{ °C}^{(1)}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 3\text{ A}$		1	1.25	$\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	450	-	pF
$C_{oss}$	Output capacitance		-	30	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1.6	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }760\text{ V}$	-	45	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	19	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0\text{ A}$	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 760\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 0\text{ to }10\text{ V},$ (see Figure 17. Test circuit for gate charge behavior)	-	13	-	nC
$Q_{gs}$	Gate-source charge		-	3	-	nC
$Q_{gd}$	Gate-drain charge		-	7	-	nC

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}, I_D = 3\text{ A}, R_G = 4.7\text{ }\Omega,$ $V_{GS} = 10\text{ V}$ (see Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform)	-	12	-	ns
$t_r$	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time		-	33	-	ns
$t_f$	Fall time		-	21	-	ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6\text{ A}, V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}, V_{DD} = 60\text{ V}$	-	372		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}$ ,	-	4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	22		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}, V_{DD} = 60\text{ V}$	-	522		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}, T_j = 150\text{ }^\circ\text{C}$	-	5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	20		A

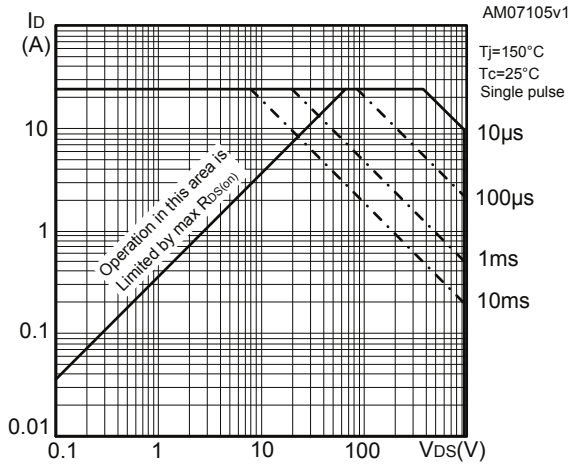
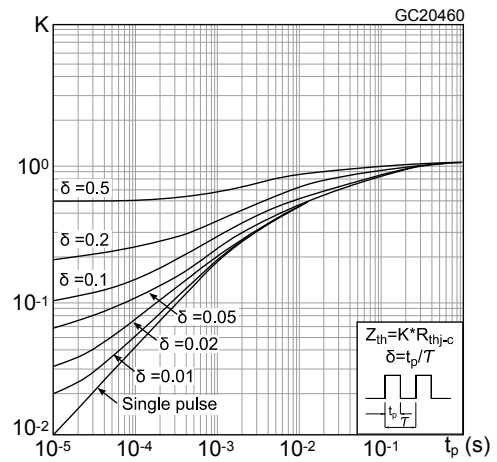
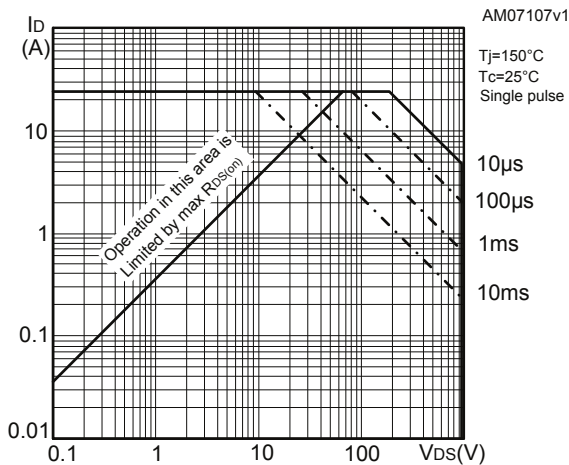
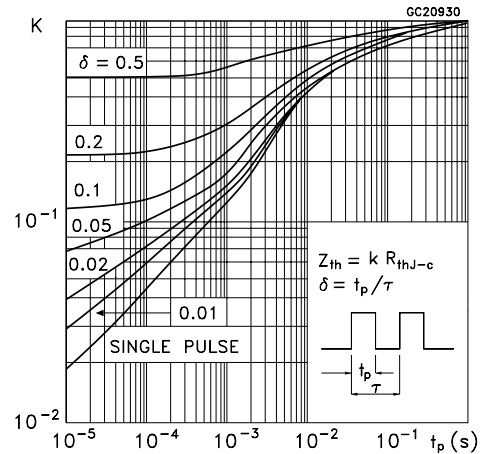
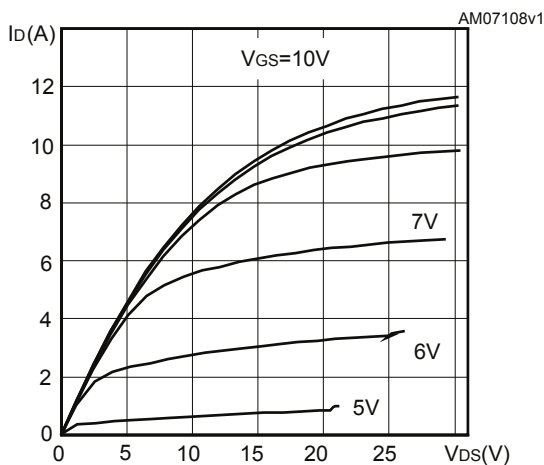
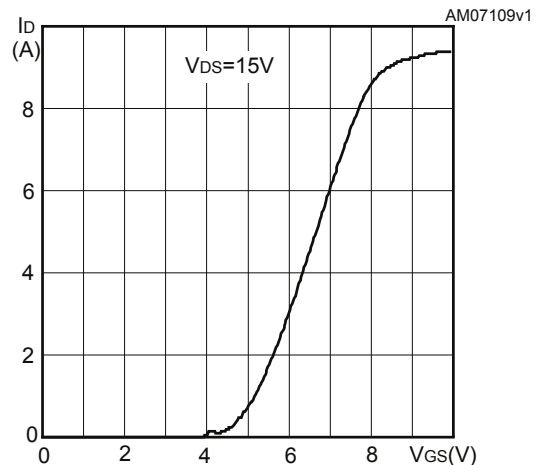
1. Pulse width limited by safe operating area.

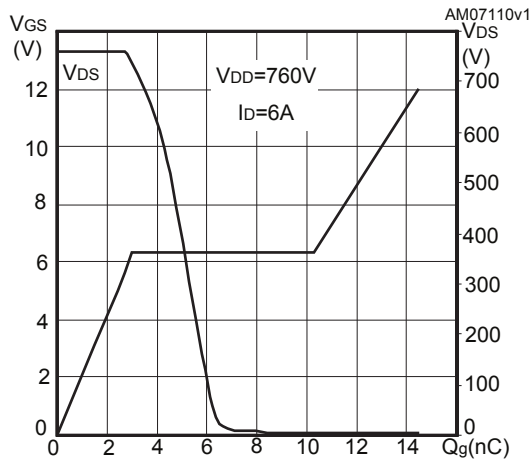
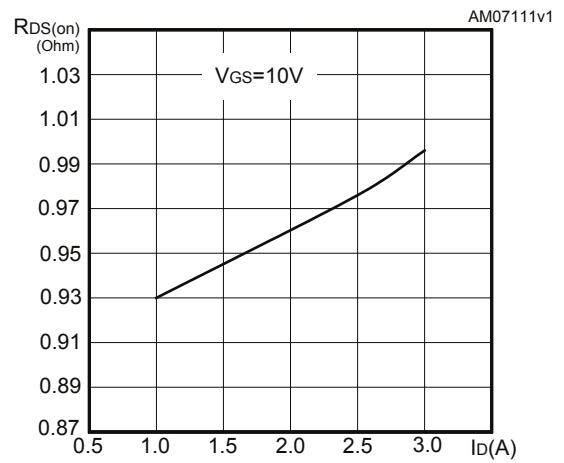
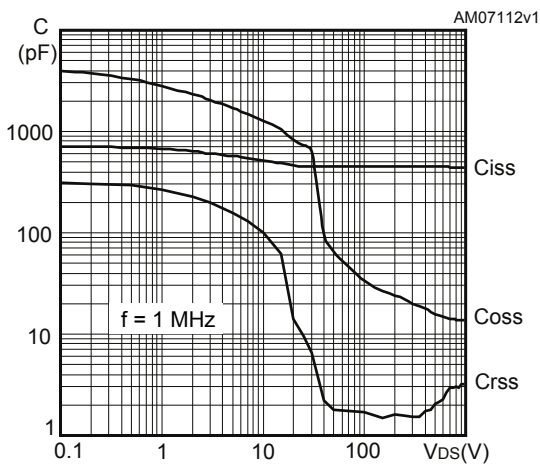
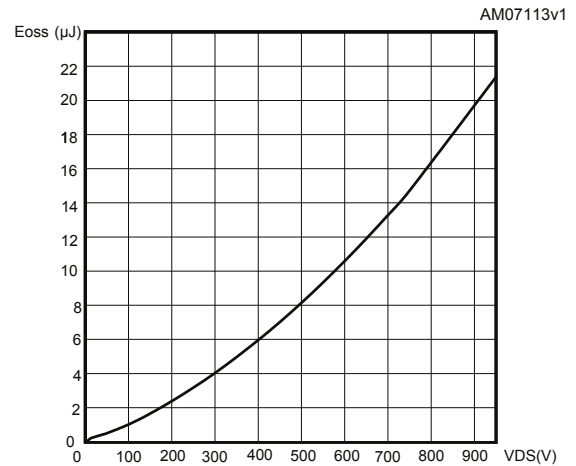
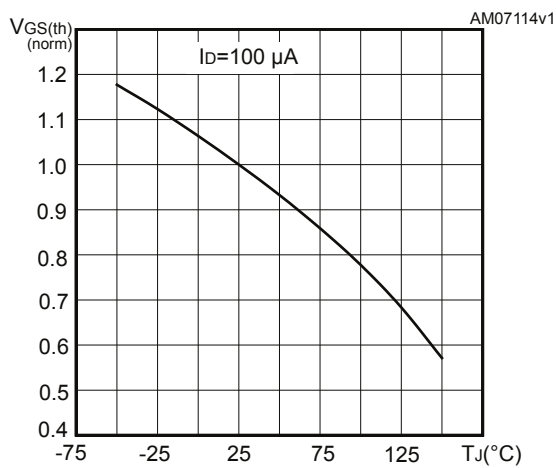
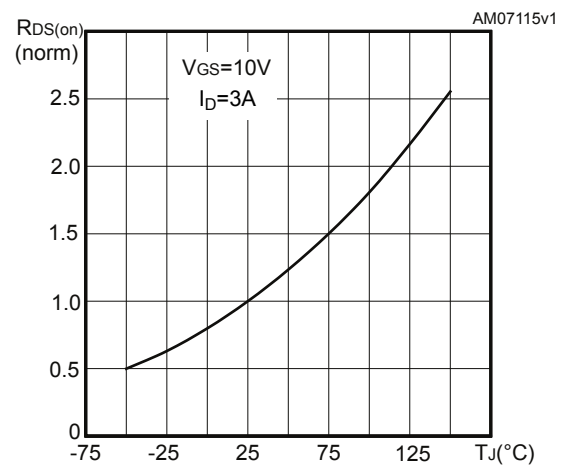
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

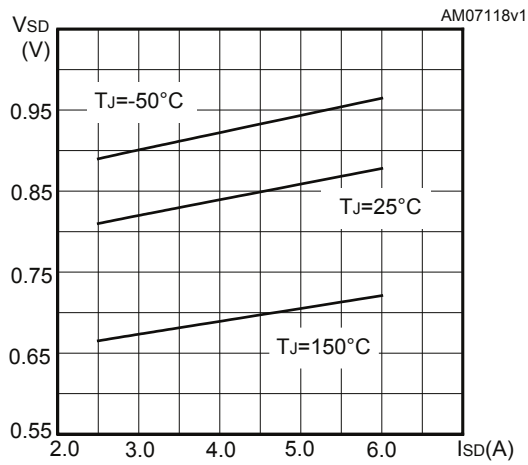
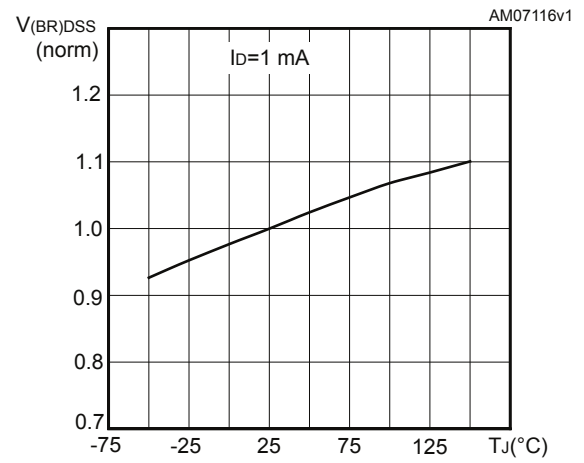
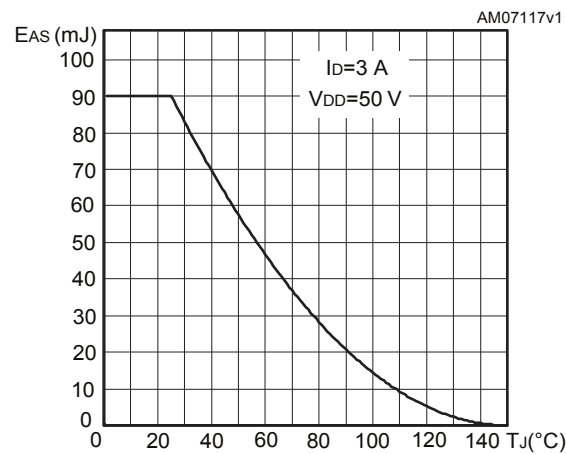
**Table 7. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}, I_D = 0\text{ A}$	$\pm 30$	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

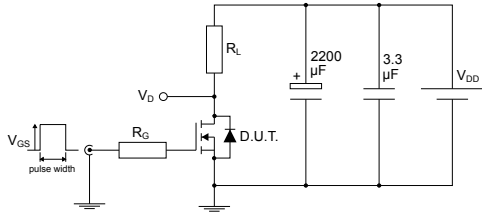
**2.1 Electrical characteristics (curves)**
**Figure 1. Safe operating area for DPAK and IPAK**

**Figure 2. Thermal impedance for DPAK and IPAK**

**Figure 3. Safe operating area for TO-220 and TO-247**

**Figure 4. Thermal impedance for TO-220 and TO-247**

**Figure 5. Output characteristics**

**Figure 6. Transfer characteristics**


**Figure 7. Gate charge vs gate-source voltage**

**Figure 8. Static drain-source on-resistance**

**Figure 9. Capacitance variations**

**Figure 10. Output capacitance storage energy**

**Figure 11. Normalized gate threshold voltage vs temperature**

**Figure 12. Normalized on-resistance vs temperature**


**Figure 13. Source-drain diode forward characteristics**

**Figure 14. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 15. Maximum avalanche energy vs starting  $T_J$** 


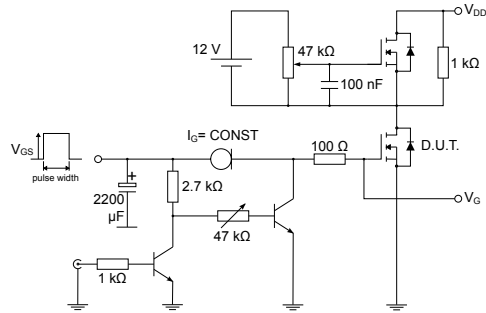
### 3 Test circuits

Figure 16. Test circuit for resistive load switching times



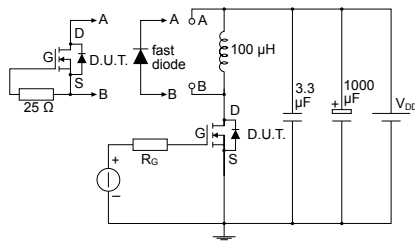
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Figure 17. Test circuit for gate charge behavior



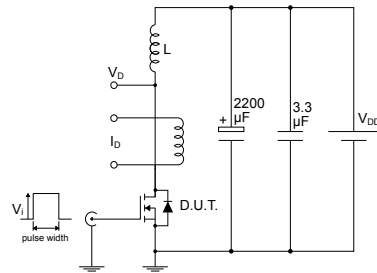
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Figure 18. Test circuit for inductive load switching and diode recovery times



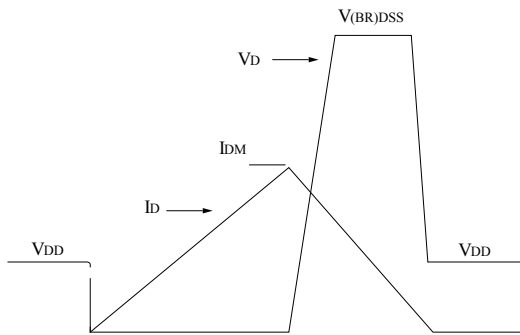
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Figure 19. Unclamped inductive load test circuit



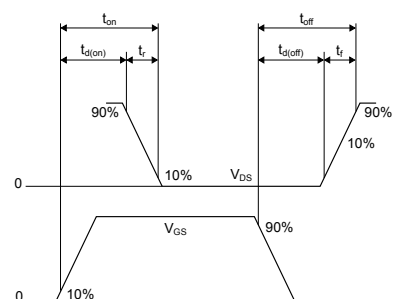
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Figure 20. Unclamped inductive waveform



AM01472v1

Figure 21. Switching time waveform



AM01473v1



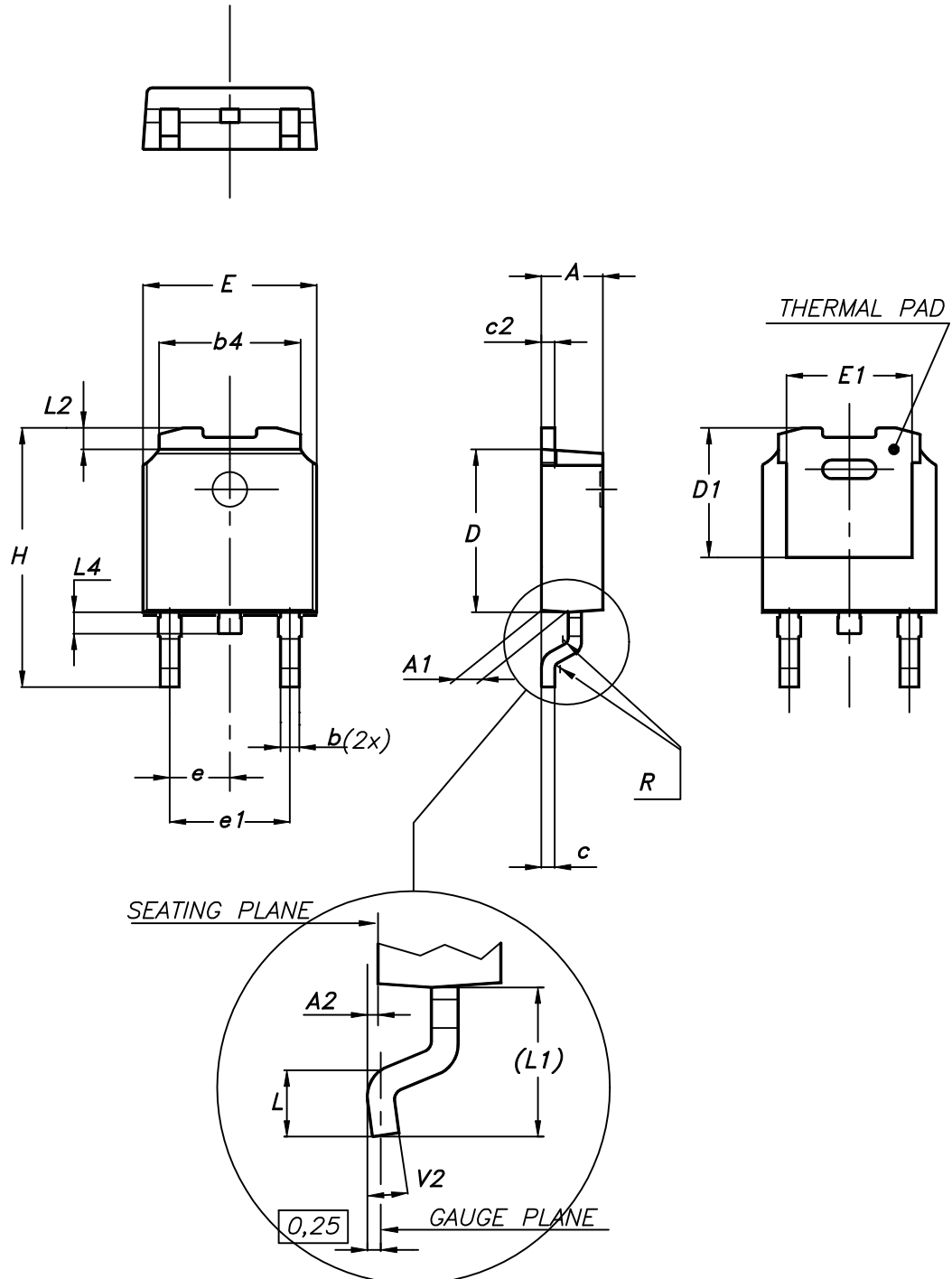
## **4 Package information**

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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 DPAK (TO-252) type A2 package information

Figure 22. DPAK (TO-252) type A2 package outline



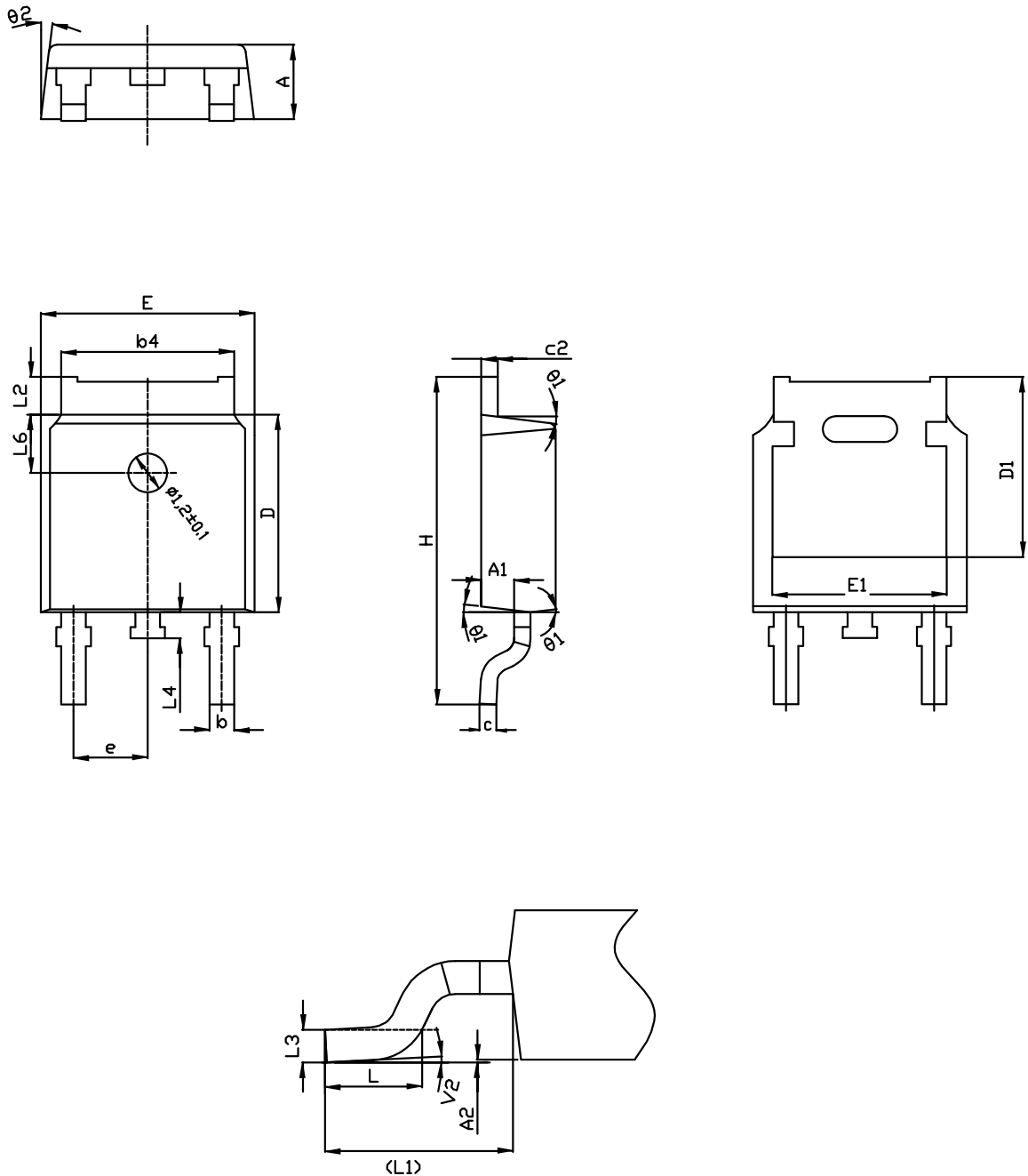
0068772\_type-A2\_rev24

**Table 8. DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

## 4.2 DPAK (TO-252) type C2 package information

Figure 23. DPAK (TO-252) type C2 package outline



0068772\_C2\_24

**Table 9. DPAK (TO-252) type C2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

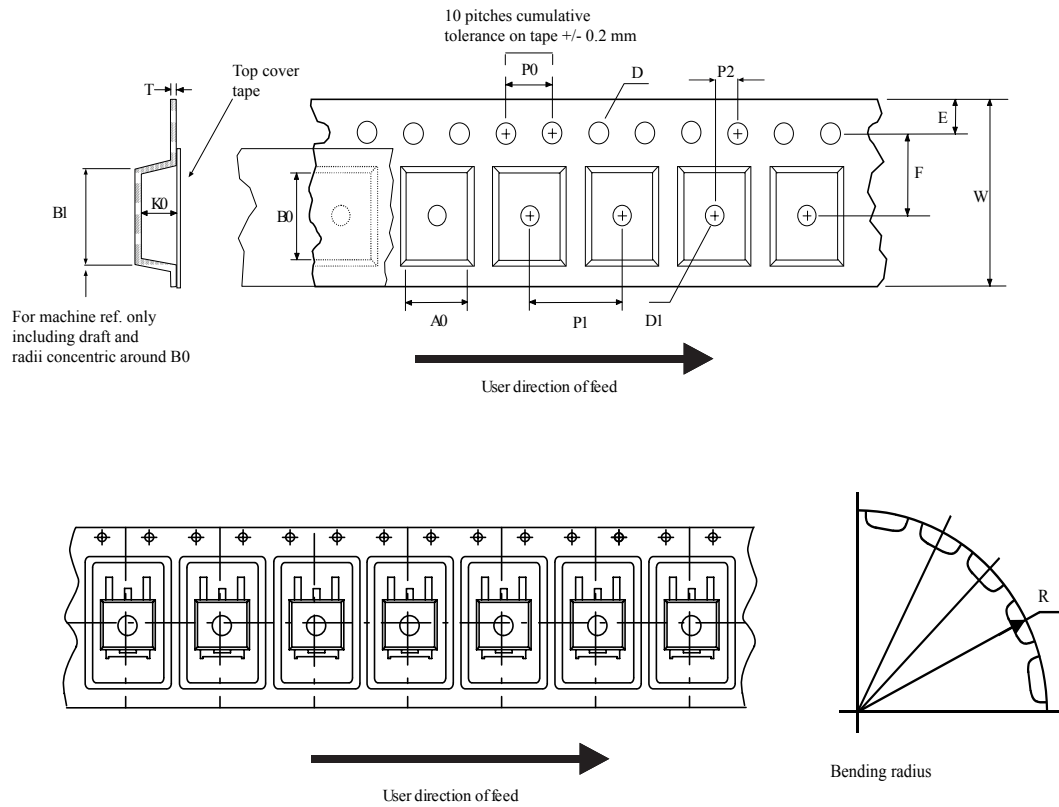
Figure 24. DPAK (TO-252) recommended footprint (dimensions are in mm)



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### 4.3 DPAK (TO-252) packing information

Figure 25. DPAK (TO-252) tape outline



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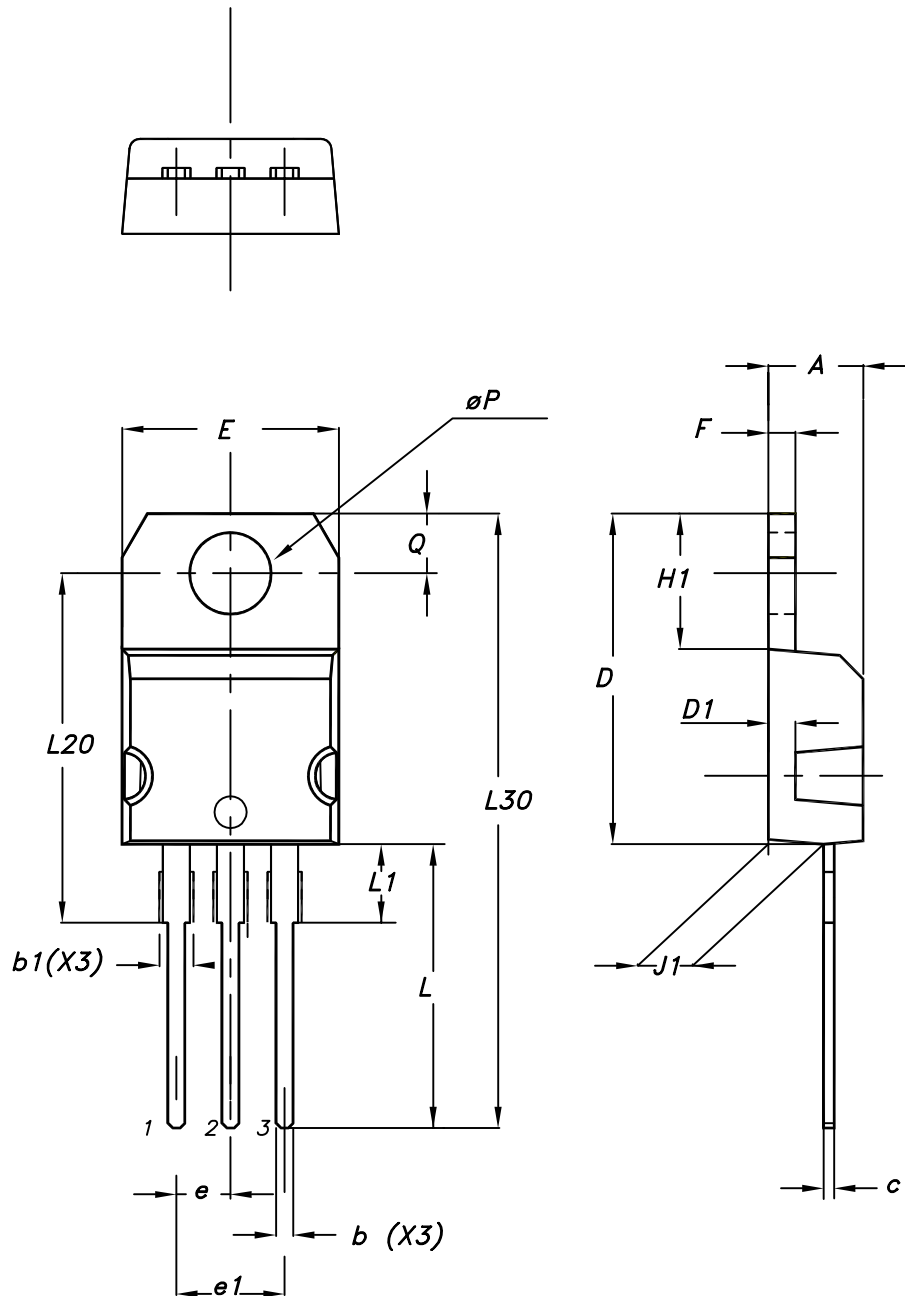
**Figure 26. DPAK (TO-252) reel outline**


AM06038v1

**Table 10. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			



**4.4 TO-220 type A package information**
**Figure 27. TO-220 type A package outline**


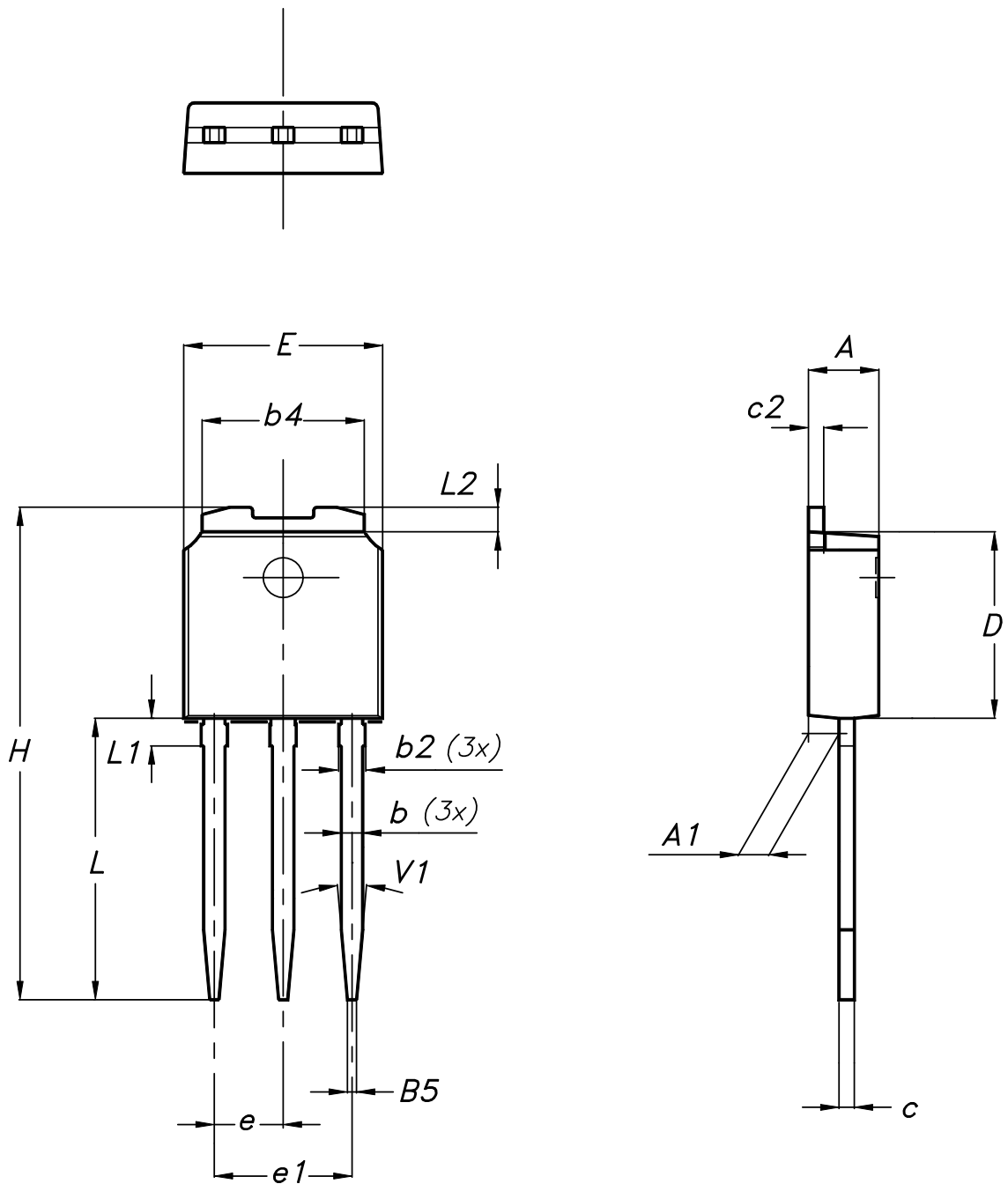
0015988\_typeA\_Rev\_21

**Table 11. TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

#### 4.5 IPAK (TO-251) type A package information

Figure 28. IPAK (TO-251) type A package outline



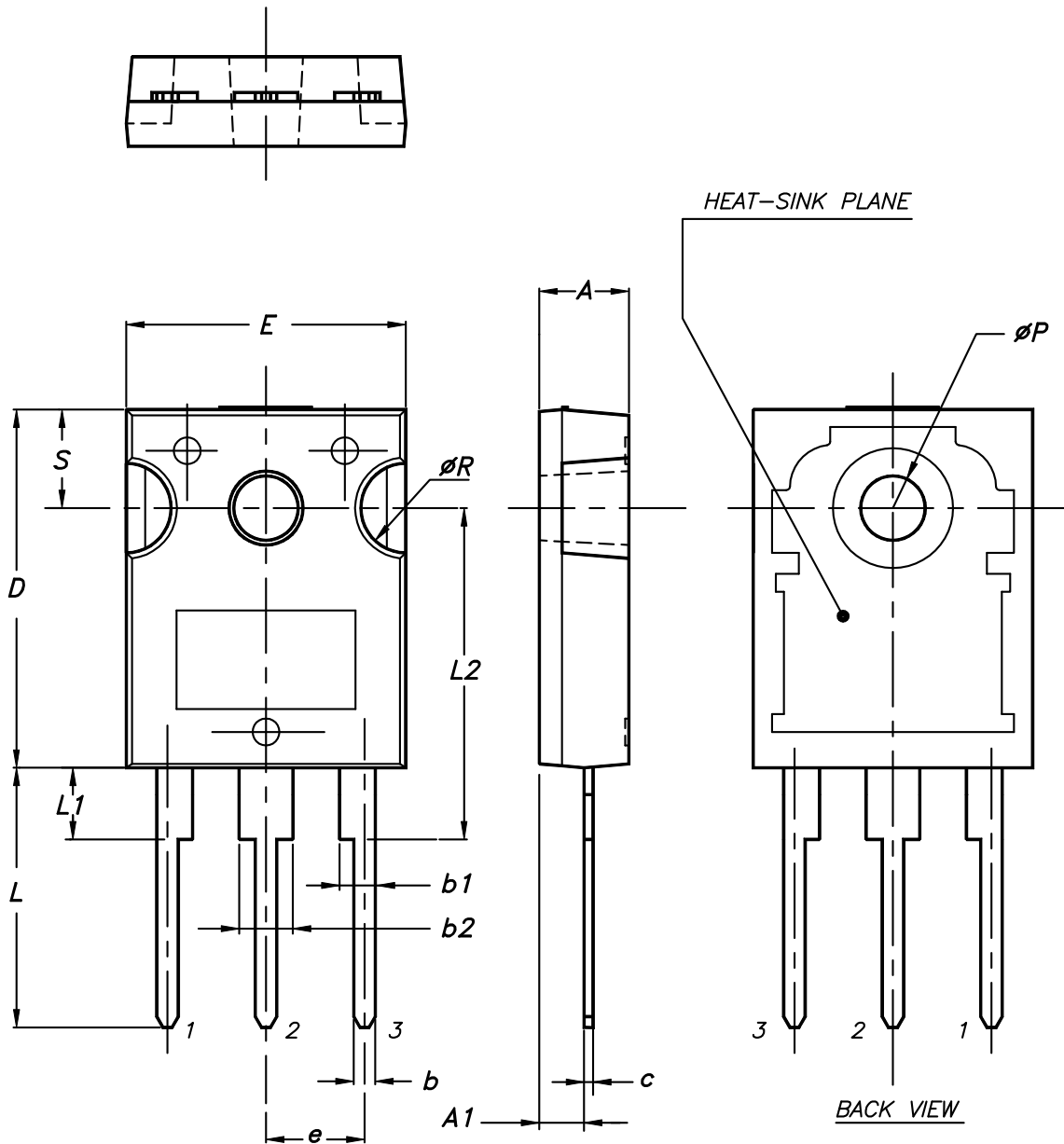
0068771\_IK\_typeA\_rev14

**Table 12. IPAK (TO-251) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.6 TO-247 package information

Figure 29. TO-247 package outline



0075325\_9

**Table 13. TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

## 5 Ordering information

Table 14. Ordering information

Order code	Marking	Package	Packing
STD6N95K5	6N95K5	DPAK	Tape and reel
STP6N95K5	6N95K5	TO-220	Tube
STU6N95K5	6N95K5	IPAK	Tube
STW6N95K5	6N95K5	TO-247	Tube

## Revision history

**Table 15. Document revision history**

Date	Revision	Changes
12-Jan-2010	1	First release.
01-Jul-2010	2	Document status promoted from preliminary data to datasheet.
31-Aug-2012	3	Inserted new device in IPAK. Updated <i>Table 1: Device summary</i> , <i>Table 2: Absolute maximum ratings</i> , and <i>Table 3: Thermal data</i> . Updated <i>Section 4: Package mechanical data</i> and <i>Section 5: Packaging mechanical data</i> . Minor text changes in the cover page.
16-May-2014	4	The part number STF6N95K5 has been moved to a separate datasheet. Added: MOSFET dv/dt ruggedness parameter in <i>Table 2</i> Updated: <i>Section 4: Package mechanical data</i> Minor text changes
22-Mar-2018	5	Removed maturity status indication and updated title and description from cover page. The document status is production data. Updated <a href="#">Section 1 Electrical ratings</a> , <a href="#">Section 2 Electrical characteristics</a> . Updated <a href="#">Figure 9. Capacitance variations</a> and <a href="#">Figure 12. Normalized on-resistance vs temperature</a> . Updated <a href="#">Section 4 Package information</a> . Minor text changes.



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