40V COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C (Notes 6 & 8)
Q1	40V	45mΩ @ V_{GS}= 10V	5.5A
		60mΩ @ V_{GS}= 4.5V	4.2A
Q2	-40V	45mΩ @ V_{GS}= -10V	-5.8A
		60mΩ @ V_{GS}= -4.5V	-4.2A

Features and Benefits

- Matched N & P $R_{DS(ON)}$ – Minimizes Power Losses
- Fast Switching – Minimizes Switching Losses
- Dual Device – Reduces PCB Area
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Description

This MOSFET is designed to ensure that $R_{DS(ON)}$ of N and P channel FET are matched to minimize losses in both arms of the bridge. The DMC4040SSD is optimized for use in 3-phase brushless DC motor circuits (BLDC), and CCFL backlighting.

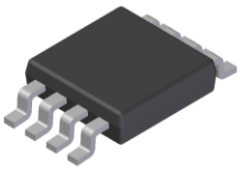
Applications

- 3-Phase BLDC Motor
- CCFL Backlighting

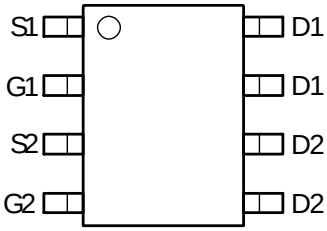
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (Approximate)

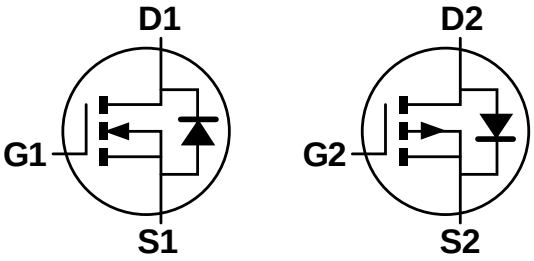
SO-8



Top View



Top View



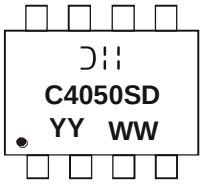
Equivalent Circuit

Ordering Information (Note 4)

Product	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DMC4050SSD-13	C4050SD	13	12	2,500

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



= Manufacturer's Marking
C4050SD = Product Type Marking Code
YYWW = Date Code Marking
YY or YY= Year (ex: 10 = 2010)
WW = Week (01 - 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

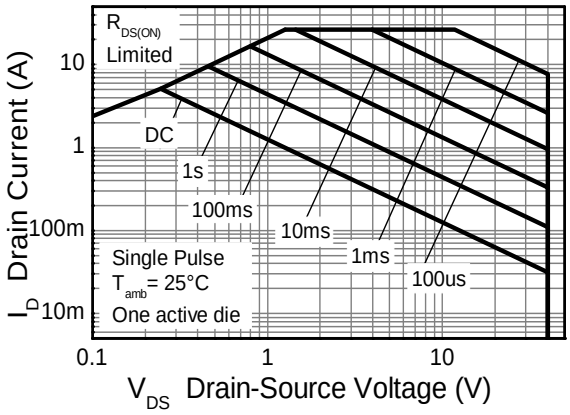
Characteristic			Symbol	N-Channel - Q1	P-Channel - Q2	Units
Drain-Source Voltage			V_{DSS}	40	-40	V
Gate-Source Voltage			V_{GSS}	±20	±20	
Continuous Drain Current	V_{GS} = 10V	(Notes 6 & 8)	I_D	5.8	-5.8	A
		T_A = +70°C (Notes 6 & 8)		4.38	-4.52	
		(Notes 5 & 8)		4.2	-4.2	
		(Notes 5 & 9)		5.3	-5.3	
Pulsed Drain Current	V_{GS} = 10V	(Notes 7 & 8)	I_{DM}	24.1	-24.9	
Continuous Source Current (Body Diode)		(Notes 6 & 8)	I_S	2.5	-2.5	
Pulsed Source Current (Body Diode)		(Notes 7 & 8)	I_{SM}	24.1	-24.9	

Thermal Characteristics

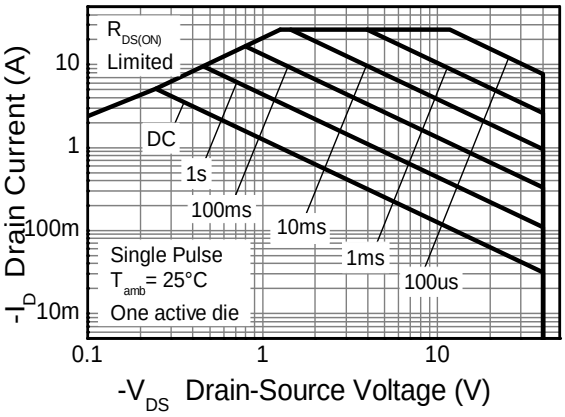
Characteristic		Symbol	N-Channel - Q1 / P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 5 & 8)	P_D	1.25 10	W mW/°C
	(Notes 5 & 9)		1.8 14.3	
	(Notes 6 & 8)		2.14 17.2	
Thermal Resistance, Junction to Ambient	(Notes 5 & 8)	$R_{\theta JA}$	100	°C/W
	(Notes 5 & 9)		70	
	(Notes 6 & 8)		58	
Thermal Resistance, Junction to Lead	(Notes 5 & 10)	$R_{\theta JL}$	51	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes:
5. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
6. Same as note (5), except the device is measured at t ≤ 10 sec.
7. Same as note (5), except the device is pulsed with D = 0.02 and pulse width 300µs.
8. For a dual device with one active die.
9. For a device with two active die running at equal power.
10. Thermal resistance from junction to solder-point (at the end of the drain lead).

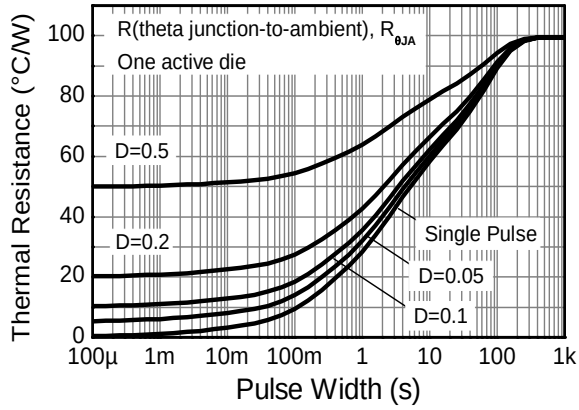
Thermal Characteristics (Continued)



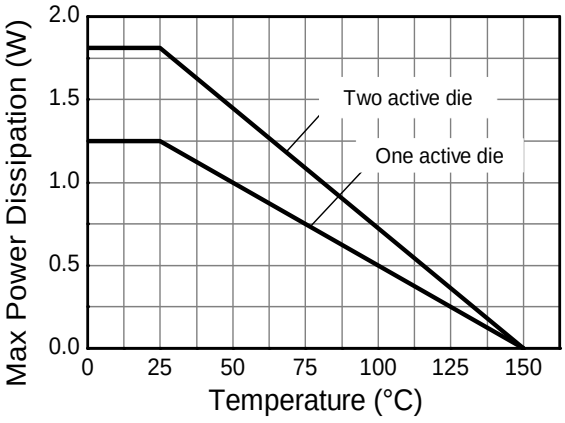
N-channel Safe Operating Area



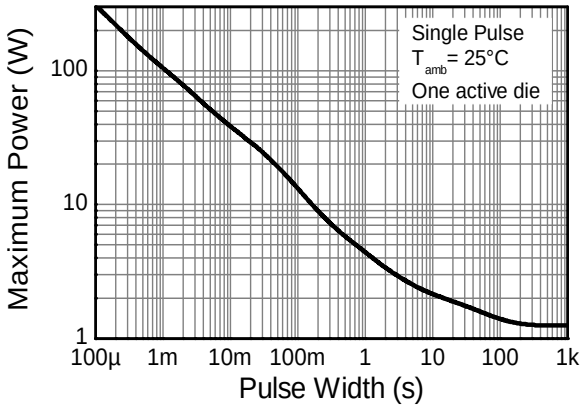
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

Electrical Characteristics (Q1 N-Channel) (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 11)						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	1.0	µA	V_{DS} = 40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 11)						
Gate Threshold Voltage	$V_{GS(th)}$	0.8	1.3	1.8	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	20 33	45 60	mΩ	V_{GS} = 10V, I_D = 3A V_{GS} = 4.5V, I_D = 3A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	12.6	—	S	V_{DS} = 5V, I_D = 3A
Diode Forward Voltage (Note 11)	V_{SD}	—	0.7	1.0	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C_{iss}	—	1790.8	—	pF	V_{DS} = 20V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	160.6	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	120.5	—	pF	
Gate Resistance	R_g	—	1.03	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	37.56	—	nC	V_{GS} = 10V, V_{DS} = 20V, I_D = 3A
Gate-Source Charge	Q_{gs}	—	7.8	—	nC	
Gate-Drain Charge	Q_{gd}	—	6.6	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	8.08	—	nS	V_{GS} = 10V, V_{DS} = 20V, I_D = 3A
Turn-On Rise Time	t_r	—	15.14	—	nS	
Turn-Off Delay Time	$t_{D(off)}$	—	24.29	—	nS	
Turn-Off Fall Time	t_f	—	5.27	—	nS	

Electrical Characteristics (Q2 P-Channel) (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 11)						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1.0	µA	V_{DS} = -40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 11)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.8	-1.3	-1.8	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	28 30	45 60	mΩ	V_{GS} = -10V, I_D = -3A V_{GS} = -4.5V, I_D = -3A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	16.6	—	S	V_{DS} = -5V, I_D = -3A
Diode Forward Voltage (Note 11)	V_{SD}	—	-0.7	-1.0	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C_{iss}	—	1643.17	—	pF	V_{DS} = -20V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	179.13	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	127.82	—	pF	
Gate Resistance	R_g	—	6.43	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	33.66	—	nC	V_{GS} = -10V, V_{DS} = -20V, I_D = -3A
Gate-Source Charge	Q_{gs}	—	5.54	—	nC	
Gate-Drain Charge	Q_{gd}	—	7.30	—	nC	
Turn-On Delay Time	$t_{D(on)}$	—	6.85	—	nS	V_{GS} = -10V, V_{DS} = -20V, I_D = -3A
Turn-On Rise Time	t_r	—	14.72	—	nS	
Turn-Off Delay Time	$t_{D(off)}$	—	53.65	—	nS	
Turn-Off Fall Time	t_f	—	30.86	—	nS	

Notes: 11. Short duration pulse test used to minimize self-heating effect.
12. Guaranteed by design. Not subject to production testing.

Typical Characteristics (Q1 N-Channel)

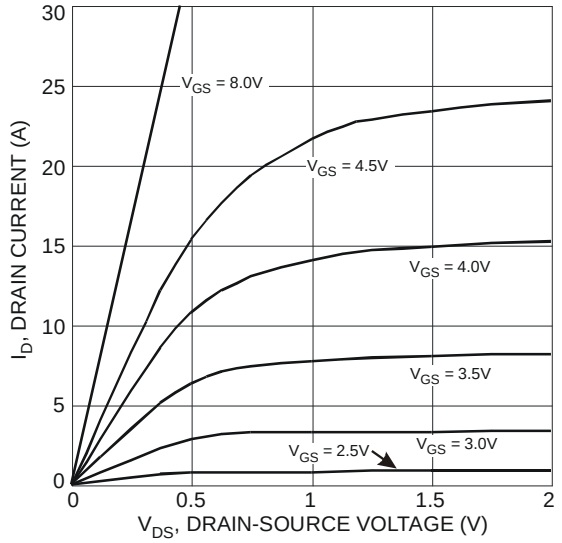


Fig. 1 Typical Output Characteristic

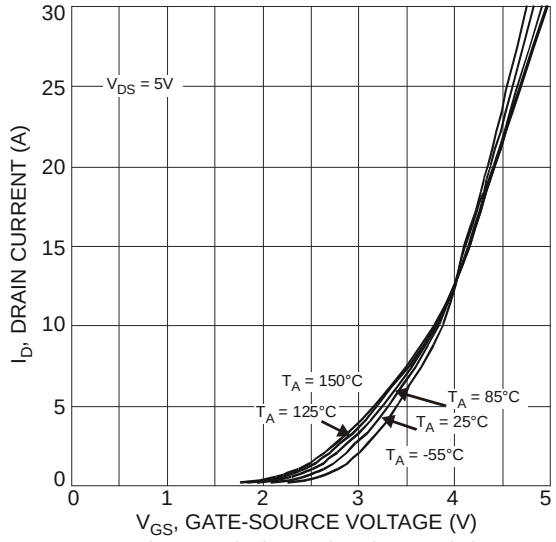


Fig. 2 Typical Transfer Characteristic

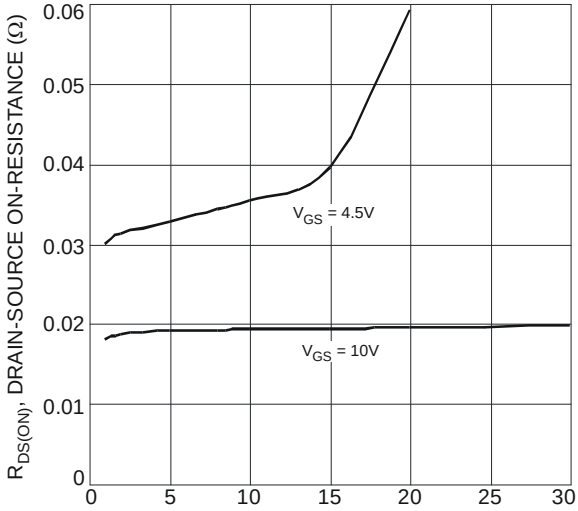


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

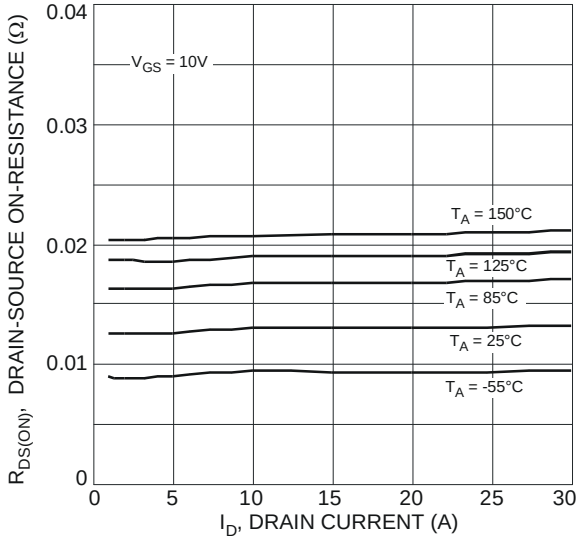


Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

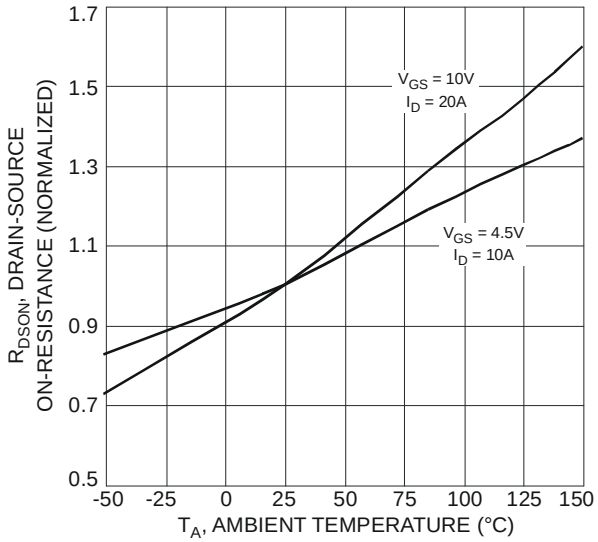


Fig. 5 On-Resistance Variation with Temperature

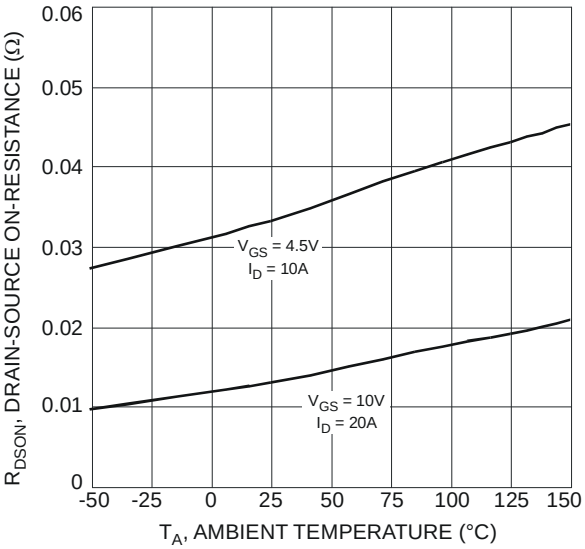


Fig. 6 On-Resistance Variation with Temperature

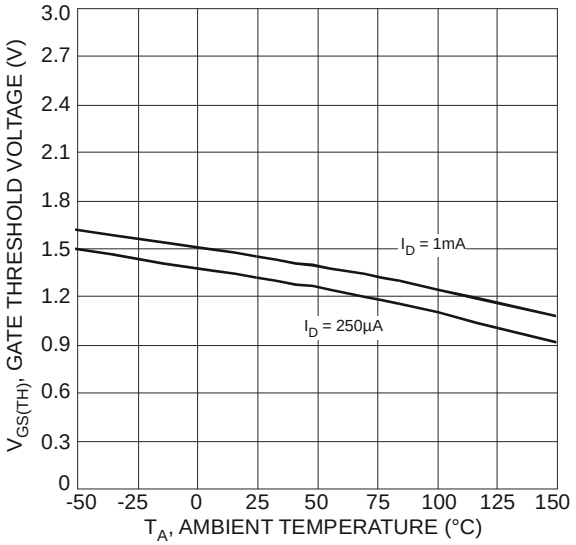


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

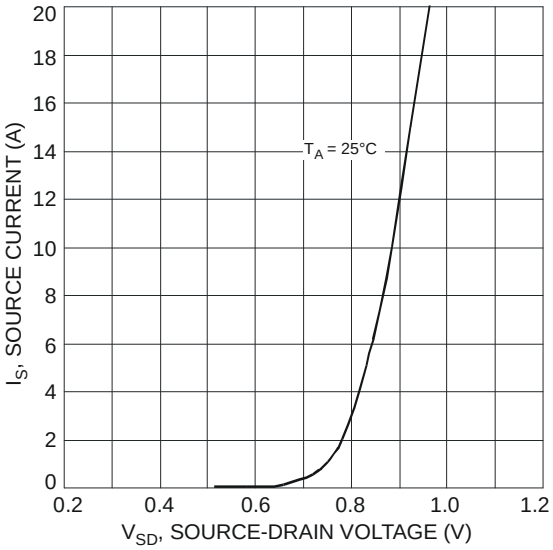


Fig. 8 Diode Forward Voltage vs. Current

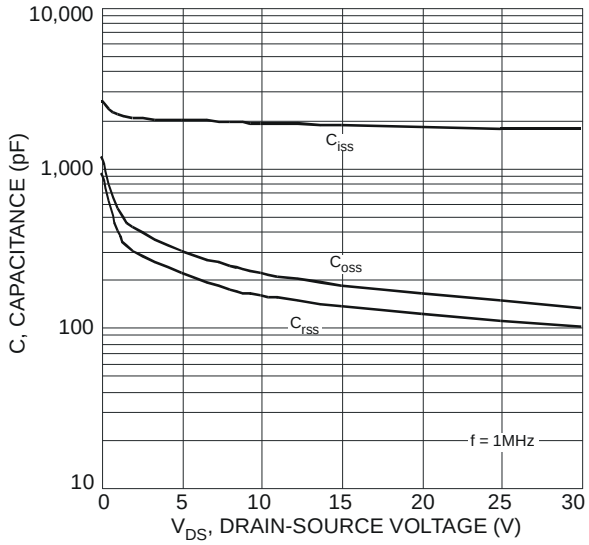


Fig. 9 Typical Total Capacitance

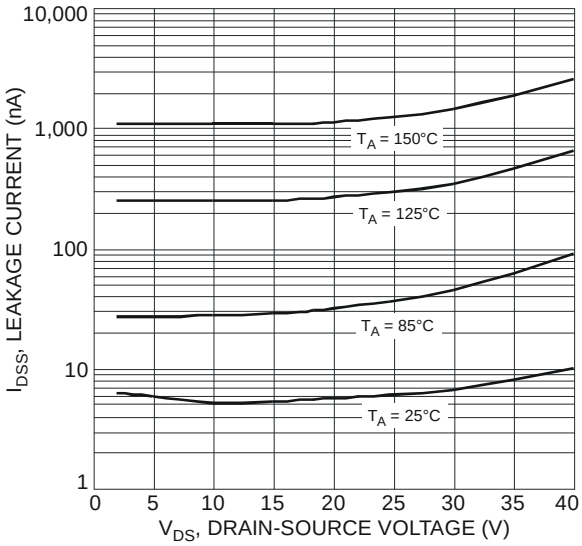


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

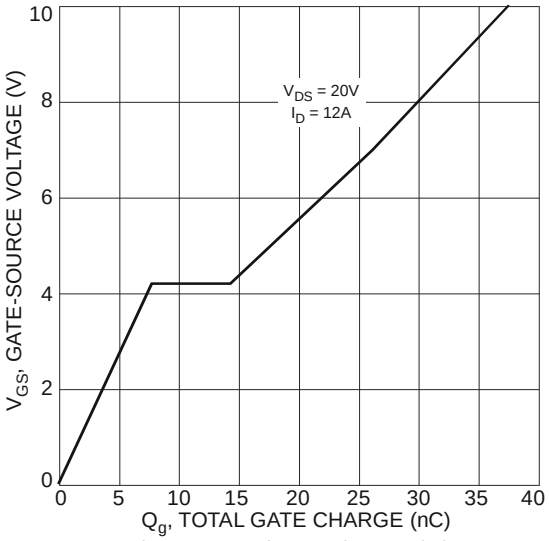


Fig. 11 Gate-Charge Characteristics

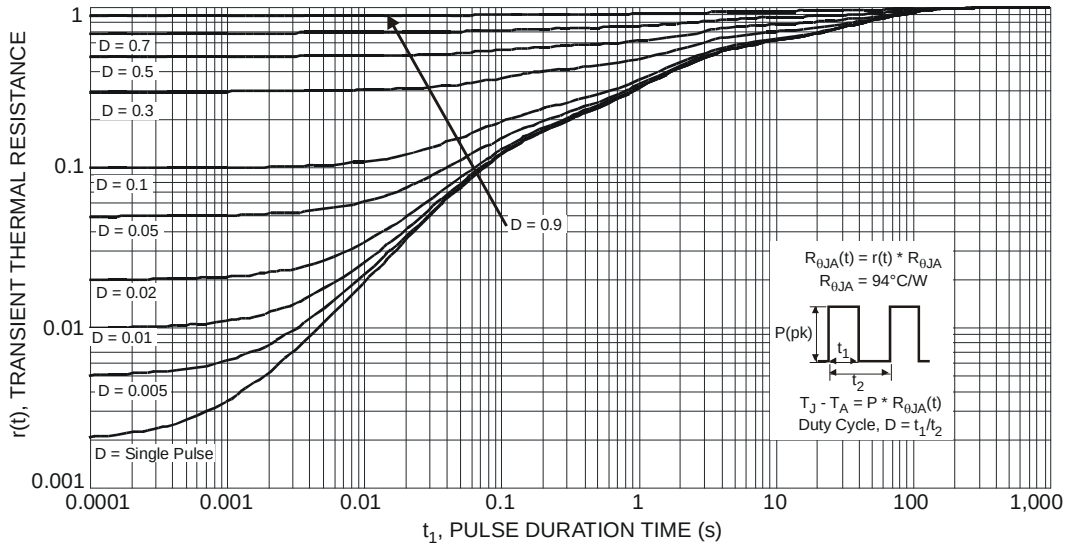


Fig. 12 Transient Thermal Response

Typical Characteristics (Q2 P-Channel)

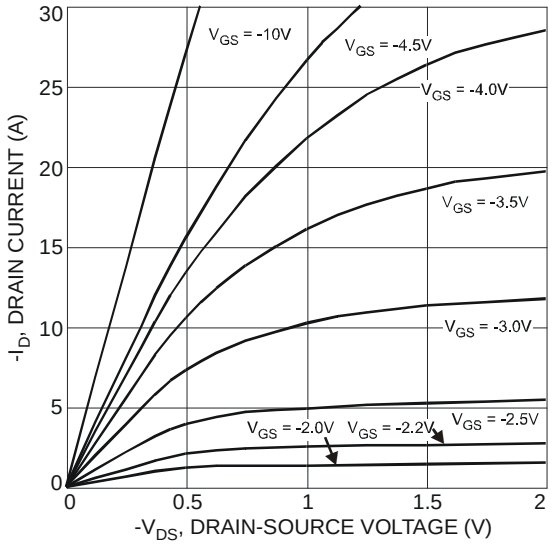


Fig. 13 Typical Output Characteristic

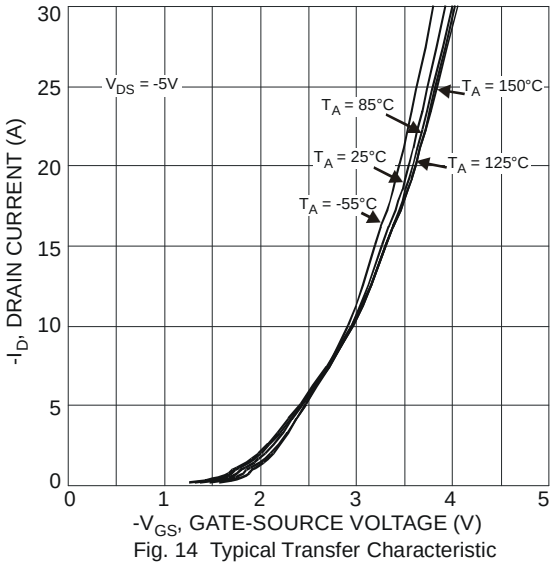


Fig. 14 Typical Transfer Characteristic

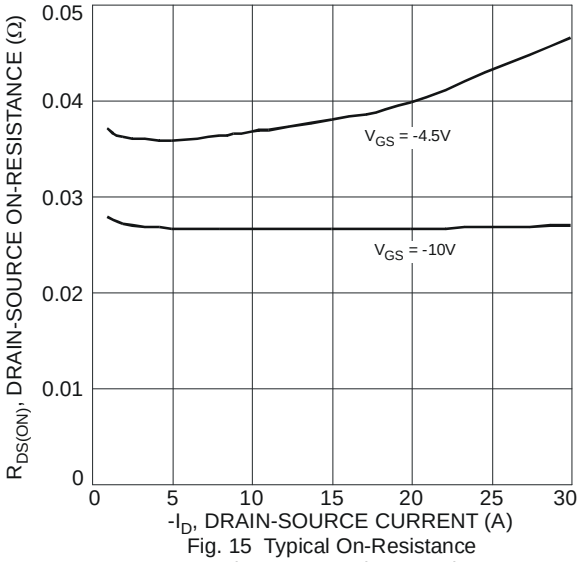


Fig. 15 Typical On-Resistance
vs. Drain Current and Gate Voltage

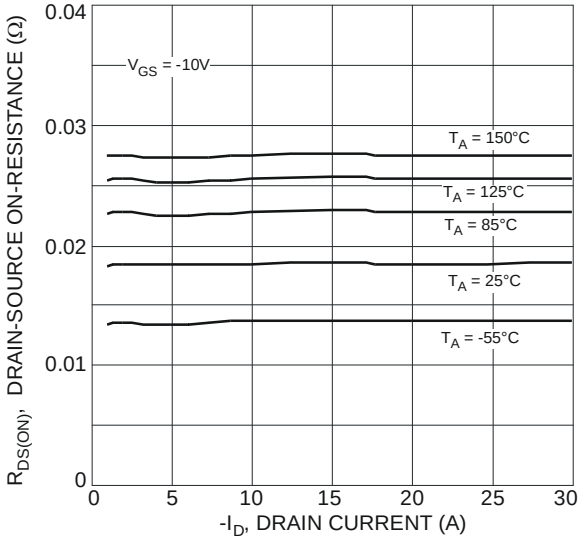


Fig. 16 Typical On-Resistance
vs. Drain Current and Temperature

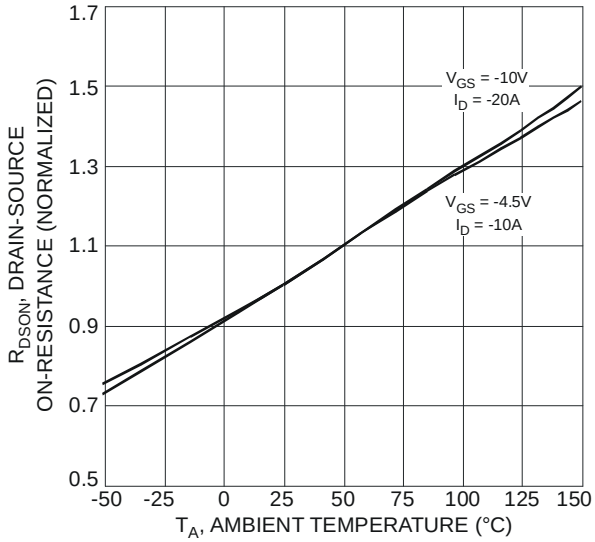


Fig. 17 On-Resistance Variation with Temperature

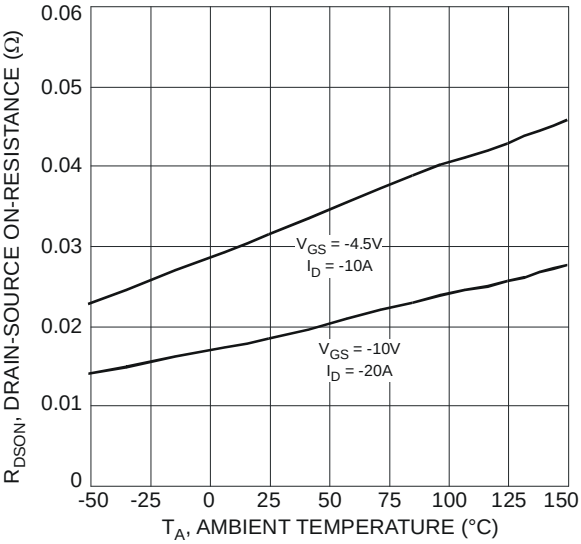


Fig. 18 On-Resistance Variation with Temperature

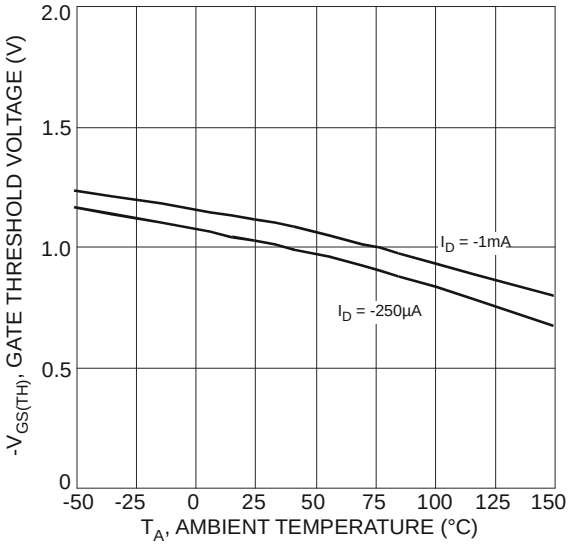


Fig. 19 Gate Threshold Variation vs. Ambient Temperature

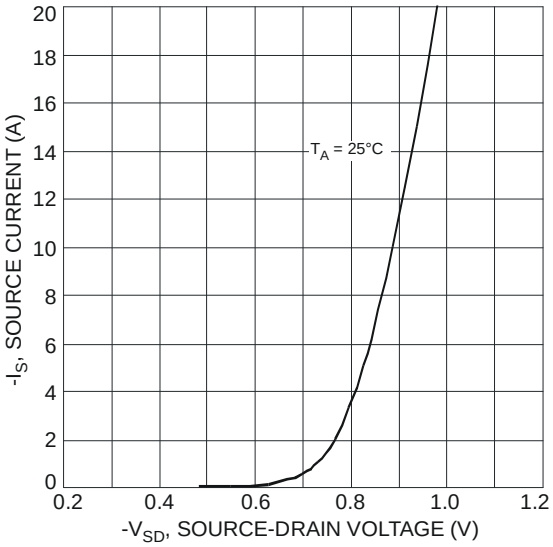


Fig. 20 Diode Forward Voltage vs. Current

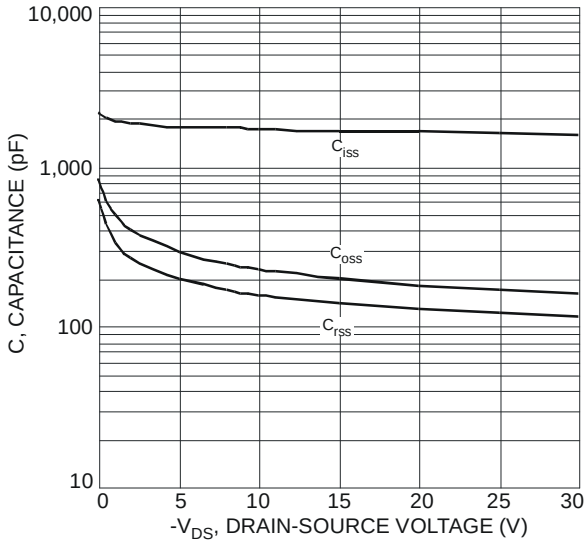


Fig. 21 Typical Total Capacitance

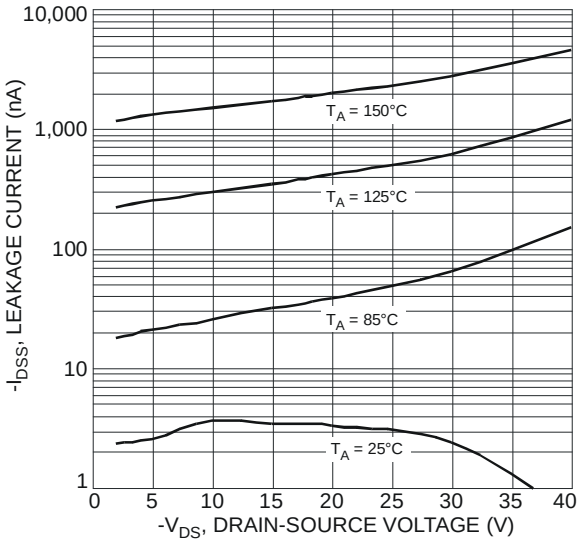


Fig. 22 Typical Leakage Current vs. Drain-Source Voltage

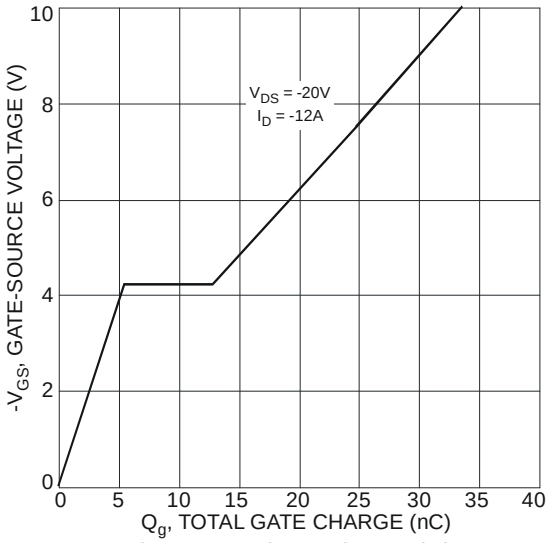


Fig. 23 Gate-Charge Characteristics

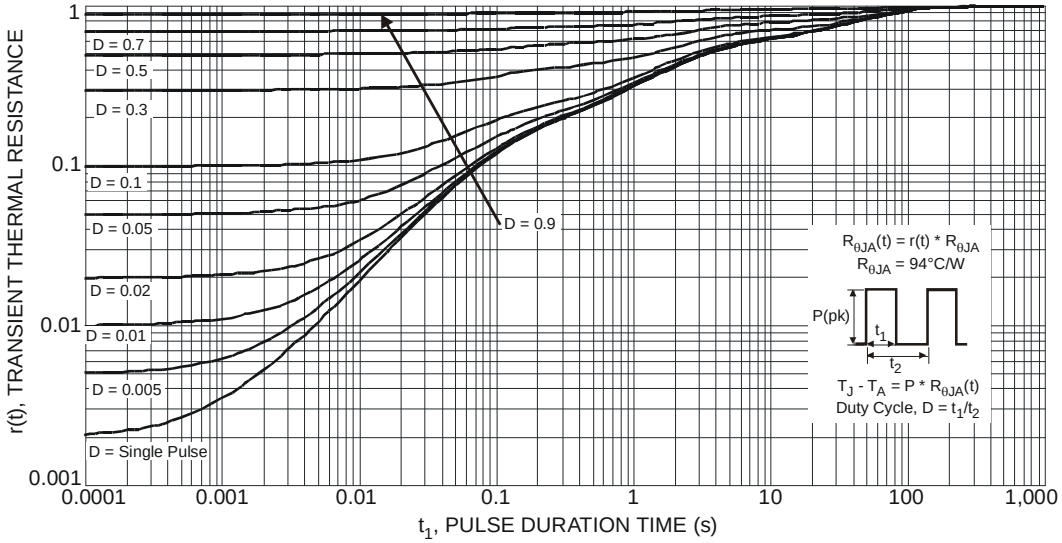
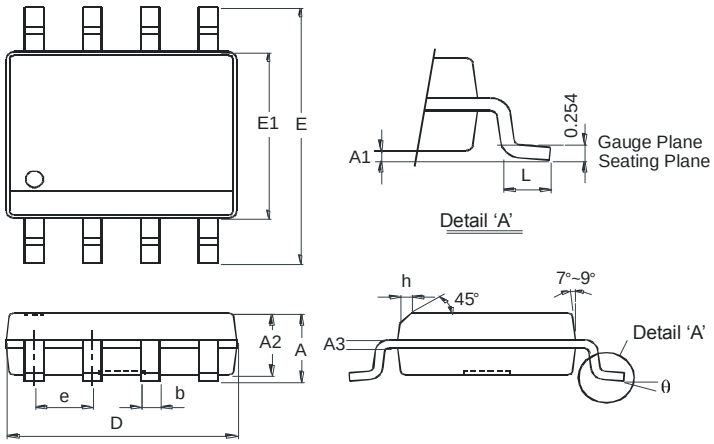


Fig. 24 Transient Thermal Response

Package Outline Dimensions

Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

SO-8

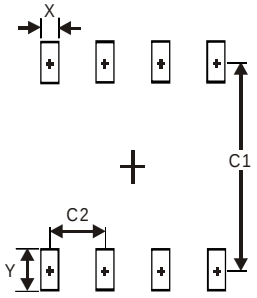


SO-8		
Dim	**Min**	**Max**
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

SO-8



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

IMPORTANT NOTICE

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