Two Channel SATA 3-Gbps Redriver

FEATURES

- **Data Rates up to 3.0 Gbps**
- **SATA Gen 2.6, eSATA Compliant**
- **SATA Hot-Plug Capable**
- **Supports Common-Mode Biasing for OOB Signaling with Fast Turn-On**
- **Channel Selectable Pre-Emphasis**
- **Fixed Receiver Equalization**
- **Integrated Termination**
- **Low Power**
  - **<200 mW Typ**
  - **<5 mW (in sleep mode)**
- **Excellent Jitter and Loss Compensation Capability to Over 20 Inch FR4 Trace**
- **20-Pin 4 × 4 QFN Package**

APPLICATIONS

- **Notebooks, Desktops, Docking Stations, Servers, Workstations**

DESCRIPTION

The SN75LVCP412 is a dual channel, single lane SATA redriver and signal conditioner supporting data rates up to 3.0 Gbps. The device complies with SATA specification revision 2.6 and eSATA requirements.

The SN75LVCP412 operates from a single 3.3-V supply and has 100-Ω line termination with self-biasing feature making the device suitable for AC coupling. The inputs incorporate an OOB detector, which automatically squelches the output while maintaining a stable output common-mode voltage compliant to SATA link. The device is also designed to handle SSC transmission per the SATA specification.

The SN75LVCP412 handles interconnect losses at both its input and output. The built-in transmitter pre-emphasis feature is capable of applying 0 dB or 2.5 dB of relative amplification at higher frequencies to counter the expected interconnect loss. On the receive side the device applies a fixed equalization of 7 dB to boost input frequencies near 1.5 GHz. Collectively, the input equalization and output pre-emphasis features of the device work to fully restore SATA signal integrity over extended cable and backplane pathways.

The device is hot-plug capable(1) preventing device damage under device *hot*-insertion such as async signal plug/removal, unpowered plug/removal, powered plug/removal, or surprise plug/removal.

(1) *Requires use of AC coupling capacitors at differential inputs and outputs.*

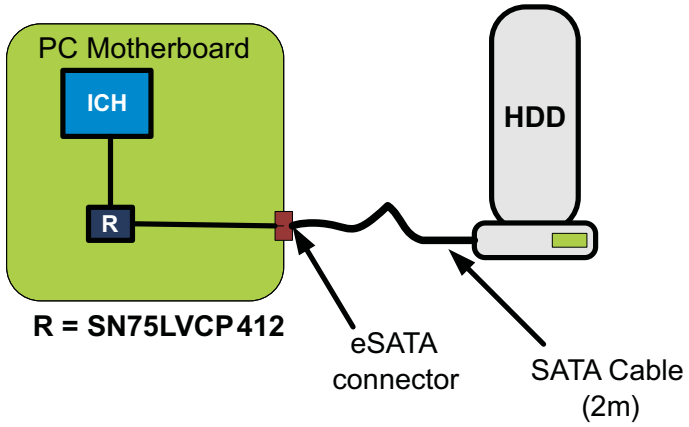
ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN75LVCP412RTJR	LVCP412	20-Pin RTJ Reel (large)

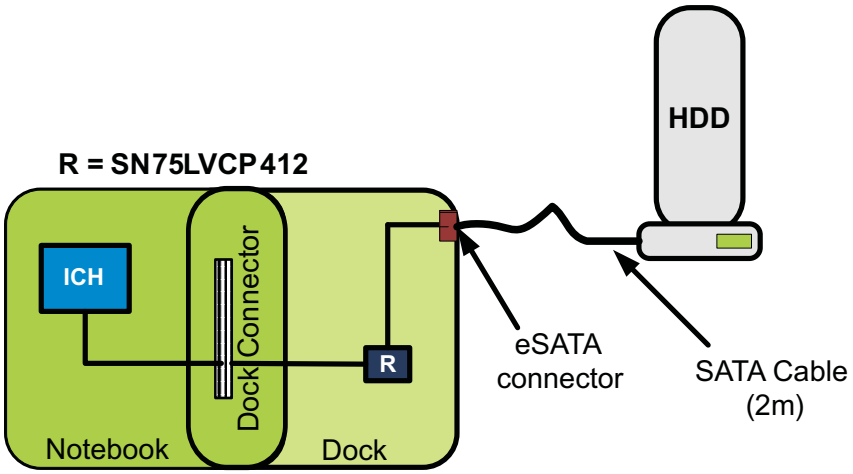
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION



In Notebook and Desktop Motherboard



In Notebook Dock

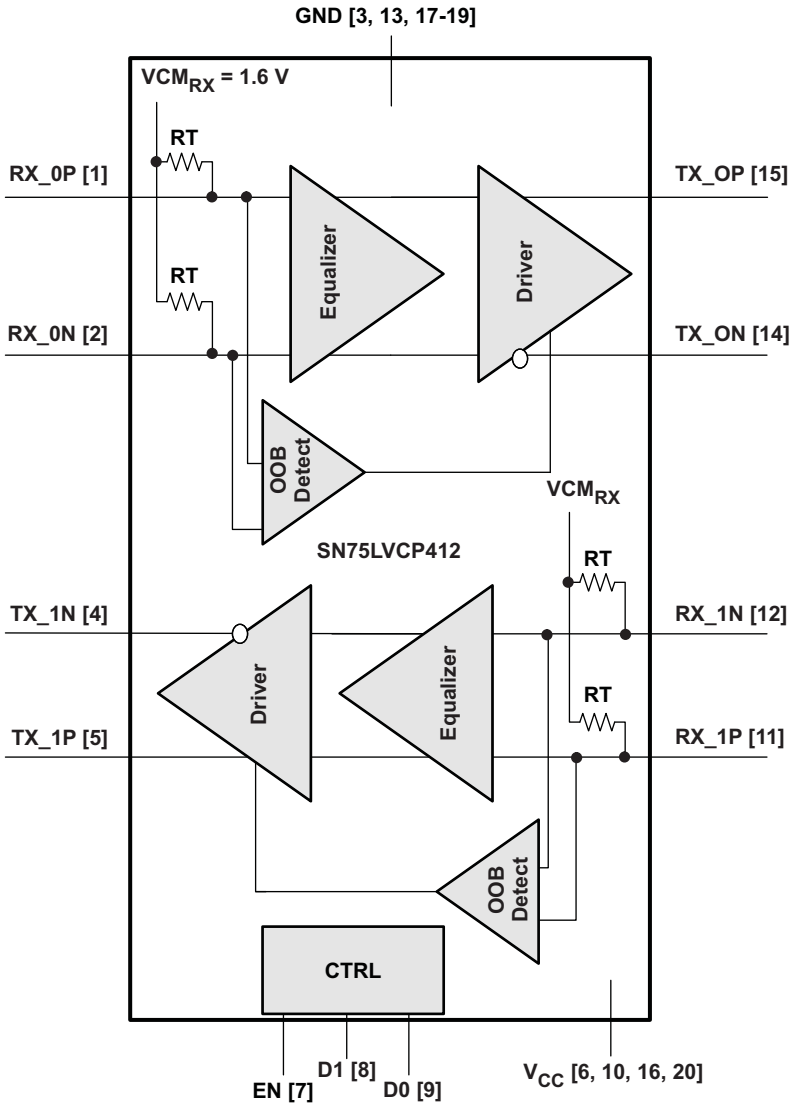


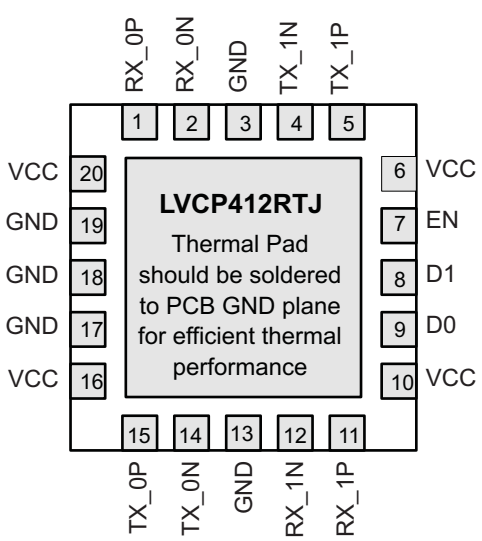
Figure 1. Data Flow Block Diagram

Table 1. Control Logic

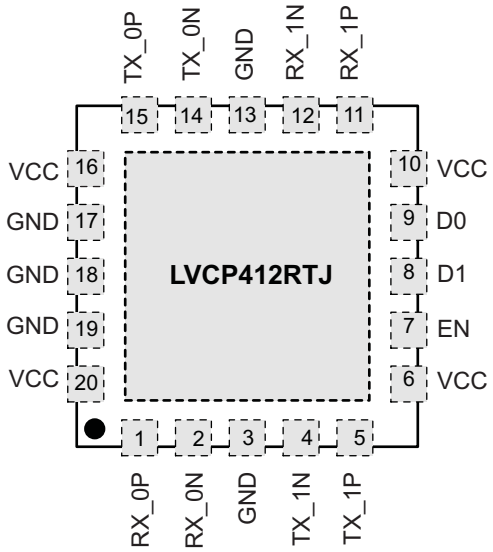
EN	D0	D1	FUNCTION
0	X	X	Low power mode
1	**0**	**0**	**Normal SATA output (default state); CH 0 and CH 1 → 0 dB**
1	1	0	CH 0 → 2.5 dB pre-emphasis; CH 1 → 0 dB
1	0	1	CH 1→ 2.5 dB pre-emphasis; CH 0 → 0 dB
1	1	1	CH 0 and CH 1 → 2.5 dB pre-emphasis

PIN ASSIGNMENT

BOTTOM VIEW



TOP VIEW

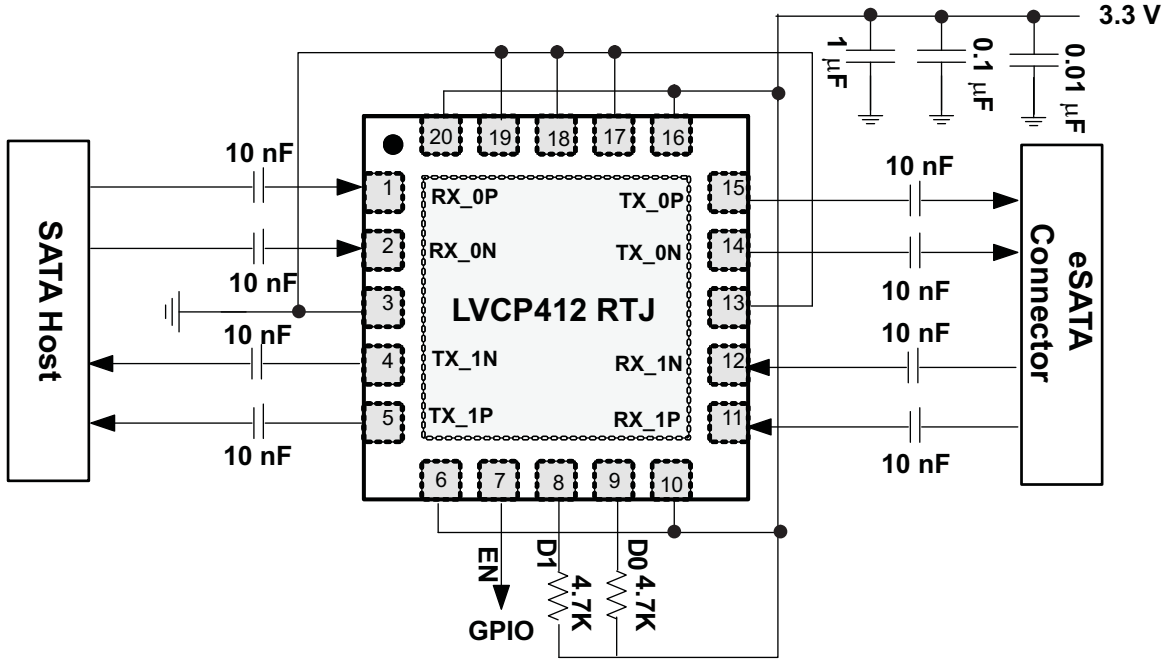


TERMINAL FUNCTIONS

PIN	NAME	DESCRIPTION		PIN	NAME	DESCRIPTION
1	RX_0P	Input 0, non-inverting		11	RX_1P	Input 1, non-inverting
2	RX_0N	Input 0, inverting		12	RX_1N	Input 1, inverting
3	GND	Ground		13	GND	Ground
4	TX_1N	Output 1, inverting		14	TX_0N	Output 0, inverting
5	TX_1P	Output 1, non-inverting		15	TX_0P	Output 0, non-inverting
6	VCC	Power		16	VCC	Power
7	EN(1)	Enable		17	GND	Ground
8	D1(2)	Pre-emphasis_1		18	GND	Ground
9	D0(2)	Pre-emphasis _0		19	GND	Ground
10	VCC	Power		20	VCC	Power

(1) EN tied to VCC via internal PU resistor
(2) D0 and D1 are tied to GND via internal PD resistor

TYPICAL DEVICE IMPLEMENTATION



Note:

1) Place supply caps close to device pin
2) EN can be left open or tied to supply when no external control is implemented
3) Output pre-emphasis (D1, D0) is shown enabled. Setting will depend on device placement relative to eSATA connector

DETAILED DESCRIPTION

INPUT EQUALIZATION

Each differential input of the SN75LVCP412 has 7 dB of fixed equalization in its front stage. The equalization amplifies high frequency signals to correct for loss from the transmission channel. The input equalizer is designed to recover a signal even when no eye is present at the receiver and effectively supports FR4 trace at the input anywhere from <4 inches to 20 inches or <10 cm to >50 cm.

OUTPUT PRE-EMPHASIS

The SN75LVCP412 provides single step pre-emphasis from 0 dB to 2.5 dB at each of its differential outputs. Pre-emphasis is controlled independently for each channel and is set by the control pins D0 and D1 as shown in Table 1. The pre-emphasis duration is 0.4 UI or 133 ps (typ) at SATA 3-Gbps speed.

LOW POWER MODE

Two low power modes are supported by the SN75LVCP412:

- Sleep Mode (triggered by EN pin, EN = 0V)
  - Low power mode is controlled by enable (EN) pin. In its default state this pin is internally pulled high. Pulling this pin LOW will put the device in sleep mode within 2µs (max). In this mode all active components of the device are driven to their quiescent level and differential outputs are driven to Hi-Z (open). Max power dissipation in this mode is 5 mW. Exiting from this mode to normal operation requires a maximum latency of 20 µs.
- Auto Low Power Mode (triggered when a given channel is in electrical idle state; EN = V_{CC})
  - The device enters and exits low power mode by actively monitoring input signal (V_{IDp-p}) level on each of its channel independently. When input signal on either or both channel is in the electrical idle state, i.e. V_{IDp-p} <50 mV and stays in this state for ≥3 µS the associated channel(s) enters into the low power state. In this

state, output of the associated channel(s) is driven to VCM and device selectively shuts off some circuitry to lower power by up to 20% of its normal operating power. Exit time from auto low power mode is less than 50 ns.

– As an example, if under normal operating conditions device is consuming typical power of 200 mW. When device enters this mode, i.e. condition for auto-low power mode is met, power consumption can drop down to 160 mW. The device enters normal operation within 50 ns of signal activity detection.

OUT-OF-BAND (OOB) SUPPORT

The squelch detector circuit within the device enables full detection of OOB signaling as specified in SATA specification 2.6. Differential signal amplitude at the receiver input of 50 mV_{p-p} or less is not detected as an activity and hence is not passed to the output. Differential signal amplitude of 150 mV_{p-p} or more is detected as an activity and therefore passed to the output indicating activity. Squelch circuit on/off time is 5 ns max. While in squelch mode outputs are held to VCM.

DEVICE POWER

The SN75LVCL412 is designed to operate from a single 3.3-V supply. Always practice proper power supply sequencing procedures. Apply V_{CC} first before any input signals are applied to the device. The power down sequence is in reverse order.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range(2)	V_{CC}	–0.5 to 6	V
Voltage range	Differential I/O	–0.5 to 4	V
	Control I/O	–0.5 to V_{CC} + 0.5	V
Electrostatic discharge	Human body model(3)	±8000	V
	Charged-device model(4)	±1000	V
	Machine model(5)	±200	V
Continuous power dissipation		See Dissipation Rating Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101-A.
(5) Tested in accordance with JEDEC Standard 22, Test Method A115-A.

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \le 25°C$	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
20-pin QFN (RTJ)	Low-K	1176 mW	11.76 mW/°C	470 mW
	High-K	2631 mW	26.3 mW/°C	1052 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance			10		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			60		°C/W
$R_{\theta JP}$	Junction-to-pad thermal resistance			15.2		°C/W

(1) The maximum rating is simulated under 3.6-V V_{CC}.

THERMAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
P_D	Device power dissipation, active mode	EN = 3.3 V, K28.5 pattern at 3 Gbps, V_{ID} = 700 mV_{p-p}, V_{CC} = 3.6 V			300	mW
P_{SD}	Device power dissipation, sleep mode	EN = 0 V, K28.5 pattern at 3 Gbps, V_{ID} = 700 mV_{p-p}, V_{CC} = 3.6 V			5	mW

RECOMMENDED OPERATING CONDITIONS

with typical values measured at V_{CC} = 3.3 V, T_A = 25°C; all temperature limits are assured by design

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage		3	3.3	3.6	V
$C_{COUPLING}$	Coupling capacitor			12		nF
T_A	Operating free-air temperature		0		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I_{CC}	Supply current, active mode	EN = 3.3 V, K28.5 pattern at 3 Gbps, V_{ID} = 700 mV_{p-p}, V_{CC} = 3.3 V		55	70	mA
$I_{CCSLEEP}$	Shutdown current, sleep mode	EN = 0V			1	mA
	Maximum data rate				3.0	Gbps
t_{PDelay}	Propagation delay	Measured using K28.5 pattern, See Figure 2		320	400	ps
t_{ENB}	Device enable time	ENB = L → H			20	µs
t_{DIS}	Device disable time	ENB = H → L			2	µs
V_{OOB}	Input OOB threshold	See Figure 3	50		150	mV_{p-p}
t_{OOB1}	OOB mode enter	See Figure 3		3	5	ns
t_{OOB2}	OOB mode exit	See Figure 3		3	5	ns
CONTROL LOGIC						
V_{IH}	High-level input voltage		1.4			V
V_{IL}	Low-level input voltage				0.5	V
V_{INHYS}	Input hysteresis			115		mV
I_{IH}	High-level input current				10	µA
I_{IL}	Low-level input current				10	µA
RECEIVER AC/DC						
Z_{DiffRX}	Differential input impedance		85	100	115	Ω
Z_{SERX}	Single-ended input impedance		40			Ω
VCM_{RX}	Common-mode voltage			1.6		V
RL_{DiffRX}	Differential mode return loss	f = 150 MHz–300 MHz	18			dB
		f = 300 MHz–600 MHz	14			
		f = 600 MHz–1.2 GHz	10			
		f = 1.2 GHz–2.4 GHz	8			
		f = 2.4 GHz–3.0 GHz	3			
RL_{CMRX}	Common-mode return loss	f = 150 MHz–300 MHz	5			dB
		f = 300 MHz–600 MHz	5			
		f = 600 MHz–1.2 GHz	2			
		f = 1.2 GHz–2.4 GHz	1			
		f = 2.4 GHz–3.0 GHz	1			

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{DiffRX}	Differential input voltage PP	f = 150 MHz–300 MHz	200		2000	mV/ppd
IB_{RX}	Impedance balance	f = 150 MHz–300 MHz	30			dB
		f = 300 MHz–600 MHz	30			
		f = 600 MHz–1.2 GHz	20			
		f = 1.2 GHz–2.4 GHz	10			
		f = 2.4 GHz–3.0 GHz	4			
$T_{20\text{-}80RX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal	67		136	ps
T_{skewRX}	Differential skew	Difference between the single-ended mid-point of the RX+ signal rising/falling edge, and the single-ended mid-point of the RX– signal falling/rising edge			50	ps
TRANSMITTER AC/DC						
Z_{DiffTX}	Pair differential Impedance		85		115	Ω
Z_{SETX}	Single-ended input impedance		40			Ω
	Output pre-emphasis	At 1.5 GHz when enabled		2.5		dB
RL_{DiffTX}	Differential mode return loss	f = 150 MHz–300 MHz	14			dB
		f = 300 MHz–600 MHz	8			
		f = 600 MHz–1.2 GHz	6			
		f = 1.2 GHz–2.4 GHz	6			
		f = 2.4 GHz–3.0 GHz	3			
RL_{CMTX}	Common-mode return loss	f = 150 MHz–300 MHz	5			dB
		f = 300 MHz–600 MHz	5			
		f = 600 MHz–1.2 GHz	2			
		f = 1.2 GHz–2.4 GHz	1			
		f = 2.4 GHz–3.0 GHz	1			
IB_{TX}	Impedance balance	f = 150 MHz–300 MHz	30			dB
		f = 300 MHz–600 MHz	20			
		f = 600 MHz–1.2 GHz	10			
		f = 1.2 GHz–2.4 GHz	10			
		f = 2.4 GHz–3.0 GHz	4			
$Diff_{VppTX}$	Differential output voltage PP	f = 1.5 GHz, D0/D1 = 0	400	525	600	mV/ppd
$Diff_{VppTX\_PE}$	Differential output voltage PP	f = 1.5 GHz, D0/D1 = 1	600	700	800	mV/ppd
t_{DE}	Pre-emphasis width	See Figure 4		0.4		UI
V_{CMTX}	Common-mode voltage			1.97		V
$T_{20\text{-}80TX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal, D1, D0 = 0 V	67	100	136	ps
T_{skewTX}	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising/falling edge, and the single-ended mid-point of the TX– signal falling/rising edge, D1, D0 = V_{CC}			20	ps
TJ_{TX}	Total jitter(1)	UI = 333 ps, +K28.5 control character		0.2	0.3	$Ui_{p\text{-}p}$
DJ_{TX}	Deterministic jitter(1)	UI = 333 ps, +K28.5 control character		0.13	0.2	$Ui_{p\text{-}p}$
RJ_{TX}	Random jitter(1)	UI = 333 ps, +K28.7 control character		2.0	2.15	ps/rms

(1) $T_J = (14.1 \times RJ_{SD} + DJ)$ where RJ_{SD} is one standard deviation value of RJ Gaussian distribution. T_J measurement is at the SATA connector and includes jitter generated at the package connection on the printed circuit board, and at the board interconnect as shown in Figure 2.

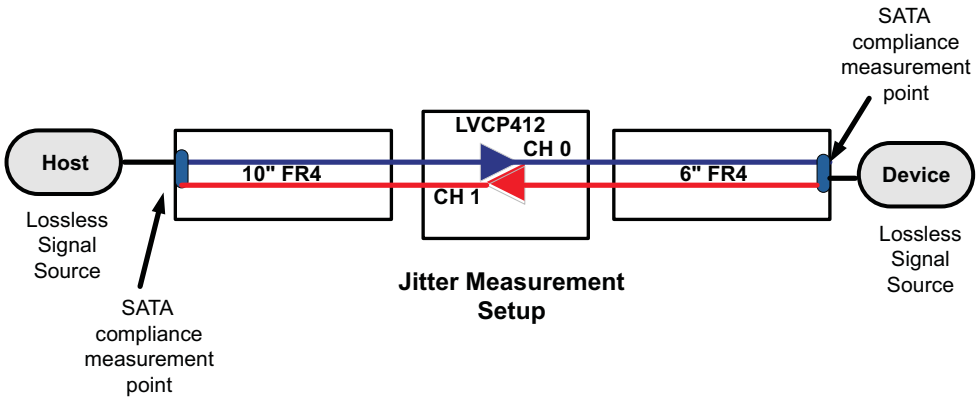


Figure 2. Jitter Measurement Test Condition

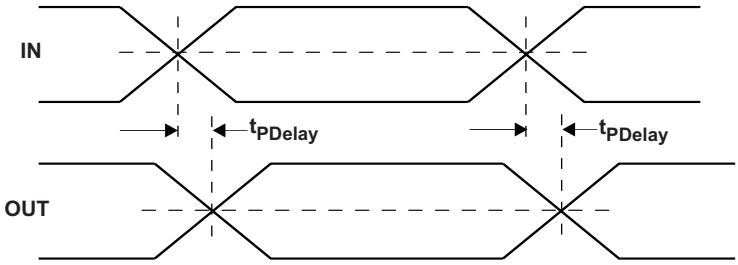


Figure 3. Propagation Delay Timing Diagram

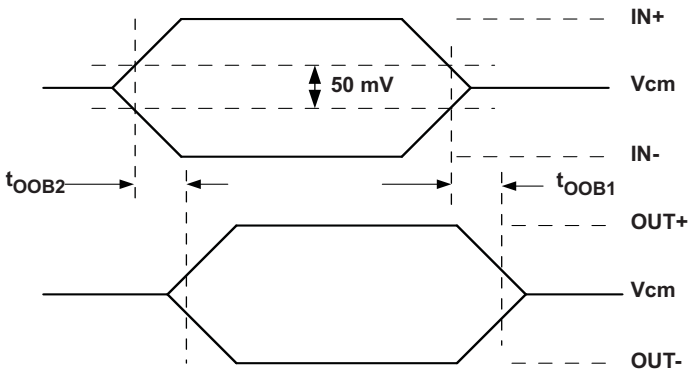


Figure 4. OOB Enter and Exit Timing

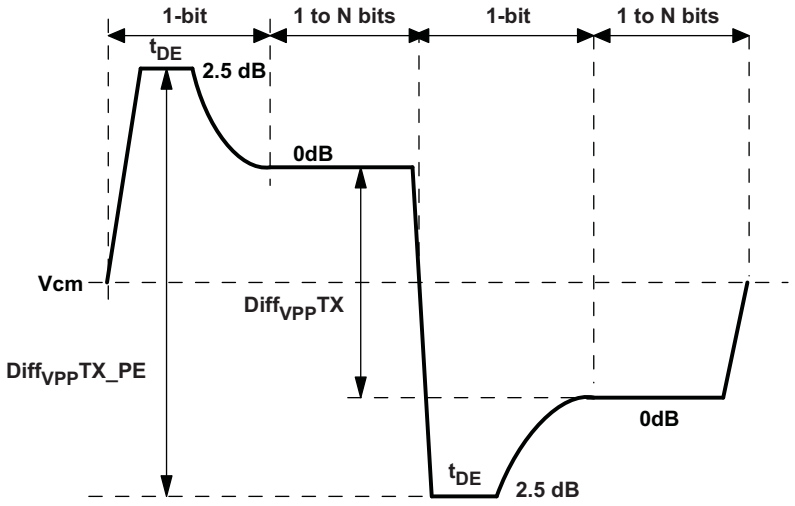


Figure 5. TX Differential Output with 2.5 dB Pre-Emphasis Step

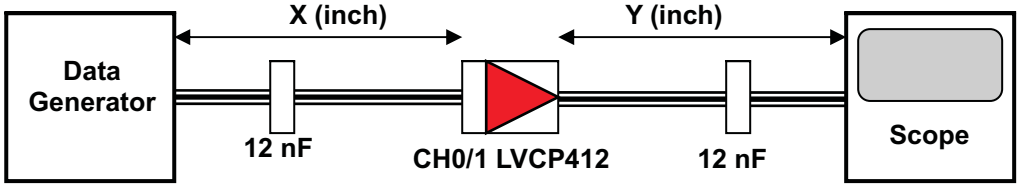
BENCH TEST DATA

Differential Output Voltage – $Diff_{VppTX}$, 2 inches from Device Pin, V_{CC} = 3.3 V, T_A = 25°C, Pattern = K28.5, Bit Rate = 3 Gbps

PARAMETER	TEST CONDITIONS	CHANNEL	INPUT VID	DO/D1	MIN	MEAN	MAXIMUM
$Diff_{VppTX}$	V_{CC} = 3.3 V, T_A = 25°C, Pattern = K28.5, Bit rate = 3 Gbps	CH0	700 mV	0	524.87mV	524.87mV	525.72mV
		CH1	700 mV	0	515.68mV	516.72mV	518.85mV
$Diff_{VppTXDE}$		CH0	700 mV	1	665.07mV	666.48mV	668.07mV
		CH1	700 mV	1	656.32mV	658.34mV	660.40mV

EYE DIAGRAM

Eye Pattern Measurement Setup



Test Condition

- **Vcc = 3.3 V**
- **Temp = 25°C**
- **Rx input voltage = 700 mVp-p**
- **Input pattern K28.5± @3 Gbps**
- **D1/D0/ENB = Vcc**
- **Trace Width = 4 mil on PCB**

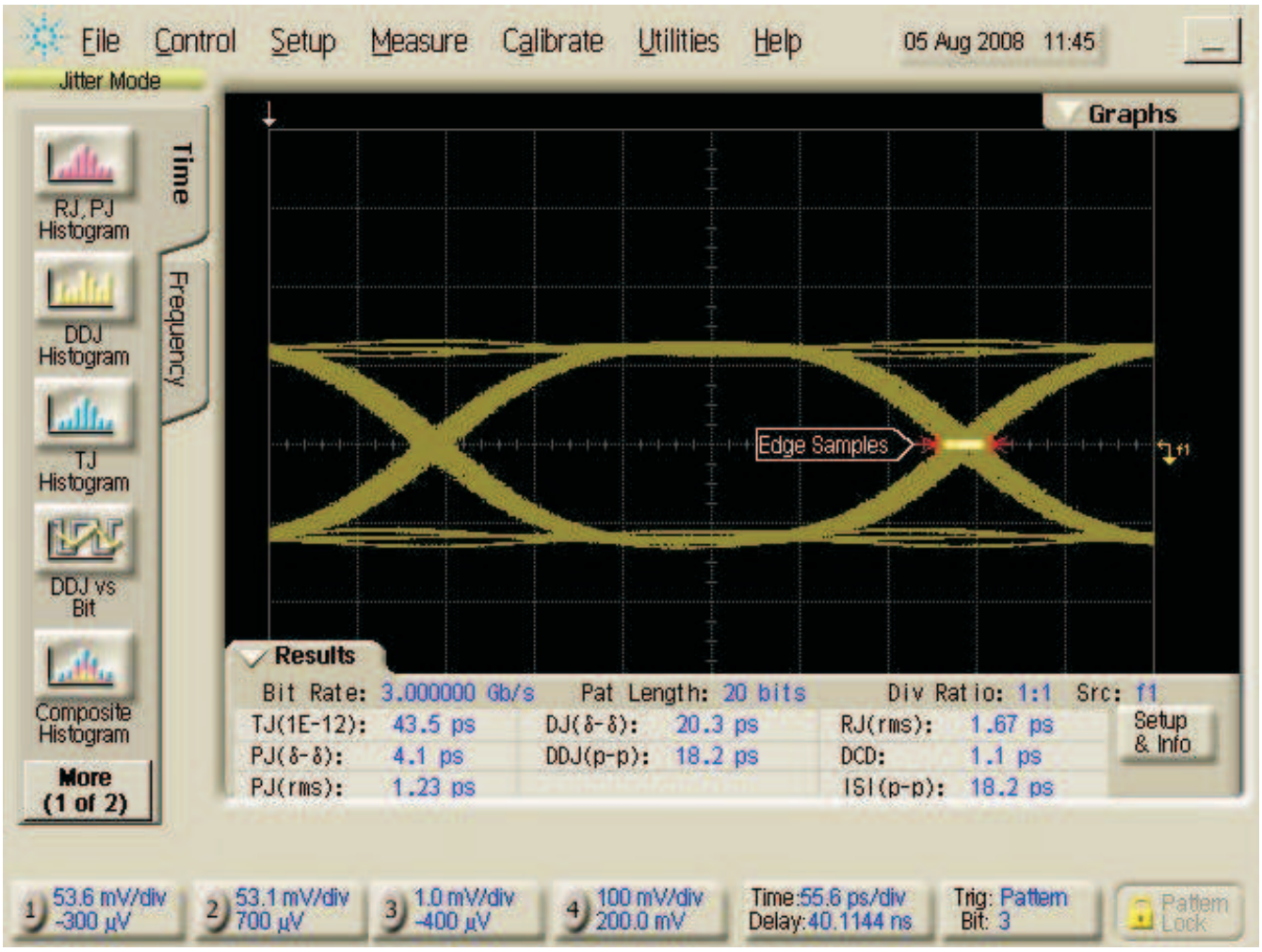


Figure 6. Eye Pattern

X=5.7”, Y =5.7” (Eye Height/Width)

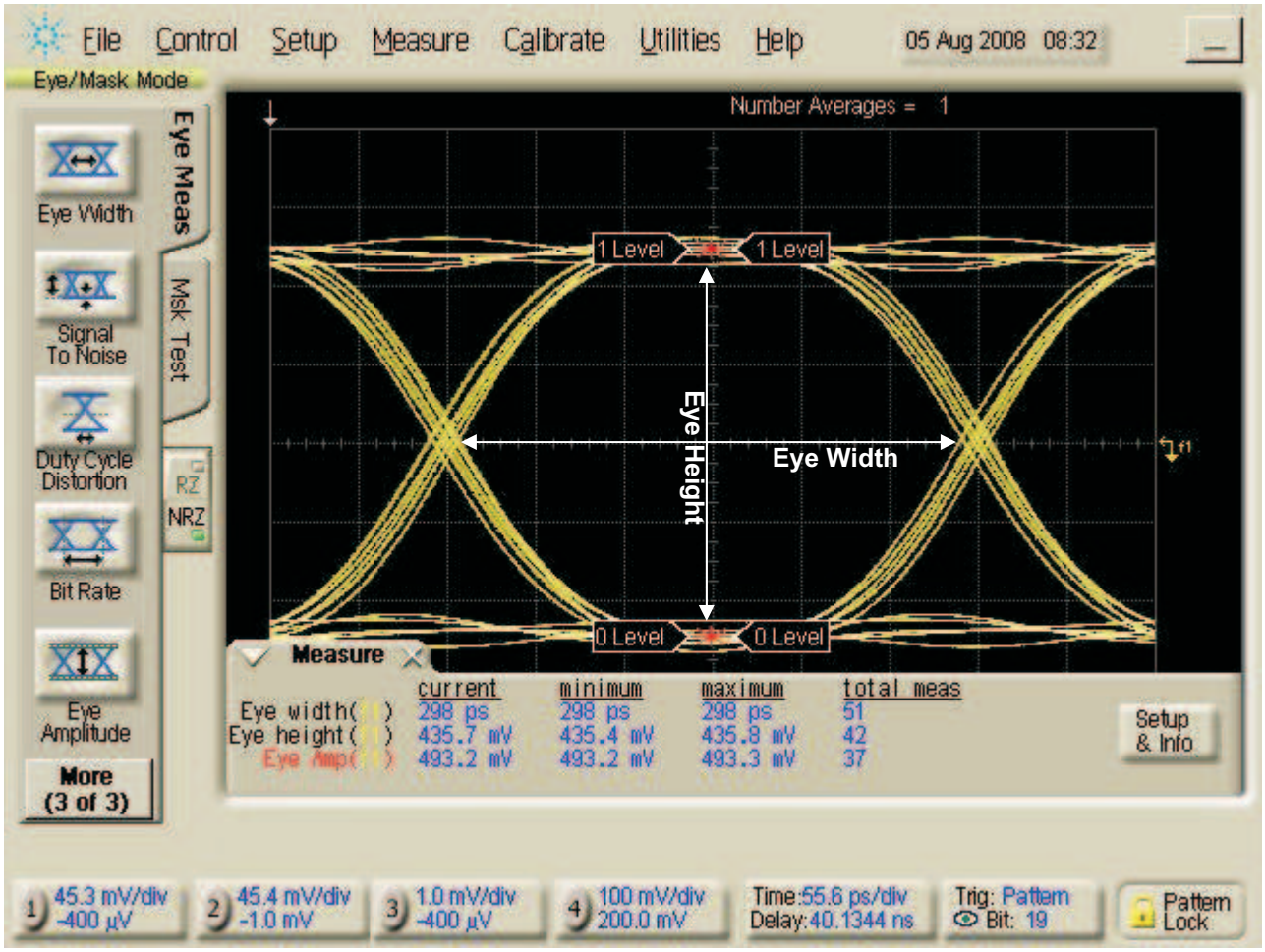


Figure 7. Eye Pattern

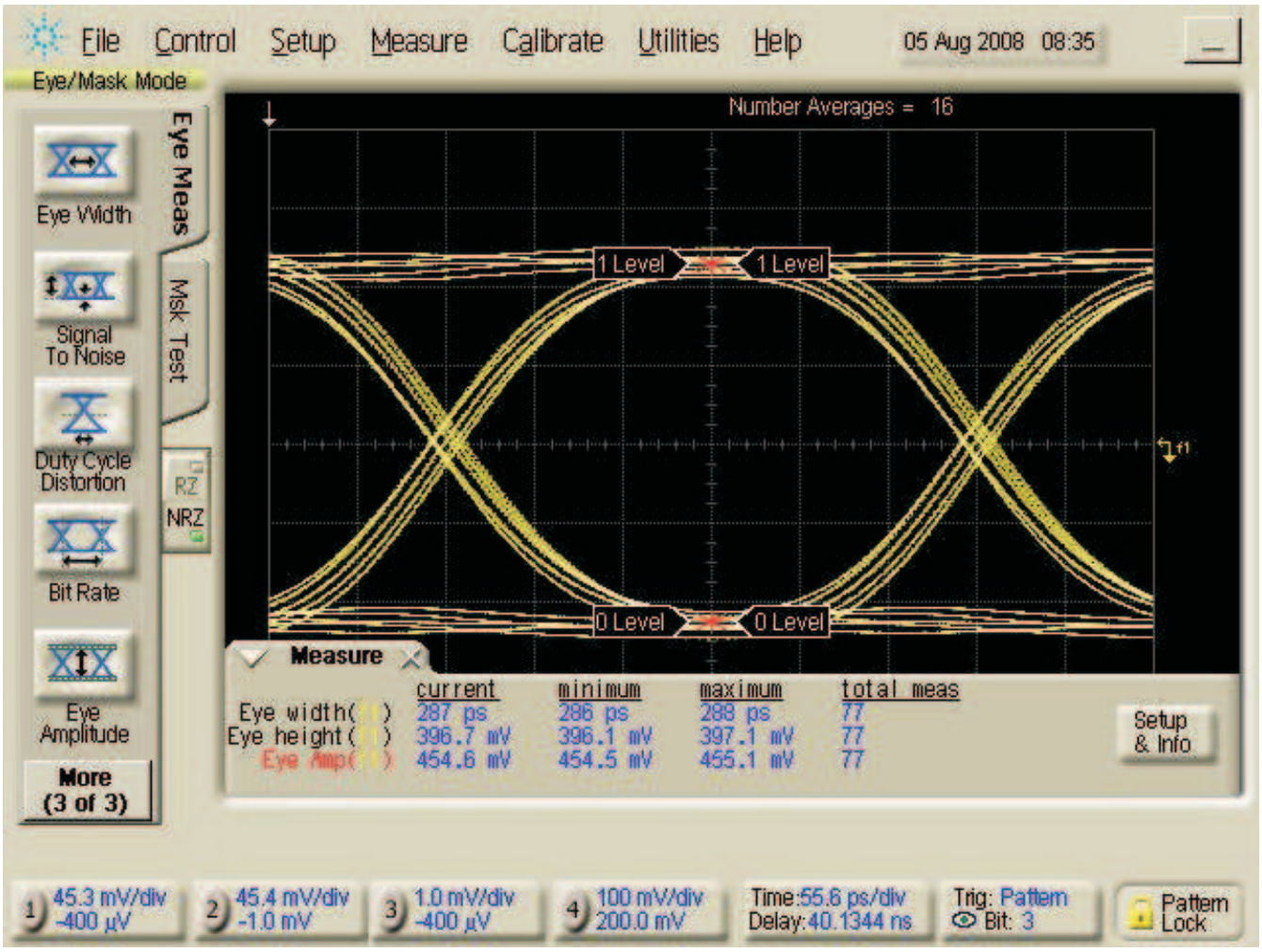


Figure 8. Eye Pattern

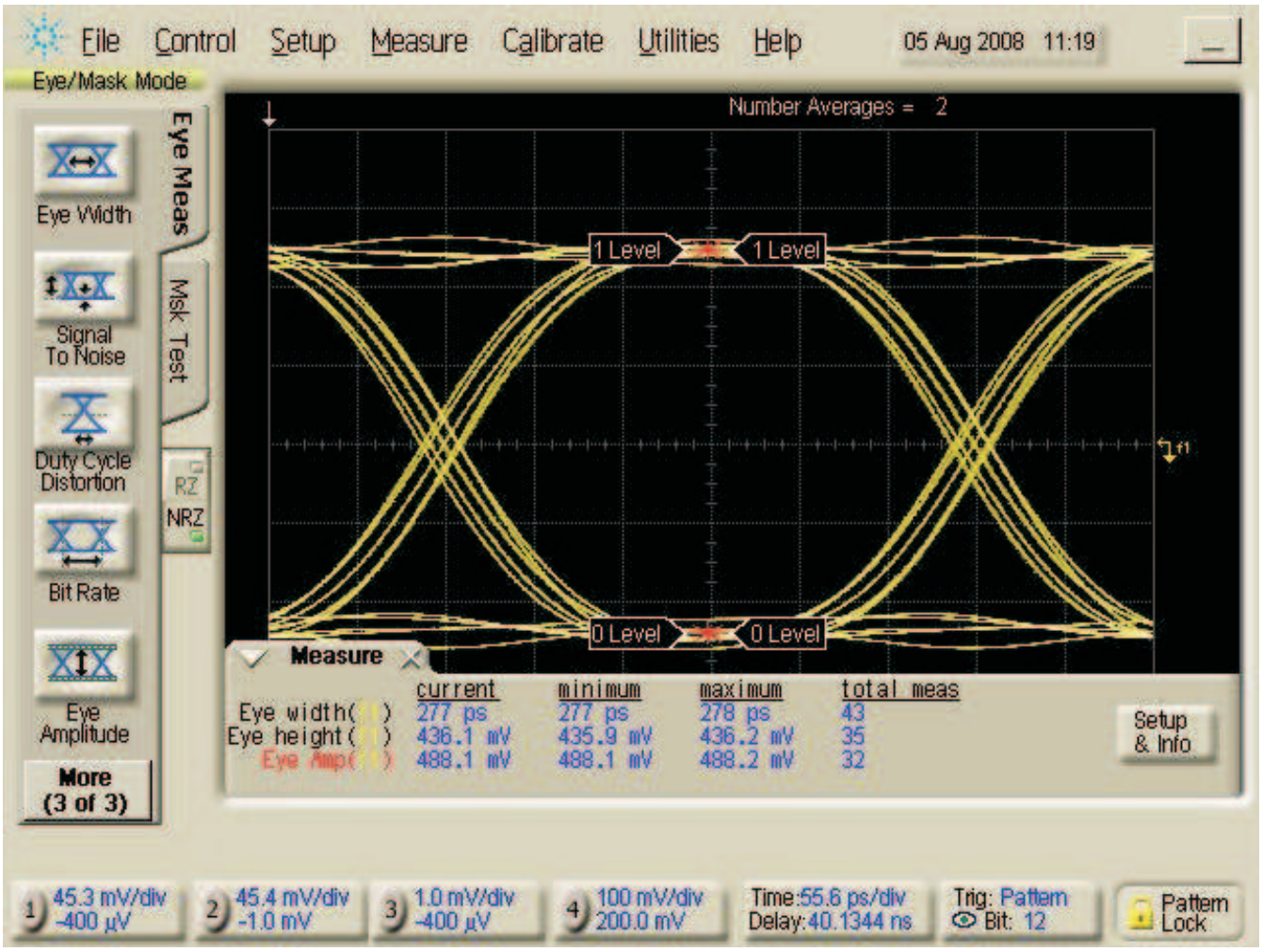


Figure 9. Eye Pattern

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75LVCP412RTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 85	LVCP412	Samples
SN75LVCP412RTJT	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	0 to 85	LVCP412	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

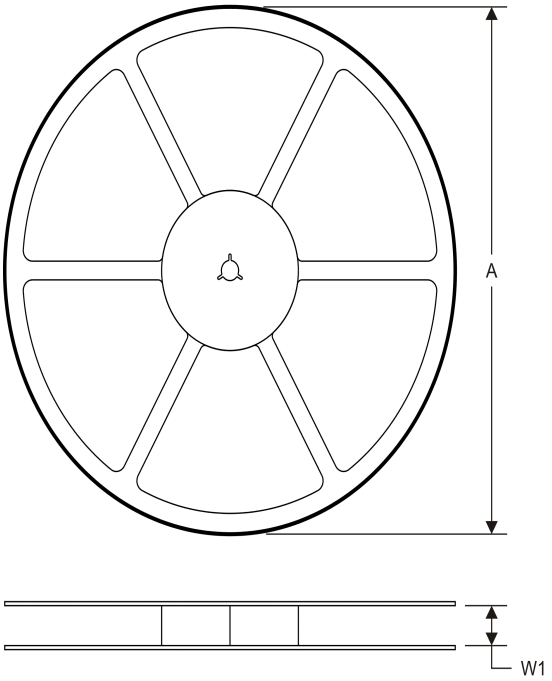
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

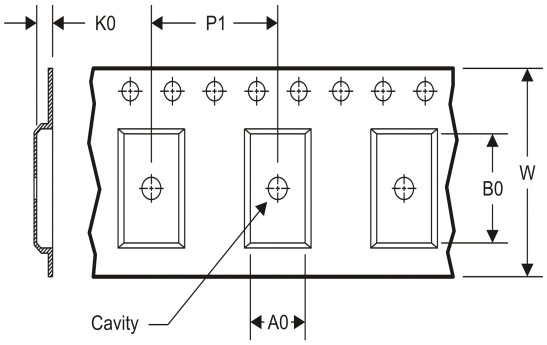
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



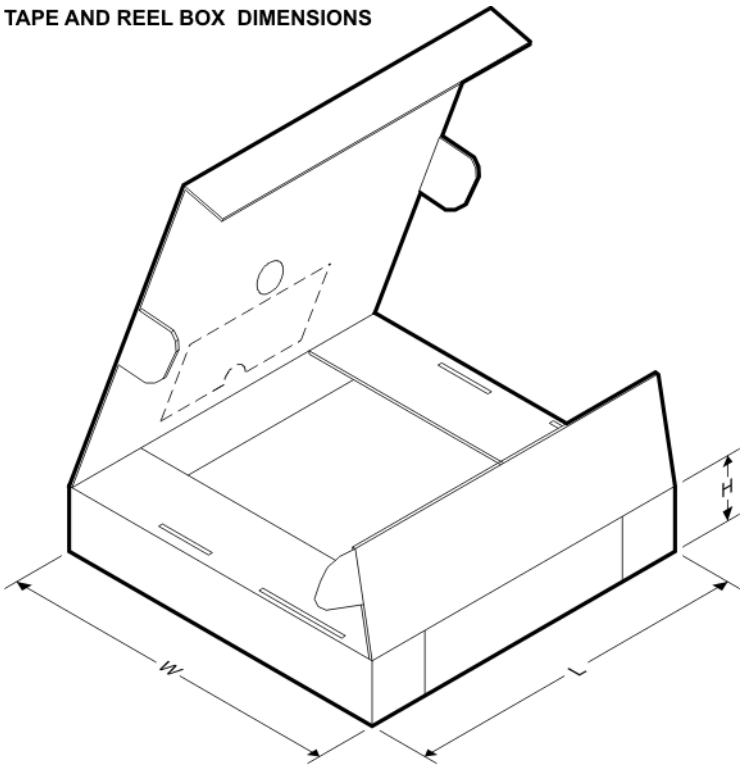
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVCP412RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN75LVCP412RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

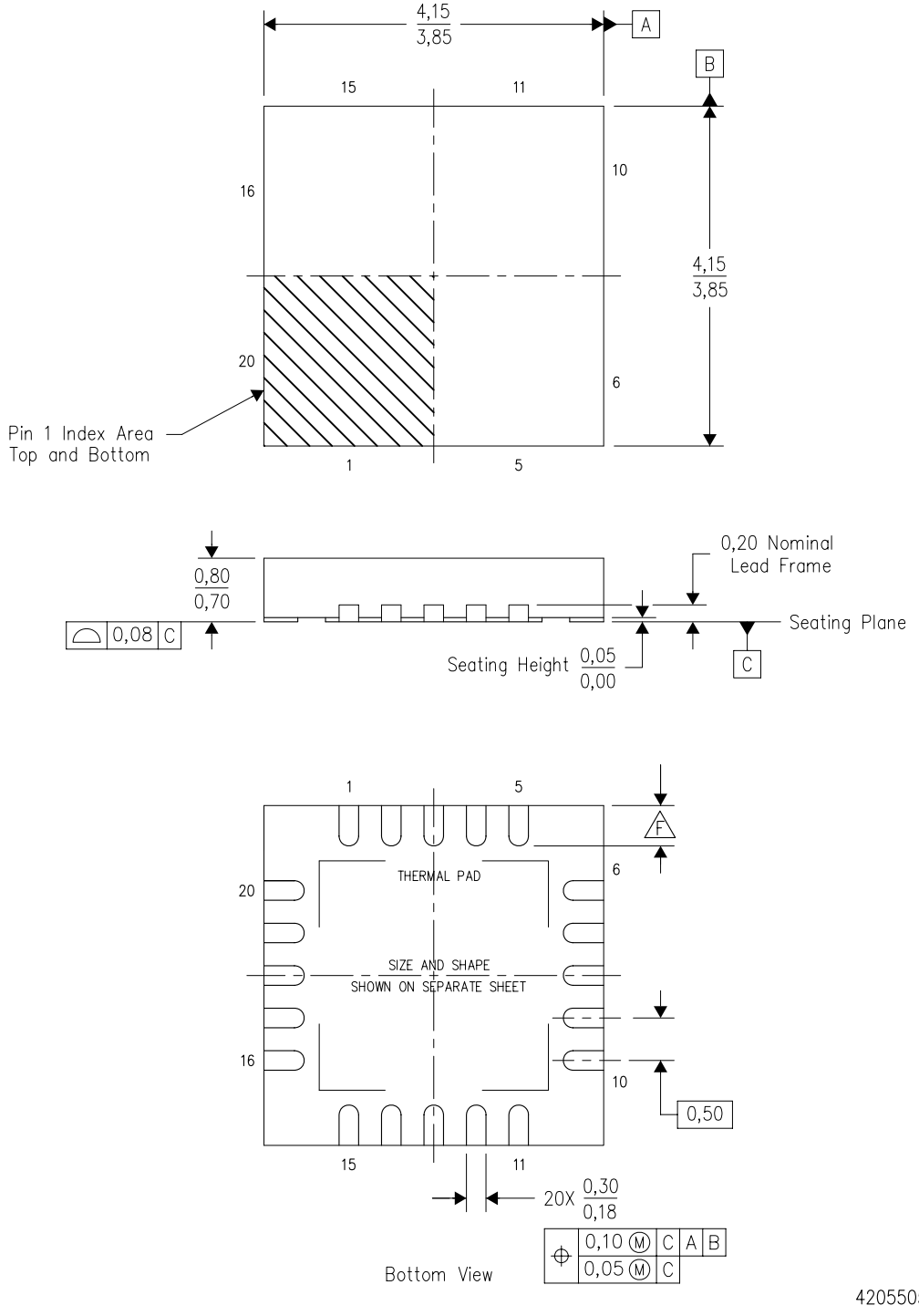
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVCP412RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
SN75LVCP412RTJT	QFN	RTJ	20	250	210.0	185.0	35.0

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

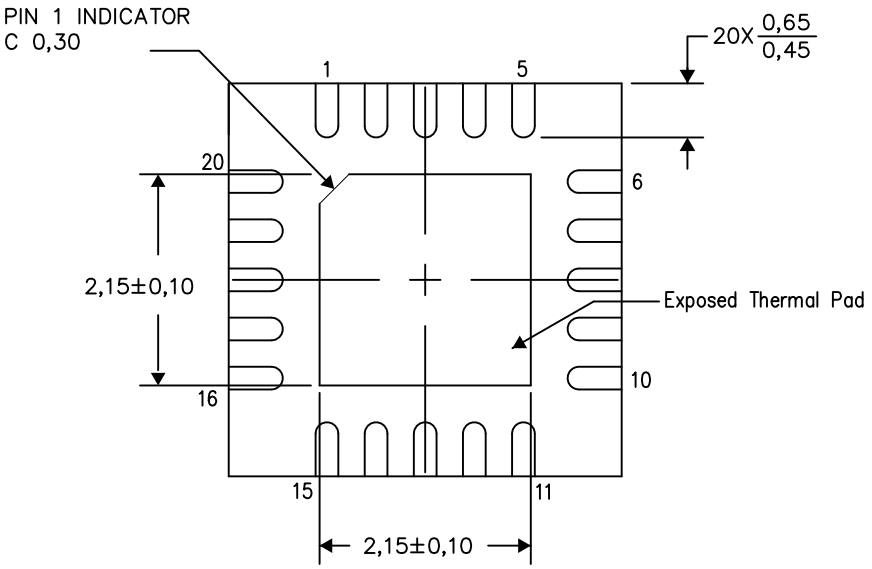
RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



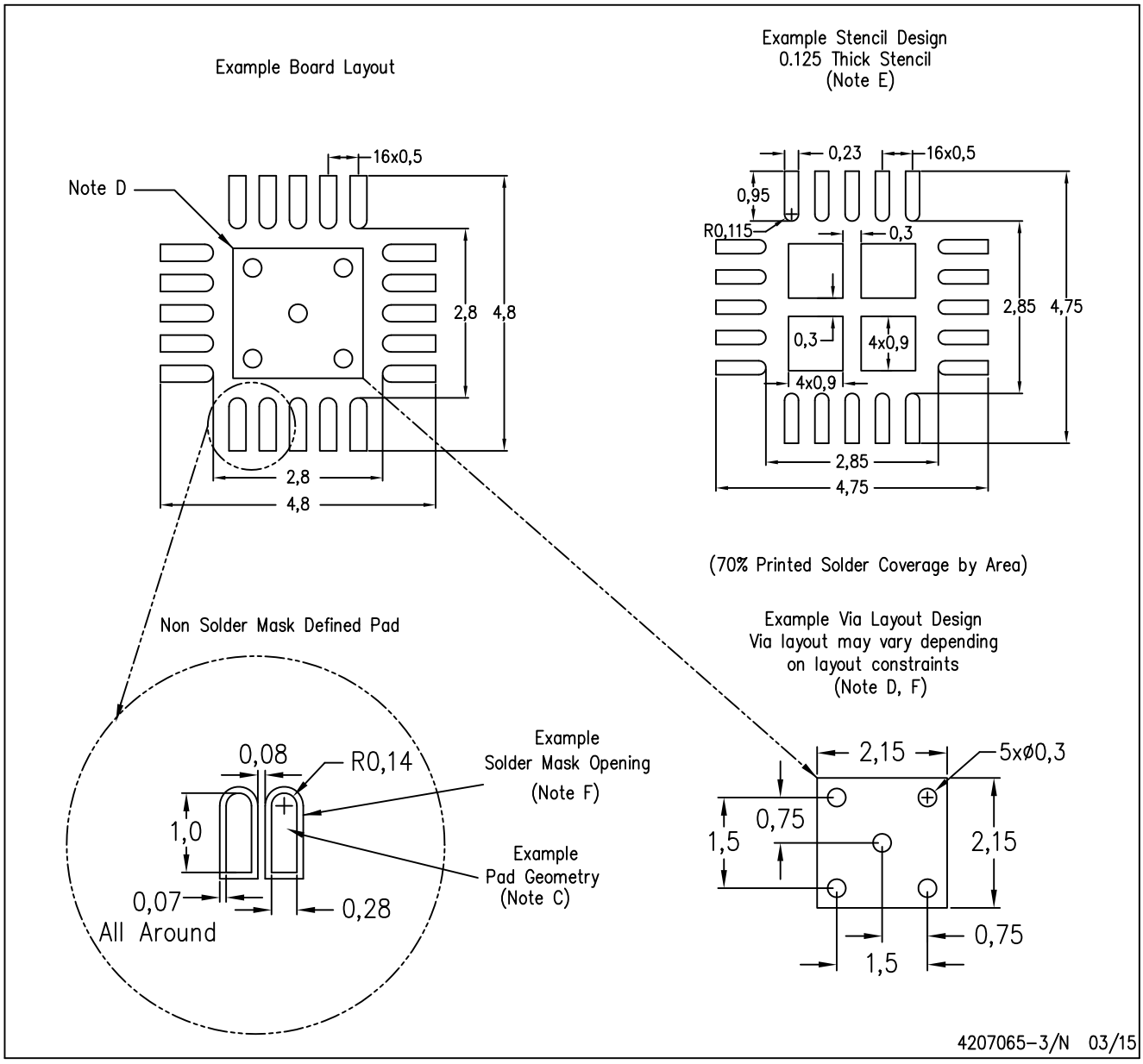
Bottom View

Exposed Thermal Pad Dimensions

4206256–3/V 05/15

NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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