

MC74AC157, MC74ACT157

Quad 2-Input Multiplexer

The MC74AC157/74ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (non-inverted) form.

The MC74AC157/74ACT157 can also be used as a function generator.

Features

- Outputs Source/Sink 24 mA
- 'ACT157 Has TTL Compatible Inputs
- Pb-Free Packages are Available

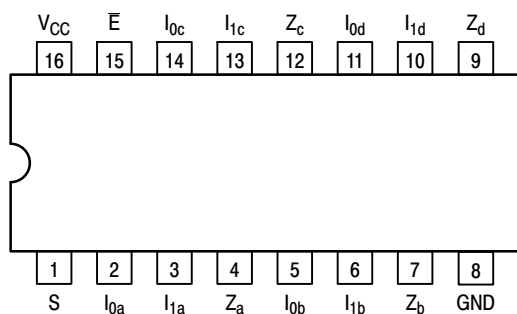


Figure 1. Pinout: 16-Lead Packages Conductors (Top View)

TRUTH TABLE

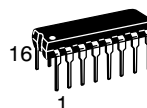
Inputs				Outputs
\bar{E}	S	I ₀	I ₁	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

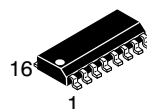


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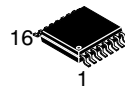
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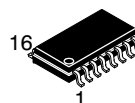
PDIP-16
N SUFFIX
CASE 648



SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



SOEIAJ-16
M SUFFIX
CASE 966

PIN NAMES

PIN	FUNCTION
I _{0a} -I _{0d}	Source 0 Data Inputs
I _{1a} -I _{1d}	Source 0 Data Inputs
\bar{E}	Enable Input
S	Select Input
Z _a -Z _d	Outputs

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 3 of this data sheet.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC74AC157, MC74ACT157

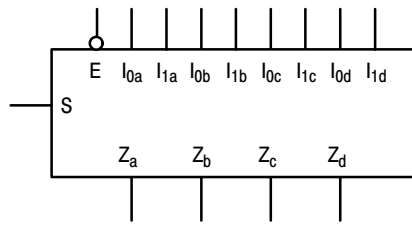


Figure 2. Logic Symbol

FUNCTIONAL DESCRIPTION

The MC74AC157/74ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active-LOW. When \bar{E} is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The MC74AC157/74ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

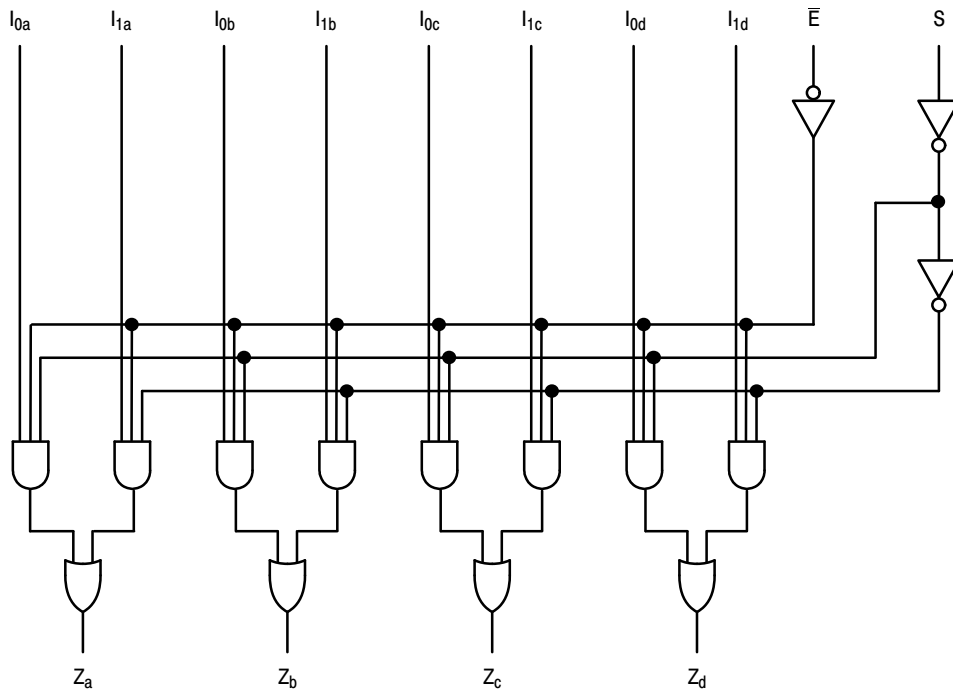
$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the MC74AC157/74ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The MC74AC157/74ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

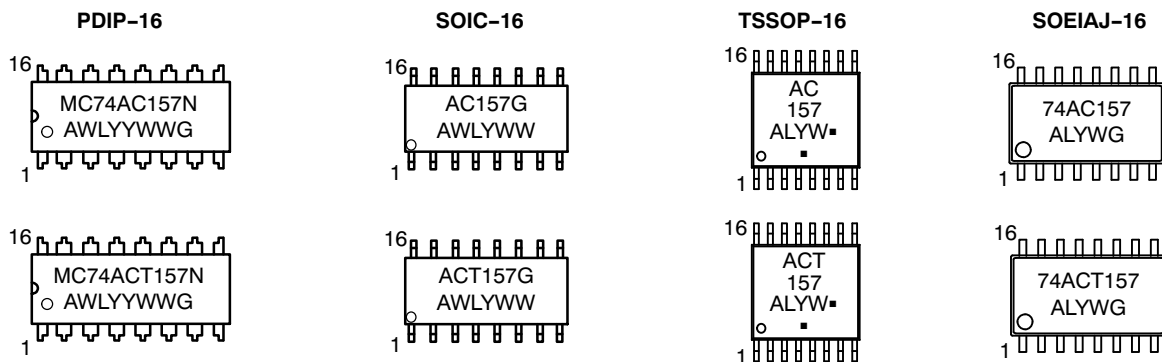


NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MC74AC157, MC74ACT157

MARKING DIAGRAMS



A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G = Pb-Free Package
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin	± 20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	± 50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)	0	-	V_{CC}	V	
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	$V_{CC} @ 3.0 V$	-	150	-	ns/V
		$V_{CC} @ 4.5 V$	-	40	-	
		$V_{CC} @ 5.5 V$	-	25	-	
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	$V_{CC} @ 4.5 V$	-	10	-	ns/V
		$V_{CC} @ 5.5 V$	-	8.0	-	
T_J	Junction Temperature (PDIP)	-	-	140	$^{\circ}C$	
T_A	Operating Ambient Temperature Range	-40	25	85	$^{\circ}C$	
I_{OH}	Output Current - High	-	-	-24	mA	
I_{OL}	Output Current - Low	-	-	24	mA	

- V_{IN} from 30% to 70% V_{CC} ; see individual Data Sheets for devices that differ from the typical input rise and fall times.
- V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

MC74AC157, MC74ACT157

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I _{OUT} = -50 μA	
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
	3.0	-	-	2.56	2.46	V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA	
				4.5	3.86			3.76
				5.5	4.86			4.76
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I _{OUT} = 50 μA	
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
	3.0	-	-	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA	
				4.5	0.36			0.44
				5.5	0.36			0.44
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5	-	-	-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms - See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S to Z _n	3.3	1.5	7.0	11.5	1.5	13.0	ns	3-6
		5.0	1.5	5.5	9.0	1.5	10.0		
t _{PHL}	Propagation Delay S to Z _n	3.3	1.5	6.5	11.0	1.5	12.0	ns	3-6
		5.0	1.5	5.0	8.5	1.0	9.5		
t _{PLH}	Propagation Delay E̅ to Z _n	3.3	1.5	7.0	11.5	1.5	13.0	ns	3-6
		5.0	1.5	5.5	9.0	1.5	10.0		
t _{PHL}	Propagation Delay E̅ _n to Z _n	3.3	1.5	6.5	11.0	1.5	12	ns	3-6
		5.0	1.5	5.5	9.0	1.0	9.5		
t _{PLH}	Propagation Delay I _n to Z _n	3.3	1.5	5.0	8.5	1.0	9.0	ns	3-5
		5.0	1.5	4.0	6.5	1.0	7.0		
t _{PHL}	Propagation Delay I _n to Z _n	3.3	1.5	5.0	8.0	1.0	9.0	ns	3-5
		5.0	1.5	4.0	6.5	1.0	7.0		

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC157, MC74ACT157

DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4			
		4.5	-	3.86	3.76		V	*V _{IN} = V _{IL} or V _{IH} -24 mA
		5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V _I = V _{CC} , GND
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	-	1.5		mA	V _I = V _{CC} - 2.1 V
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	-	-	-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms - See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S to Z _n	5.0	2.0	-	9.0	1.5	10.0	ns	3-6
t _{PHL}	Propagation Delay S to Z _n	5.0	2.0	-	9.5	2.0	10.5	ns	3-6
t _{PLH}	Propagation Delay \bar{E}_n to Z _n	5.0	1.5	-	10	1.5	11.5	ns	3-6
t _{PHL}	Propagation Delay \bar{E}_n to Z _n	5.0	1.5	-	8.5	1.0	9.0	ns	3-6
t _{PLH}	Propagation Delay I _n to Z _n	5.0	1.5	-	7.0	1.0	8.5	ns	3-5
t _{PHL}	Propagation Delay I _n to Z _n	5.0	1.5	-	7.5	1.0	8.5	ns	3-5

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

MC74AC157, MC74ACT157

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	50	pF	V _{CC} = 5.0 V

ORDERING INFORMATION

Device Order Number	Package	Shipping†
MC74AC157N	PDIP-16	25 Units / Rail
MC74AC157NG	PDIP-16 (Pb-Free)	
MC74ACT157NG	PDIP-16 (Pb-Free)	
MC74AC157D	SOIC-16	48 Units / Rail
MC74AC157DG	SOIC-16 (Pb-Free)	
MC74ACT157D	SOIC-16	
MC74ACT157DG	SOIC-16 (Pb-Free)	
MC74AC157DR2	SOIC-16	2500 Tape & Reel
MC74AC157DR2G	SOIC-16 (Pb-Free)	
MC74ACT157DR2	SOIC-16	
MC74ACT157DR2G	SOIC-16 (Pb-Free)	
MC74AC157DTR2	TSSOP-16*	
MC74AC157DTR2G	TSSOP-16*	
MC74ACT157DTR2	TSSOP-16*	
MC74ACT157DTR2G	TSSOP-16*	
MC74ACT157M	SOEIAJ-16	50 Units / Rail
MC74AC157MELG	SOEIAJ-16 (Pb-Free)	2000 Tape & Reel
MC74ACT157MELG	SOEIAJ-16 (Pb-Free)	

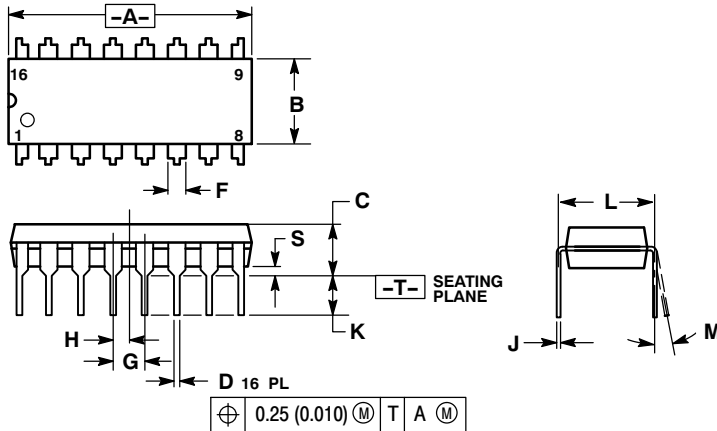
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb-Free.

MC74AC157, MC74ACT157

PACKAGE DIMENSIONS

PDIP-16
N SUFFIX
CASE 648-08
ISSUE T



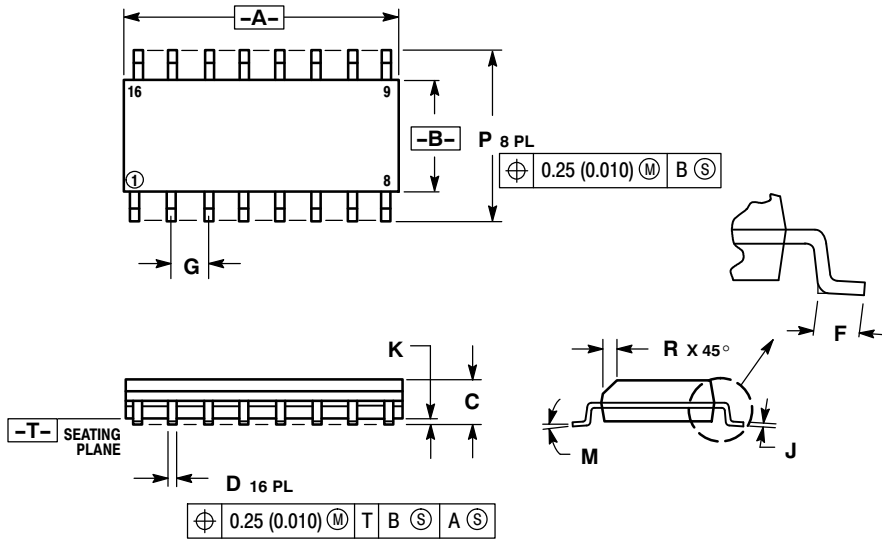
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

MC74AC157, MC74ACT157

PACKAGE DIMENSIONS

SOIC-16
D SUFFIX
CASE 751B-05
ISSUE K

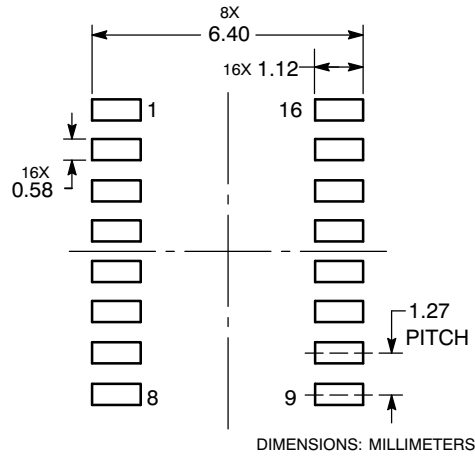


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

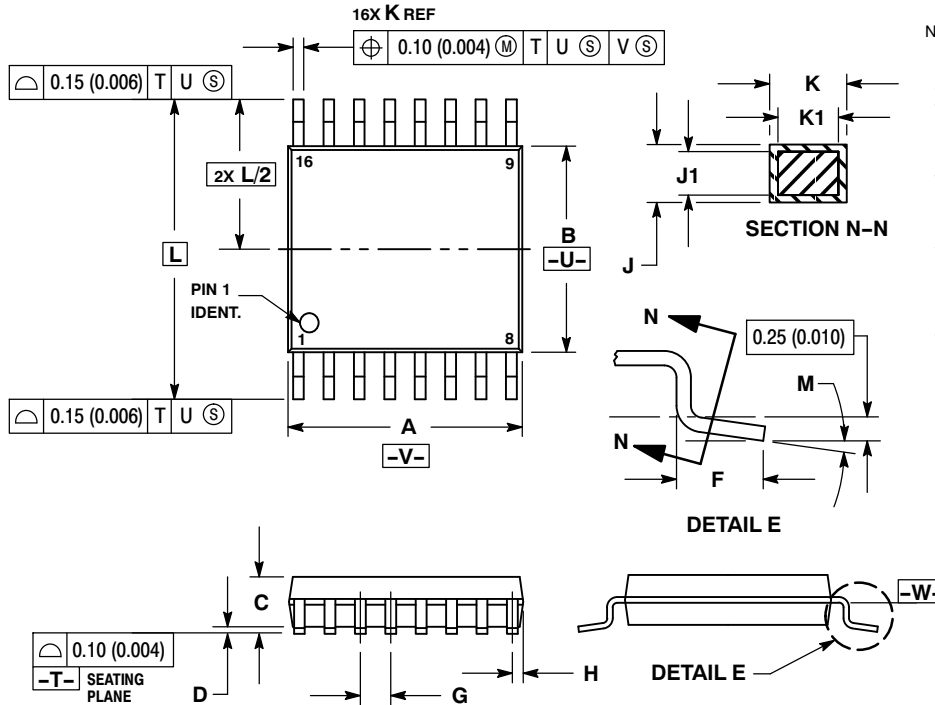


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74AC157, MC74ACT157

PACKAGE DIMENSIONS

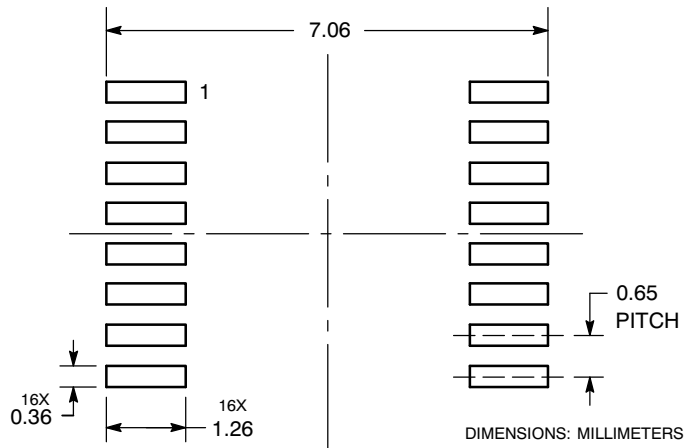
TSSOP-16
DT SUFFIX
CASE 948F-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

SOLDERING FOOTPRINT*

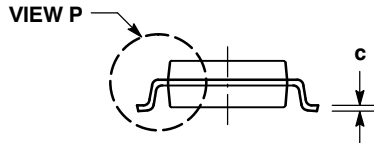
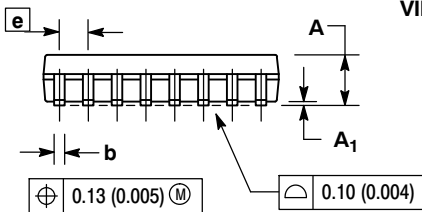
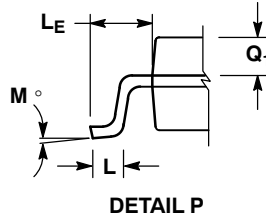
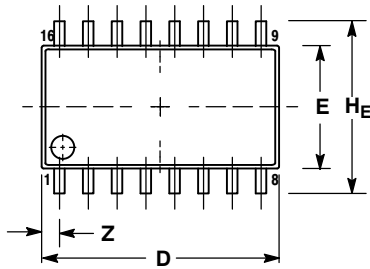


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74AC157, MC74ACT157

PACKAGE DIMENSIONS

SOEIAJ-16
M SUFFIX
CASE 966-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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