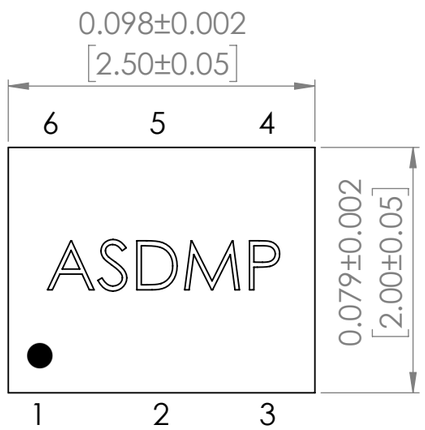
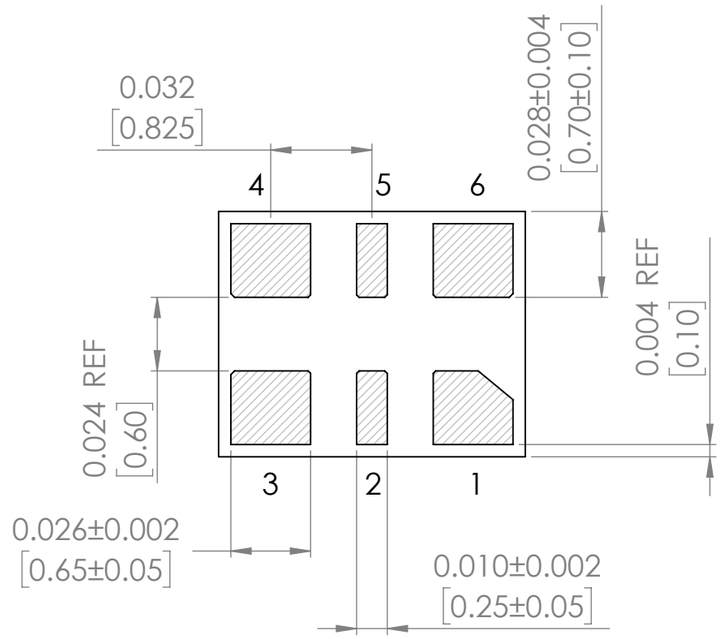
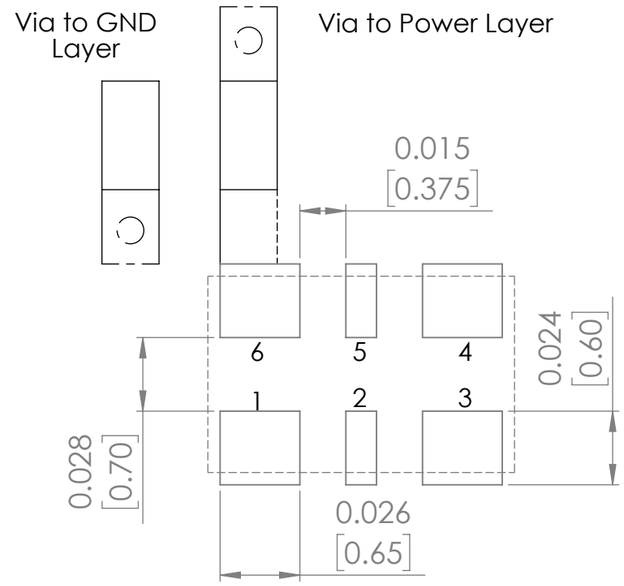
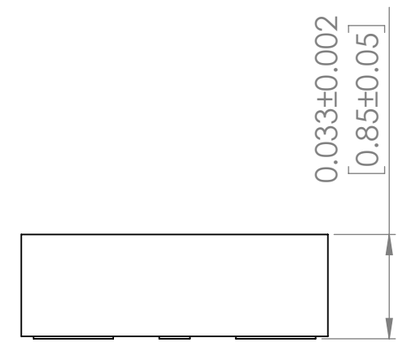
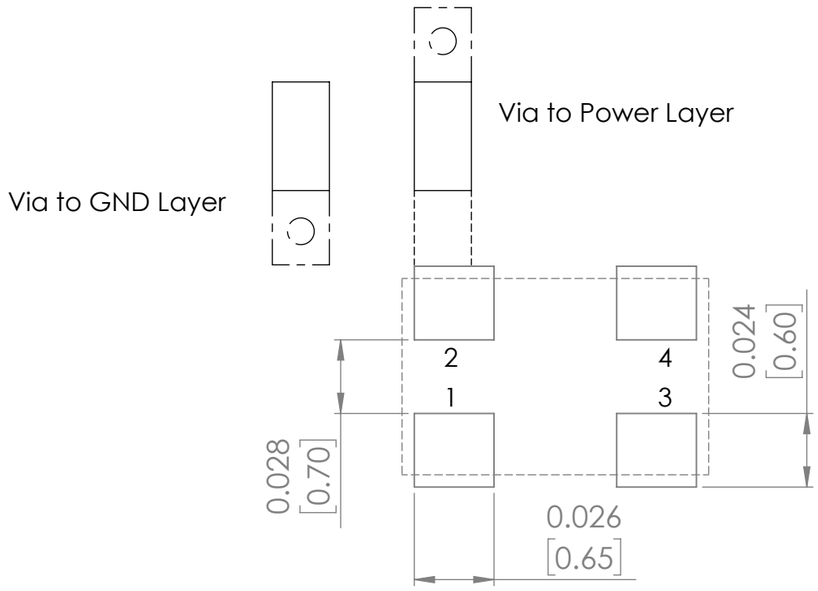






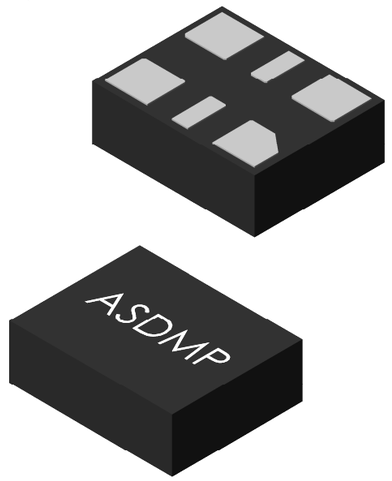
Recommended Land Pattern FOR LVPECL,LVDS,HCSL





Recommended Land Pattern FOR CMOS

Pin	Function
1	Tri-state
2	NC
3	GND
4	Output
5	NC (CMOS) Output (LVPECL, LVDS, HCSL)
6	Vdd



NOTE: Recommended using approximately
0.01uf bypass capacitor between PIN 6 and 3

**TOP PACKAGE MARKING IS
FOR ILLUSTRATION PURPOSES ONLY**

DO NOT SCALE DRAWING | REVISION -

ABRACON® LLC
The Power of Linking Together
5101 Hidden Creek Lane, Spicewood Texas-78669

TITLE: VOLTAGE CONTROLLED TEMP. COMPENSATED SMD CRYSTAL OSCILLATOR

DWG NO. ASDMP | A3

SCALE: 7:1 | SHEET 1 OF 1