ISL28118, ISL28218

40V Precision Single-Supply, Rail-to-rail Output, Low-power Operational Amplifiers

FN7532
Rev 7.00
July 27, 2015

The ISL28118, ISL28218 are single and dual, low-power precision amplifiers optimized for single-supply applications. These devices feature a common mode input voltage range extending to 0.5V below the V_- rail, a rail-to-rail differential input voltage range for use as a comparator and rail-to-rail output voltage swing, which makes them ideal for single-supply applications where input operation at ground is important.

These op amps feature low power, low offset voltage and low temperature drift, making them the ideal choice for applications requiring both high DC accuracy and AC performance. These amplifiers are designed to operate over a single supply range of 3V to 40V or a split supply voltage range of +1.8V/-1.2V to ±20V. The combination of precision and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision instrumentation, data acquisition, precision power supply controls and industrial controls.

Both parts are offered in 8 Ld SOIC and 8 Ld MSOP packages. All devices are offered in standard pin configurations and operate across the extended temperature range of -40°C to +125°C.

Related Literature

- AN1595, “ISL28218SOICEVAL1Z Evaluation Board User’s Guide”

Features

- Rail-to-rail output . . . . <10mV
- Below-ground (V_-) input capability to -0.5V, ground sensing
- Single-supply range . . . . 3V to 40V
- Low current consumption 850µA
- Low noise voltage. . . . . 5.6nV/√Hz
- Low noise current. . . . . 355fA/√Hz
- Low input offset voltage
  - ISL28118 . . . . 150µV (max)
  - ISL28218 . . . . 230µV (max)
- Superb offset voltage temperature drift
  - ISL28118 . . . . 1.2µV/°C (max)
  - ISL28218 . . . . 1.4µV/°C (max)
- Operating temperature range. . . . . -40°C to +125°C
- No phase reversal

Applications

- Precision instruments
- Medical instrumentation
- Data acquisition
- Power supply control
- Industrial process control

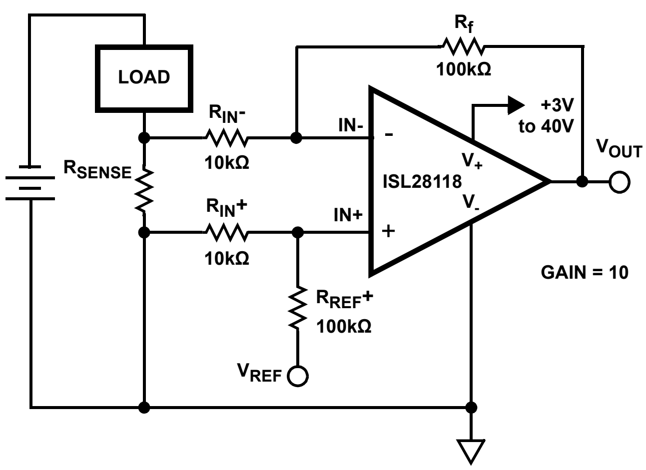

FIGURE 1. TYPICAL APPLICATION: SINGLE-SUPPLY, LOW-SIDE CURRENT SENSE AMPLIFIER

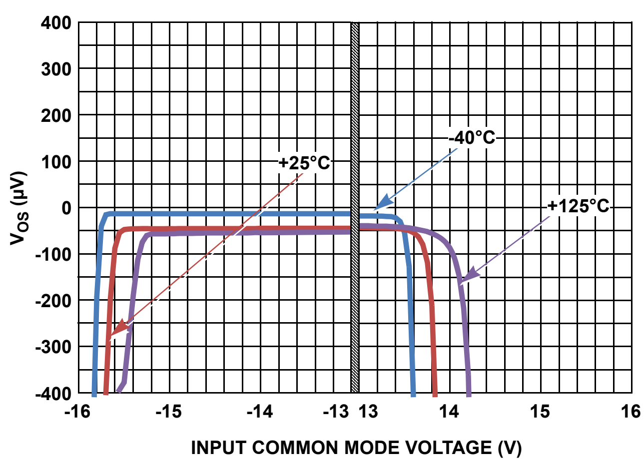

FIGURE 2. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, V_S = ±15V

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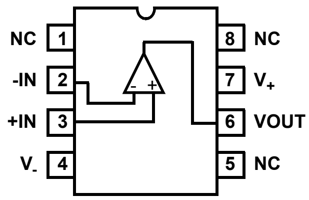
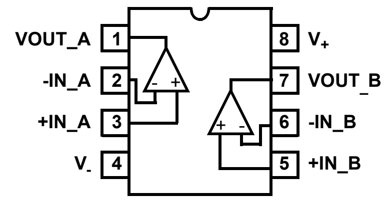
Pin Configurations

ISL28118
(8 LD SOIC, 8 LD MSOP)
TOP VIEW

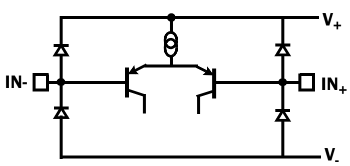


ISL28218
(8 LD SOIC, 8 LD MSOP)
TOP VIEW

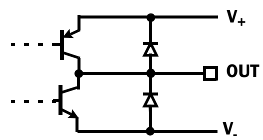


Pin Descriptions

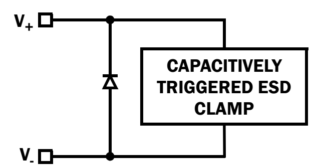
ISL28118 (8 LD SOIC, MSOP)	ISL28218 (8 LD SOIC, MSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	3	+IN, +IN_A	1	Amplifier A noninverting input
2	2	-IN, -IN_A	1	Amplifier A inverting input
6	1	VOUT, VOUT_A	2	Amplifier A output
4	4	V_-	3	Negative power supply
	5	+IN_B	1	Amplifier B noninverting input
	6	-IN_B	1	Amplifier B inverting input
	7	VOUT_B	2	Amplifier B output
7	8	V_+	3	Positive power supply
1, 5, 8	-	NC	-	No Connect



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL28118FBZ	28118 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28118FUZ	8118Z	-40 to +125	8 Ld MSOP	M8.118B
ISL28218FBZ	28218 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28218FUZ	8218Z	-40 to +125	8 Ld MSOP	M8.118B
ISL28218SOICEVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information pages for ISL28118, ISL28218. For more information on MSL, please see Technical Brief TB363.

Absolute Maximum Ratings

Maximum Supply Voltage 42V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage . . . . 42V or V_- - 0.5V to V_+ + 0.5V
Min/Max Input Voltage . . . . 42V or V_- - 0.5V to V_+ + 0.5V
Max/Min Input Current . . . . ±20mA
Output Short-circuit Duration (1 output at a time) . . . . Indefinite
ESD Tolerance
- Human Body Model (Tested per JESD22-A114F) 3kV
- Machine Model (Tested per JESD22-A115-A) 300V
- Charged Device Model (Tested per JESD22-Cl0ID) 2kV

ESD Tolerance (ISL28118 SOIC package only)
- Human Body Model (Tested per JESD22-A114F) 5.5kV
- Machine Model (Tested per JESD22-A115-C) 300V
- Charged Device Model (Tested per JESD22-Cl0ID) 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
ISL28118		
8 Ld SOIC Package (Notes 4, 5)	120	60
8 Ld MSOP Package (Notes 4, 5)	165	57
ISL28218		
8 Ld SOIC Package (Notes 4, 5)	120	55
8 Ld MSOP Package (Notes 4, 5)	150	58

Storage Temperature Range . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . see TB493

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . -40°C to +125°C
Maximum Operating Junction Temperature . . . . +150°C
Supply Voltage . . . . 3V (+1.8V/-1.2V) to 40V (±20V)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the “case temp” location is taken at the package top center.

Electrical Specifications (V_S ±15V)

V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface entries apply across the operating temperature range, -40°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Input Offset Voltage	ISL28118	-150	25	150	µV
			-270		**270**	µV
		ISL28218	-230	40	230	µV
			-290		**290**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	ISL28118	**-1.2**	**0.2**	**1.2**	µV/°C
		ISL28218	**-1.4**	**0.3**	**1.4**	µV/°C
ΔV_{OS}	Input Offset Voltage Match (ISL28218 only)	All packages	-280	44	280	µV
		SOIC	**-365**		**365**	µV
		MSOP	**-390**		**390**	µV
I_B	Input Bias Current		-575	-230		nA
			-800			nA
TCI_B	Input Bias Current Temperature Coefficient			**-0.8**		nA/°C
I_{OS}	Input Offset Current		-50	4	50	nA
			-75		**75**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} = V_- - 0.5V to V_+ - 1.8V		118		dB
		V_{CM} = V_- to V_+ -1.8V ISL28118 SOIC	102	118		dB
			98			dB
		V_{CM} = V_- to V_+ -1.8V ISL28218 SOIC	103	118		dB
			99			dB
		V_{CM} = V_- to V_+ -1.8V ISL28118 and ISL28218 MSOP	102	118		dB
			97			dB
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V_- - 0.5		V_+ - 1.8	V
			V_-		**V_+ - 1.8**	V

Electrical Specifications (V_S ±15V)

V_{CM} = 0, V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface entries apply across the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
PSRR	Power Supply Rejection Ratio	V_S = 3V to 40V, V_{CMIR} = Valid Input Voltage	109	124		dB
			105			dB
A_{VOL}	Open-loop Gain	V_O = -13V to +13V, R_L = 10kΩ to ground, ISL28118 SOIC	125	136		dB
			120			dB
		V_O = -13V to +13V, R_L = 10kΩ to ground, ISL28218 SOIC	125	136		dB
			122			dB
		V_O = -13V to +13V, R_L = 10kΩ to ground, ISL28118 and ISL28218 MSOP	120	136		dB
			116			dB
V_{OL}	Output Voltage Low, V_{OUT} to V_- (see Figure 32)	ISL28118 R_L = 10kΩ			70	mV
					85	mV
		ISL28218 R_L = 10kΩ			70	mV
					73	mV
V_{OH}	Output Voltage High, V_+ to V_{OUT} (see Figure 32)	ISL28118 ISL28218 R_L = 10kΩ			110	mV
					120	mV
I_S	Supply Current/Amplifier	ISL28118 R_L = Open		0.85	1.2	mA
					1.6	mA
		ISL28218 R_L = Open		0.85	1.1	mA
					1.4	mA
I_{SC+}	Output Short-circuit Source Current	R_L = 10Ω to V_-		16		mA
I_{SC-}	Output Short-circuit Sink Current	R_L = 10Ω to V_+		28		mA
V_{SUPPLY}	Supply Voltage Range	Guaranteed by PSRR	**3**		**40**	V
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_{CL} = 101, V_{OUT} = 100mV_{P-P}; R_L = 2k		4		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz, V_S = ±18V		300		nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz, V_S = ±18V		8.5		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz, V_S = ±18V		5.8		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz, V_S = ±18V		5.6		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz, V_S = ±18V		5.6		nV/√Hz
in	Current Noise Density	f = 1kHz, V_S = ±18V		355		fA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 3.5V_{RMS}, R_L = 10kΩ		0.0003		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 1, R_L = 2kΩ, V_O = 10V_{P-P}		±1.2		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
t_s	Settling Time to 0.01% 10V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		8.5		µs

Electrical Specifications (V_S ±5V) V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface entries apply across the operating temperature range, -40°C to +125°C. Temperature data established by characterization.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
V_{OS}	Input Offset Voltage	ISL28118	-150	25	150	µV
			-270		**270**	µV
		ISL28218	-230	40	230	µV
			-290		**290**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	ISL28118	**-1.2**	**0.2**	**1.2**	µV/°C
		ISL28218	**-1.4**	**0.3**	**1.4**	µV/°C
ΔV_{OS}	Input Offset Voltage Match (ISL28218 only)		-280	44	280	µV
			-365		**365**	µV
I_B	Input Bias Current		-575	-230		nA
			-800			nA
TCI_B	Input Bias Current Temperature Coefficient			**-0.8**		nA/°C
I_{OS}	Input Offset Current		-50	4	50	nA
			-75		**75**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} = V_- - 0.5V to V_+ - 1.8V		119		dB
		V_{CM} = V_- to V_+ -1.8V ISL28118 and ISL28218 SOIC	101	117		dB
			97			dB
		V_{CM} = V_- to V_+ -1.8V ISL28118 and ISL28218 MSOP	101	117		dB
			96			dB
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V_- - 0.5		V_+ - 1.8	V
			V_-		**V_+ - 1.8**	V
PSRR	Power Supply Rejection Ratio	V_S = 3V to 10V, V_{CMIR} = Valid Input Voltage, ISL28118 and ISL28218 SOIC	109	124		dB
			105			dB
		ISL28118 MSOP	108	124		dB
		ISL28218 MSOP	107	124		dB
		ISL28118 and ISL28218 MSOP	**103**			dB
A_{VOL}	Open-loop Gain	V_O = -3V to +3V, R_L = 10kΩ to ground, ISL28118 and ISL28218 SOIC	122	132		dB
			117			dB
		ISL28118 and ISL28218 MSOP	120	132		dB
			115			dB
V_{OL}	Output Voltage Low, V_{OUT} to V_- (see Figure 32)	R_L = 10kΩ			38	mV
					45	mV
V_{OH}	Output Voltage High, V_+ to V_{OUT} (see Figure 31)	R_L = 10kΩ			65	mV
					70	mV
I_S	Supply Current/Amplifier	R_L = Open		0.85	1.1	mA
					1.4	mA
I_{SC+}	Output Short-circuit Source Current	R_L = 10Ω to V_-		13		mA
I_{SC-}	Output Short-circuit Sink Current	R_L = 10Ω to V_+		20		mA

Electrical Specifications (V_S ±5V) V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface entries apply across the operating temperature range, -40°C to +125°C. Temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_{CL} = 101, V_{OUT} = 100mV_{P-P}; R_L = 2k		3.2		MHz
e_{np-p}	Voltage Noise	0.1Hz to 10Hz		320		nV_{P-P}
e_n	Voltage Noise Density	f = 10Hz		9		nV/√Hz
e_n	Voltage Noise Density	f = 100Hz		5.7		nV/√Hz
e_n	Voltage Noise Density	f = 1kHz		5.5		nV/√Hz
e_n	Voltage Noise Density	f = 10kHz		5.5		nV/√Hz
in	Current Noise Density	f = 1kHz		380		fA/√Hz
THD + N	Total Harmonic Distortion + Noise	1kHz, G = 1, V_O = 1.25V_{RMS}, R_L = 10kΩ		0.0003		%
TRANSIENT RESPONSE						
SR	Slew Rate	A_V = 1, R_L = 2kΩ, V_O = 4V_{P-P}		±1		V/µs
t_r, t_f, Small Signal	Rise Time 10% to 90% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
	Fall Time 90% to 10% of V_{OUT}	A_V = 1, V_{OUT} = 100mV_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
t_s	Settling Time to 0.01% 4V Step; 10% to V_{OUT}	A_V = 1, V_{OUT} = 4V_{P-P}, R_f = 0Ω, R_L = 2kΩ to V_{CM}		4		µs

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves
V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified.

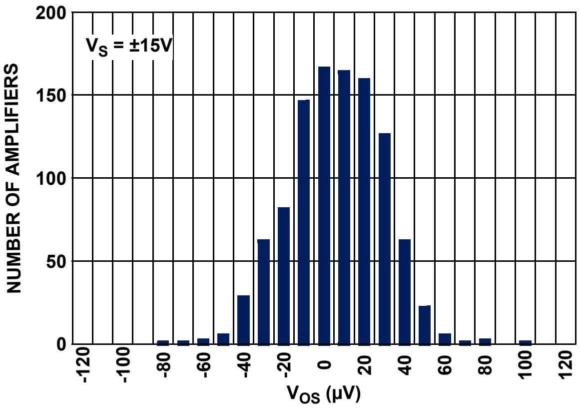


FIGURE 3. ISL28118 INPUT OFFSET VOLTAGE DISTRIBUTION

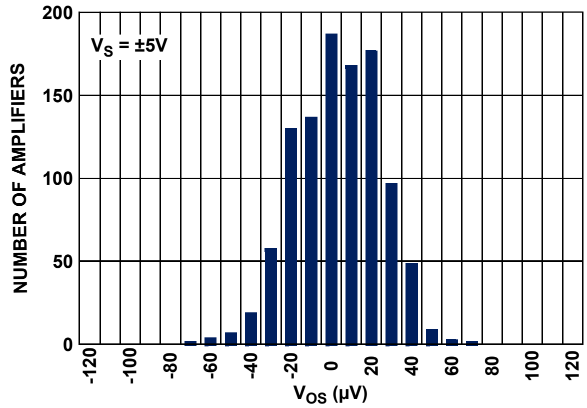


FIGURE 4. ISL28118 INPUT OFFSET VOLTAGE DISTRIBUTION

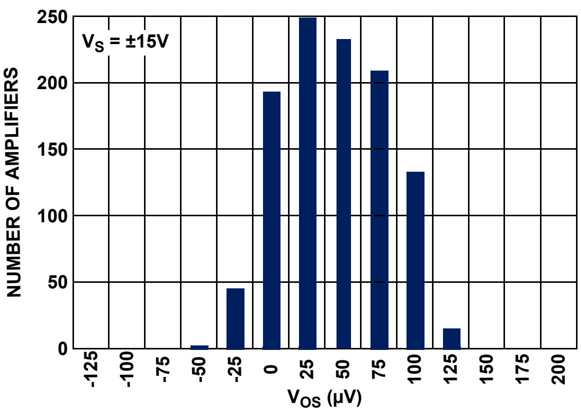


FIGURE 5. ISL28218 INPUT OFFSET VOLTAGE DISTRIBUTION

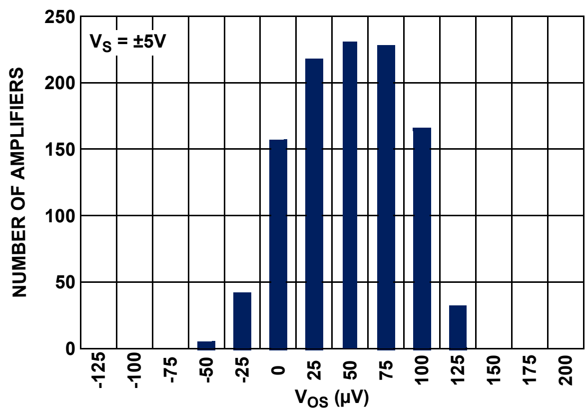


FIGURE 6. ISL28218 INPUT OFFSET VOLTAGE DISTRIBUTION

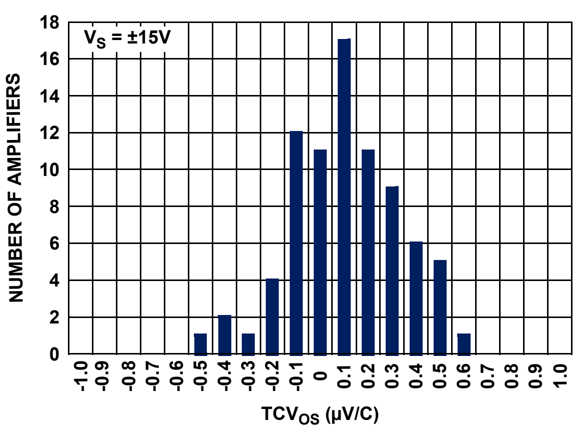


FIGURE 7. ISL28118 TCV_{OS} vs NUMBER OF AMPLIFIERS ±15V

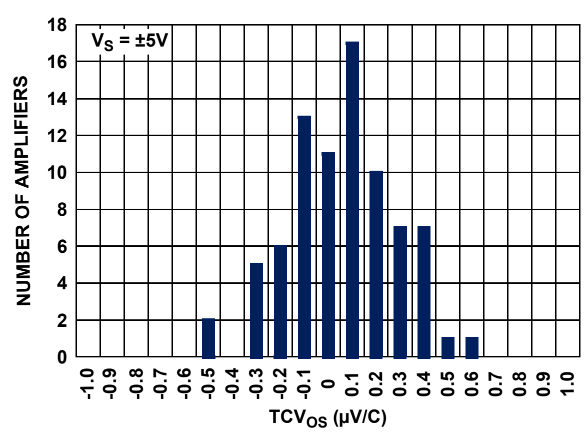


FIGURE 8. ISL28118 TCV_{OS} vs NUMBER OF AMPLIFIERS ±5V

Typical Performance Curves
$V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

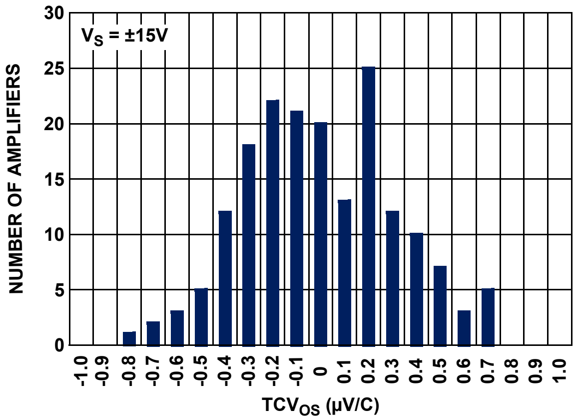


FIGURE 9. ISL28218 TCV_{OS} vs NUMBER OF AMPLIFIERS ±15V

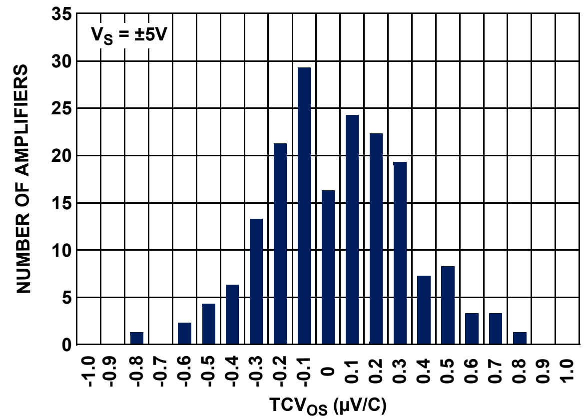


FIGURE 10. ISL28218 TCV_{OS} vs NUMBER OF AMPLIFIERS ±5V

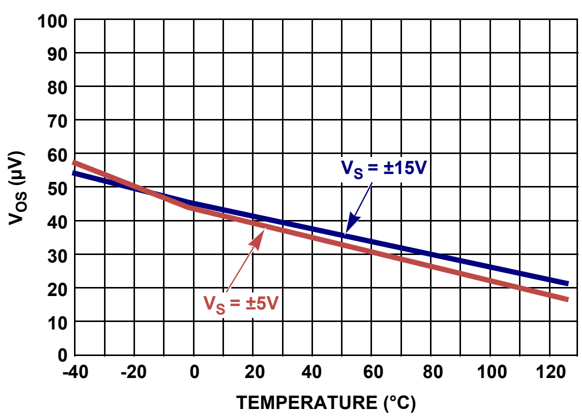


FIGURE 11. V_{OS} vs TEMPERATURE

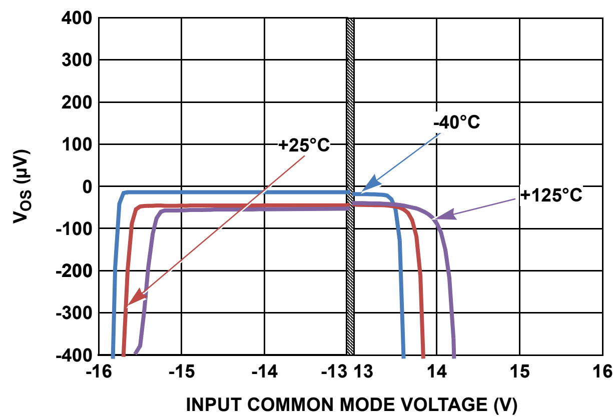


FIGURE 12. INPUT OFFSET VOLTAGE vs INPUT COMMON MODE VOLTAGE, $V_S = \pm15V$

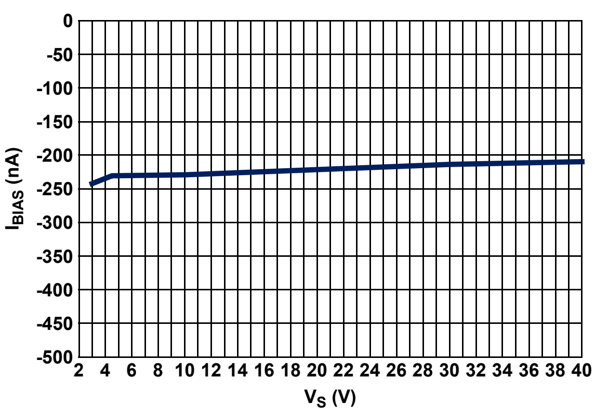


FIGURE 13. I_{BIAS} vs V_S

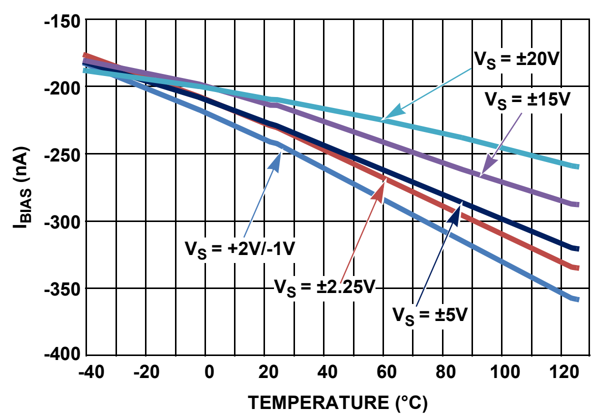


FIGURE 14. I_{BIAS} vs TEMPERATURE vs SUPPLY

Typical Performance Curves
V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

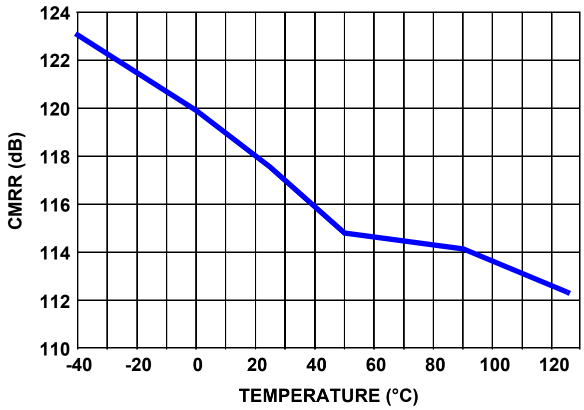


FIGURE 15. ISL28118 CMRR vs TEMPERATURE, V_S = ±15V

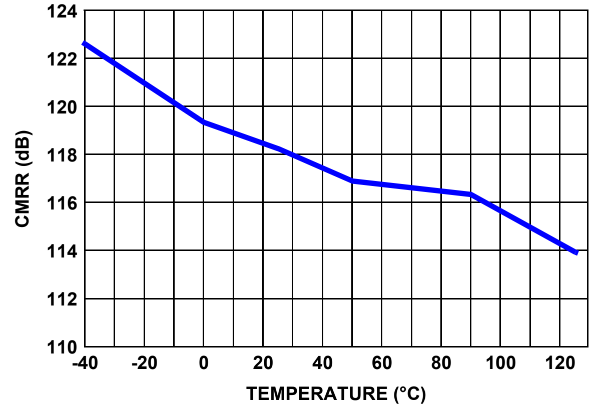


FIGURE 16. ISL28118 CMRR vs TEMPERATURE, V_S = ±5V

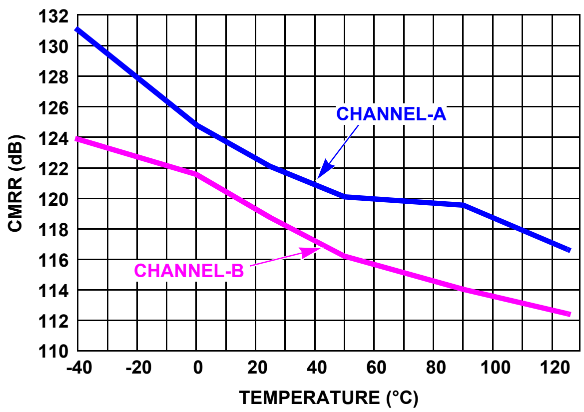


FIGURE 17. ISL28218 CMRR vs TEMPERATURE, V_S = ±15V

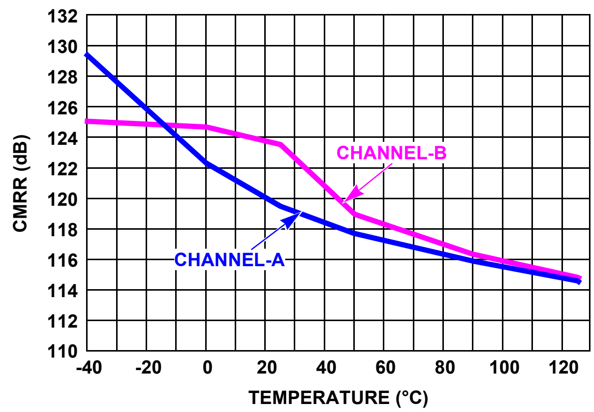


FIGURE 18. ISL28218 CMRR vs TEMPERATURE, V_S = ±5V

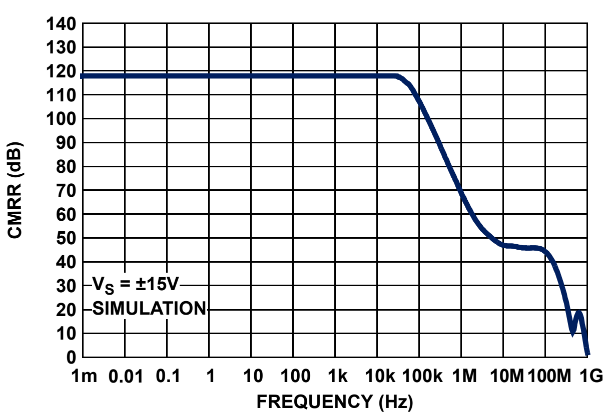


FIGURE 19. CMRR vs FREQUENCY, V_S = ±15V

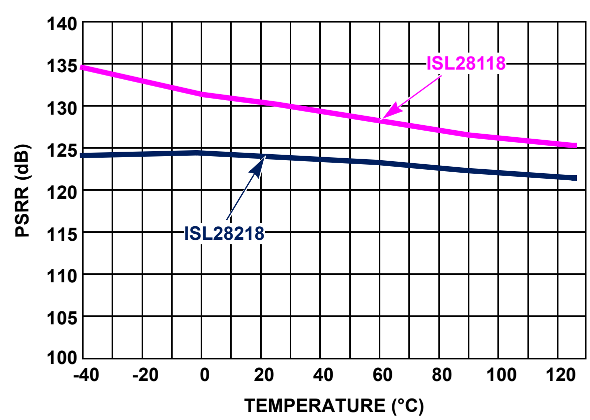


FIGURE 20. PSRR vs TEMPERATURE, V_S = ±15V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

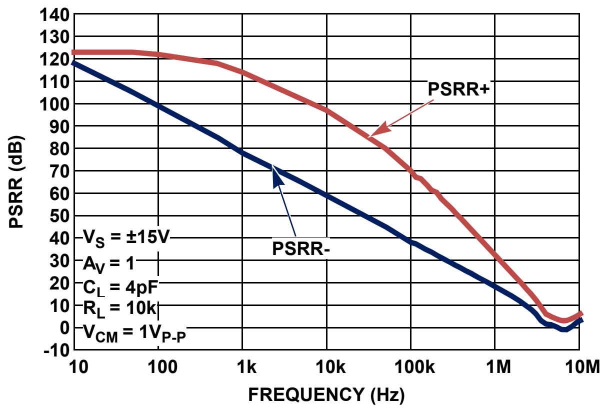


FIGURE 21. PSRR vs FREQUENCY, V_S = ±15V

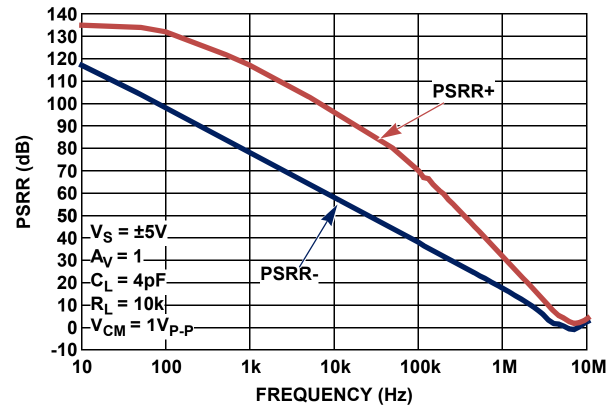


FIGURE 22. PSRR vs FREQUENCY, V_S = ±5V

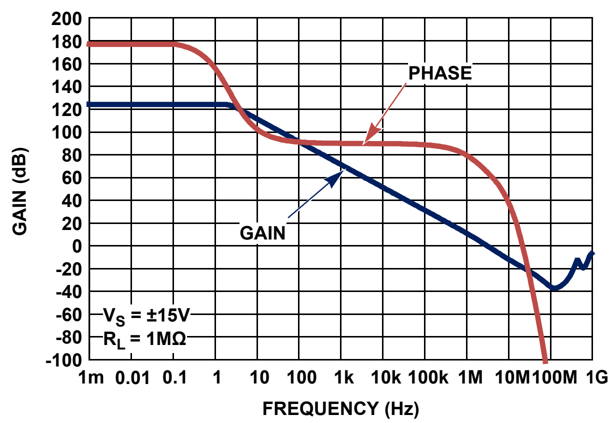


FIGURE 23. OPEN-LOOP GAIN, PHASE vs FREQUENCY, V_S = ±15V

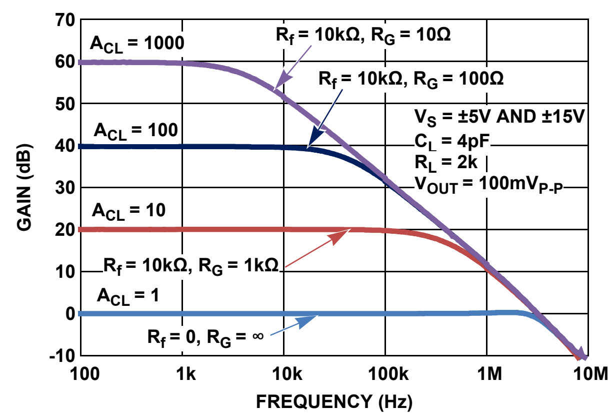


FIGURE 24. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

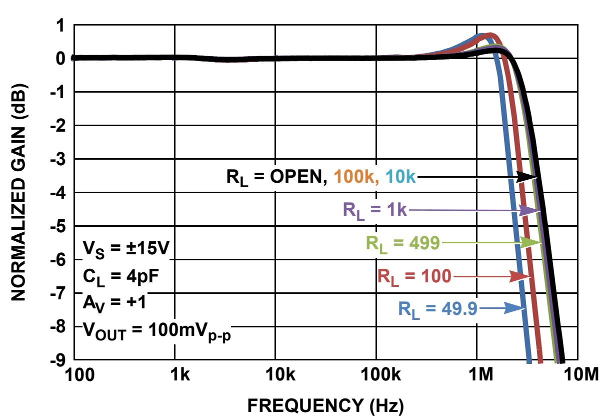


FIGURE 25. GAIN vs FREQUENCY vs R_L, V_S = ±15V

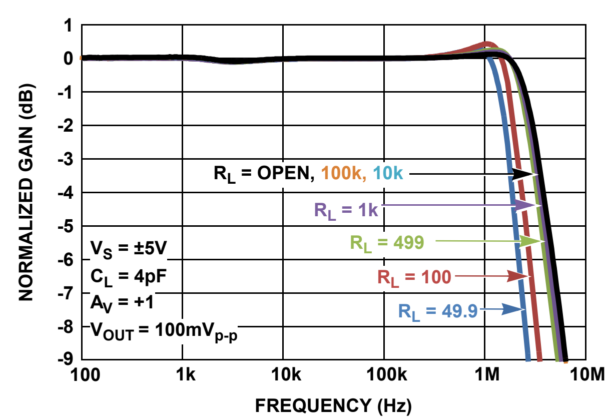


FIGURE 26. GAIN vs FREQUENCY vs R_L, V_S = ±5V

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

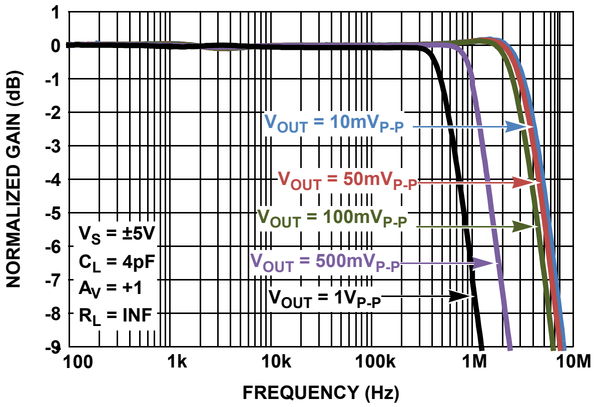


FIGURE 27. GAIN vs FREQUENCY vs OUTPUT VOLTAGE

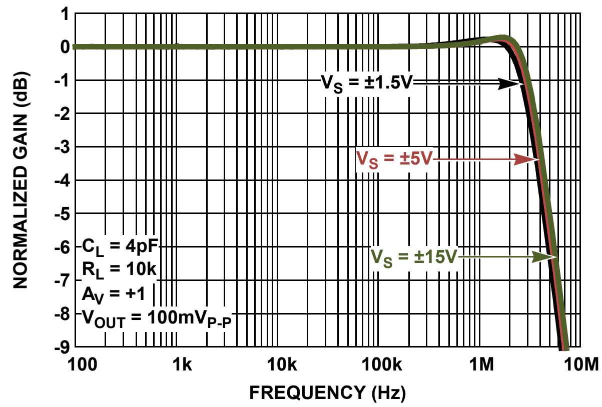


FIGURE 28. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

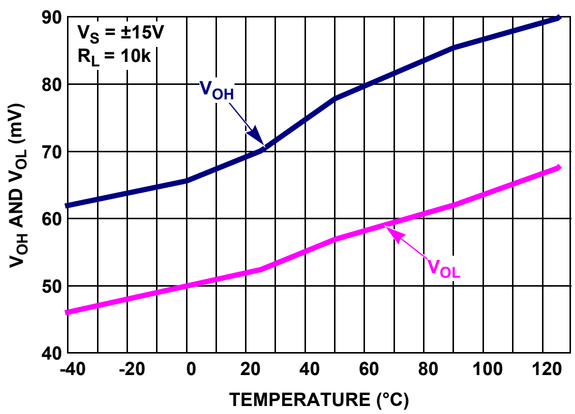


FIGURE 29. OUTPUT OVERHEAD VOLTAGE vs TEMPERATURE, V_S = ±15V, R_L = 10k

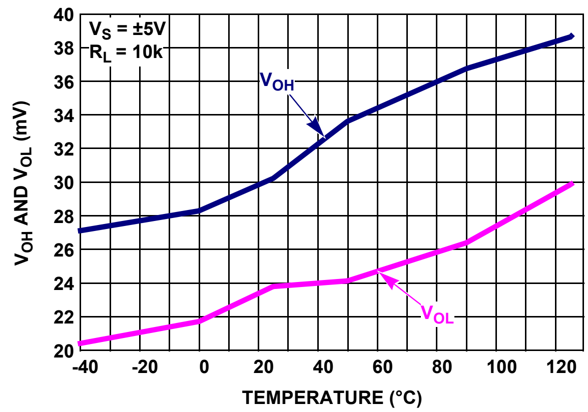


FIGURE 30. OUTPUT OVERHEAD VOLTAGE vs TEMPERATURE, V_S = ±5V, R_L = 10k

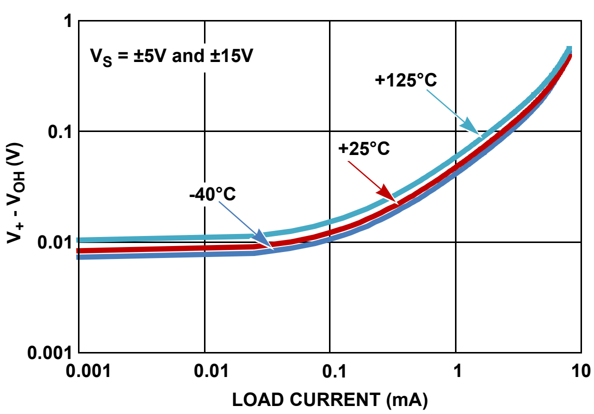


FIGURE 31. OUTPUT OVERHEAD VOLTAGE HIGH vs LOAD CURRENT, V_S = ±5V AND ±15V

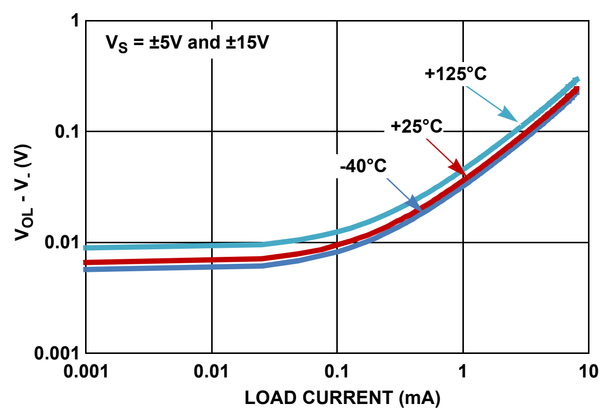


FIGURE 32. OUTPUT OVERHEAD VOLTAGE LOW vs LOAD CURRENT, V_S = ±5V AND ±15V

Typical Performance Curves $V_S = \pm15V, V_{CM} = 0V, R_L = Open, T_A = +25°C$, unless otherwise specified. **(Continued)**

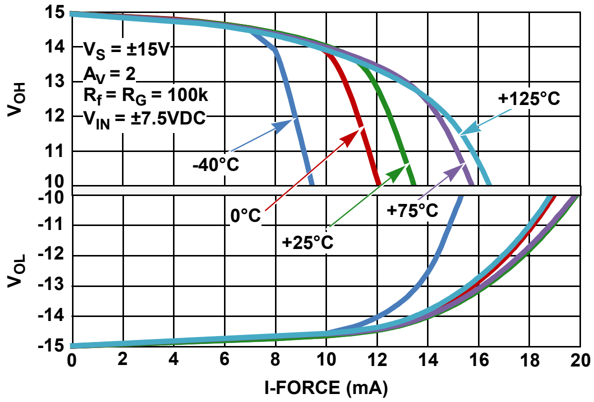


FIGURE 33. OUTPUT VOLTAGE SWING vs LOAD CURRENT $V_S = \pm15V$

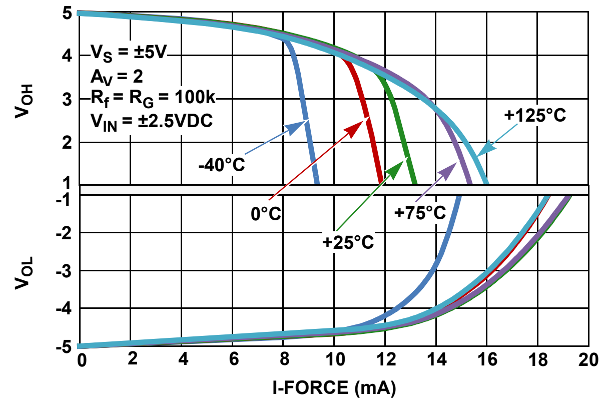


FIGURE 34. OUTPUT VOLTAGE SWING vs LOAD CURRENT $V_S = \pm5V$

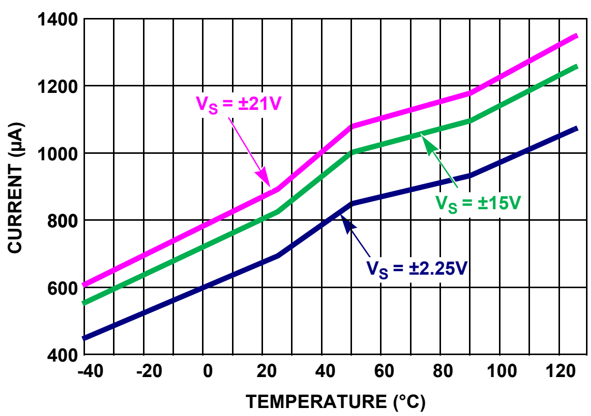


FIGURE 35. ISL28118 SUPPLY CURRENT vs TEMPERATURE vs SUPPLY VOLTAGE

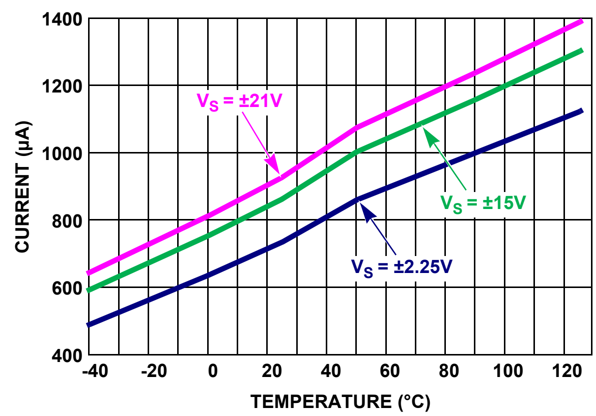


FIGURE 36. ISL28218 SUPPLY CURRENT vs TEMPERATURE vs SUPPLY VOLTAGE

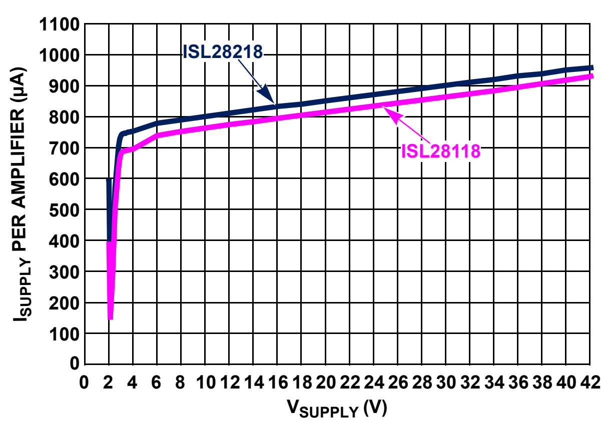


FIGURE 37. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. **(Continued)**

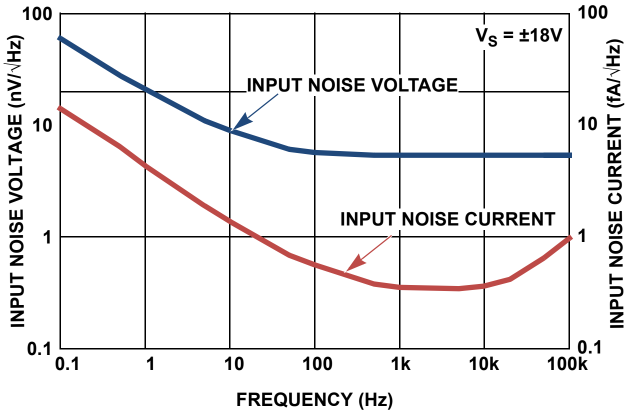


FIGURE 38. INPUT NOISE VOLTAGE (en) AND CURRENT (in) vs FREQUENCY, $V_S = \pm18V$

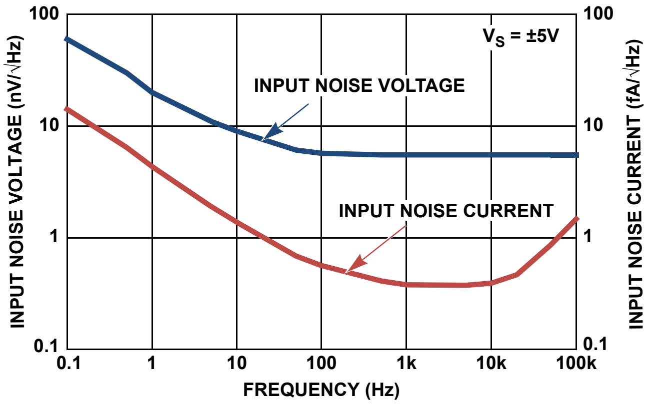


FIGURE 39. INPUT NOISE VOLTAGE (en) AND CURRENT (in) vs FREQUENCY, $V_S = \pm5V$

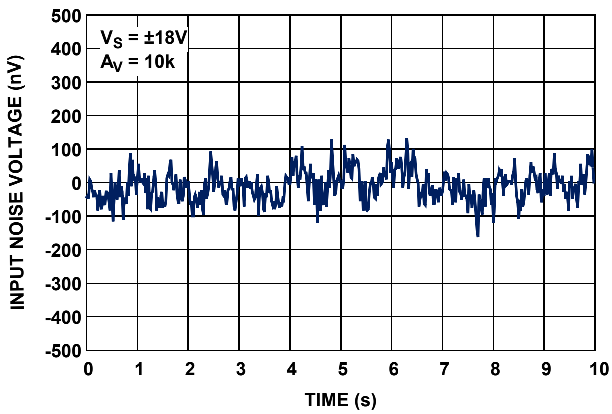


FIGURE 40. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz, $V_S = \pm18V$

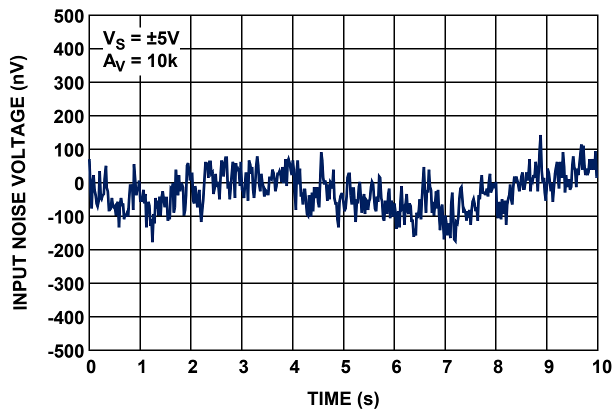


FIGURE 41. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz, $V_S = \pm5V$

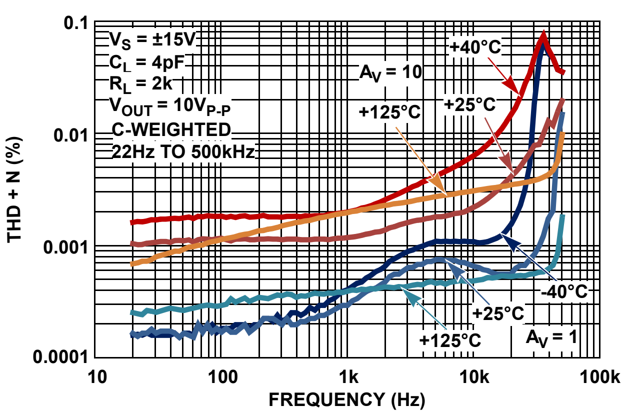


FIGURE 42. THD+N vs FREQUENCY vs TEMPERATURE, $A_V = 1, 10$, $R_L = 2k$

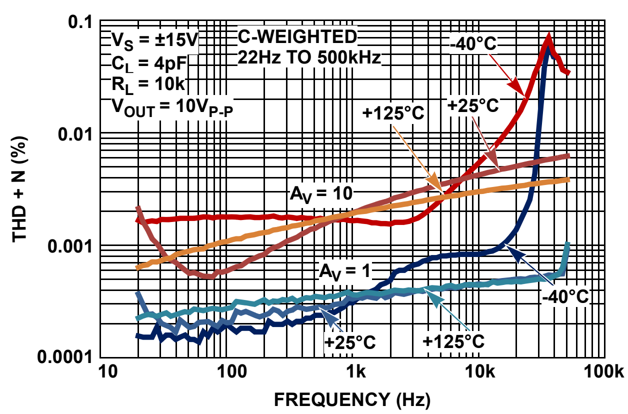


FIGURE 43. THD+N vs FREQUENCY vs TEMPERATURE, $A_V = 1, 10$, $R_L = 10k$

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Continued)

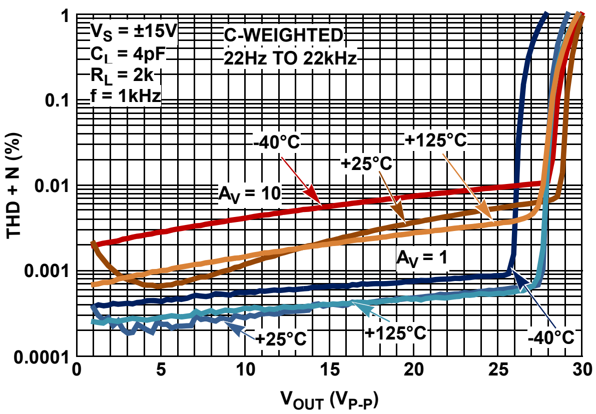


FIGURE 44. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, A_V = 1, 10, R_L = 2k

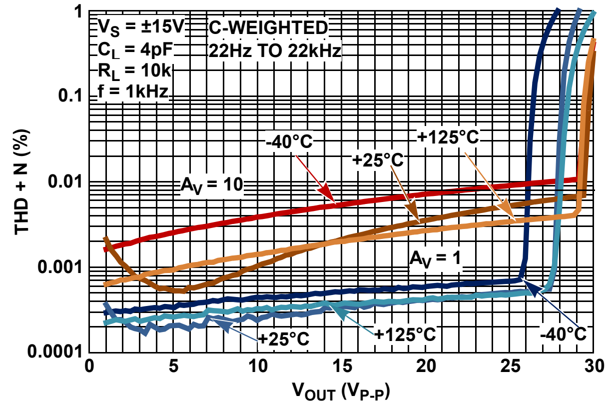


FIGURE 45. THD+N vs OUTPUT VOLTAGE (V_{OUT}) vs TEMPERATURE, A_V = 1, 10, R_L = 10k

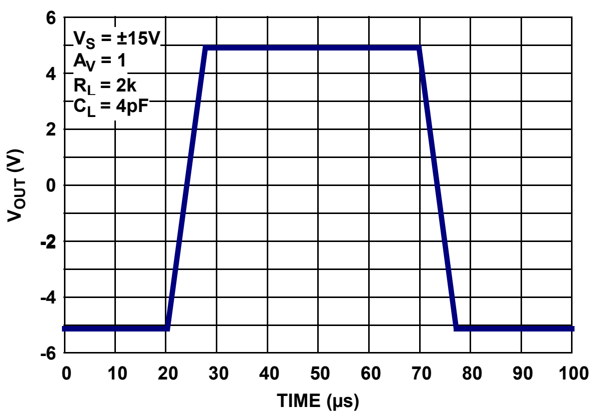


FIGURE 46. LARGE SIGNAL 10V STEP RESPONSE, V_S = ±15V

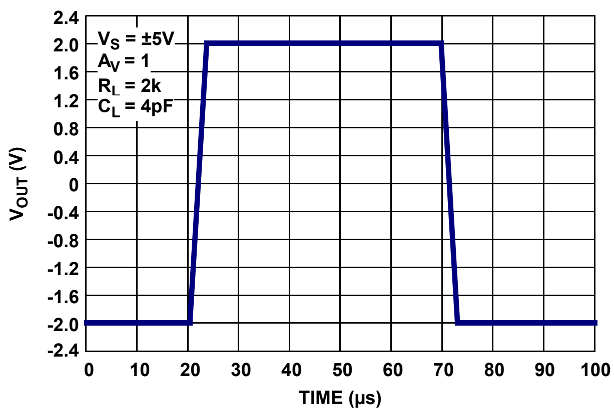


FIGURE 47. LARGE SIGNAL 4V STEP RESPONSE, V_S = ±5V

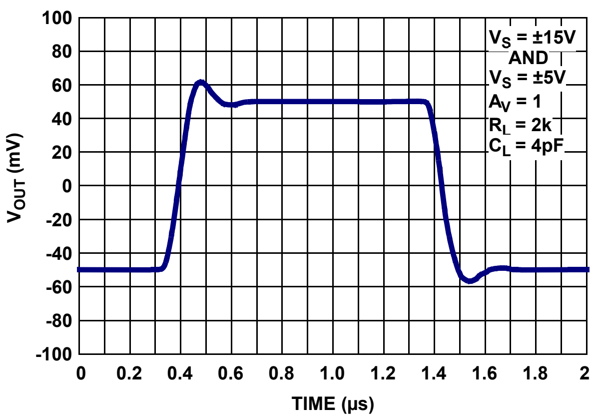


FIGURE 48. SMALL SIGNAL TRANSIENT RESPONSE, V_S = ±5V, ±15V

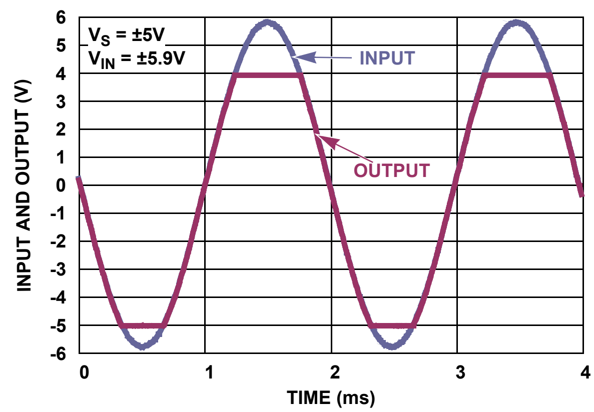


FIGURE 49. NO PHASE REVERSAL

Typical Performance Curves V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

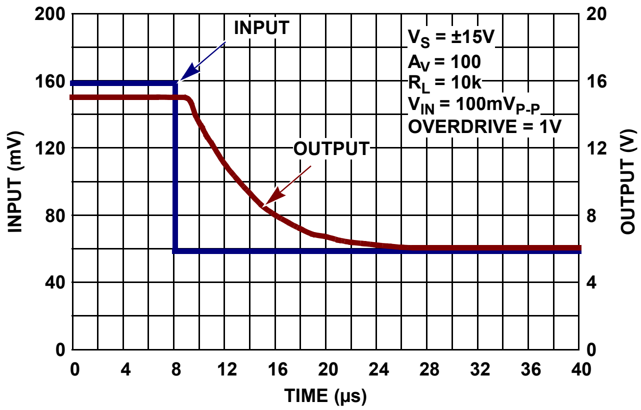


FIGURE 50. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

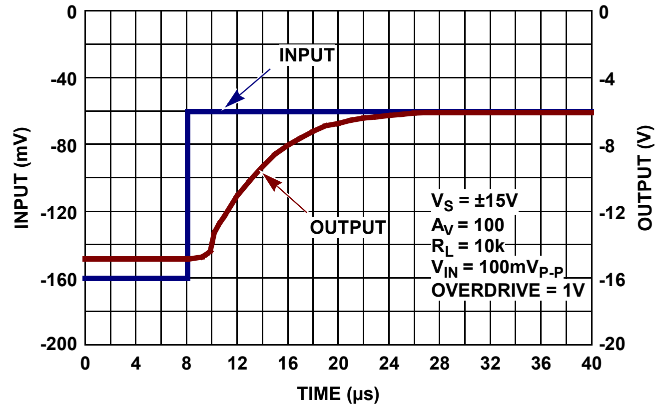


FIGURE 51. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±15V

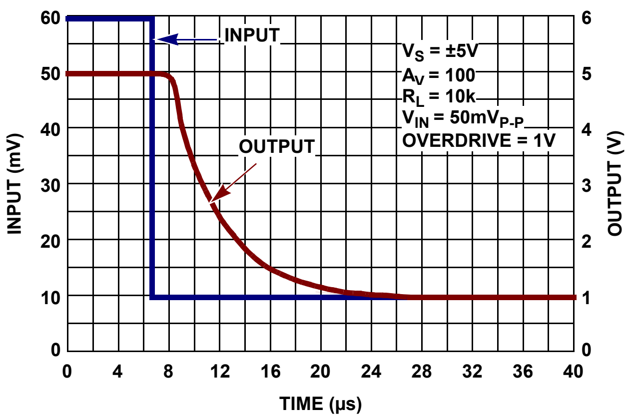


FIGURE 52. POSITIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V

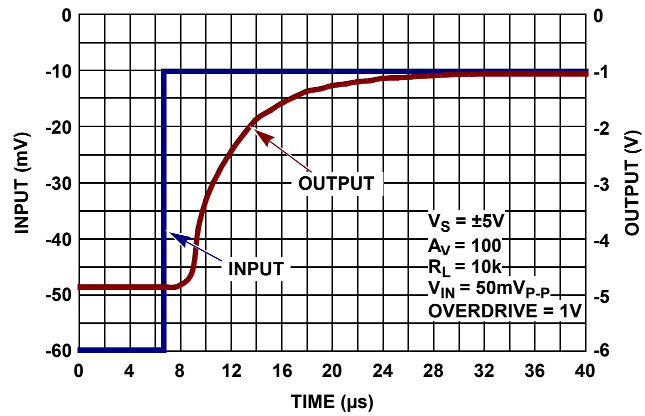


FIGURE 53. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME, V_S = ±5V

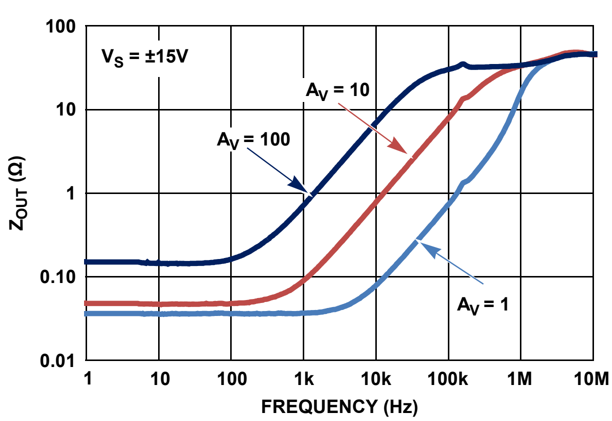


FIGURE 54. OUTPUT IMPEDANCE vs FREQUENCY, V_S = ±15V

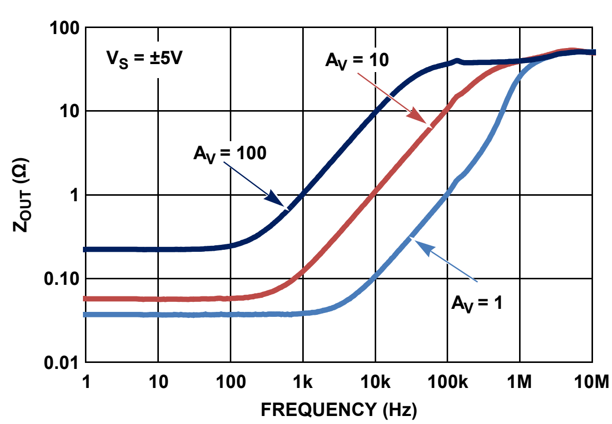


FIGURE 55. OUTPUT IMPEDANCE vs FREQUENCY, V_S = ±5V

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

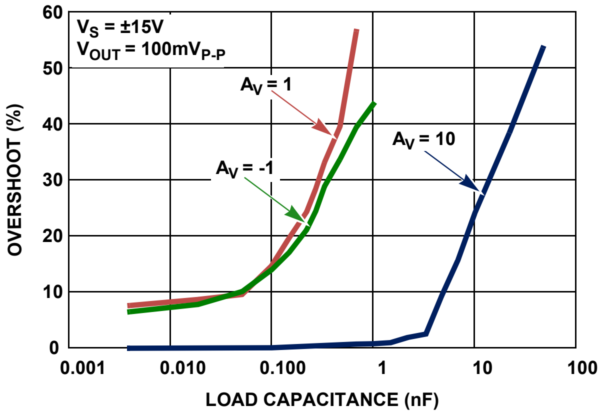


FIGURE 56. OVERSHOOT vs CAPACITIVE LOAD, V_S = ±15V

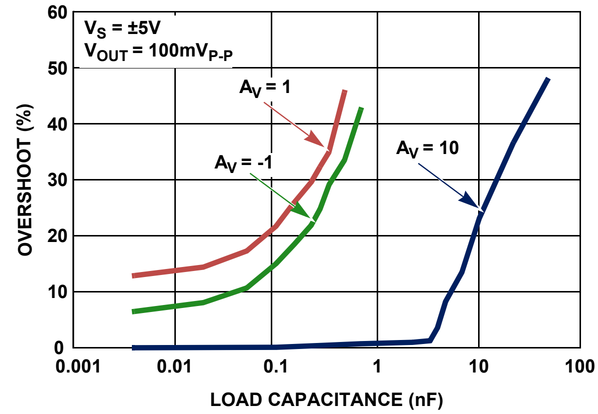


FIGURE 57. OVERSHOOT vs CAPACITIVE LOAD, V_S = ±5V

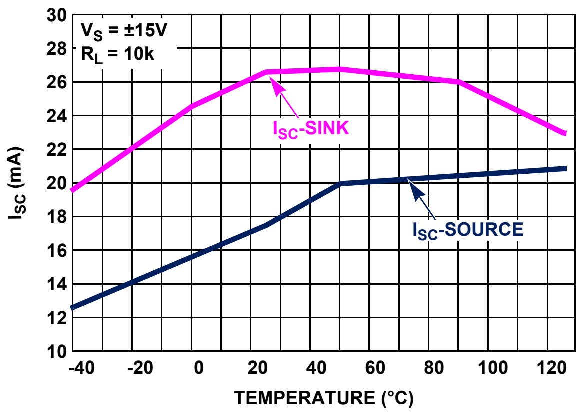


FIGURE 58. ISL28118 SHORTCIRCUIT CURRENT vs TEMPERATURE, V_S = ±15V

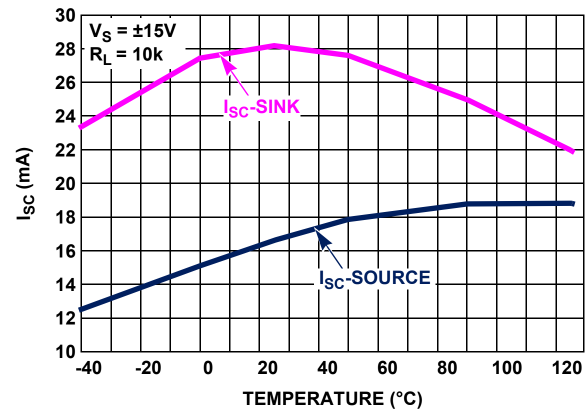


FIGURE 59. ISL28218 SHORTCIRCUIT CURRENT vs TEMPERATURE, V_S = ±15V

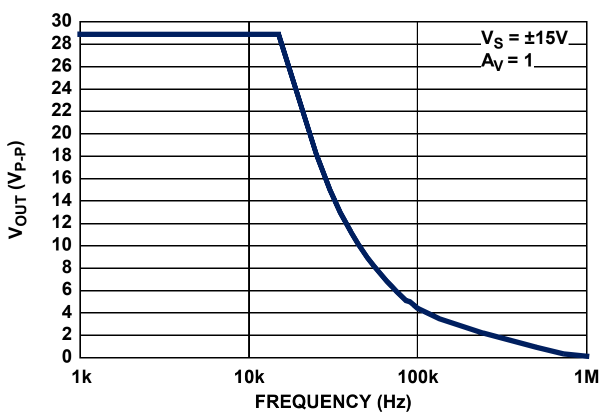


FIGURE 60. MAX OUTPUT VOLTAGE vs FREQUENCY

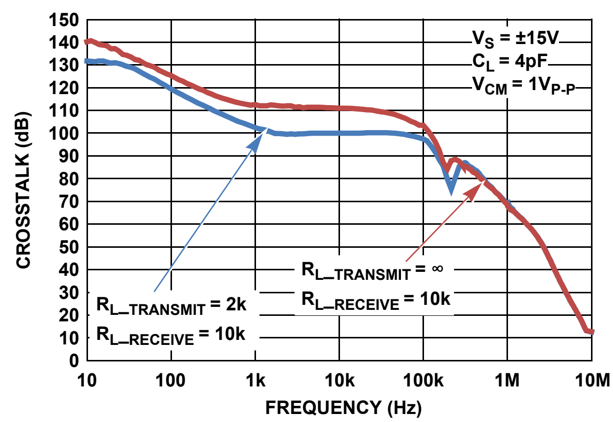


FIGURE 61. CHANNEL SEPARATION vs FREQUENCY, R_L = INF, V_S = ±15V

Applications Information

Functional Description

The ISL28118 and ISL28218 are single and dual, 3.2MHz, single-supply, rail-to-rail output amplifiers with a common mode input voltage range extending to a range of 0.5V below the V_- rail. Their input stages are optimized for precision sensing of ground-referenced signals in single-supply applications. The input stage is able to handle large input differential voltages without phase inversion, making these amplifiers suitable for high-voltage comparator applications. Their bipolar design features high open loop gain and excellent DC input and output temperature stability. These op amps feature very low quiescent current of 850µV and low temperature drift. Both devices are fabricated in a new precision 40V complementary bipolar DI process and are immune from latch-up.

Operating Voltage Range

The op amp is designed to operate over a single supply range of 3V to 40V or a split supply voltage range of +1.8V/-1.2V to ±20V. The device is fully characterized at 10V (±5V) and 30V (±15V). Both DC and AC performance remain virtually unchanged over the complete operating voltage range. Parameter variation with operating voltage is shown in the "Typical Performance Curves" on page 9.

The input common mode voltage to the V_+ rail (V_+ -1.8V over the full temperature range) may limit amplifier operation when operating from split V_+ and V_- supplies. Figure 12 on page 10 shows the common mode input voltage range variation over-temperature.

Input Stage Performance

The ISL28118 and ISL28218 PNP input stage has a common mode input range extending up to 0.5V below ground at +25°C (Figure 12). Full amplifier performance is guaranteed down for input voltage down to ground (V_-) over the -40°C to +125°C temperature range. For common mode voltages down to -0.5V below ground (V_-), the amplifiers are fully functional, but performance degrades slightly over the full temperature range. This feature provides excellent CMRR, AC performance and DC accuracy when amplifying low-level, ground-referenced signals.

The input stage has a maximum input differential voltage equal to a diode drop greater than the supply voltage (max 42V) and does not contain the back-to-back input protection diodes found on many similar amplifiers. This feature enables the device to function as a precision comparator by maintaining very high input impedance for high-voltage differential input comparator voltages. The high differential input impedance also enables the device to operate reliably in large signal pulse applications, without the need for anti-parallel clamp diodes required on MOSFET and most bipolar input stage op amps. Thus, input signal distortion caused by nonlinear clamps under high slew rate conditions is avoided.

In applications where one or both amplifier input terminals are at risk of exposure to voltages beyond the supply rails, current-limiting resistors may be needed at each input terminal (see Figure 62, $R_{IN}+$, $R_{IN}-$) to limit current through the power-supply ESD diodes to 20mA.

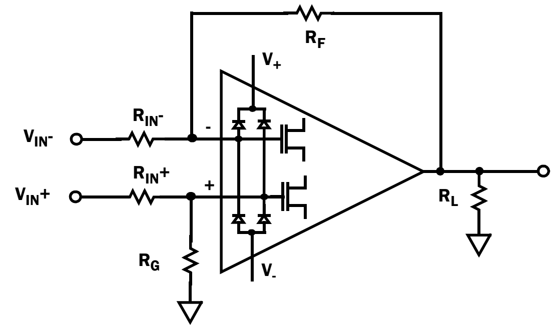


FIGURE 62. INPUT ESD DIODE CURRENT LIMITING

Output Drive Capability

The bipolar rail-to-rail output stage features low saturation levels that enable an output voltage swing to less than 15mV when the total output load (including feedback resistance) is held below 50µA (Figures 31 and 32). With ±15V supplies, this can be achieved by using feedback resistor values >300kΩ.

The output stage is internally current limited. Output current limit over-temperature is shown in Figures 33 and 34. The amplifiers can withstand a short-circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only one amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long-term reliability.

The amplifiers perform well when driving capacitive loads (Figures 56 and 57). The unity gain, voltage follower (buffer) configuration provides the highest bandwidth but is also the most sensitive to ringing produced by load capacitance found in BNC cables. Unity gain overshoot is limited to 35% at capacitance values to 0.33nF. At gains of 10 and higher, the device is capable of driving more than 10nF without significant overshoot.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28118 and ISL28218 are immune to output phase reversal out to 0.5V beyond the rail ($V_{ABS\ MAX}$) limit (Figure 49).

Single Channel Usage

The ISL28218 is a dual op amp. If the application requires only one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel oscillates if the input and output pins are floating. This results in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent oscillation is to short the output to the inverting input and ground the positive input (Figure 63).

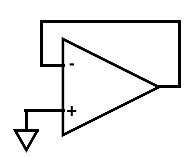


FIGURE 63. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

Where

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package

PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

Where

- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of one amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

ISL28118 and ISL28218 SPICE Model

Figure 64 on page 21 shows the SPICE model schematic and Figure 65 on page 22 shows the net list for the SPICE model. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise voltage, slew rate, CMRR and gain and phase. The DC parameters are I_{OS}, total supply current and output voltage swing. The model uses typical parameters given in the “Electrical Specifications” table beginning on page 5. The AVOL is adjusted for 136dB with the dominant pole at 0.6Hz. The CMRR is set at 120dB, f = 50kHz. The input stage models the actual device to present an accurate AC representation. The model is configured for an ambient temperature of +25°C.

Figures 66 through 80 show the characterization vs simulation results for the noise voltage, open loop gain phase, closed loop gain vs frequency, gain vs frequency vs R_L, CMRR, large signal 10V step response, small signal 0.1V step and output voltage swing ±15V supplies.

LICENSE STATEMENT

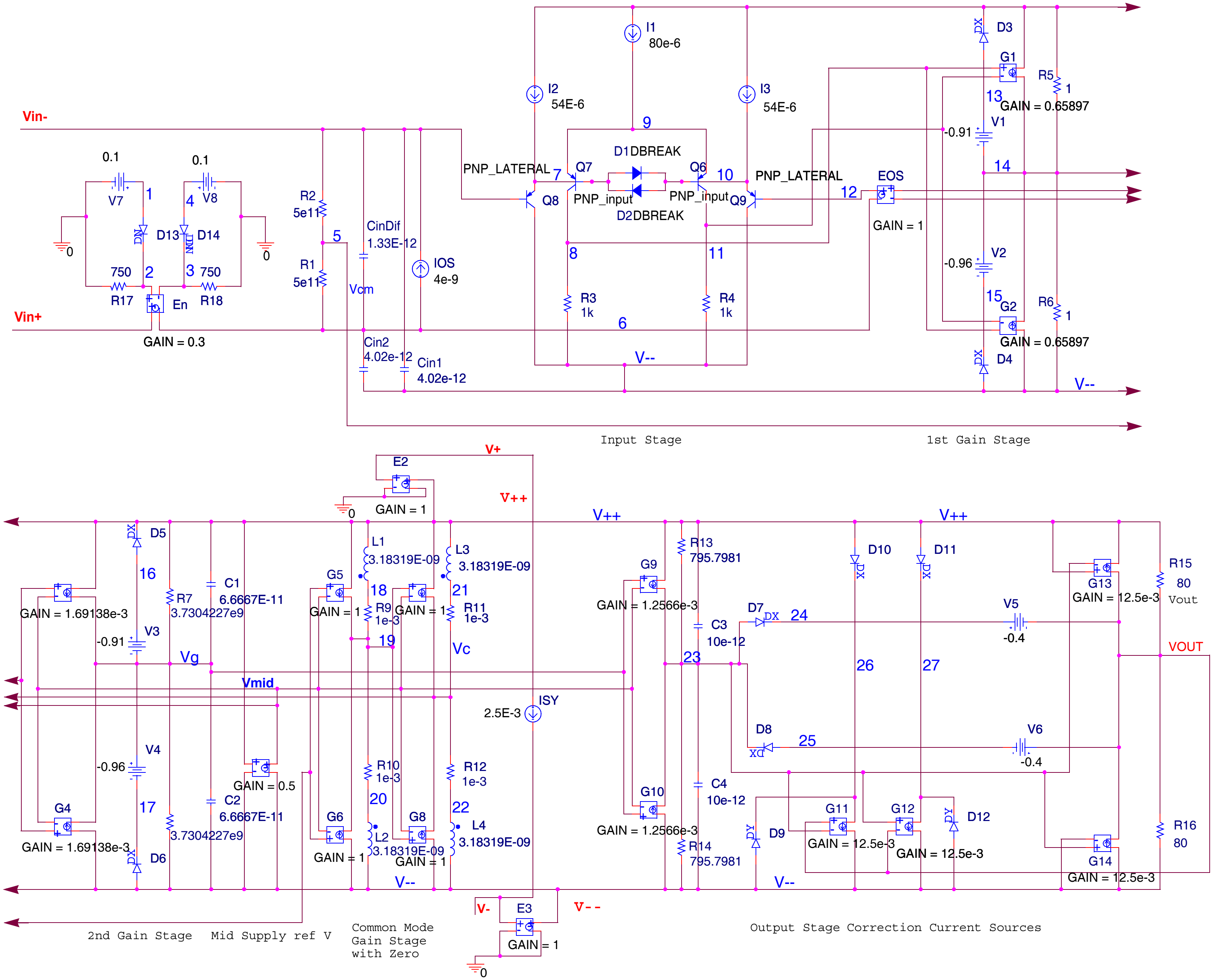


FIGURE 64. SPICE SCHEMATIC

```
*ISL28118_218 Macromodel - covers following *products
*ISL28118
*ISL28218
*
*Revision History:
* Revision B, LaFontaine January 22 2014
* Model for Noise, supply currents, CMRR
*120dB f = 40kHz, AVOL 136dB f = 0.5Hz
* SR = 1.2V/us, GBWP 4MHz.
*Copyright 2011 by Intersil Corporation
*Refer to data sheet "LICENSE STATEMENT"
*Use of this model indicates your acceptance
*with the terms and provisions in the License
*Statement.
*
*Intended use:
*This Pspice Macromodel is intended to give
*typical DC and AC performance characteristics *under a wide range of external circuit *configurations using compatible simulation *platforms – such as iSim PE.
*
*Device performance features supported by this *model:
*Typical, room temp., nominal power supply
*voltages used to produce the following
*characteristics:
*Open and closed loop I/O impedances,
*Open loop gain and phase,
*Closed loop bandwidth and frequency
*response,
*Loading effects on closed loop frequency
*response,
*Input noise terms including 1/f effects,
*Slew rate,
*Input and Output Headroom limits to I/O
*voltage swing,
*Supply current at nominal specified supply
*voltages,
*
*Device performance features NOT supported *by this model:
*Harmonic distortion effects,
*Output current limiting (current will limit at
*40mA),
*Disable operation (if any),
*Thermal effects and/or over-temperature
*parameter variation,
*Limited performance variation vs. supply
*voltage is modeled,
*Part to part performance variation due to
*normal process parameter spread,
*Any performance difference arising from
*different packaging,
*Load current reflected into the power supply
*current.

* source ISL28118_218 SPICEmodel
*
* Connections:        +input
*                      |    -input
*                      |    |    +Vsupply
*                      |    |    |    -Vsupply
*                      |    |    |    |    output
.subckt ISL28118_218  Vin+ Vin-V+ V- VOUT
* source ISL28118_218_presubckt_0
*
*Voltage Noise
E_En        VIN+ 6 2 0 0.3
D_D13       1 2 DN
D_D14       1 2 DN
V_V7        1 0 0.1
V_V8        4 0 0.1
R_R17       2 0  750
*R_R18      3 0  750
*
*Input Stage
Q_Q6        11 10 9 PNP_input
Q_Q7        8 7 9 PNP_input
Q_Q8        V-- VIN- 7 PNP_LATERAL
Q_Q9        V-- 12 10 PNP_LATERAL
I_I1        V++ 9 DC 80e-6
I_I2        V++ 7 DC 54E-6
I_I3        V++ 10 DC 54E-6
I_IOS       6 VIN- DC 4e-9
D_D1        7 10 DBREAK
D_D2        10 7 DBREAK
R_R1        5 6  5e11
R_R2        VIN- 5  5e11
R_R3        V-- 8  1000
R_R4        V-- 11  1000
C_Cin1      V-- VIN-  4.02e-12
C_Cin2      V-- 6  4.02e-12
C_CinDif    6 VIN-  1.33E-12
*
*1st Gain Stage
G_G1        V++ 14 8 11 0.65897
G_G2        V-- 14 8 11 0.65897
V_V1        13 14 -0.91
V_V2        14 15 -0.96
D_D3        13 V++ DX
D_D4        V-- 15 DX
R_R5        14 V++  1
R_R6        V-- 14  1
*
*2nd Gain Stage
G_G3        V++ VG 14 VMID 1.69138e-3
G_G4        V-- VG 14 VMID 1.69138e-3
V_V3        16 VG -0.91
V_V4        VG 17 -0.96
D_D5        16 V++ DX
D_D6        V-- 17 DX
R_R7        VG V++  3.7304227e9
R_R8        V-- VG  3.7304227e9
C_C1        VG V++  6.6667E-11
C_C2        V-- VG  6.6667E-11
*
*Mid supply Ref
E_E2        V++ 0 V+ 0 1
E_E3        V-- 0 V- 0 1
E_E4        VMID V-- V++ V-- 0.5
I_ISY       V+ V- DC 0.85E-3
*
*Common Mode Gain Stage with Zero
G_G5        V++ 19 5 VMID 1
G_G6        V-- 19 5 VMID 1
G_G7        V++ VC 19 VMID 1
G_G8        V-- VC 19 VMID 1
E_EOS       12 6 VC VMID 1
L_L1        18 V++  3.18319E-09
L_L2        20 V--  3.18319E-09
L_L3        21 V++  3.18319E-09
L_L4        22 V--  3.18319E-09
R_R9        19 18  1e-3
R_R10       20 19  1e-3
R_R11       VC 21  1e-3
R_R12       22 VC  1e-3
*
*Pole Stage
G_G9        V++ 23 VG VMID 1.2566e-3
G_G10       V-- 23 VG VMID 1.2566e-3
R_R13       23 V++  795.7981
R_R14       V-- 23  795.7981
C_C3        23 V++  10e-12
C_C4        V-- 23  10e-12
*
*Output Stage with Correction Current Sources
G_G11       26 V-- VOUT 23 12.5e-3
G_G12       27 V-- 23 VOUT 12.5e-3
G_G13       VOUT V++ V++ 23 12.5e-3
G_G14       V-- VOUT 23 V-- 12.5e-3
D_D7        23 24 DX
D_D8        25 23 DX
D_D9        V-- 26 DY
D_D10       V++ 26 DX
D_D11       V++ 27 DX
D_D12       V-- 27 DY
V_V5        24 VOUT -0.4
V_V6        VOUT 25 -0.4
R_R15       VOUT V++  80
R_R16       V-- VOUT  80
.model PNP_LATERAL pnp(is=1e-016 bf=250 va=80
+ ik=0.138 rb=0.01 re=0.101 rc=180 kf=0 af=1)
.model PNP_input pnp(is=1e-016 bf=100 va=80
+ ik=0.138 rb=0.01 re=0.101 rc=180 kf=0 af=1)
.model DBREAK D(bv=43 rs=1)
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends ISL28118_218
```

FIGURE 65. SPICE NET LIST

Characterization vs Simulation Results

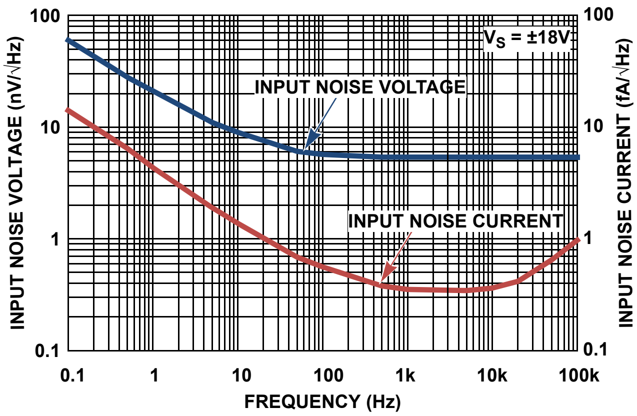


FIGURE 66. CHARACTERIZED INPUT NOISE VOLTAGE

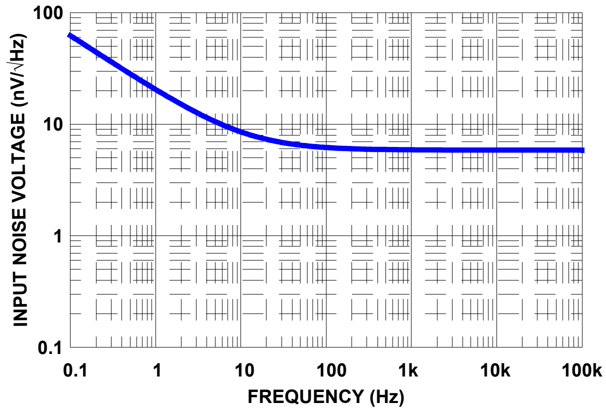


FIGURE 67. SIMULATED INPUT NOISE VOLTAGE

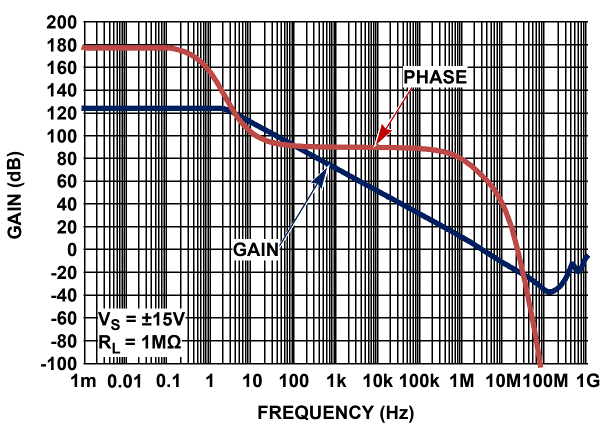


FIGURE 68. CHARACTERIZED OPEN-LOOP GAIN, PHASE vs FREQUENCY

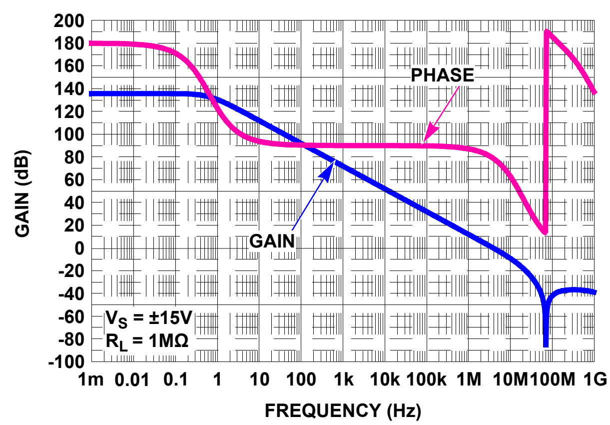


FIGURE 69. SIMULATED OPEN-LOOP GAIN, PHASE vs FREQUENCY

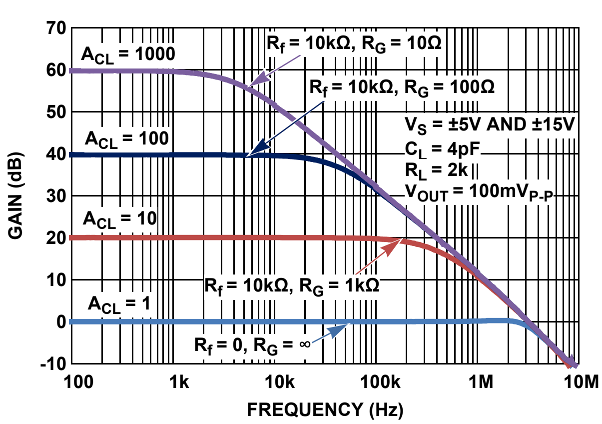


FIGURE 70. CHARACTERIZED CLOSED-LOOP GAIN vs FREQUENCY

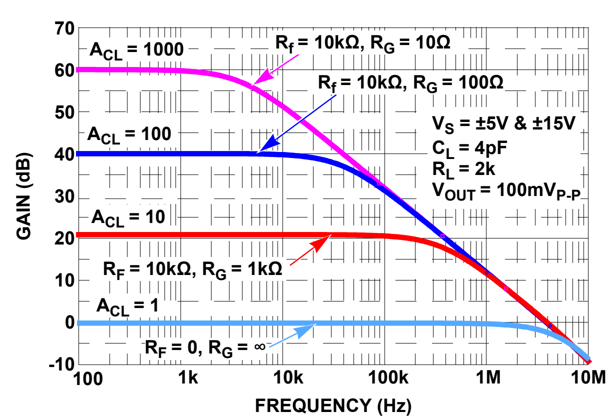


FIGURE 71. SIMULATED CLOSED-LOOP GAIN vs FREQUENCY

Characterization vs Simulation Results (Continued)

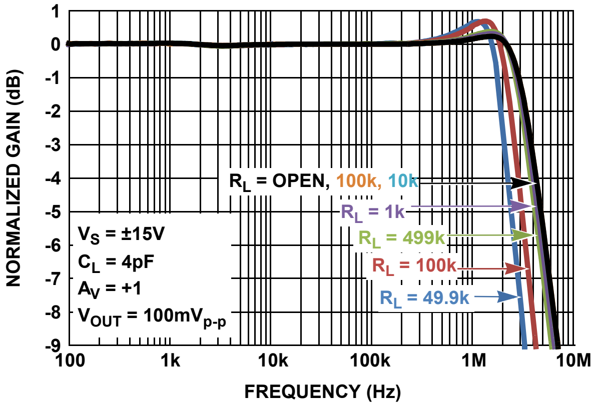


FIGURE 72. CHARACTERIZED GAIN vs FREQUENCY vs R_L

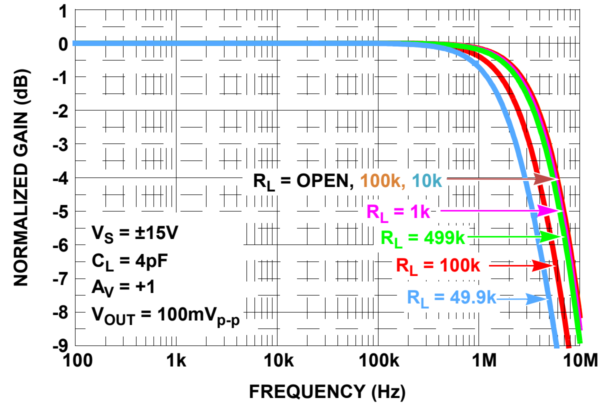


FIGURE 73. SIMULATED GAIN vs FREQUENCY vs R_L

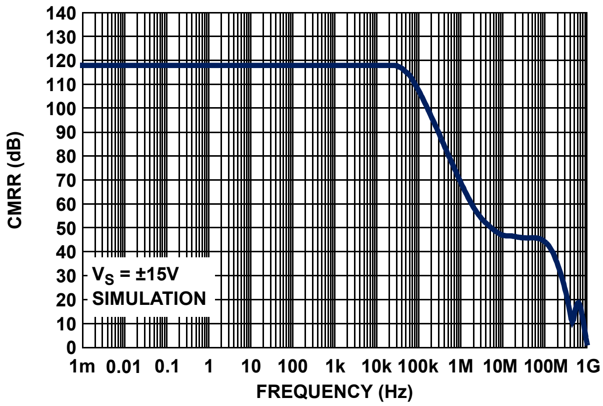


FIGURE 74. CHARACTERIZED CMRR vs FREQUENCY

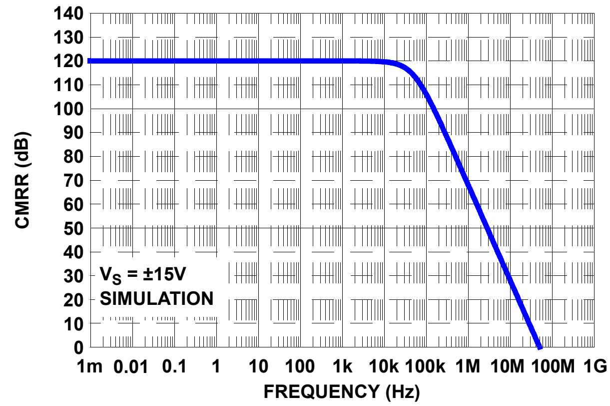


FIGURE 75. SIMULATED CMRR vs FREQUENCY

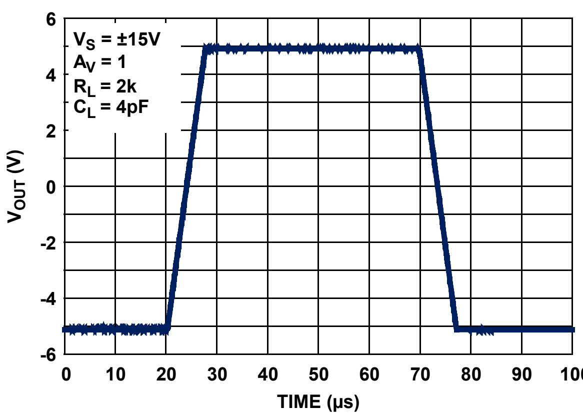


FIGURE 76. CHARACTERIZED LARGE-SIGNAL 10V STEP RESPONSE

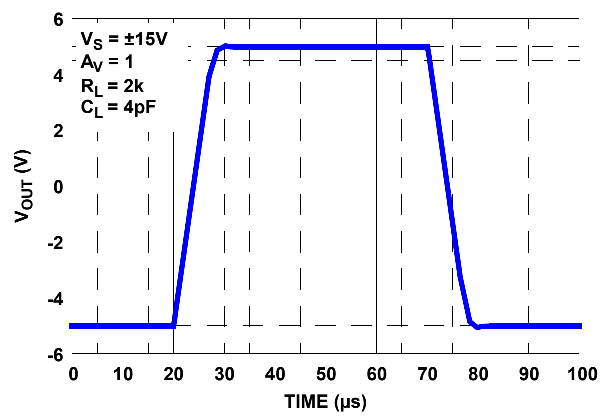


FIGURE 77. SIMULATED LARGE-SIGNAL 10V STEP RESPONSE

Characterization vs Simulation Results (Continued)

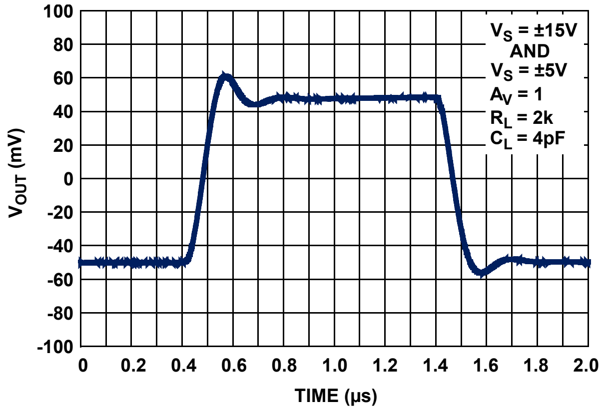


FIGURE 78. CHARACTERIZED SMALL-SIGNAL TRANSIENT RESPONSE

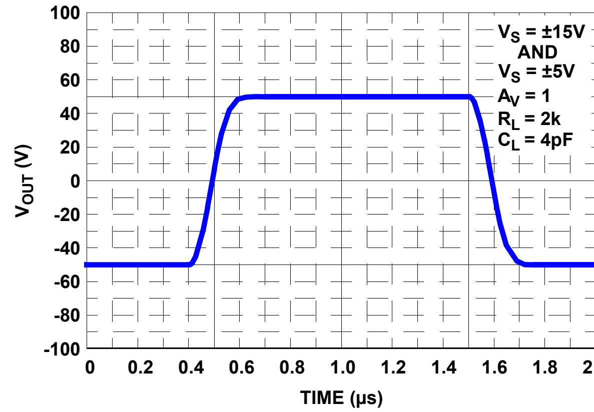


FIGURE 79. SIMULATED SMALL-SIGNAL TRANSIENT RESPONSE

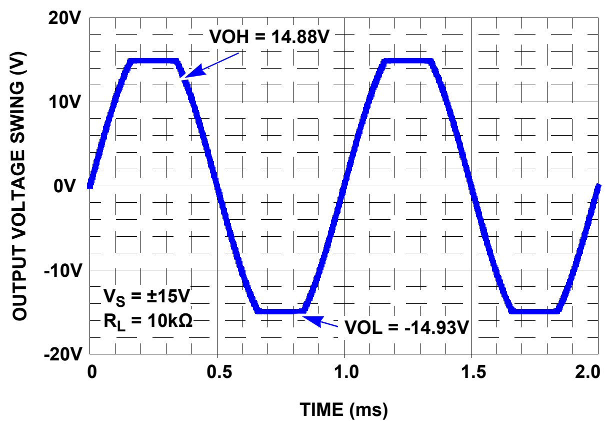


FIGURE 80. SIMULATED OUTPUT VOLTAGE SWING

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
July 27, 2015	FN7532.7	Page 1 under Features: Removed bullet 3 (Rail-to-rail input differential voltage range for comparator application). Added to the end of bullet 2 "ground sensing".
July 15, 2015	FN7532.6	Figures 48 and 78 changed Y-axis from (V) to (mV).
May 1, 2014	FN7532.5	Updated Spice model netlist on page 22. Absolute Maximum Ratings table on page 5: Added ESD Tolerance (ISL28118 SOIC package only). Changed POD: FROM M8.118: Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36" To M8.118B: Correct lead dimension in side view 2 from 0.15 - 0.05mm to 0.15+/-0.05mm.
January 24, 2013	FN7532.4	Added ISL28218 MSOP specifications, and removed references to ISL28118 and ISL28218 TDFN options. page 1: Removed “8 Ld TDFN” from last paragraph of description. page 3: Removed TDFN “Pin Configurations”, and TDFN columns and the “PAD” row from “Pin Descr” table. Moved Ordering Information table from pg 3 to page 2. Removed “Coming Soon” from ISL28218FUZ and added “Note 1” reference, and deleted 2 TDFN offerings in “Ordering Info” table. page 5: Removed TDFN entries from “Thermal Resistance” section, and removed notes 5 and 6. Added delta Vos MSOP row, with limits of ±390µA, and added “ISL28218” to the CMRR MSOP entry. page 6: added “ISL28218” to the existing AVOL MSOP entry. page 7: added new +25°C 28218 MSOP row with 107dB min limit, and added “ISL28218 MSOP” to the existing ISL28118 MSOP full temp row for PSRR. page 7: added “ISL28218” to the existing CMRR SOIC and MSOP rows, and deleted the “ISL28218” rows. page 7: added “ISL28218 MSOP” to the existing ISL28118 MSOP rows for AVOL. page 9: added “+25°C” to “default conditions” info at top of page. Moved “sales Info” from p25 to p23. Removed TDFN package outline drawing.
August 31, 2011	FN7532.3	Page 7: Electrical Spec Table for Supply Current/Amplifier Change from: 1.4µA Full Temp Max Change to: 1.4mA Full Temp Max Page 28: Updated POD M8.118 to current revision. Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36".
May 9, 2011	FN7532.2	Page 2: Added NC pin to Pin Descriptions table. Page 3: Added ISL28218EVAL1Z evaluation board to the Ordering Information table. Page 12: Added new Output Overhead Voltage plots (Figs. 31,32) Pages 19 through 24: Added SPICE model schematic, netlist, description and Figs. 66 through 80.
November 12, 2010	FN7532.1	On page 1: Features Section, added Low input offset voltage and superb offset voltage temperature drift for ISL28118. Updated Intersil trademark statement (bottom of page) On page 4: Removed “coming soon” from ISL28118FBZ. Updated tape & reel note. On page 5: Change ISL28118 Theta JA value from 158 to 165. Added ISL28118 min/max specs to VOS (input offset voltage), TCVOS and min specs to CMRR. On page 6: Added AVOL MIN spec for ISL28118 in dB. Changed existing AVOL spec from V/mV to dB. Added VOL max spec for ISL28118, IS Typ and Max spec for ISL28118. Changed TS from 18µs to 8.5µs. On page 7: Added Min Max VOS spec, TCVOS spec for ISL28118. Changed AVOL specs from V/mV to dB. On page 8: Changed Slew Rate TYP from ±1.2V/µs to ±1V/µs. Added for TS TYP spec = 4µs. Changed min/max note 6 to “Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.” Added Figs 3 & 4 for ISL28118. Figures 5 & 6 moved to page 9. On page 9: Added Figures 7 & 8 On page 11: Added Figures 15 & 16 for ISL28118 On page 11, in Figure 19, changed VS from ±5V to ±15V On page 13 and page 14: Added Figures 27, 28, 31 & 34 for ISL28118 On page 14: Added Figure 35 for ISL28118 On page 15: Figure 41 changed VS from ±18V to ±5V, Figure 42 added RL = 2k, Figure 43 added RL = 10k and corrected "HD+N" to "THD+N" On page 16, Figure 44 added RL = 2k, Figure 45 RL = 10k. On page 18: Added Figure 58 for ISL28118 On page 18, Figure 58 and 59, graph upper left corner changed VS = ±5V to VS = ±15V On page 18, Figure 61, deleted VS = ±5V
September 16, 2010	FN7532.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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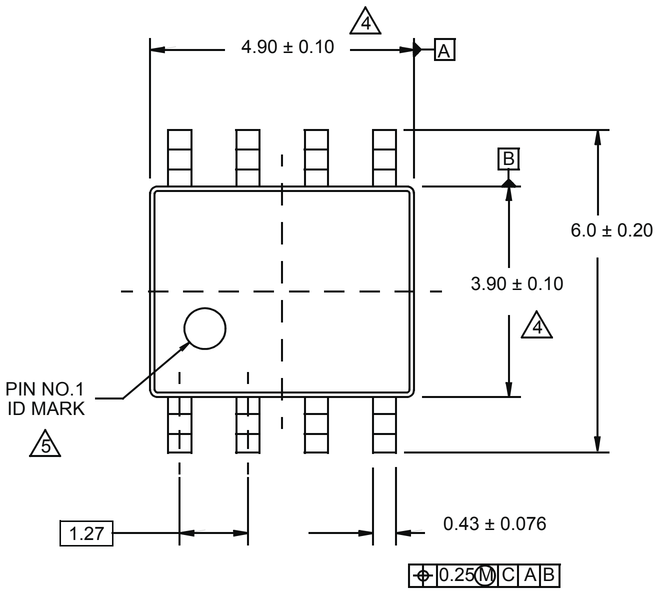
Package Outline Drawing

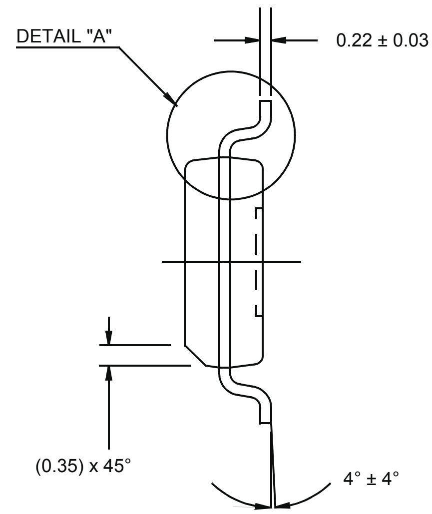
M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

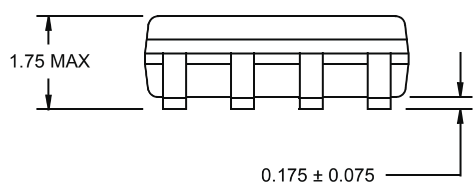
Rev 0, 08/09



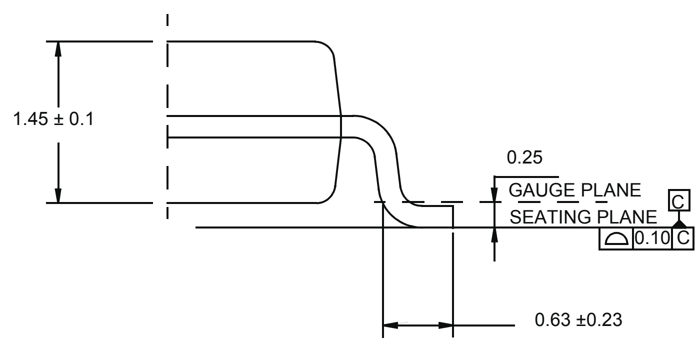
TOP VIEW



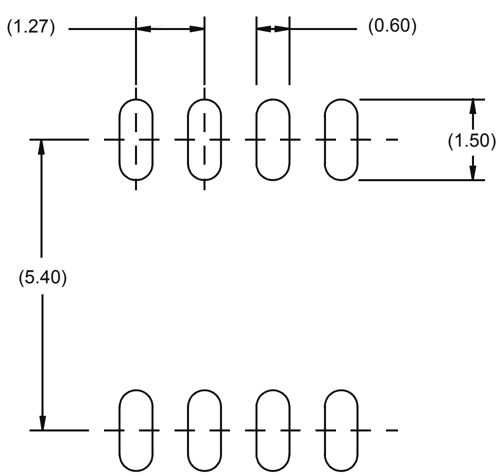
SIDE VIEW “B”



SIDE VIEW “A



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

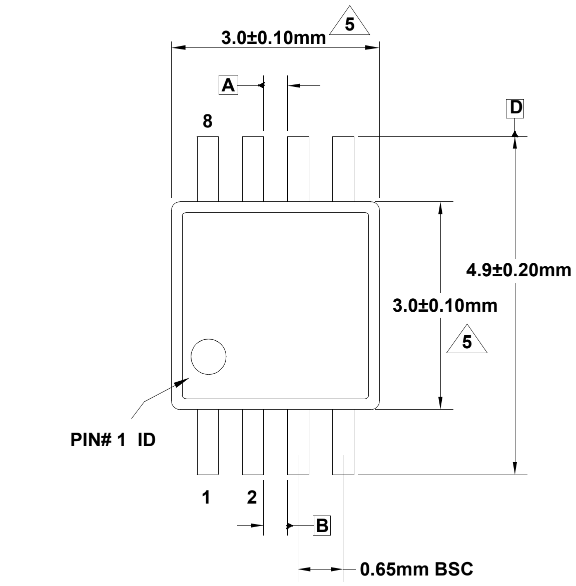
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Package Outline Drawing

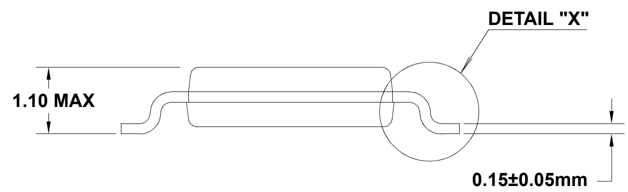
M8.118B

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

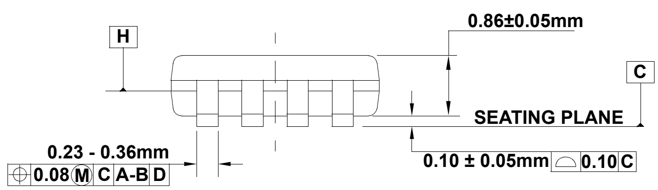
Rev 1, 3/12



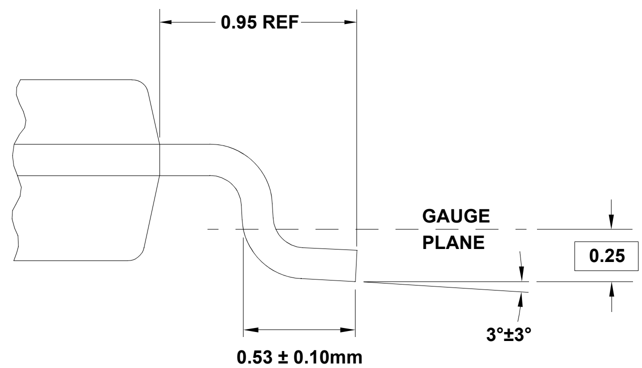
TOP VIEW



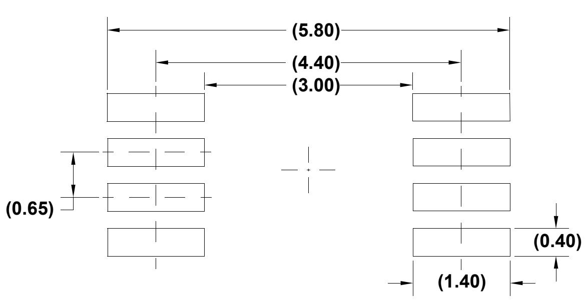
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.