## SN54ABTH16244, SN74ABTH16244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

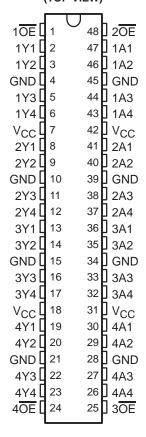
SCBS677D - SEPTEMBER 1996 - REVISED MARCH 2000

- **Members of the Texas Instruments** Widebus™ Family
- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical V<sub>OLP</sub> (Output Ground Bounce) <1 V at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$
- Distributed V<sub>CC</sub> and GND Pins Minimize **High-Speed Switching Noise**
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA I<sub>OH</sub>, 64-mA I<sub>OL</sub>)
- Bus Hold on Data Inputs Eliminates the **Need for External Pullup/Pulldown** Resistors
- **ESD Protection Exceeds 2000 V Per** MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- **Package Options Include Plastic Shrink** Small-Outline (DL), Thin Shrink Small-Outline (DGG), Thin Very Small-Outline (DGV) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages

#### description

The 'ABTH16244 devices are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide true outputs and symmetrical active-low output-enable (OE) inputs.

SN54ABTH16244 . . . WD PACKAGE SN74ABTH16244...DGG, DGV, OR DL PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH16244 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ABTH16244 is characterized for operation from -40°C to 85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

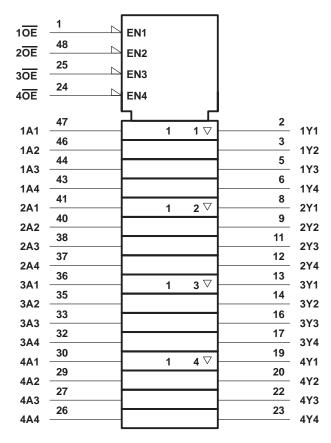
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# FUNCTION TABLE (each buffer)

INPU	JTS	OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

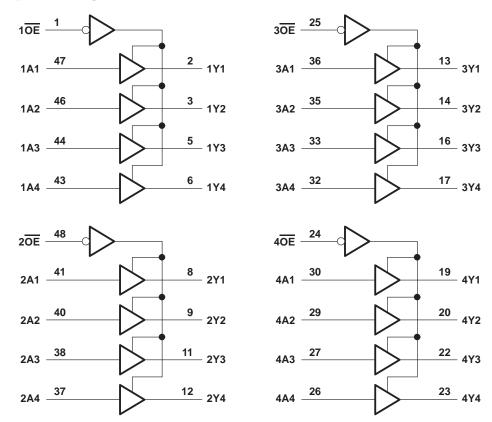
# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



### logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high or power	r-off state, V <sub>O</sub> –0.5 V to 5.5 V
Current into any output in the low state, IO: SN54ABTH	l16244 96 mA
SN74ABTH	l16244 128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–18 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Package thermal impedance, θ <sub>.IA</sub> (see Note 2): DGG p	ackage 70°C/W
DGV p	ackage 58°C/W
DL pad	kage 63°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51.



# SN54ABTH16244, SN74ABTH16244 **16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS**

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### recommended operating conditions (see Note 3)

			SN54ABT	H16244	SN74ABTI	H16244	UNIT
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2		2		V	
VIL	Low-level input voltage		0.8		0.8	V	
VI	Input voltage		0	Vcc	0	Vcc	V
ЮН	High-level output current			-24		-32	mA
loL	Low-level output current		48		64	mA	
Δt/Δν	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
TA	Operating free-air temperature	•	<b>–</b> 55	125	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

BABAMETER		AND TIONS	Т	A = 25°C	;	SN54ABT	H16244	SN74ABTI		
PARAMETER	IESI C	ONDITIONS	MIN	TYP <sup>†</sup>	MAX	MIN	MAX	MIN	MAX	UNIT
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V
	$V_{CC} = 4.5 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.5			2.5		2.5		
Vari	$V_{CC} = 5 V$ ,	$I_{OH} = -3 \text{ mA}$	3			3		3		V
VOH	V <sub>CC</sub> = 4.5 V	$I_{OH} = -24 \text{ mA}$	2			2				V
	VCC = 4.5 V	$I_{OH} = -32 \text{ mA}$	2*					2		
Voi	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA			0.55		0.55			V
VOL	VCC = 4.5 V	I <sub>OL</sub> = 64 mA			0.55*				0.55	V
V <sub>hys</sub>	T			100						mV
lį	$V_{CC} = 5.5 \text{ V},$	$V_I = V_{CC}$ or GND			±1		±1		±1	μΑ
lin in	V 45V	V <sub>I</sub> = 0.8 V	100			100		100		
l(hold)	V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 2 V	-40			-40		-40		μΑ
lozh	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.7 V			10		10		10	μА
lozL	$V_{CC} = 5.5 \text{ V},$	V <sub>O</sub> = 0.5 V			-10		-10		-10	μА
l <sub>off</sub>	$V_{CC} = 0$ ,	$V_I$ or $V_O \le 4.5 \text{ V}$			±100				±100	μΑ
ICEX	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high			50		50		50	μΑ
IO <sup>‡</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
	V <sub>CC</sub> = 5.5 V,	Outputs high			3		3		3	
l <sub>CC</sub>	$I_{O} = 0$ ,	Outputs low			32		32		32	mA
	$V_I = V_{CC}$ or GND	Outputs disabled			3		3		3	
ΔlCC§	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA
Ci	V <sub>I</sub> = 2.5 V or 0.5 V		3						pF	
Co	V <sub>O</sub> = 2.5 V or 0.5 V			8						pF

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter does not apply.



<sup>†</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ .

<sup>‡</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

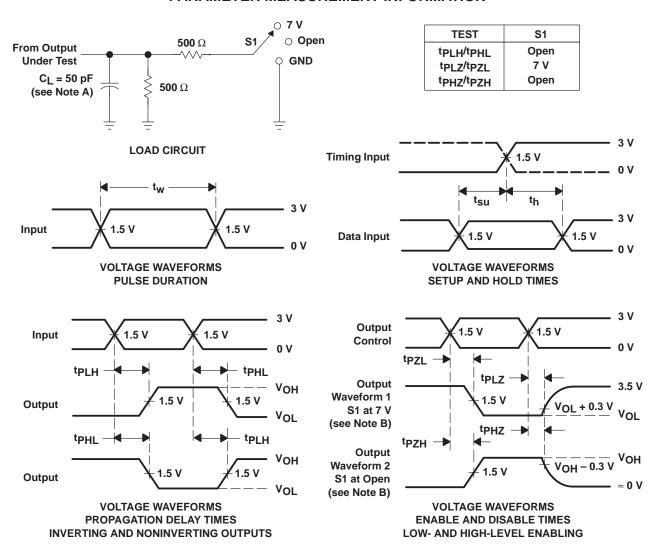
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# switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V( T)	CC = 5 V 4 = 25°C	<u>',</u>	SN54ABTI	H16244	SN74ABTI	H16244	UNIT
	(1141 01)	(0011-01)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	А	V	1	2.3	3.2	0.7	3.6	1	3.5	20
t <sub>PHL</sub>	A	Ť	1	2.6	3.7	0.5	4.2	1	4.1	ns
<sup>t</sup> PZH	ŌĒ	<b>V</b>	1	3	3.8	0.7	4.9	1	4.8	20
tPZL	OE	ī	1	3.2	4	0.9	5.3	1	4.8	ns
<sup>t</sup> PHZ	ŌĒ	V	1	3.6	4.4	0.7	5.3	1	4.8	20
tPLZ	OE OE	Ť	1	2.9	3.7	1	4.6	1	4.1	ns

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50~\Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







6-Feb-2020

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABTH16244DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16244	Samples
SN74ABTH16244DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16244	Samples
SN74ABTH16244DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16244	Samples
SN74ABTH16244DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH16244	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## **PACKAGE OPTION ADDENDUM**

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## PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABTH16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH16244DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABTH16244DLR	SSOP	DL	48	1000	367.0	367.0	55.0

# DL (R-PDSO-G48)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

#### **48 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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