

Switch-mode Power Rectifier

MUR550APFG, MURD550PFG, MUR550PFG, MURF550PFG, NRVUD550PFT4G, NRVUD550PFT4G-VF01

These state-of-the-art devices are designed for power factor correction in discontinuous and critical conduction mode.

Features

- 520 V Rating Meets 80% Derating Requirements of Major OEMs
- Low Forward Voltage Drop
- Low Leakage
- Ultrafast 95 Nanosecond Recovery Time
- Reduces Forward Conduction Loss
- NRVUD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DCM PFC Designs
- Switching Power Supplies
- Power Inverters

Mechanical Characteristics:

- Case: Epoxy, Molded
- Epoxy Meets UL 94 V-0 @ 0.125 in
- Weight: MUR550APFG: 1.1 Gram (Approximately)
MURD550PFG, NRVUD550PFT4G,
NRVUD550PFT4G-VF01: 0.4 Gram
(Approximately)
MUR550PFG, MURF550PFG: 1.9 Gram
(Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead and Mounting Surface Temperature for Soldering Purposes: 260°C Max. for 10 Seconds

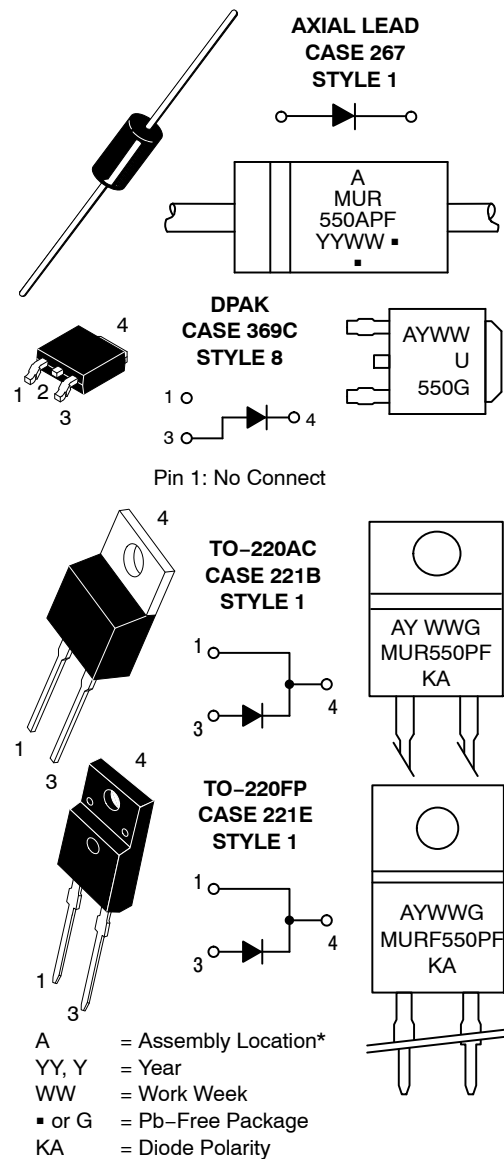


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ULTRAFAST RECTIFIER 5.0 AMPERES, 520 VOLTS

MARKING DIAGRAMS



*The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejector pin), the front side assembly code may be blank.

(Note: Microdot may be in either location)

MUR550APFG, MURD550PFG, MUR550PFG, MURF550PFG, NRVUD550PFT4G,

ORDERING INFORMATION

Device	Package	Shipping†
MUR550APFG	Axial	500 Units/Bag
MUR550APFRLG	Axial	1,500 Tape & Reel
MURD550PFT4G	DPAK (Pb-Free)	2,500 Tape & Reel
NRVUD550PFT4G*	DPAK (Pb-Free)	2,500 Tape & Reel
NRVUD550PFT4G-VF01*	DPAK (Pb-Free)	50 Units / Rail
MUR550PFG	TO-220AC (Pb-Free)	50 Units / Rail
MURF550PFG	TO-220FP (Pb-Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*NRVUD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	520	V
Average Rectified Forward Current (Rated V_R) $T_C = 65^\circ\text{C}$ (Rated V_R) $T_C = 160^\circ\text{C}$ MUR550APFG, NRVUD550PFT4G-VF01 MURD550PFG, NRVUD550PFT4G, MUR550PFG, MURF550PFG	$I_{F(AV)}$	5.0 5.0	A
Non-Repetitive Peak Surge Current (Surge Applied at Rated Load Conditions Halfwave, 60 Hz) MUR550APFG NRVUD550PFT4G, NRVUD550PFT4G-VF01, MURD550PFG MUR550PFG, MURF550PFG	I_{FSM}	85 75 100	A
Operating Junction Temperature Range	T_J	-65 to +175	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +175	$^\circ\text{C}$
ESD Ratings: Machine Model = C Human Body Model = 3B	ESD	> 400 > 8000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 1) MURD550PFG, MUR550PFG, NRVUD550PFT4G, NRVUD550PFT4G-VF01 MURF550PFG	$R_{\theta JC}$	2.8 5.75	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient MUR550APFG NRVUD550PFT4G, NRVUD550PFT4G-VF01, MURD550PFG (Note 3), MURF550PFG	$R_{\theta JA}$	Note 2 62 75	$^\circ\text{C/W}$

1. Rating applies when surface mounted on the minimum pad sizes recommended.
2. See Note 2, Ambient Mounting Data.
3. 1 inch square pad size on FR4 board.

MUR550APFG, MURD550PFG, MUR550PFG, MURF550PFG, NRVUD550PFT4G,

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Maximum Instantaneous Forward Voltage Drop (Note 4) ($I_F = 5.0\text{ A}$, $T_J = 25^\circ\text{C}$) ($I_F = 5.0\text{ A}$, $T_J = 150^\circ\text{C}$)	V_F	1.15 0.98	V
Maximum Instantaneous Reverse Current (Note 4) ($V_R = 520\text{ V}$, $T_J = 25^\circ\text{C}$) ($V_R = 520\text{ V}$, $T_J = 150^\circ\text{C}$)	I_R	5.0 400	μA
Maximum Reverse Recovery Time ($I_F = 1.0\text{ A}$, $di/dt = 50\text{ A}/\mu\text{s}$, $V_R = 30\text{ V}$, $T_J = 25^\circ\text{C}$)	t_{rr}	95	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2.0\%$.

NOTE 2 — AMBIENT MOUNTING DATA

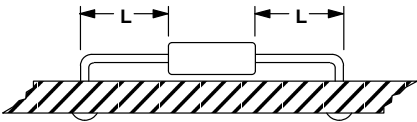
Data shown for thermal resistance junction-to-ambient ($R_{\theta JA}$) for the mountings shown is to be used as typical guideline values for preliminary engineering or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

Mounting Method		Lead Length, L (IN)				Units
		1/8	1/4	1/2	3/4	
1	$R_{\theta JA}$	50	51	53	55	°C/W
2		58	59	61	63	°C/W
3		28				°C/W

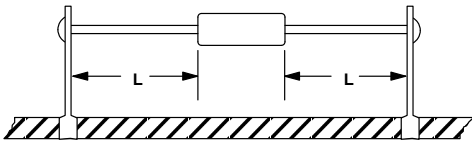
MOUNTING METHOD 1

P.C. Board Where Available Copper Surface area is small.



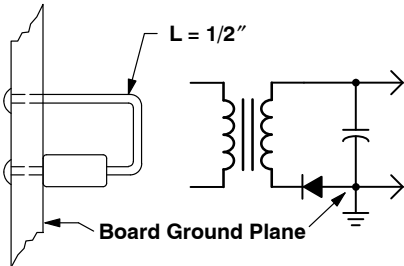
MOUNTING METHOD 2

Vector Push-In Terminals T-28



MOUNTING METHOD 3

P.C. Board with
1-1/2" x 1-1/2" Copper Surface



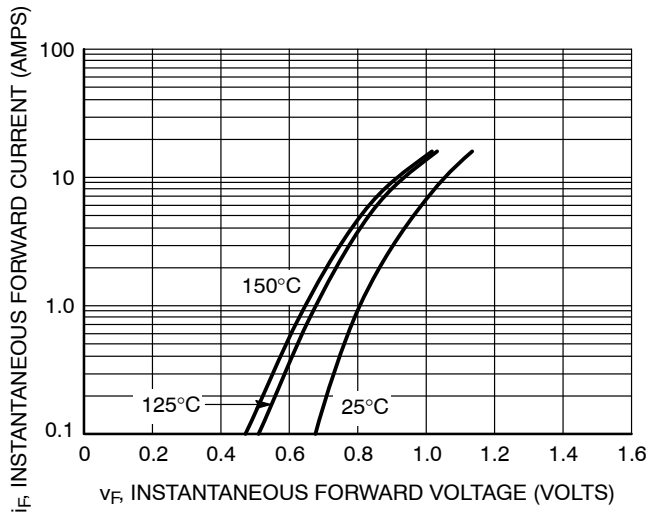


Figure 1. Typical Forward Voltage

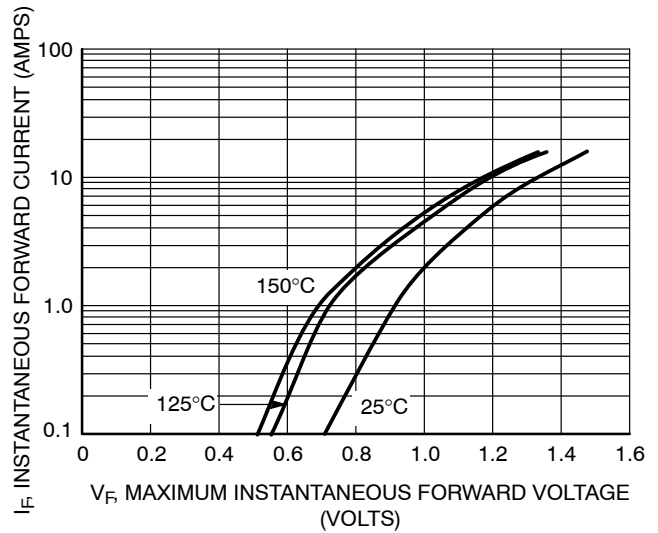


Figure 2. Maximum Forward Voltage

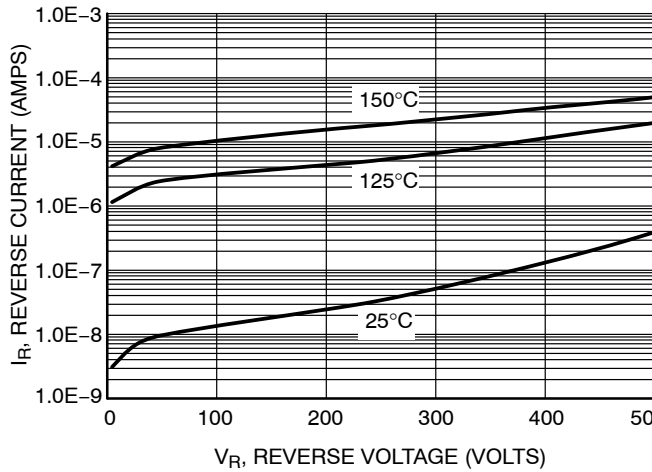


Figure 3. Typical Reverse Current

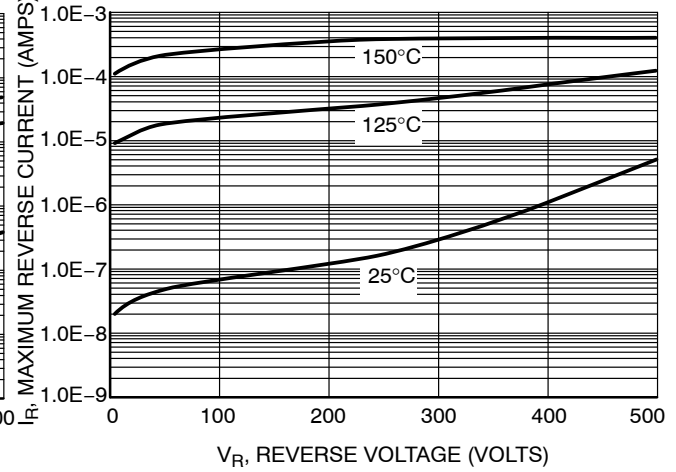


Figure 4. Maximum Reverse Current

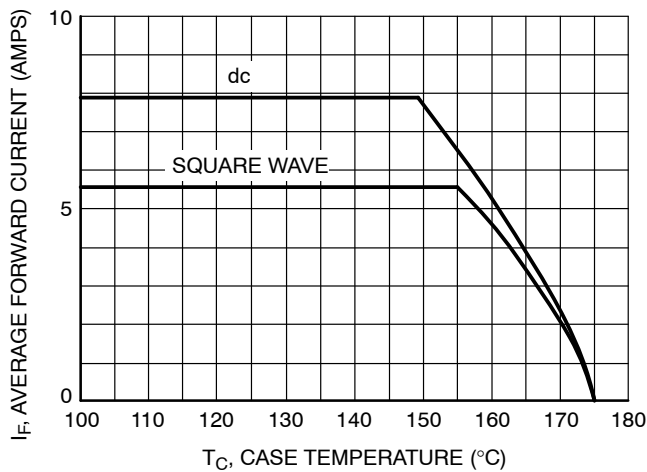


Figure 5. Current Derating

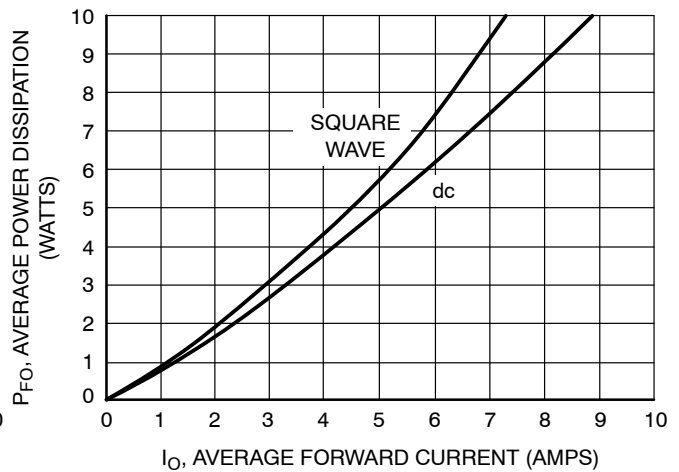


Figure 6. Forward Power Dissipation

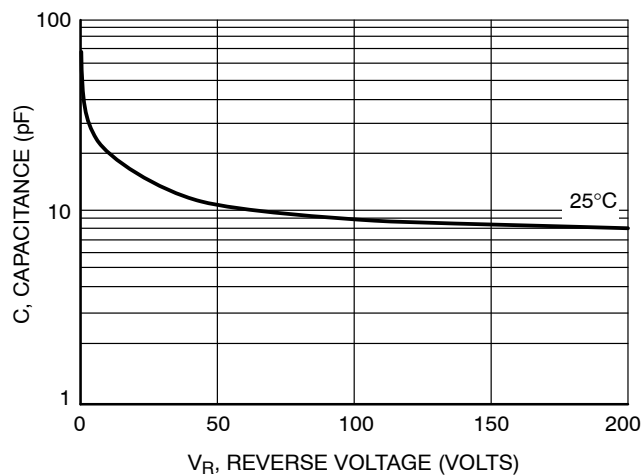


Figure 7. Capacitance

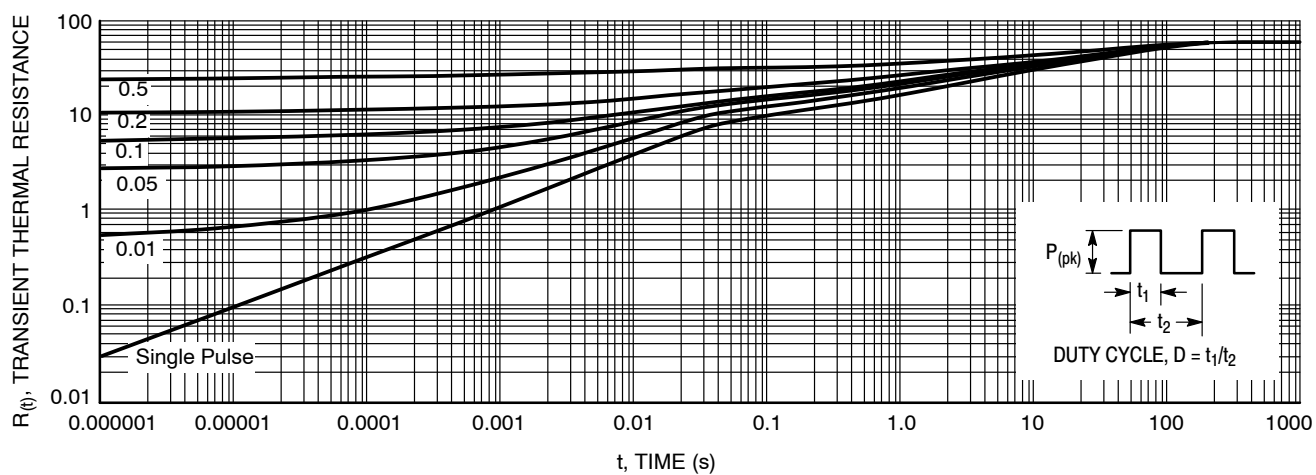


Figure 8. Thermal Response for MUR550APFG

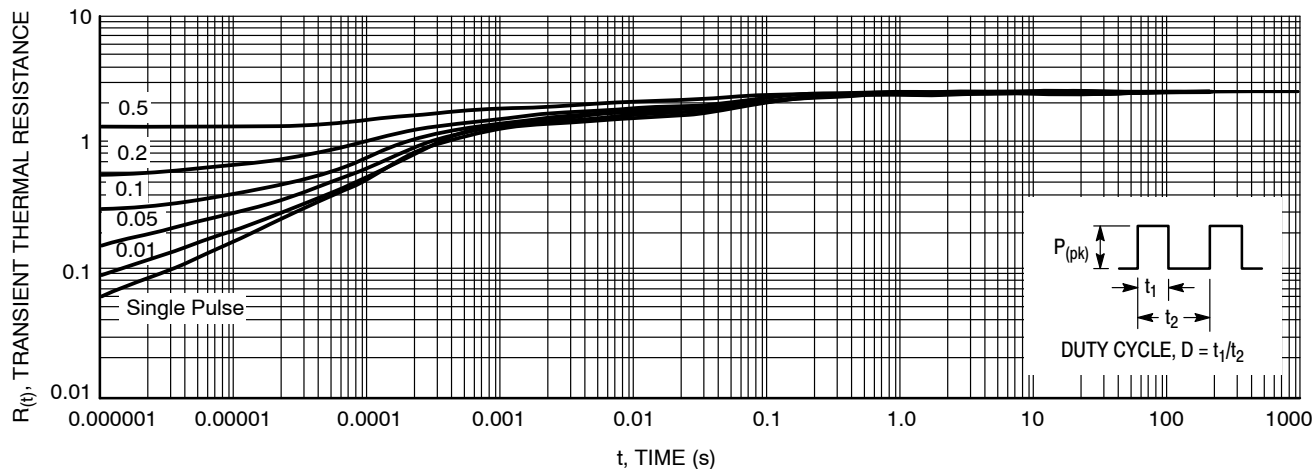


Figure 9. Thermal Response for MURD550PFG, NRVUD550PFT4G, NRVUD550PFT4G-VF01

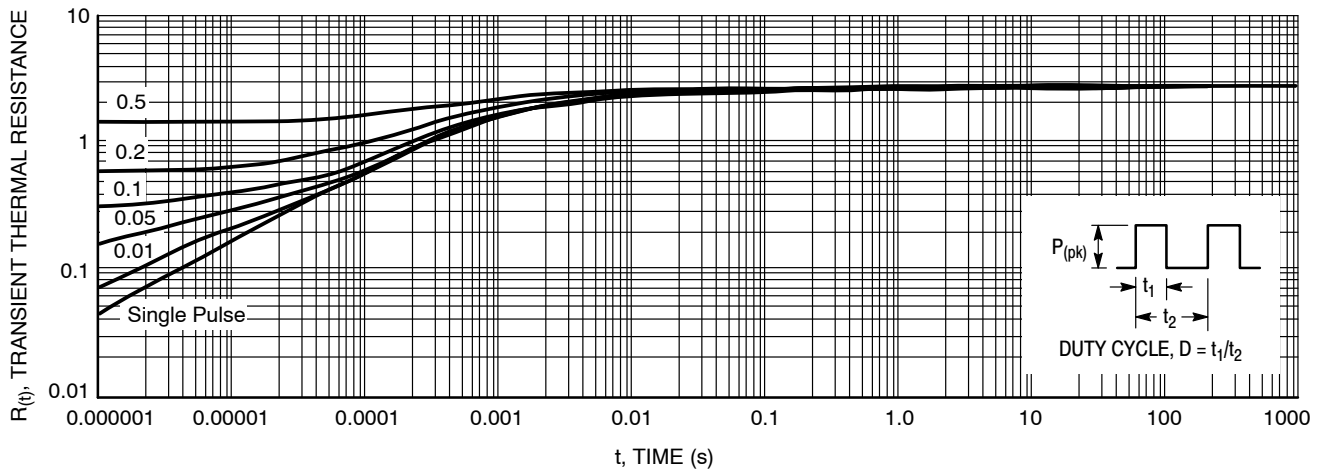


Figure 10. Thermal Response for MUR550PFG

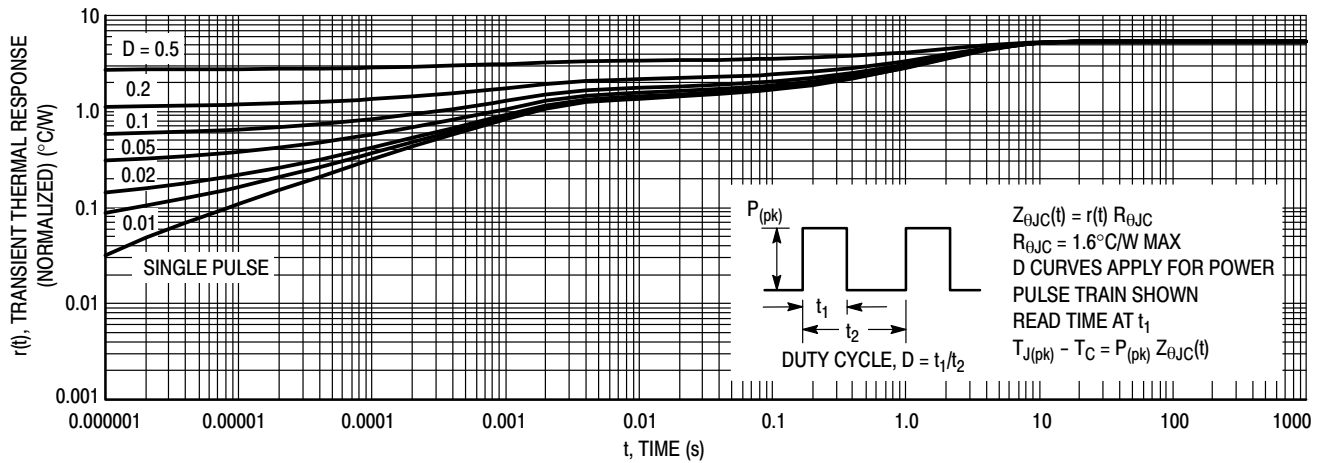


Figure 11. Thermal Response, (MURF550PFG) Junction-to-Case ($R_{\theta JC}$)

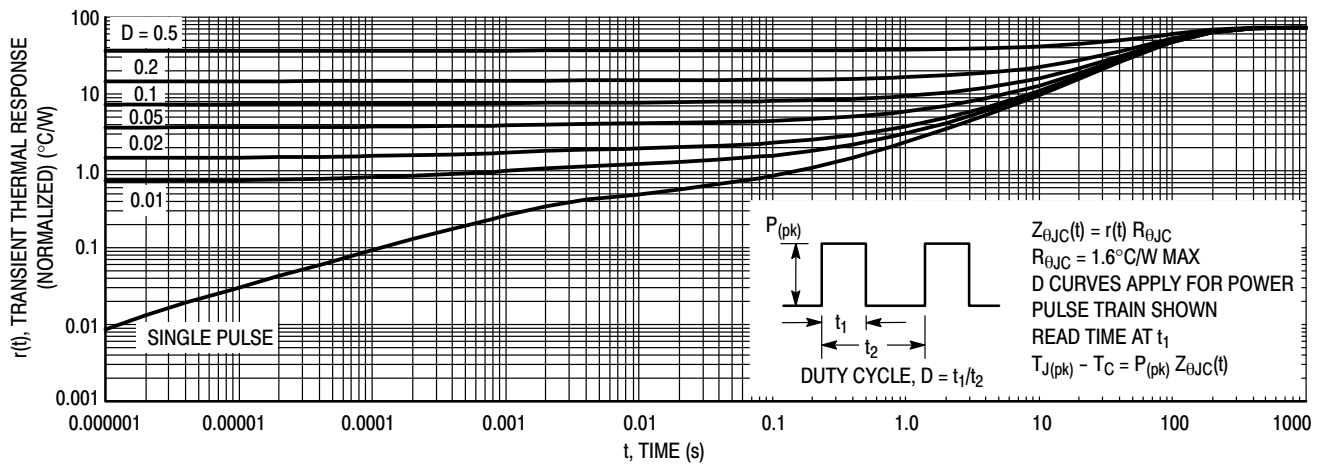


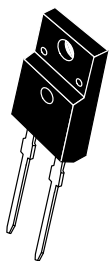
Figure 12. Thermal Response, (MURF550PFG) Junction-to-Ambient ($R_{\theta JA}$)

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

ON



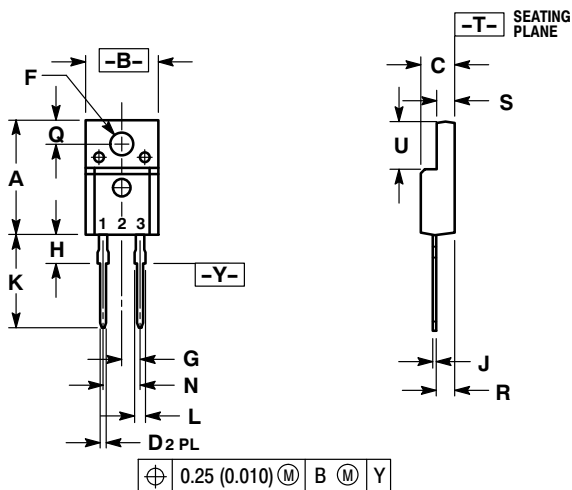
SCALE 1:1

TO-220 FULLPAK, 2-LEAD

CASE 221E-01

ISSUE A

DATE 21 JAN 2008



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.633	15.67	16.07
B	0.392	0.408	9.96	10.36
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.121	0.129	3.08	3.28
G	0.100 BSC		2.54 BSC	
H	0.117	0.133	2.98	3.38
J	0.018	0.025	0.45	0.64
K	0.499	0.562	12.68	14.27
L	0.045	0.060	1.14	1.52
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.101	0.117	2.56	2.96
S	0.092	0.108	2.34	2.74
U	0.255	0.271	6.48	6.88

STYLE 1:
PIN 1. CATHODE
2. N/A
3. ANODE

GENERIC MARKING DIAGRAM*




Rectifier

A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package
xxxxxx = Device Code
KA = Polarity Designator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO-220 FULLPAK, 2-LEAD	
		PAGE 1 OF 2

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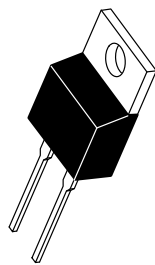
PACKAGE DIMENSIONS

ON Semiconductor®

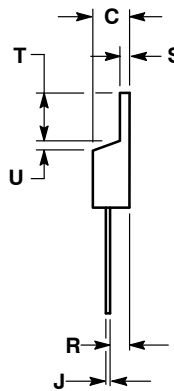
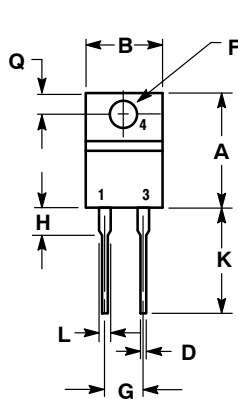


TO-220, 2-LEAD CASE 221B-04 ISSUE F

DATE 12 APR 2013



SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.595	0.620	15.11	15.75
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.82
D	0.025	0.039	0.64	1.00
F	0.142	0.161	3.61	4.09
G	0.190	0.210	4.83	5.33
H	0.110	0.130	2.79	3.30
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.14	1.52
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.14	1.39
T	0.235	0.255	5.97	6.48
U	0.000	0.050	0.000	1.27

STYLE 1:
PIN 1. CATHODE
2. N/A
3. ANODE
4. CATHODE

STYLE 2:
PIN 1. ANODE
2. N/A
3. CATHODE
4. ANODE

DOCUMENT NUMBER: 98ASB42149B

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DESCRIPTION: TO-220, 2-LEAD

PAGE 1 OF 1

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MECHANICAL CASE OUTLINE

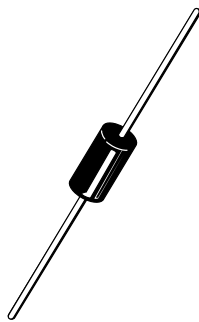
PACKAGE DIMENSIONS

ON Semiconductor®

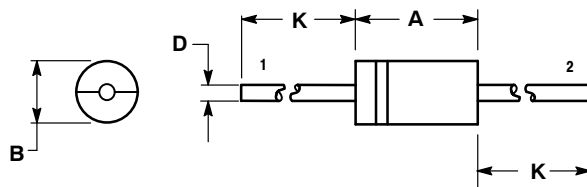


AXIAL LEAD CASE 267-05 ISSUE G

DATE 06/06/2000



SCALE 1:1



NOTES:

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 267-04 OBSOLETE, NEW STANDARD 267-05.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.287	0.374	7.30	9.50
B	0.189	0.209	4.80	5.30
D	0.047	0.051	1.20	1.30
K	1.000	---	25.40	---

STYLE 1:
PIN 1. CATHODE (POLARITY BAND)
2. ANODE

STYLE 2:
NO POLARITY

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DESCRIPTION:	AXIAL LEAD	PAGE 1 OF 1

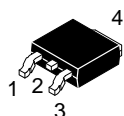
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

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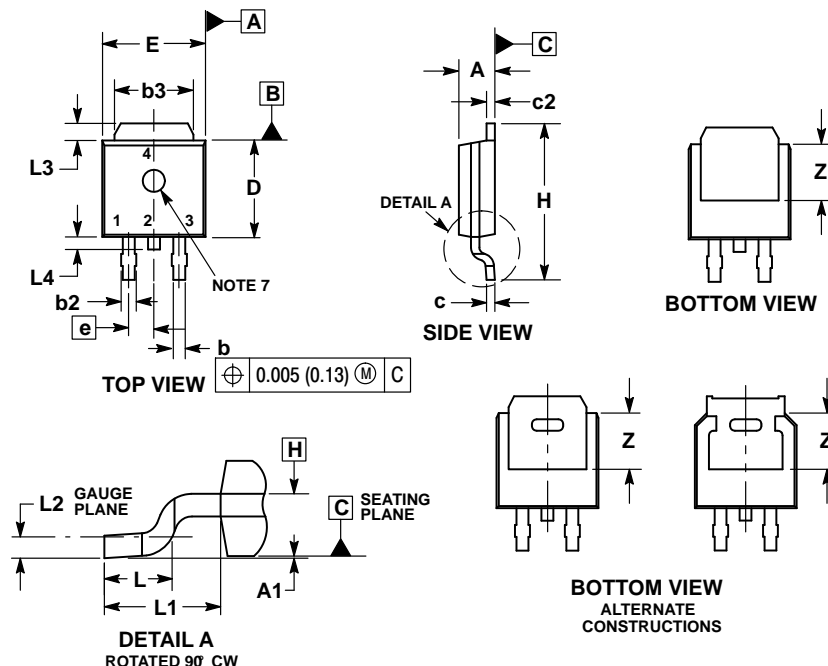
SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369C

ISSUE F

DATE 21 JUL 2015

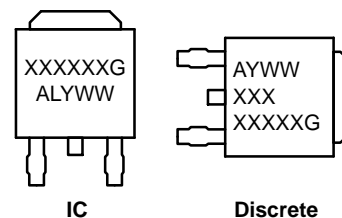


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

GENERIC MARKING DIAGRAM*

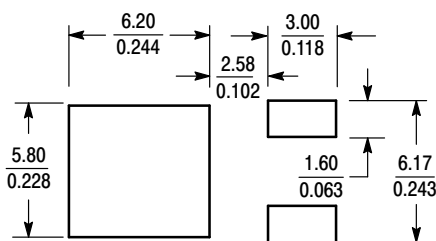


XXXXXX = Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

- STYLE 1:**
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR
- STYLE 2:**
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN
- STYLE 3:**
 PIN 1. ANODE
 2. CATHODE
 3. ANODE
 4. CATHODE
- STYLE 4:**
 PIN 1. CATHODE
 2. ANODE
 3. GATE
 4. ANODE
- STYLE 5:**
 PIN 1. GATE
 2. ANODE
 3. CATHODE
 4. ANODE
- STYLE 6:**
 PIN 1. MT1
 2. MT2
 3. GATE
 4. MT2
- STYLE 7:**
 PIN 1. GATE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR
- STYLE 8:**
 PIN 1. N/C
 2. CATHODE
 3. ANODE
 4. CATHODE
- STYLE 9:**
 PIN 1. ANODE
 2. CATHODE
 3. RESISTOR ADJUST
 4. CATHODE
- STYLE 10:**
 PIN 1. CATHODE
 2. ANODE
 3. CATHODE
 4. ANODE

SOLDERING FOOTPRINT*




SCALE 3:1 (mm inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:	REF TO JEDEC TO-252	
DESCRIPTION:	DPAK SINGLE GAUGE SURFACE MOUNT	PAGE 1 OF 2

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