

AN-2279 LMR12020 Evaluation Module

1 Introduction

The LMR12020 evaluation module is designed to provide the power supply design engineer with a fully functional regulator design which can be synchronized to an external clock between 1000 kHz and 2350 kHz. The evaluation module provides two output voltage options viz. 3.3V and 5V with a 2A current capability. Without an external synchronization signal, the design operates at 2000 kHz reducing the solution size and keeping switching noise out of the AM radio band. The PCB consists of 4 layers of copper on FR4 material. The first middle layer is a solid ground layer which helps in minimizing the AC current loop. The LMR12020 is thermally tied to the other layers by thermal vias directly underneath the device. This user's guide contains the evaluation module schematic, a quick setup procedure, and a Bill-of-Materials (BOM). For complete circuit design information, see *LMR12015/LMR12020 SIMPLE SWITCHER 20Vin, 1.5A/2A Step-Down Voltage Regulator in WSON-10* (SNVS817).

2 Features

Parameter	3.3V Output Voltage Option	5V Output Voltage Option	
Input Range	5 to 20V	7 to 20V	
Output Voltage	3.3V	5V	
Output Current	0 to 2A	0 t0 2A	
Frequency of Operation	1000 kHz - 2350 kHz	1000 KHz - 2350 KHz	
Default Frequency of Operation	2000 kHz	2000 kHz	
Board Size	1.944 × 1.35 inches (49.37 × 34.29 mm)	1.944 x 1.35 inches (49.37 x 34.29 mm)	

3 Evaluation Module Schematic

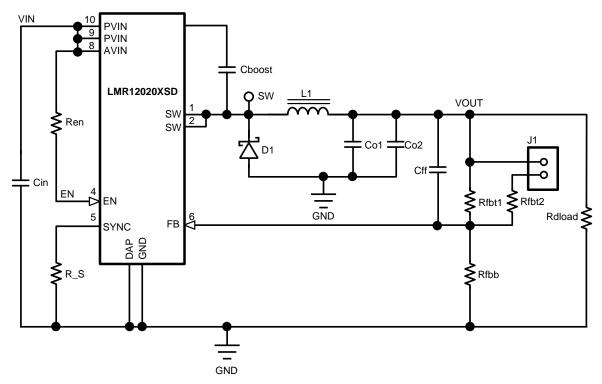


Figure 1. LMR12020 Evaluation Module Schematic

4 Powering and Loading Considerations

Read this entire section prior to attempting to power the evaluation board.

4.1 Quick Start Procedure

Step 1: Set the bench power supply current limit to 2A. Set the power supply voltage to 12V. Turn off the power supply output. Connect the power supply to the LMR12020 demo board. Positive connection to V_{IN} and negative connection to GND.

Step 2: Connect a load, as high as 2A, to the V_{OUT} terminal. Positive connection to V_{OUT} and negative connection to GND.

Step 3: Turn on the bench power supply with no load applied to the LMR12020 and the shunt for the jumper J1 in place. The V_{OUT} would be in regulation at a nominal 3.3V output. With the shunt out, a minimum load of 10mA would be required to have the V_{OUT} in regulation at 5V.

Step 4: Gradually increase the load and V_{OUT} should remain in regulation as the load is increased up to 2 Amps. The V_{OUT} should also be regulated when the input is swept from the minimum input to 20V.

4.2 Starting Up

The EN pin is tied to V_{IN} to simplify start-up. The pull-up resistor allows the power supply design engineer to toggle EN independently, if desired, and observe the start-up behavior of the LMR12020. Use the EN post to disable the device by pulling this node to GND. A logic signal may be applied to the post to test startup and shutdown of the device.



4.3 Synchronization

A SYNC pin has been provided on the evaluation board. This pin can be used to synchronize the regulator to an external clock or multiple evaluation boards can be synchronized together by connecting their SYNC pins together. For complete information, see *LMR12015/LMR12020 SIMPLE SWITCHER 20Vin, 1.5A/2A Step-Down Voltage Regulator in WSON-10* (SNVS817).

4.4 No Load Startup at High Output Voltage

The LMR12020 cannot startup at no load when the output voltage goes above 3.3V. Refer to the LMR12020 datasheet for more information regarding minimum load requirements. A position for a dummy load is provided on the board. Populating that with a 500 ohm resistor facilitates the startup at no load for the 5V output voltage options.

4.5 Adjusting the Output Voltage

The output voltage is set using the following equation where R_{fbb} is connected between the FB pin and GND, and R_{fbt} is connected between V_{OLT} and FB.

$$V_{OUT} = V_{FB}(1 + (R_{fbt}/R_{fbb})) \tag{1}$$

Adjusting the output voltage will affect the performance of the LMR12020. In addition, output capacitors might not be rated for the new output voltage. For more information, see *LMR12015/LMR12020 SIMPLE SWITCHER 20Vin, 1.5A/2A Step-Down Voltage Regulator in WSON-10* (SNVS817).

4.6 Typical Test Setup

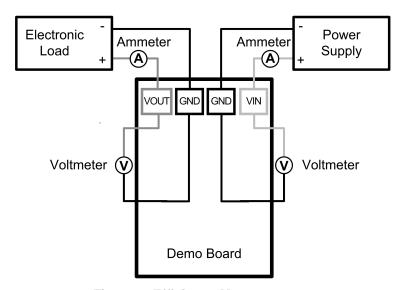


Figure 2. Efficiency Measurements



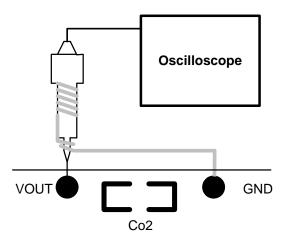


Figure 3. Voltage Ripple Measurements

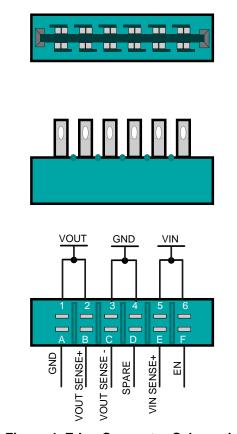


Figure 4. Edge Connector Schematic



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5 Board Images

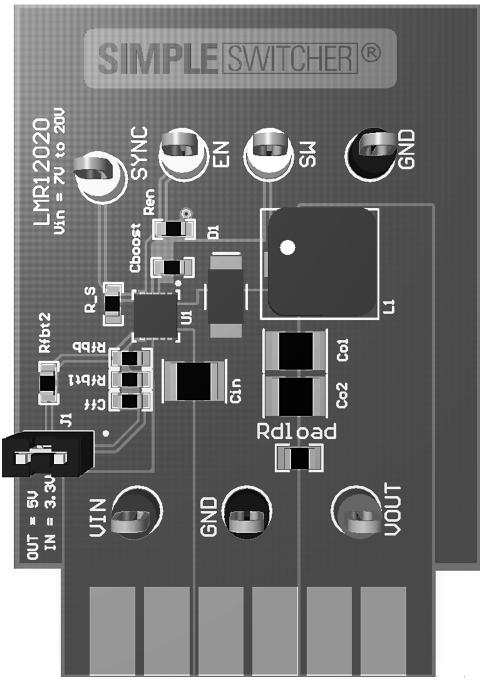


Figure 5. Top Side



Board Images www.ti.com

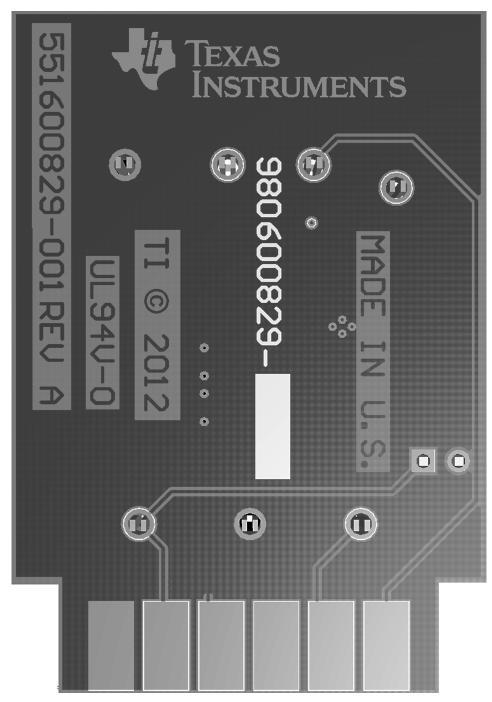
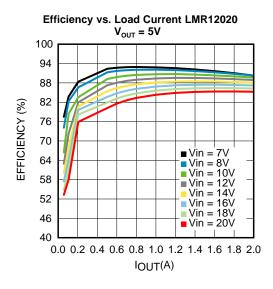
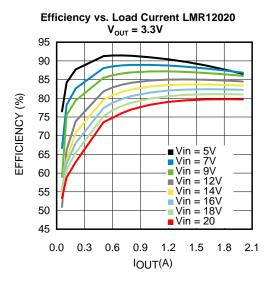


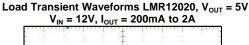
Figure 6. Bottom Side

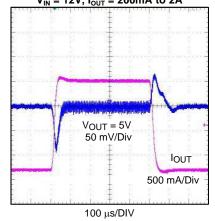


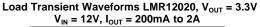
6 Performance Characteristics

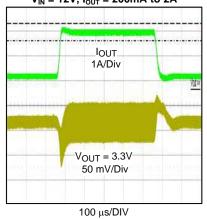


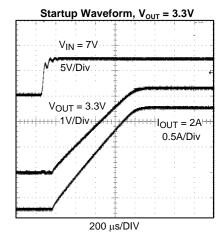


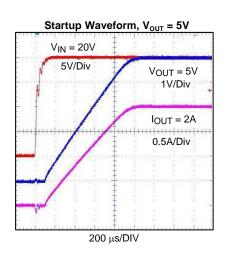








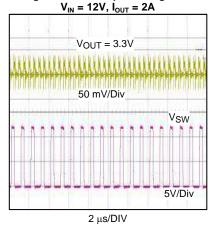






Bill of Materials www.ti.com

Switching Node and Output Voltage Waveforms



7 Bill of Materials

Part Name	Part ID	Part Value	Part Number	Manufacturer
Buck Regulator	U1	2A Buck Regulator	LMR12020	Texas Instruments
Input Capacitor	Cin	10 μF	C1210C106K8PACTU	Kemet
Bootstrap Capacitor	Cboost	0.1 μF	C0603C104K8RACTU	Kemet
Output Capacitor	Co1	22 μF	GRM32ER71C226KE18L	Murata
Output Capacitor	Co2	22 μF	GRM32ER71C226KE18L	Murata
Catch Diode	D1	Schottky Diode Vf = 0.32V	CMS01	Toshiba
Inductor	L1	3.3 µH	7447789003	Wurth Elektronik eiSos
Feedback Resistor	Rfbt1	4.02k Ω	CRCW06034K02FKEA	Vishay-Dale
Feedback Resistor	Rfbt2	5.49k Ω	CRCW06035K49FKEA	Vishay-Dale
Feedback Resistor	Rfbb	1.02k Ω	CRCW06031K02FKEA	Vishay-Dale
Pull-up Resistor	Ren	4.75 kΩ	CRCW06034K75FKEA	Vishay-Dale
Pull-down Resistor	R_S	4.75 kΩ	CRCW06034K75FKEA	Vishay-Dale
Test Point	VIN	Test Point Loop	5010	Keystone
Test Point	SW	Test Point Loop	5012	Keystone
Test Point	GND	Test Point Loop	5011	Keystone
Test Point	GND	Test Point Loop	5011	Keystone
Test Point	VOUT	Test Point Loop	5013	Keystone
Test Point	EN	Test Point Loop	5014	Keystone
Test Point	SYNC	Test Point Loop	5014	Keystone
Header	J1	2X1 Header, TH, 100mil	TSW-102-07-G-S	Samtec, Inc.
Shunt	SH-J1	Black 100mil Gold Plated Shunt	969102-0000-DA	3M



www.ti.com PCB Layout

8 PCB Layout

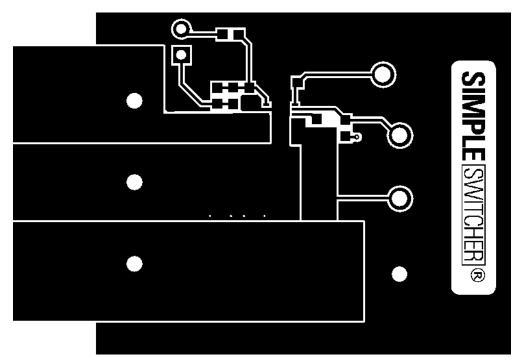


Figure 7. Top Copper

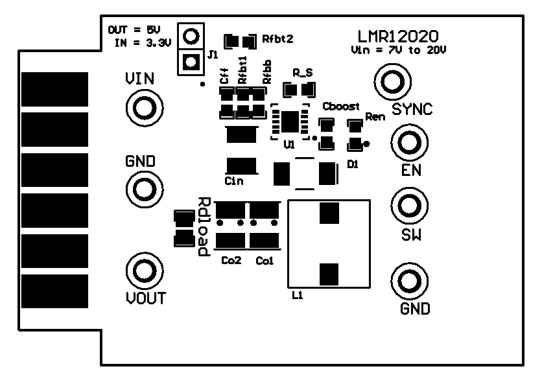


Figure 8. Top Overlay



PCB Layout www.ti.com

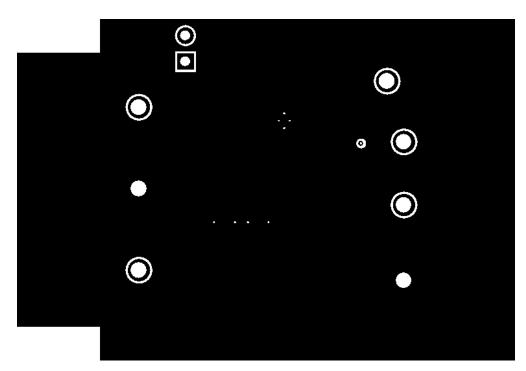


Figure 9. Internal Layer 1

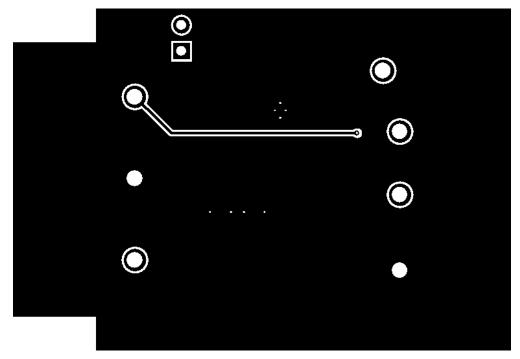


Figure 10. Internal Layer 2



www.ti.com PCB Layout

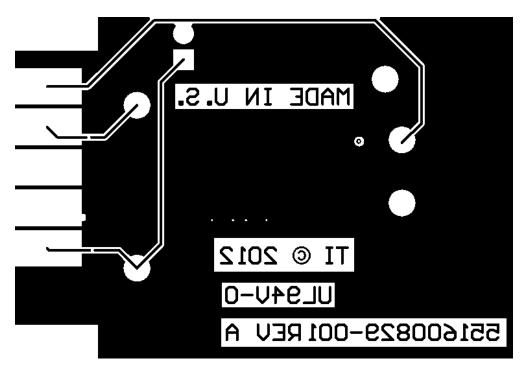


Figure 11. Bottom Copper

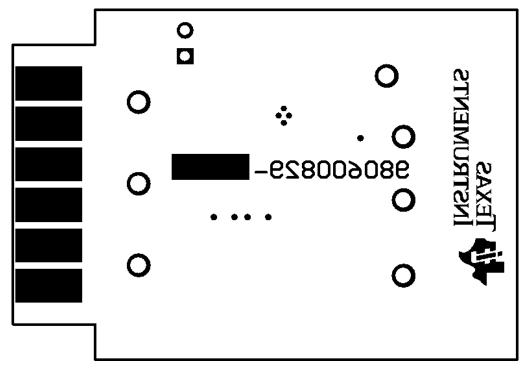


Figure 12. Bottom Overlay

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