3-Channel Low Power Video Buffer with I²C Control, Selectable Filters, External Gain Control, 2:1 Input MUX, and Selectable Input Modes

Check for Samples: THS7353

FEATURES

- 3-Video Buffers for CVBS, S-Video, SD/ED/HD $Y'P'_BP'_R$, and G'B'R' (R'G'B') Video
- I²C™ Control of All Functions
- Integrated Low-Pass Filters
  - 5th Order Butterworth Characteristics
  - Selectable Corner Frequencies of 9-MHz, 16-MHz, 35-MHz, and Bypass (150-MHz)
- Selectable Input Bias Modes
  - AC-Coupled with Sync-Tip Clamp
  - AC-Coupled with Bias
  - DC-Coupled with 250-mV Input Shift
  - DC-Coupled
- 2:1 Input MUX Allows Multiple Input Sources
- External Gain Control Range From 0 dB to 14 dB
- 2.7-V to 5-V Single Supply Operation
- Low 16.2-mA (3.3 V) Total Quiescent Current
- Disable (< 1 µA) and Mute Control Functions
- Rail-to-Rail Output:
  - Allows AC or DC Output Coupling
- Low Differential Gain/Phase of 0.15%/0.3°

APPLICATIONS

- HDTV Video Buffering
- PVR/DVDR Video Buffering
- Projector Video Buffering
- USB/Portable Low Power Video Buffering

DESCRIPTION

Fabricated using the new complimentary silicon-germanium (SiGe) BiCom-III process, the THS7353 is a low-power, single-supply 2.7-V to 5-V, 3-channel integrated video buffer. It incorporates a selectable 5th order Butterworth anti-aliasing / DAC reconstruction filter to eliminate data converter images. The 9-MHz is a perfect choice for SDTV video including composite, S-Video™, and 480i/576i $Y'P'_BP'_R$ or G'B'R' (R'G'B') video. The 16-MHz filter is ideal for EDTV 480p/576p $Y'P'_BP'_R$, G'B'R', and VGA signals. The 35-MHz filter is useful for HDTV 720p/1080i $Y'P'_BP'_R$, G'B'R', and SVGA/XGA signals. For 1080p or SXGA/UXGA signals, the filter can be bypassed allowing a 150-MHz bandwidth, 300-V/µs amplifier to buffer the signal.

Each channel of the THS7353 is individually I²C configurable for all functions which makes it flexible for any application. Its rail-to-rail output stage allows for both ac and dc coupling applications. The externally controlled gain adjust pin allows for fine tuning of the gain such as line driving, compensating for cable losses, or Sin-X/X compensation.

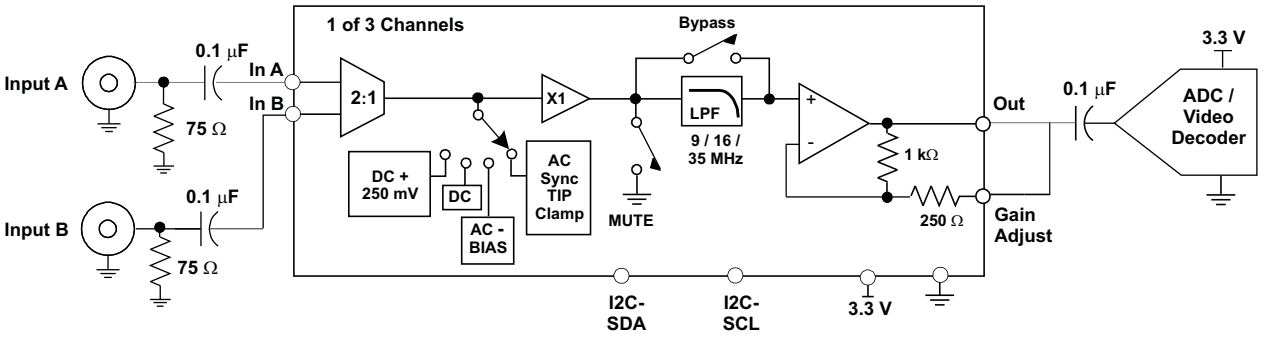


Figure 1. 3.3 V Single-Supply AC-Input/AC-Video Output System w/SAG Correction (1 of 3 Channels Shown)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

As part of the THS7353 flexibility, the 2:1 MUX input can be selected for ac or dc coupled inputs. The ac coupled modes include a sync-tip clamp option for CVBS/Y'/G'B'R' with sync or a fixed bias for the C'/P'$_B$/P'$_R$ channels. The dc input options include a dc input or a dc + 250-mV input offset shift to allow for a full sync dynamic range at the output with 0-V input.

The THS7353 is the perfect choice for all video buffer applications. The 16.2-mA total quiescent current (54 mW total power) makes it an excellent choice for USB powered or portable video applications. While fully disabled, the THS7353 consumes less than 1 µA.

PACKAGING/ORDERING INFORMATION(1)

PACKAGED DEVICES	PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
THS7353PW	TSSOP-20	Rails, 70
THS7353PWR		Tape and reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		UNIT
V_{SS}	Supply voltage, V_{S+} to GND	5.5 V
V_I	Input voltage	–0.4 V to V_{S+}
I_O	Output current	±125 mA
	Continuous power dissipation	See Dissipation Ratings Table
T_J	Maximum junction temperature, any condition(2)	150°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)	125°C
T_{stg}	Storage temperature range	–65°C to 150°C
ESD ratings	HBM	1500 V
	CDM	2000 V
	MM	100 V

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1) (T_J = 125°C)	
			T_A = 25°C	T_A = 85°C
TSSOP – 20 (PW)	32.3	83(2)	1.2 W	0.48 W

(1) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase and long-term reliability starts to be reduced. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and reliability.
(2) This data was taken with the JEDEC High-K test PCB. For the JEDEC low-K test PCB, the θ_{JA} is 125.8°C.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage, V_{S+}	2.7		5	V
T_A	Ambient temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS, V_{S+} = 3.3 V

R_L = 150 Ω to GND, Filter Select = 9 MHz, Input Bias = dc, Gain Adjust pin shorted to the output pin (unless otherwise noted).

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
AC PERFORMANCE							
Small-signal bandwidth (–3 dB) V_O – 0.2 V_{PP}	Filter Select = 9 MHz(1)	9	7.6/10.4	7.4/10.6	7.3/10.7	MHz	Min/Max
	Filter Select = 16 MHz(1)	16	13.4/18.6	13.1/18.9	13/19	MHz	Min/Max
	Filter Select = 35 MHz(1)	35	26.9/40.6	26.6/40.9	26.5/41	MHz	Min/Max
	Filter Select = Bypass	150				MHz	
Large-signal bandwidth (–3 dB) V_O – 1 V_{PP}	Filter Select = 9 MHz	9				MHz	
	Filter Select = 16 MHz	16				MHz	
	Filter Select = 35 MHz	35				MHz	
	Filter Select = Bypass	100				MHz	
Slew rate	Filter Select = Bypass: 2 V_{PP}	300				V/µs	
Group delay at 100 kHz	Filter Select = 9 MHz	53.5				ns	
	Filter Select = 16 MHz	31				ns	
	Filter Select = 35 MHz	17.2				ns	
	Filter Select = Bypass	3.25				ns	
Group delay variation with respect to 100 kHz	Filter Select = 9 MHz: at 5.1 MHz	10.3				ns	
	Filter Select = 16 MHz: at 11 MHz	7.5				ns	
	Filter Select = 35 MHz: at 27 MHz	4.7				ns	
Group delay matching	All filters: channel-to-channel	0.5				ns	
Attenuation with respect to 100 kHz	Filter Select = 9 MHz: at 5.75 MHz	0.25	-0.3/1.2	-0.5/1.4	-0.6/1.5	dB	Min/Max
	Filter Select = 9 MHz: at 27 MHz	43	33	32	31	dB	Min
	Filter Select = 16 MHz: at 11 MHz	0.35	-0.4/1.2	-0.6/1.4	-0.7/1.5	dB	Min/Max
	Filter Select = 16 MHz: at 54 MHz	47	35	34	33	dB	Min
	Filter Select = 35 MHz: at 27 MHz	0.75	-0.5/3.2	-0.6/3.4	-0.7/3.5	dB	Min/Max
	Filter Select = 35 MHz: at 74 MHz	29	13	12	11	dB	Min
Mute feed thru	Filter Select = Bypass: at 30 MHz	-73				dB	
Differential gain	Filter Select = 9 MHz: NTSC/PAL	0.15%/0.22%					
Differential phase	Filter Select = 9 MHz: NTSC/PAL	0.3°/0.36°					
Total harmonic distortion f = 1 MHz, 1 V_{PP}	Filter Select = 9 MHz	–59				dB	
	Filter Select = 16 MHz	–58				dB	
	Filter Select = 35 MHz	–55				dB	
	Filter Select = Bypass	–59				dB	
Signal to noise ratio (unified weighting per CCIR 576-2 recommendation)	Filter Select = 9 MHz, 480i source	83				dB	
	Filter Select = 16 MHz, 480p source	81				dB	
	Filter Select = 35 MHz, 720p source	78				dB	
	Filter Select = Bypass(2), 720p source	66				dB	
Channel-to-Channel Crosstalk (V_O = 1 V_{PP})	Filter Select = 9 MHz: at 1 MHz	–70				dB	
	Filter Select = 16 MHz: at 1 MHz	–73				dB	
	Filter Select = 35 MHz: at 1 MHz	–78				dB	
	Filter Select = Bypass: at 1 MHz	–84				dB	

(1) The Min/Max values listed are specified by design only.
(2) Bandwidth up to 100-MHz, No Weighting, Tilt Null

ELECTRICAL CHARACTERISTICS, V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND, Filter Select = 9 MHz, Input Bias = dc, Gain Adjust pin shorted to the output pin (unless otherwise noted).

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
MUX Isolation	Filter Select = 9 MHz: at 5.1 MHz	75				dB	
	Filter Select = 16 MHz: at 11 MHz	74				dB	
	Filter Select = 35 MHz: at 27 MHz	74				dB	
	Filter Select = Bypass: at 60 MHz	75				dB	
Output impedance	f = 10 MHz	0.8				Ω	
DC PERFORMANCE							
Output offset voltage	Bias = dc	20	70	80	85	mV	Max
Average offset voltage drift	Bias = dc				20	µV/°C	
Bias output voltage	Bias = dc + 250 mV, V_I = 0 V	255	210/300	200/310	190/320	mV	Min/Max
	Bias = ac	1.05	0.9/1.2	0.85/1.25	0.85/1.25	V	Min/Max
Sync tip clamp voltage	Bias = ac STC, clamp voltage	250	190/310	180/320	175/325	mV	Min/Max
Input bias current	Bias = dc - implies Ib out of the pin	–0.6	–4	–5	–5	µA	Max
Average bias current drift	Bias = dc				10	nA/°C	
Sync tip clamp bias current	Bias = ac STC, low bias	1.6	0.6/3.3	0.5/3.5	0.4/3.6	µA	Min/Max
	Bias = ac STC, mid bias	5.8	4.3/8.2	4.1/8.4	4/8.5	µA	Min/Max
	Bias = ac STC, high bias	7.4	6.2/10.8	6/11	5.9/11.1	µA	Min/Max
INPUT CHARACTERISTICS							
Input voltage range	Bias = dc - ensured by output	0/2.1	0/1.8	0/1.7	0/1.6	V	Min/Max
Input resistance	Bias = ac bias mode	21				kΩ	
	Bias = dc, dc + 250 mV, ac STC	3				MΩ	
Input capacitance		2				pF	
OUTPUT CHARACTERISTICS							
High output voltage swing (limited by input voltage with gain = 0 dB)	R_L = 150 Ω to Midrail	2.1				V	
	R_L = 150 Ω to GND	2.1	1.8	1.7	1.6	V	Min
	R_L = 75 Ω to Midrail	2.1				V	
	R_L = 75 Ω to GND	2.1				V	
Low output voltage swing	R_L = 150 Ω to Midrail	0.14	0.24	0.27	0.28	V	Max
	R_L = 150 Ω to GND	0.09	0.17	0.2	0.21	V	Max
	R_L = 75 Ω to Midrail	0.24	0.33	0.36	0.37	V	Max
	R_L = 75 Ω to GND	0.09	0.17	0.2	0.21	V	Max
Output current	R_L = 10 Ω to GND, sourcing	70				mA	
	R_L = 10 Ω to Midrail, sinking	70	45	42	40	mA	Min

ELECTRICAL CHARACTERISTICS, V_{S+} = 3.3 V (continued)

R_L = 150 Ω to GND, Filter Select = 9 MHz, Input Bias = dc, Gain Adjust pin shorted to the output pin (unless otherwise noted).

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
POWER SUPPLY							
Maximum operating voltage		3.3	5.5	5.5	5.5	V	Max
Minimum operating voltage		3.3	2.7	2.7	2.7	V	Min
Maximum quiescent current	Per channel V_I = 400 mV	5.9	7.1	7.3	7.4	mA	Max
Minimum quiescent current	Per channel V_I = 400 mV	5.9	4.7	4.5	4.4	mA	Min
Total quiescent current	All channels ON, V_I = 400 mV(3)	16.2				mA	
Power supply rejection (+PSRR)	V_{S+} = 3.5 V to 3.1 V	48	40	38	37	dB	Min
DISABLE CHARACTERISTICS							
Quiescent current	All 3 channels disabled (4)	0.1				µA	
Turn-on time delay (t_{ON})	Time reaches 50% of final value after I^2C control is completed	5				µs	
Turn-on time delay (t_{OFF})		2				µs	
DIGITAL CHARACTERISTICS(5)							
High-level input voltage (V_{IH})		2.3				V	Typ
Low-level input voltage (V_{IL})		1.0				V	Typ

(3) Due to sharing of internal bias circuitry, the quiescent current, with all channels operating, is less than the single individual channel quiescent currents added together.
(4) Note that the I^2C circuitry is still active while in Disable mode. The current shown is while there is no activity with the THS7353 I^2C circuitry.
(5) Standard CMOS logic.

ELECTRICAL CHARACTERISTICS, V_{S+} = 5 V

R_L = 150 Ω to GND, Filter Select = 9 MHz, Input Bias = dc, Adjust pin shorted to the output pin (unless otherwise noted).

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
AC PERFORMANCE							
Small-signal bandwidth (–3 dB) V_O – 0.2 V_{PP}	Filter Select = 9 MHz(1)	9	7.6/10.4	7.4/10.6	7.3/10.7	MHz	Min/Max
	Filter Select = 16 MHz(1)	16	13.4/18.6	13.1/18.9	13/19	MHz	Min/Max
	Filter Select = 35 MHz(1)	35	26.9/40.6	26.6/40.9	26.5/41	MHz	Min/Max
	Filter Select = Bypass	150				MHz	
Large-signal bandwidth (–3 dB) V_O – 1 V_{PP}	Filter Select = 9 MHz	9				MHz	
	Filter Select = 16 MHz	16				MHz	
	Filter Select = 35 MHz	35				MHz	
	Filter Select = Bypass	100				MHz	
Slew rate	Filter Select = Bypass, V_O = 2 V_{PP}	300				V/µs	
Group delay at 100 kHz	Filter Select = 9 MHz	53				ns	
	Filter Select = 16 MHz	30.8				ns	
	Filter Select = 35 MHz	17				ns	
	Filter Select = Bypass	3				ns	
Group delay variation with respect to 100 kHz	Filter Select = 9 MHz: at 5.1 MHz	10.2				ns	
	Filter Select = 16 MHz: at 11 MHz	7.3				ns	
	Filter Select = 35 MHz: at 27 MHz	4.4				ns	
Attenuation with respect to 100 kHz	Filter Select = 9 MHz: at 5.75 MHz	0.2	-0.3/1.2	-0.5/1.4	-0.6/1.5	dB	Min/Max
	Filter Select = 9 MHz: at 27 MHz	43	33	32	31	dB	Min
	Filter Select = 16 MHz: at 11 MHz	0.3	-0.4/1.2	-0.6/1.4	-0.7/1.5	dB	Min/Max
	Filter Select = 16 MHz: at 54 MHz	47	35	34	33	dB	Min
	Filter Select = 35 MHz: at 27 MHz	0.75	-0.5/3	-0.6/3.2	-0.7/3.3	dB	Min/Max
	Filter Select = 35 MHz: at 74 MHz	29	13	12	11	dB	Min
Mute feed thru	Filter Select = Bypass: at 30 MHz	-73				dB	
Differential gain	Filter Select = 9 MHz: NTSC/PAL	0.22%/0.33 %					
Differential phase	Filter Select = 9 MHz: NTSC/PAL	0.55°/0.65°					
Total harmonic distortion f = 1 MHz, 1 V_{PP}	Filter Select = 9 MHz	–64				dB	
	Filter Select = 16 MHz	–73				dB	
	Filter Select = 35 MHz	–70				dB	
	Filter Select = Bypass	–71				dB	
Signal to noise ratio (unified weighting per CCIR 576-2 recommendation)	Filter Select = 9 MHz, 480i source	83				dB	
	Filter Select = 16 MHz, 480p source	81				dB	
	Filter Select = 35 MHz, 720p source	78				dB	
	Filter Select = Bypass(2), 720p source	66				dB	
Channel-to-Channel Crosstalk (V_O = 1 V_{PP})	Filter Select = 9 MHz: at 1 MHz	–70				dB	
	Filter Select = 16 MHz: at 1 MHz	–73				dB	
	Filter Select = 35 MHz: at 1 MHz	–78				dB	
	Filter Select = Bypass: at 1 MHz	–84				dB	
MUX Isolation	Filter Select = 9 MHz: at 5.1 MHz	76				dB	
	Filter Select = 16 MHz: at 11 MHz	74				dB	
	Filter Select = 35 MHz: at 27 MHz	74				dB	
	Filter Select = Bypass: at 60 MHz	69				dB	
Output impedance	f = 10 MHz	0.7				Ω	
DC PERFORMANCE							
Output offset voltage	Bias = dc	20	70	80	85	mV	Max
Average offset voltage drift	Bias = dc				20	µV/°C	

(1) The Min/Max values listed are specified by design only.
(2) Bandwidth up to 100-MHz, No Weighting, Tilt Null

ELECTRICAL CHARACTERISTICS, V_{S+} = 5 V (continued)

R_L = 150 Ω to GND, Filter Select = 9 MHz, Input Bias = dc, Adjust pin shorted to the output pin (unless otherwise noted).

PARAMETER	TEST CONDITIONS	TYP	OVERTEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
Bias output voltage	Bias = dc + 250 mV, V_I = 0 V	260	225/305	215/315	205/325	mV	Min/Max
	Bias = ac	1.55	1.4/1.7	1.35/1.75	1.35/1.75	V	Min/Max
Sync tip clamp voltage	Bias = ac STC, clamp voltage	265	205/325	195/335	190/340	mV	Min/Max
Input bias current	Bias = dc - implies Ib out of the pin	–0.6	–4	–5	–5	µA	Max
Average bias current drift	Bias = dc				10	nA/°C	
Sync tip clamp bias current	Bias = ac STC, low bias	1.7	0.6/3.3	0.5/3.5	0.4/3.6	µA	Min/Max
	Bias = ac STC, mid bias	6.2	4.3/8.2	4.1/8.4	4/8.5	µA	Min/Max
	Bias = ac STC, high bias	7.9	6.2/10.8	6/11	5.9/11.1	µA	Min/Max
INPUT CHARACTERISTICS							
Input voltage range	Bias = dc - ensured by out swing	0/3.4	0/2.95	0/2.85	0/2.8	V	Min/Max
Input resistance	Bias = ac bias mode	21				kΩ	
	Bias = dc, dc + 250 mV, ac STC	3				MΩ	
Input capacitance		2				pF	
OUTPUT CHARACTERISTICS							
High output voltage swing (limited by input voltage with gain = 0 dB)	R_L = 150 Ω to Midrail	3.4				V	
	R_L = 150 Ω to GND	3.4	2.95	2.85	2.8	V	Min
	R_L = 75 Ω to Midrail	3.4				V	
	R_L = 75 Ω to GND	3.4				V	
Low output voltage swing	R_L = 150 Ω to Midrail	0.2	0.34	0.37	0.37	V	Max
	R_L = 150 Ω to GND	0.09	0.23	0.26	0.27	V	Max
	R_L = 75 Ω to Midrail	0.35	0.46	0.5	0.5	V	Max
	R_L = 75 Ω to GND	0.09	0.23	0.26	0.27	V	Max
Output current	R_L = 10 Ω to GND, sourcing	85	60	57	55	mA	Min
	R_L = 10 Ω to Midrail, sinking	85	60	57	55	mA	Min
POWER SUPPLY							
Maximum operating voltage		5	5.5	5.5	5.5	V	Max
Minimum operating voltage		5	2.7	2.7	2.7	V	Min
Maximum quiescent current	Per channel V_I = 400 mV	6.5	7.8	8	8.1	mA	Max
Minimum quiescent current	Per channel V_I = 400 mV	6.5	5.2	5	4.9	mA	Min
Total quiescent current	All channels ON, V_I = 400 mV[3]	18.75				mA	
Power supply rejection (+PSRR)	V_{S+} = 5.2 V to 4.8 V	45	40	38	37	dB	Min
DISABLE CHARACTERISTICS							
Quiescent current	All 3 channels disabled [4]	0.4				µA	
Turn-on time delay (t_{ON})	Time reaches 50% of final value after I^2C control is completed	5				µs	
Turn-on time delay (t_{OFF})		2				µs	
DIGITAL CHARACTERISTICS[5]							
High-level input voltage (V_{IH})		3.5				V	Typ
Low-level input voltage (V_{IL})		1.5				V	Typ

(3) Due to sharing of internal bias circuitry, the quiescent current, with all channels operating, is less than the single individual channel quiescent currents added together.
(4) Note that the I^2C circuitry is still active while in Disable mode. The current shown is while there is no activity with the THS7353 I^2C circuitry.
(5) Standard CMOS logic.

TIMING REQUIREMENTS(1)

V_{S+} = 2.7 V to 5 V

PARAMETER		STANDARD MODE		FAST MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	Clock frequency, SCL	0	100	0	400	kHz
$t_{w(H)}$	Pulse duration, SCL high	4		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low	4.7		1.3		µs
t_r	Rise time, SCL and SDA		1000		300	ns
t_f	Fall time, SCL and SDA		300		300	ns
$t_{su(1)}$	Setup time, SDA to SCL	250		100		ns
$t_{h(1)}$	Hold time, SCL to SDA	0		0		ns
$t_{(buf)}$	Bus free time between stop and start conditions	4.7		1.3		µs
$t_{su(2)}$	Setup time, SCL to start condition	4.7		0.6		µs
$t_{h(2)}$	Hold time, start condition to SCL	4		0.6		µs
$t_{su(3)}$	Setup time, SCL to stop condition	4		0.6		µs
C_b	Capacitive load for each bus line		400		400	pF

(1) The THS7353 I^2C address = 01011(A1)(A0)(R/W). See the Application Information section for more information.

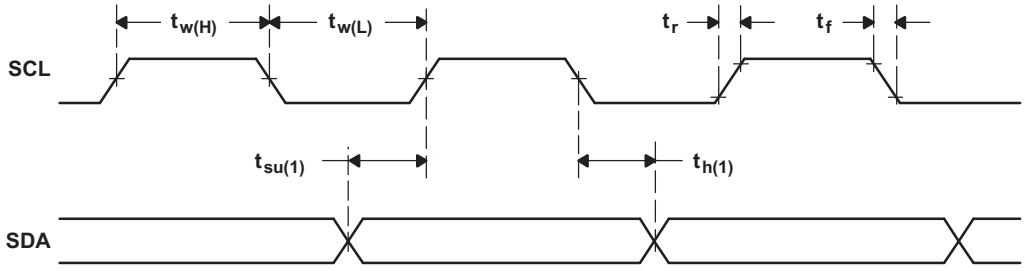


Figure 2. SCL and SDA Timing

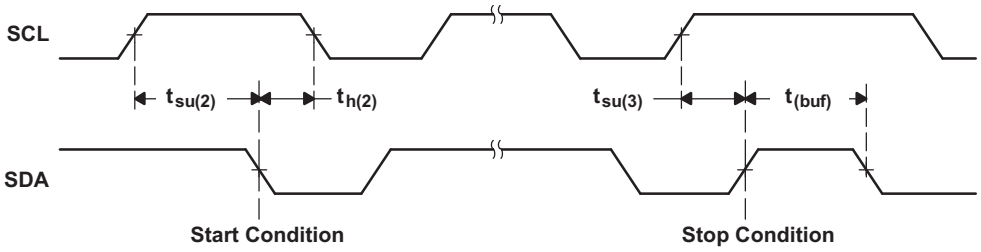
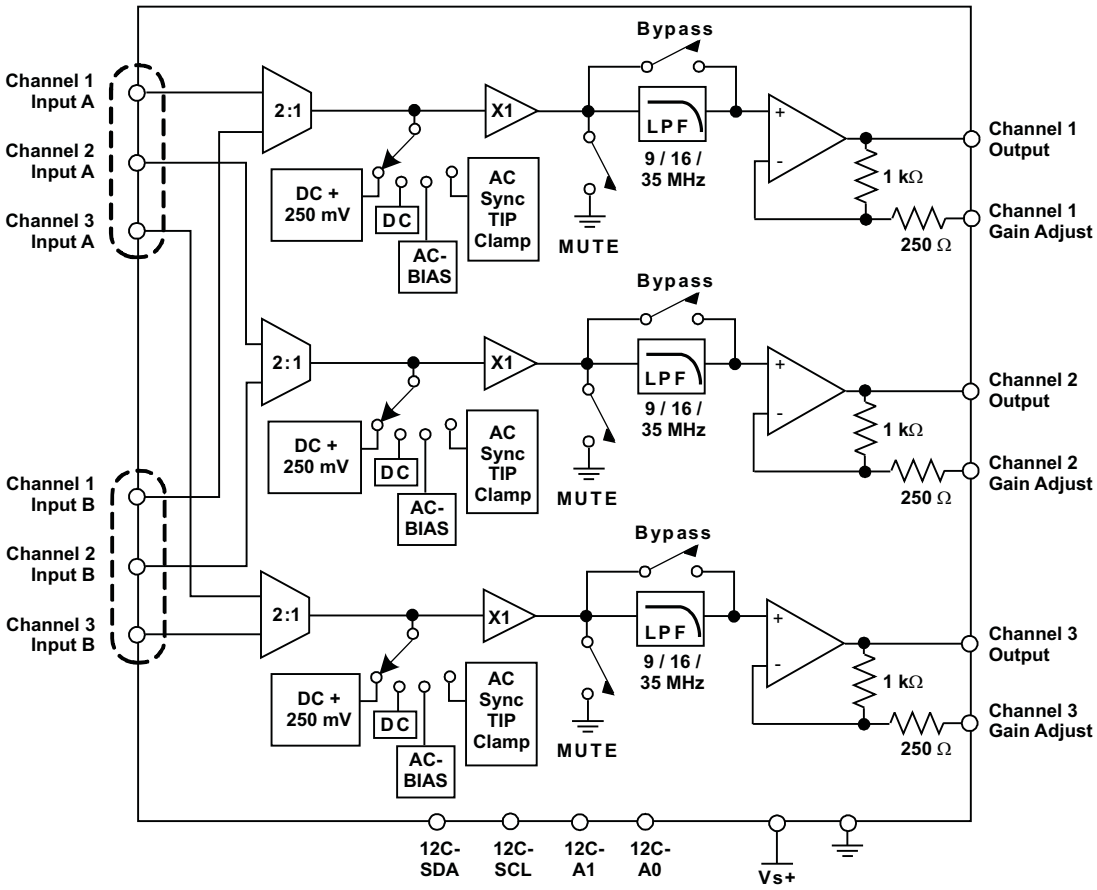


Figure 3. Start and Stop Conditions

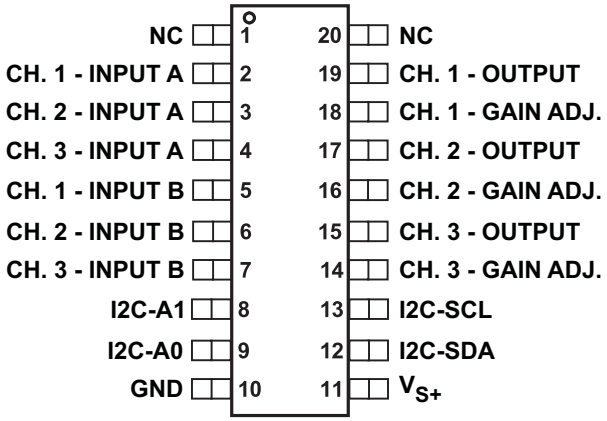
FUNCTIONAL DIAGRAM



NOTE: The I^2C Address of the THS7353 is 01011(A1)(A0)(R/W)

PIN CONFIGURATION

THS7353PW
TSSOP (20-Pin)
(Top View)



A. NC indicates there is no internal connection to these pins. It is recommended, but not required, to connect these pins to GND.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
N/C	1, 20	No Internal Connection. It is recommended, but not required, to connect these pins to GND
CH. 1 – INPUT A	2	Video Input Channel 1. Input A
CH. 2 – INPUT A	3	Video Input Channel 2. Input A
CH. 3 – INPUT A	4	Video Input Channel 3. Input A
CH. 1 – INPUT B	5	Video Input Channel 1. Input B
CH. 2 – INPUT B	6	Video Input Channel 2. Input B
CH. 3 – INPUT B	7	Video Input Channel 3. Input B
I2C-A1	8	I^2C Slave Address Control Bit A1. Connect to Vs+ for a logic 1 preset value or GND for a logic 0 preset value.
I2C-A0	9	I^2C Slave Address Control Bit A0. Connect to Vs+ for a logic 1 preset value or GND for a logic 0 preset value.
GND	10	Ground reference pin for all internal circuitry
V_{S+}	11	Positive Power Supply Input Pin. Connect to 2.7 V to 5 V
SDA	12	Serial data line of the I^2C bus. Pull-up resistor should have a minimum value = 2-kΩ and a maximum value = 19-kΩ. Pull up to Vs+
SCL	13	I^2C bus clock line. Pull-up resistor should have a minimum value = 2-kΩ and a maximum value = 19-kΩ. Pull up to Vs+
CH. 3 – GAIN ADJ.	14	Channel 3 gain adjustment pin. Short to CH. 3 – OUTPUT pin for 0-dB gain. Or add external resistors and/or capacitors to analog ground for signal gain.
CH. 3 – OUTPUT	15	Video output channel 3 from either CH. 3 – INPUT A or CH. 3 – INPUT B
CH. 2 – GAIN ADJ.	16	Channel 2 gain adjustment pin. Short to CH. 2 – OUTPUT pin for 0-dB gain. Or add external resistors and/or capacitors to analog ground for signal gain.
CH. 2 – OUTPUT	17	Video output channel 2 from either CH. 2 – INPUT A or CH. 2 – INPUT B
CH. 1 – GAIN ADJ.	18	Channel 1 gain adjustment pin. Short to CH. 1 – OUTPUT pin for 0-dB gain. Or add external resistors and/or capacitors to analog ground for signal gain.
CH. 1 – OUTPUT	19	Video output channel 1 from either CH. 1 – INPUT A or CH. 1 – INPUT B

TYPICAL CHARACTERISTICS

SMALL-SIGNAL FREQUENCY RESPONSE

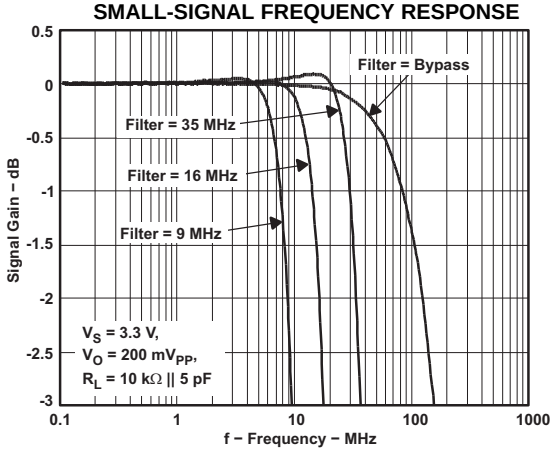


Figure 4.

SMALL-SIGNAL FREQUENCY RESPONSE

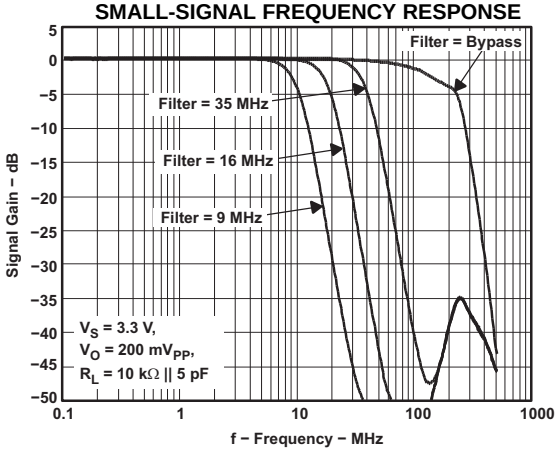


Figure 5.

GROUP DELAY vs FREQUENCY

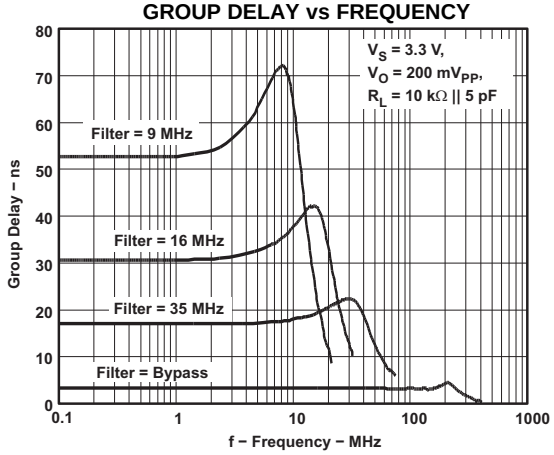


Figure 6.

PHASE RESPONSE vs FREQUENCY

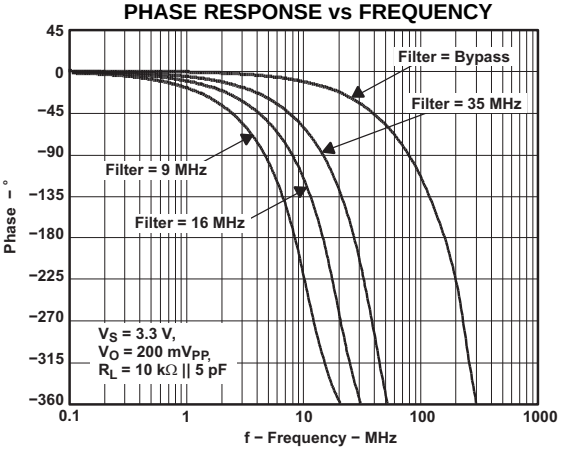


Figure 7.

SMALL AND LARGE-SIGNAL FREQUENCY RESPONSE

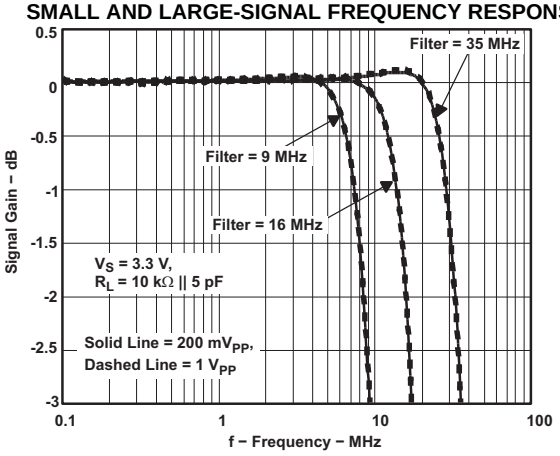


Figure 8.

SMALL AND LARGE-SIGNAL FREQUENCY RESPONSE

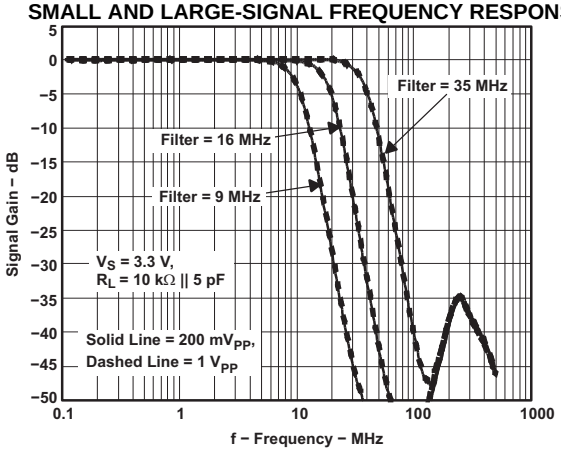


Figure 9.

TYPICAL CHARACTERISTICS (continued)

SMALL AND LARGE-SIGNAL FREQUENCY RESPONSE

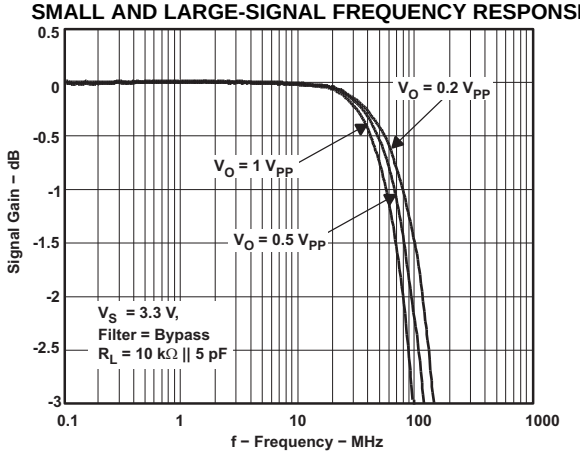


Figure 10.

OUTPUT IMPEDANCE vs FREQUENCY

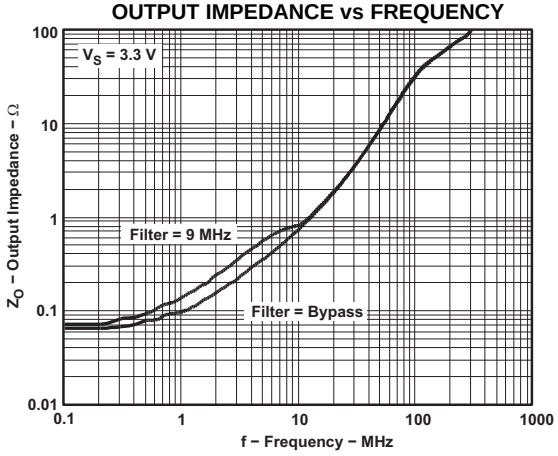


Figure 11.

3.3 V DIFFERENTIAL GAIN

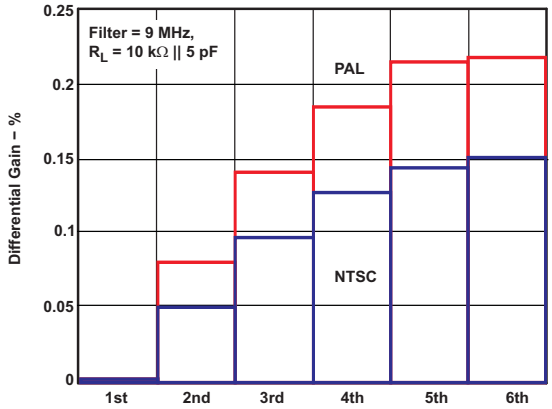


Figure 12.

3.3 V DIFFERENTIAL PHASE

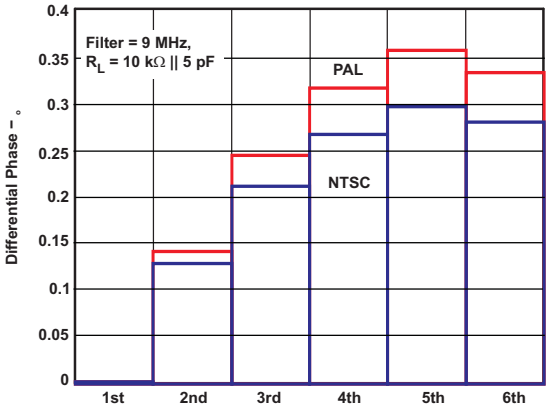


Figure 13.

HD2 vs FREQUENCY

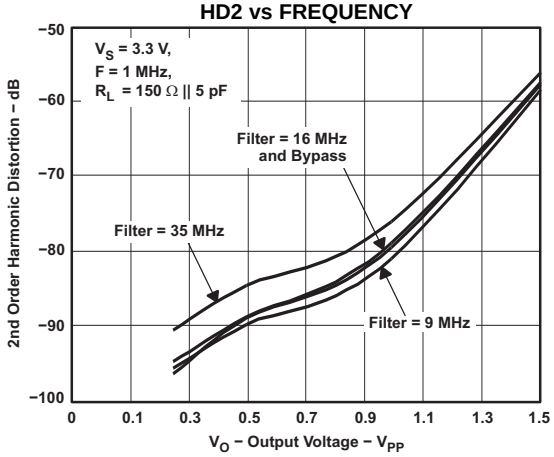


Figure 14.

HD3 vs FREQUENCY

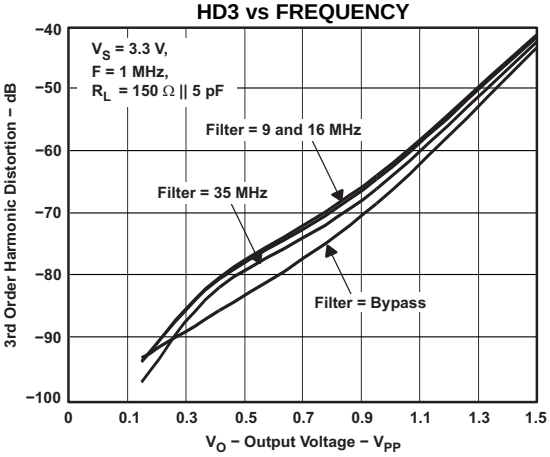


Figure 15.

TYPICAL CHARACTERISTICS (continued)

SMALL-SIGNAL FREQUENCY RESPONSE WITH CAPACITIVE LOADING

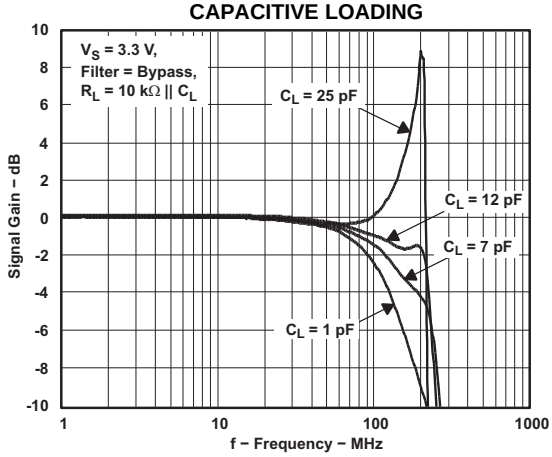


Figure 16.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 1 pF CAPACITIVE LOAD

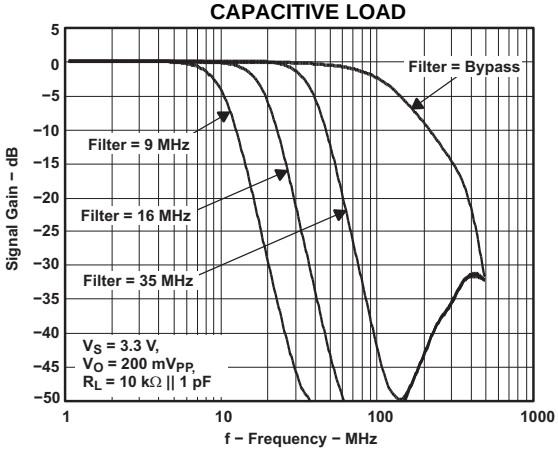


Figure 17.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 12 pF CAPACITIVE LOAD

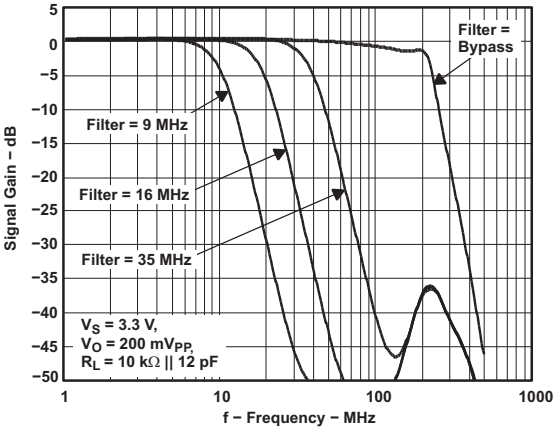


Figure 18.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 25 pF CAPACITIVE LOAD

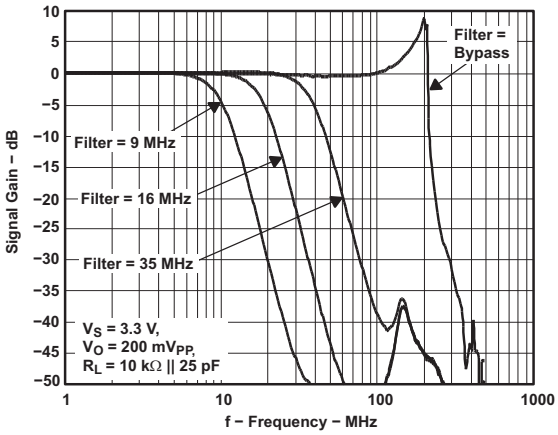


Figure 19.

SMALL-SIGNAL PULSE RESPONSE

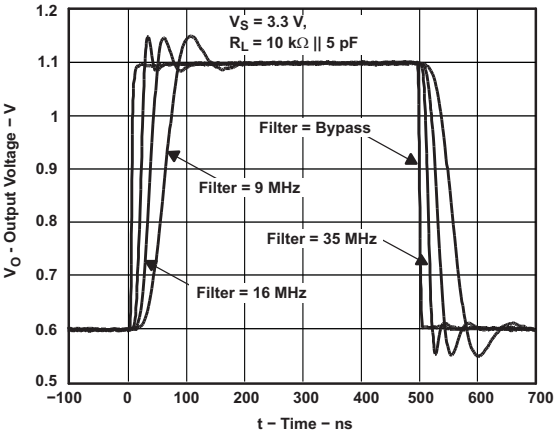


Figure 20.

SLEW RATE vs OUTPUT VOLTAGE

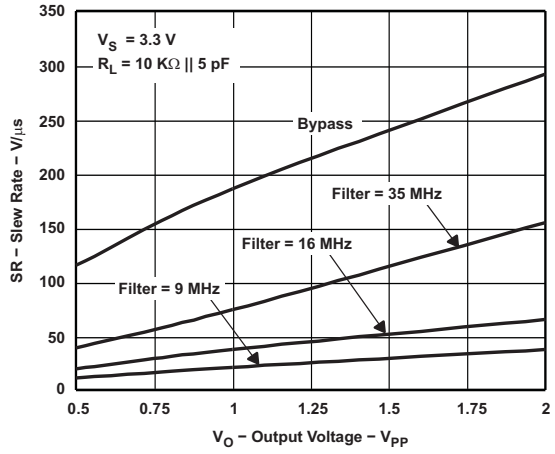


Figure 21.

TYPICAL CHARACTERISTICS (continued)

576p G'B'R' 2T PULSE

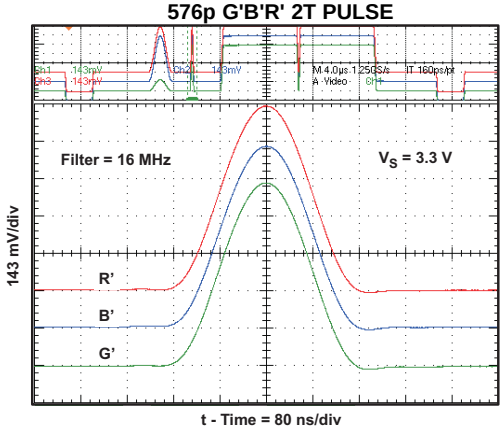


Figure 22.

1080i 2T30 PULSE—INPUT SOURCE

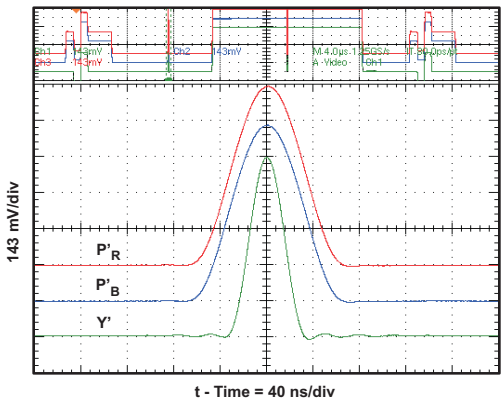


Figure 23.

1080i 2T30 PULSE—OUTPUT

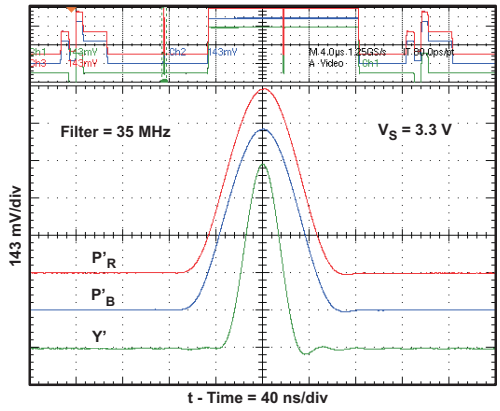


Figure 24.

1080i 2T30 PULSE—OUTPUT

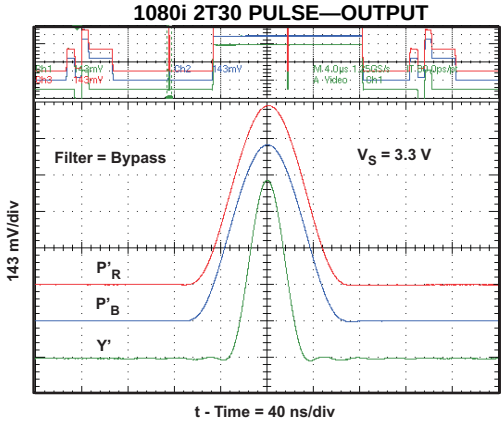


Figure 25.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

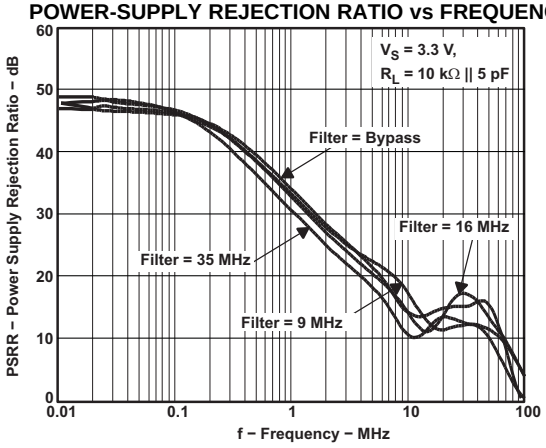


Figure 26.

MUX FEED THROUGH vs FREQUENCY

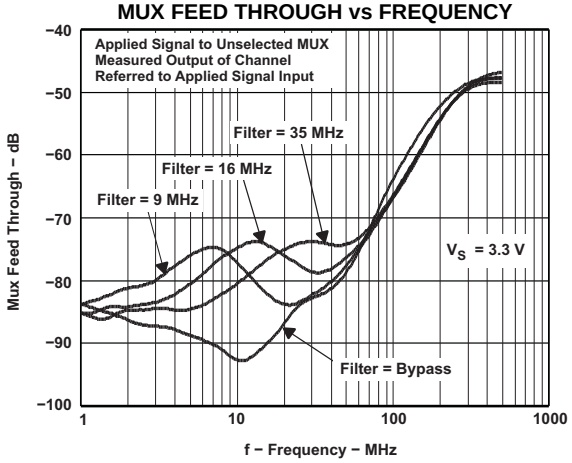


Figure 27.

TYPICAL CHARACTERISTICS (continued)

CROSSTALK vs FREQUENCY

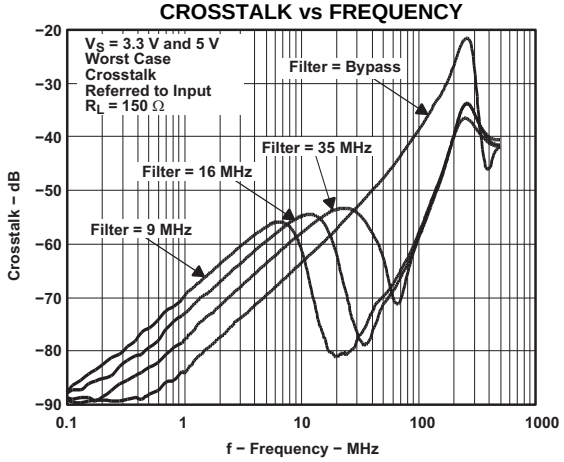


Figure 28.

INPUT BIAS CURRENT vs TEMPERATURE

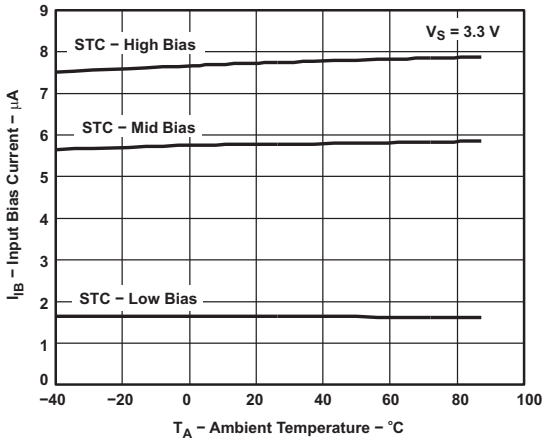


Figure 29.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

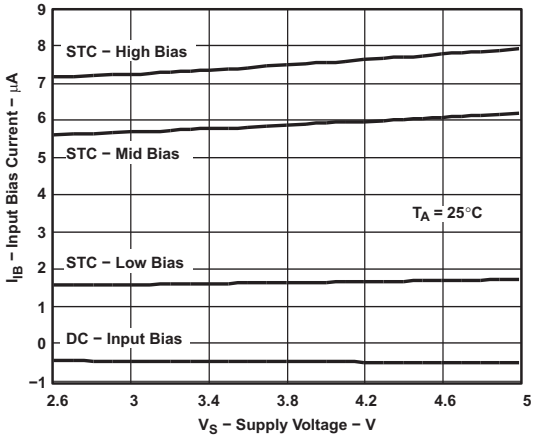


Figure 30.

SMALL-SIGNAL FREQUENCY RESPONSE

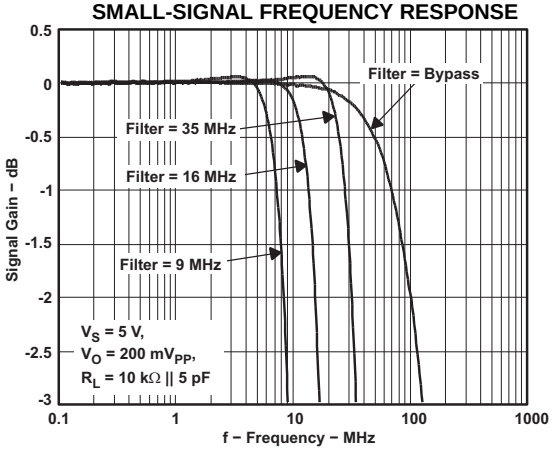


Figure 31.

SMALL-SIGNAL FREQUENCY RESPONSE

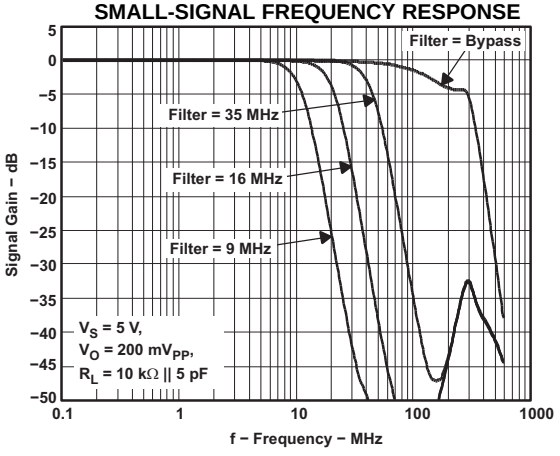


Figure 32.

GROUP DELAY vs FREQUENCY

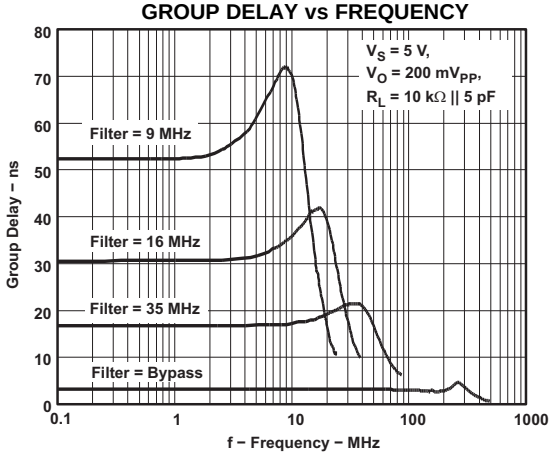


Figure 33.

TYPICAL CHARACTERISTICS (continued)

PHASE vs FREQUENCY

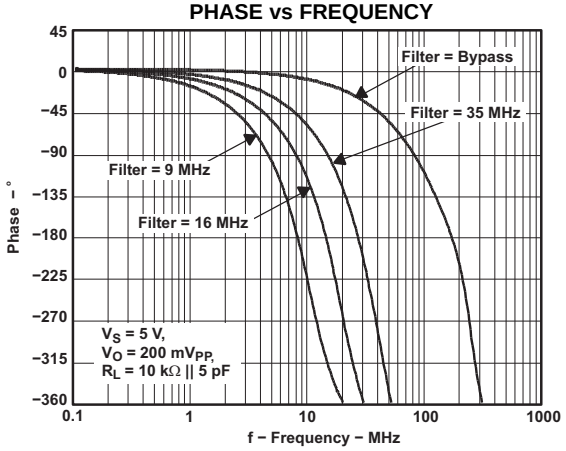


Figure 34.

SMALL- AND LARGE-SIGNAL FREQUENCY RESPONSE

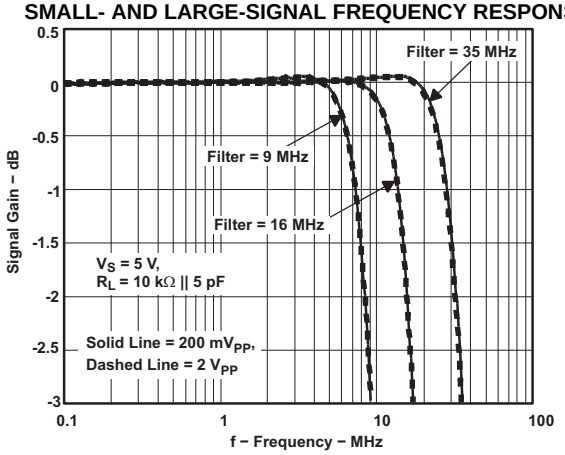


Figure 35.

SMALL- AND LARGE-SIGNAL FREQUENCY RESPONSE

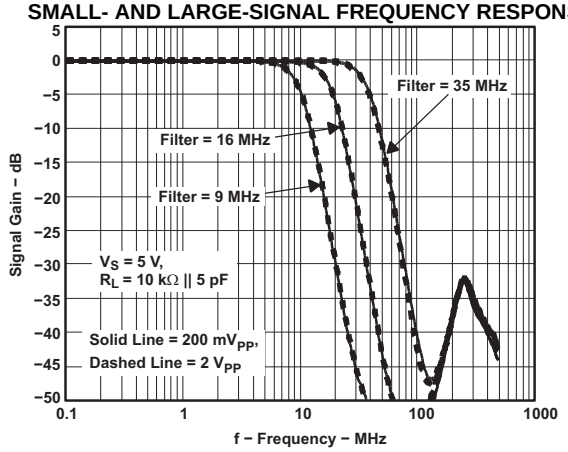


Figure 36.

SMALL- AND LARGE-SIGNAL FREQUENCY RESPONSE

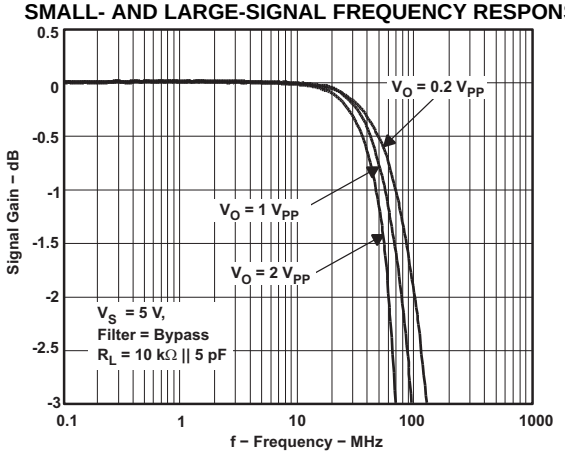


Figure 37.

5 V DIFFERENTIAL GAIN

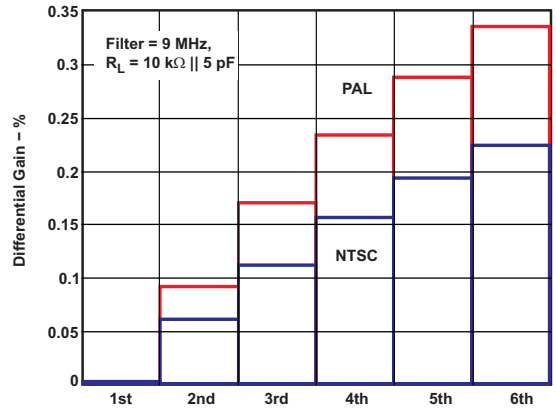


Figure 38.

5 V DIFFERENTIAL PHASE

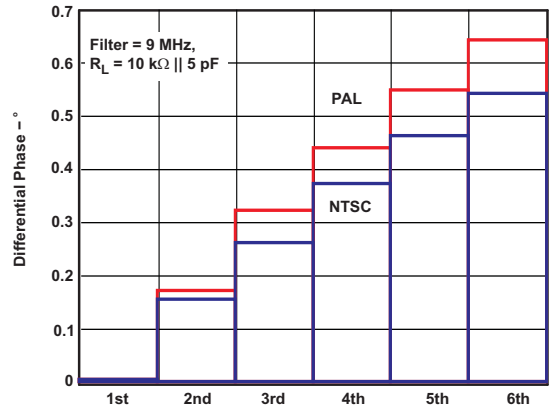


Figure 39.

TYPICAL CHARACTERISTICS (continued)

HD2 vs FREQUENCY

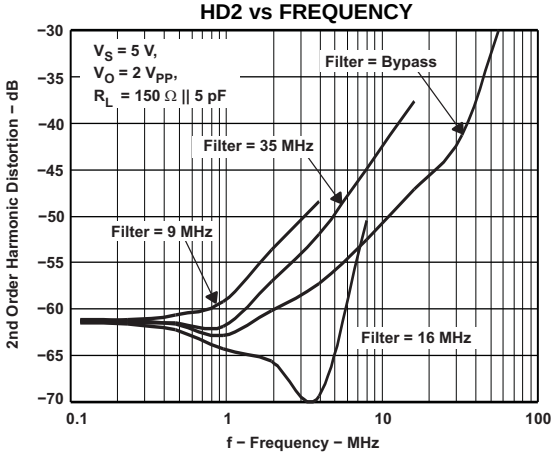


Figure 40.

HD3 vs FREQUENCY

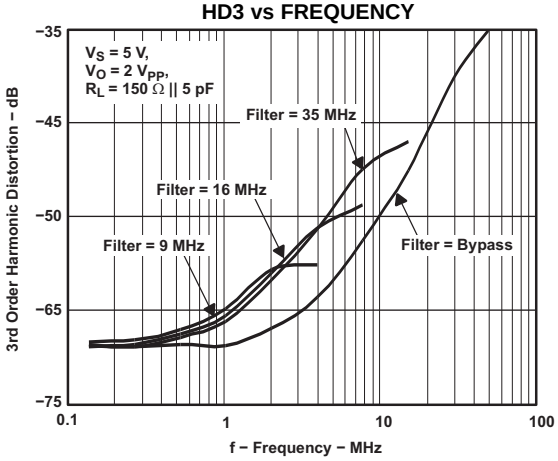


Figure 41.

HD2 vs OUTPUT VOLTAGE

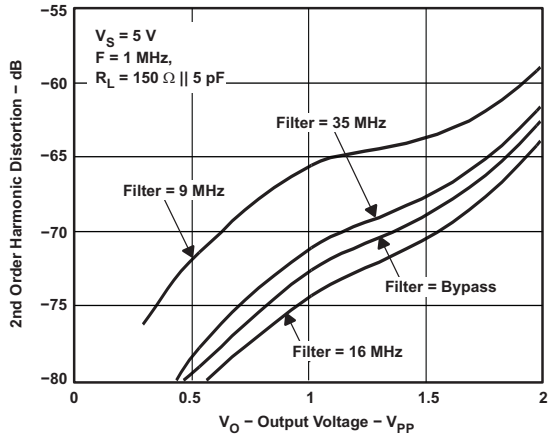


Figure 42.

HD3 vs OUTPUT VOLTAGE

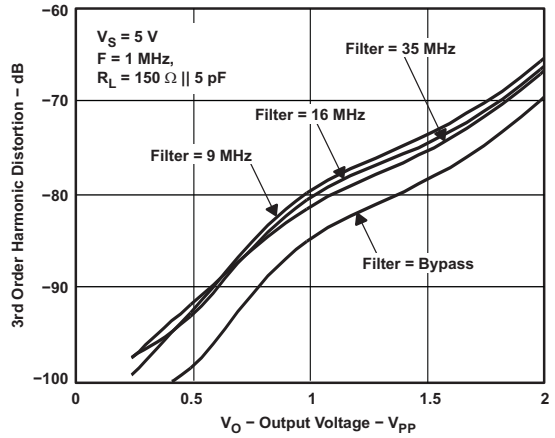


Figure 43.

SMALL-SIGNAL FREQUENCY RESPONSE WITH CAPACITIVE LOADING

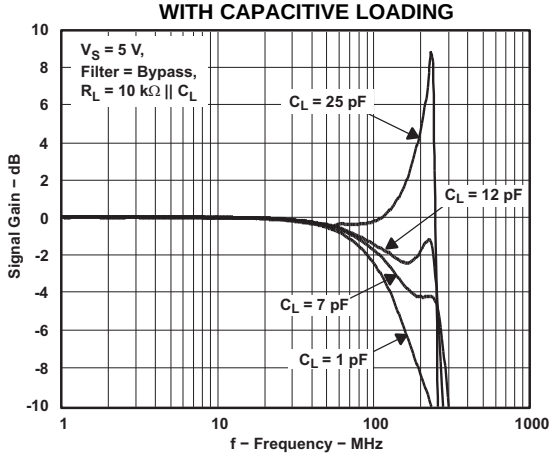


Figure 44.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 1 pF CAPACITIVE LOAD

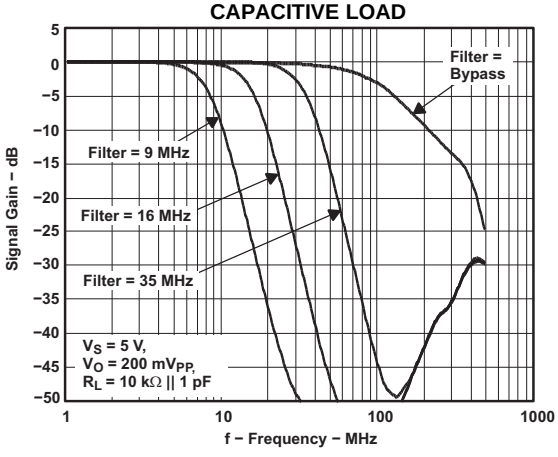


Figure 45.

TYPICAL CHARACTERISTICS (continued)

SMALL-SIGNAL FREQUENCY RESPONSE WITH 12 pF CAPACITIVE LOAD

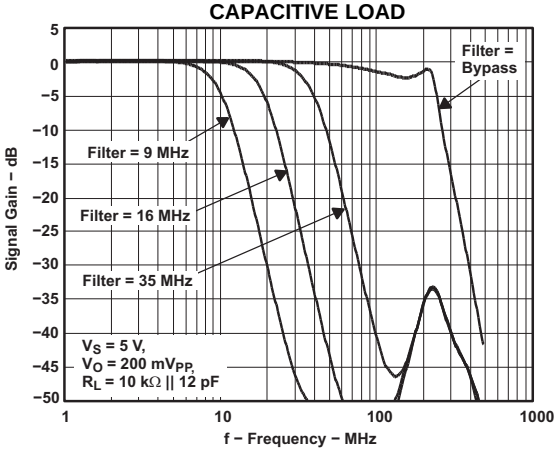


Figure 46.

SMALL-SIGNAL FREQUENCY RESPONSE WITH 25 pF CAPACITIVE LOAD

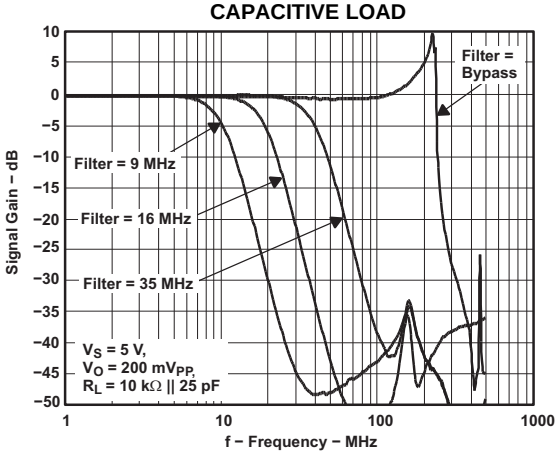


Figure 47.

SMALL SIGNAL PULSE RESPONSE

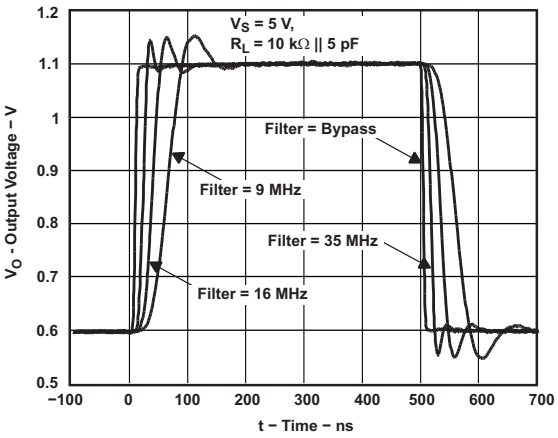


Figure 48.

LARGE SIGNAL PULSE RESPONSE

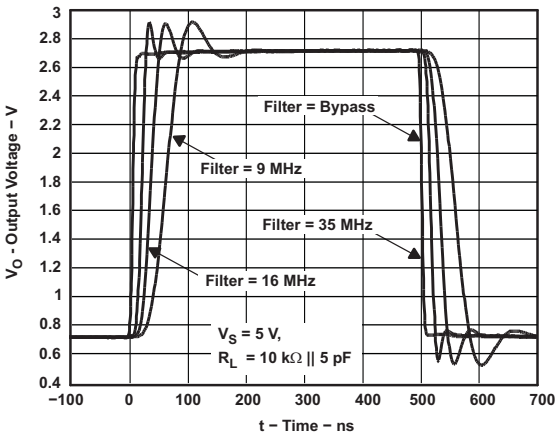


Figure 49.

PAL MULTIPULSE

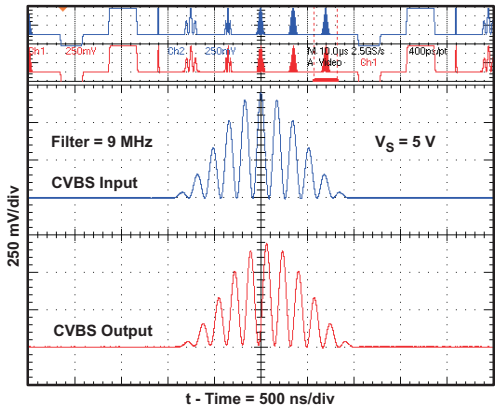


Figure 50.

480i G'B'R' 2T PULSE

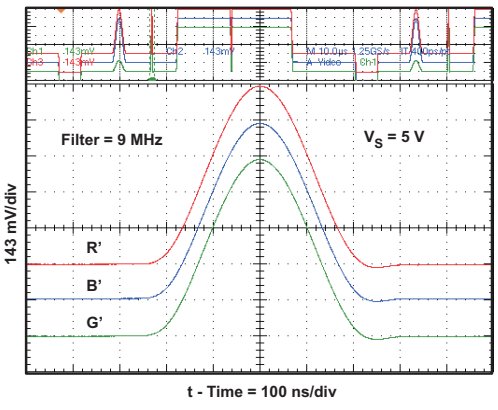


Figure 51.

TYPICAL CHARACTERISTICS (continued)

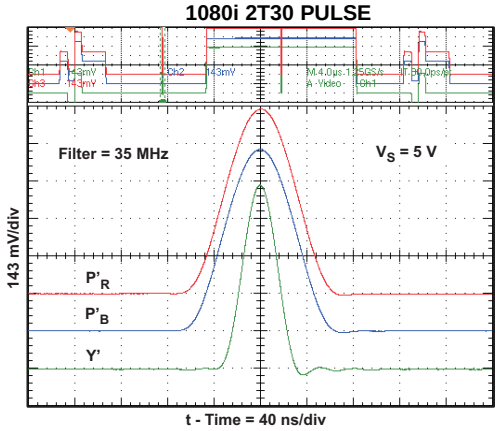


Figure 52.

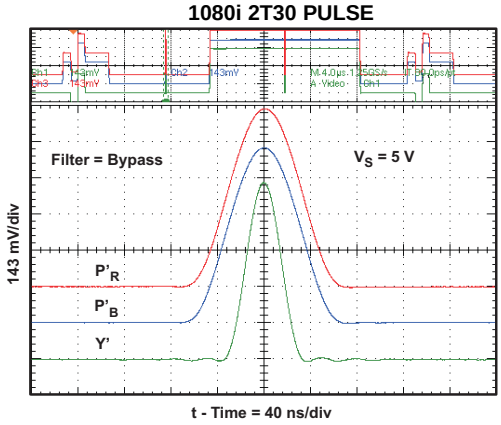


Figure 53.

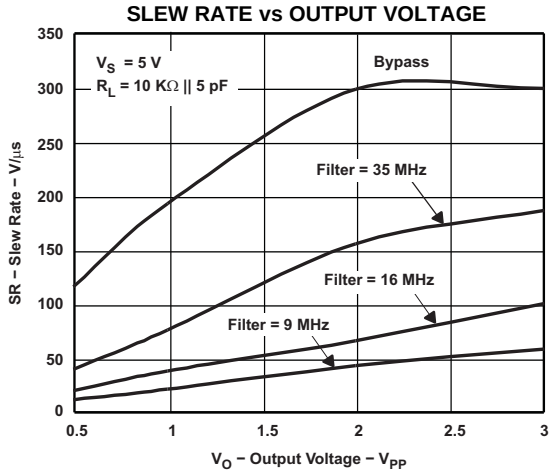


Figure 54.

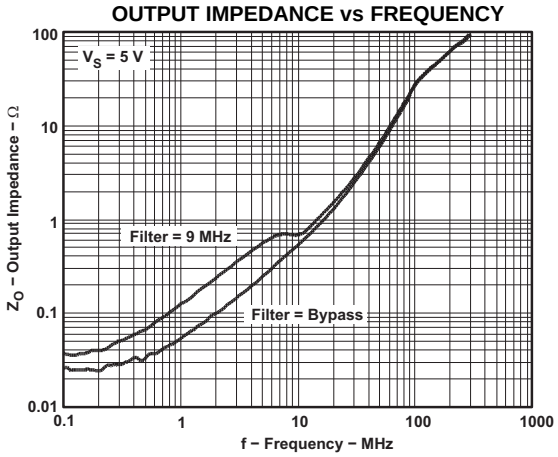


Figure 55.

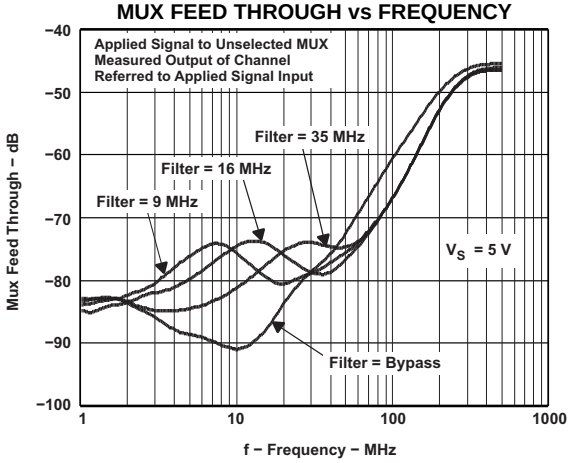


Figure 56.

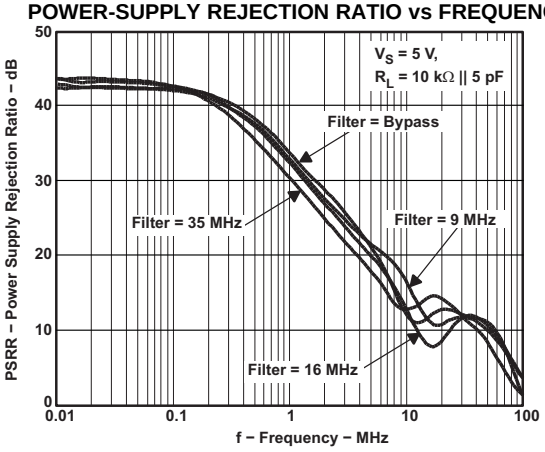


Figure 57.

APPLICATION INFORMATION

The THS7353 is targeted for video output buffer applications. Although it can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters of the THS7353. Built on the complimentary silicon germanium (SiGe) BiCom-3 process, the THS7353 incorporates many features not typically found in integrated video parts while consuming low power. Each channel configuration is completely independent of the other channels. This allows for configurations for each channel to be dictated by the end user and not device. This results in a highly flexible system for most video systems. The THS7353 contains the following features:

- I^2C Interface for easy interfacing to the system with up to 4 addresses.
- Single-supply 2.7-V to 5-V operation with low quiescent current of 16.2-mA with 3.3-V supply and 18.75-mA with 5-V supply.
- 2:1 input MUX.
- Input configuration accepting dc, dc + 250 mV shift, ac bias, or ac sync-tip clamp selection.
- Selectable 5^{th} order, low-pass filter for ADC anti-aliasing image rejection or DAC reconstruction:
  - 9-MHz for SDTV NTSC and 480i, PAL/SECAM and 576i, S-Video, and G'B'R' (R'G'B') signals.
  - 16-MHz for EDTV 480p and 576p $Y'P'_BP'_R$ signals, G'B'R', and VGA signals.
  - 35-MHz for HDTV 720p and 1080i $Y'P'_BP'_R$ signals, G'B'R', and SVGA/XGA signals.
  - Bypass mode for passing HDTV 1080p $Y'P'_BP'_R$, G'B'R', and SXGA/UXGA signals.
- Externally configured gain setting allowing from 0-dB buffering up to 14-dB gain allowing for system loss compensation, high-frequency cable loss compensation, or SinX/X DAC compensation.
- Output can be used with dc coupling or ac coupling.
- Disable mode which reduces quiescent current to as low as 0.1-µA or a mute function that keeps the THS7353 powered on, but does not allow a signal to pass through.
- Signal flow-through configuration using a 20-pin TSSOP package that complies with the latest lead-free (RoHS compatible) and green manufacturing requirements.

OPERATING VOLTAGE

The THS7353 is designed to operate from 2.7 V to 5 V over a -40°C to 85°C temperature range. The impact on performance over the entire temperature range is negligible due to the implementation of thin film resistors and low-temperature coefficient capacitors.

The power supply pins should have a 0.1-µF to 0.01-µF capacitor placed as close as possible to these pins. Failure to do so may result in the THS7353 outputs ringing or oscillating. Additionally, a large capacitor, such as 22µF to 100 µF, should be placed on the power supply line to minimize issues with 50/60 Hz line frequencies.

INPUT VOLTAGE

The THS7353 input range allows for an input signal range from Ground to (V_{S+} – 1.4 V). But, if the gain is configured to be greater than 0 dB, the output voltage swing range is generally the limiting factor for the allowable linear input range. For example, with a 5-V supply and a gain set to 6 dB, the linear input range is from GND to 3.6 V. But due to the gain, the linear output range limits the allowable linear input range to be from GND to a maximum of 2.5 V.

The THS7353 operates down to 2.7-V. But, due to the input voltage range limitation, the signal may clip. For example, with ac-bias selected, the bias point is about 1 V with 3.3-V supply. Under certain video signal conditions, the signal may clip with this mode due strictly to the input voltage range.

INPUT OVERVOLTAGE PROTECTION

The THS7353 is built using a high-speed complementary bipolar and CMOS process. The internal junction breakdown voltages are low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 58.

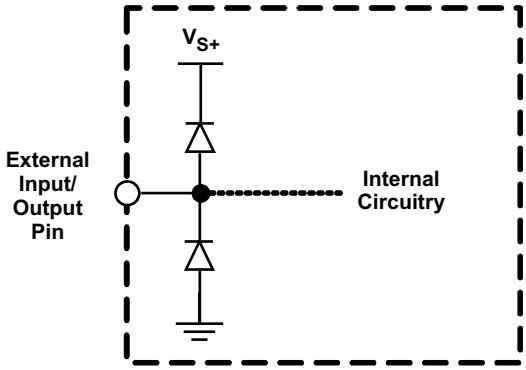


Figure 58. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above and below the supplies. The protection diodes can typically support 30-mA of continuous current when overdriven.

TYPICAL CONFIGURATION and VIDEO TERMINOLOGY

A typical application circuit using the THS7353 as a video input buffer is shown in Figure 59. It shows the A-channel inputs of the THS7353 buffering and filtering a set of HDTV inputs and driving a video ADC / decoder. Although the high-definition video (HD) or enhanced-definition (ED) $Y'P'_BP'_R$ (sometimes labeled Y'U'V' or incorrectly labeled $Y'C'_BC'_R$) channels are shown, these channels can easily be S-Video Y'/C' channels and the composite video baseband signal (CVBS) of a standard definition video (SD) system. These signals can also be G'B'R' (R'G'B') signals or other variations. Note that for computer signals the sync should be embedded within the signal for a system with only 3-signals. This is sometimes labeled as R'G'sB' (sync on green) or R'sG'sB's (sync on all signals).

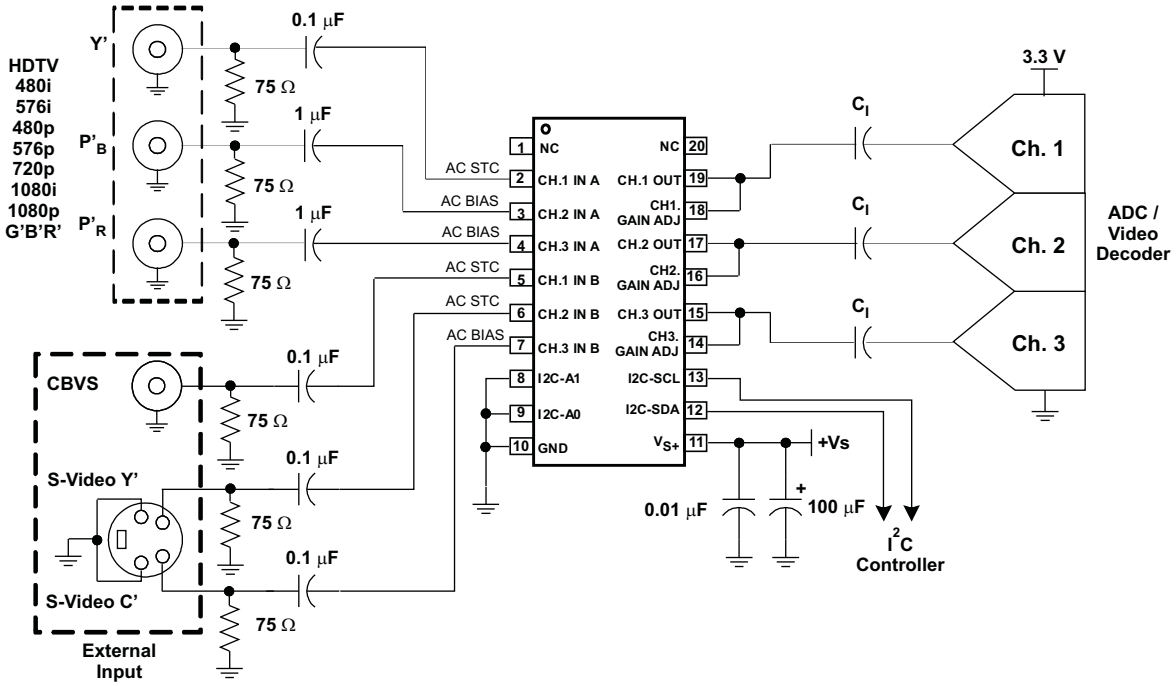
The second set of inputs (B-Channels) shown can be HD, ED, SD, or G'B'R' video signals. The THS7353's flexibility allows for almost any input signal to be driven into the THS7353 regardless of the other set of inputs. Simple control of the I^2C configures the THS7353. For example, the THS7353 can be configured to have Channel 1 Input connected to input A while Channels 2 and 3 are connected to input B. See the various sections explaining the I^2C interface later in this data sheet.

Note that the Y' term is used for the luma channels throughout this document rather than the more common luminance (Y) term. The reason is to account for the definition of luminance as stipulated by the CIE (International Commission on Illumination). Video departs from true luminance since a nonlinear term, gamma, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus luminance (Y) is not maintained requiring a difference in terminology.

This rationale is also used for the chroma (C') term. Chroma is derived from the non-linear R'G'B' terms and thus it is nonlinear. Chrominance (C) is derived from linear RGB giving the difference between chroma (C') and chrominance (C). The color difference signals (P'_B / P'_R / U' / V') are also referenced this way to denote the nonlinear (gamma corrected) signals.

R'G'B' (commonly mislabeled RGB) is also called G'B'R' (again commonly mislabeled as GBR) in professional video systems. The SMPTE component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This is consistent with the $Y'P'_BP'_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be

placed first in the system. Since the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel respectfully. Thus hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems sync is embedded on all three channels, but may not always be the case in all systems.



A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-µF capacitor in parallel with these large capacitors.

Figure 59. Typical HDTV + SDTV Inputs Buffering a Video ADC / Decoder

INPUT MODES OF OPERATION – DC

The inputs to the THS7353 allows for both ac coupled and dc coupled inputs. Many DACs or video encoders can be dc connected to the THS7353. But, one of the drawbacks to dc coupling is when 0 V is applied to the input of the THS7353. Although the input of the THS7353 allows for a 0-V input signal, the output swing of the THS7353 cannot yield a 0-V signal. This applies to any traditional single-supply amplifier due to the limitations of the output transistors. Both CMOS and bipolar transistors cannot go to 0 V while sinking a finite amount of current. This trait of a transistor is also the same reason why the highest output voltage is always less than the power supply voltage when sourcing a significant amount of current.

The signal gain is externally set from 0 dB (1 V/V) to 14 dB (5 V/V), and dictates what the allowable linear input voltage range or output voltage range is without clipping concerns. For example, if the power supply is set to 3 V with gain set to 6 dB, the maximum output is about 2.9 V. Thus, to avoid clipping, the allowable input is 2.9 V / 2 = 1.45 V. This is true for a 5-V power supply that allows about a 4.9 V / 2 = 2.45 V input range while avoiding clipping on the output. But, if the gain is set to 0 dB, the allowable input range is dictated by the input range and not the output range. This is about 2.1-V for a 3.3-V supply and 3.4-V for a 5-V supply.

The input impedance of the THS7353 in this mode of operation is >1 MΩ. This is due to the input buffer being configured as a unity gain amplifier as shown in Figure 60.

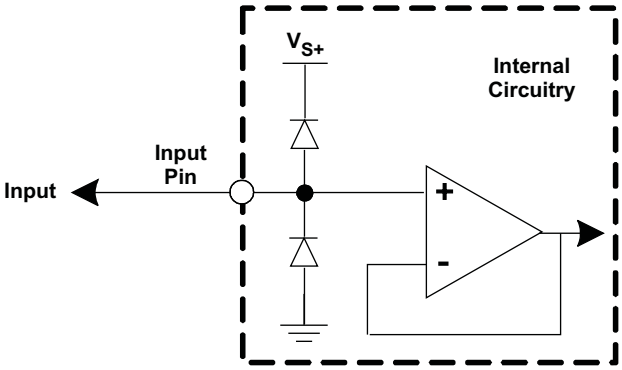


Figure 60. Equivalent DC Input Mode Circuit

The input stage of the THS7353 is designed with PNP bipolar transistors. Thus, there is a finite amount of bias current flowing *out* of the THS7353 input pin. This bias current, typically about 0.6 µA, must have a path to flow or else the input stage voltage increases. For example, if there is a 1-MΩ resistance to ground on the input node, the resulting voltage appearing at the input node is 0.6 µA × 1 MΩ = 0.6 V. Therefore, it should be noted that if a channel is powered on and has no input termination, the input bias current causes the input stage to *float* high until saturation of the input stage exists, about 1.4 V from the power supply. Typically, this is not a concern as most terminations result in an equivalent source impedance of 37.5 Ω if connected or 75 Ω if unconnected.

INPUT MODES OF OPERATION – DC + 250 mV SHIFT

Output clipping occurs with a 0-V applied input signal when the input mode is set to dc. The clipping can reduce the sync amplitudes (both horizontal and vertical sync amplitudes) on the video signal. A problem occurs if the receiver of this video signal uses an AGC loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much, resulting in too much luma and/or chroma amplitude gain correction. This may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits use the chroma burst amplitude for amplitude control, and a reduction in the sync signals does not alter the proper gain setting. But, it is good engineering design practice to ensure saturation/clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations on the signals.

To eliminate saturation / clipping problems, the THS7353 has a dc + 250 mV shift input mode. This mode takes the input voltage and adds an internal +250 mV shift to the signal. This shift cannot be measured at the input pin because it is internal, thus, it does not impact the source in any way. Because the THS7353 also has a default gain of 0 dB (1 V/V), the resulting output with a 0-V applied input signal is 250 mV. The THS7353 rail-to-rail output stage creates this level while connected to a typical load. This ensures that no saturation / clipping of the sync signals occurs. This is a constant shift regardless of the input signal. For example, if a 1-V is applied to the input the output is at 1.25 V.

As with the dc-input mode, the input impedance of the THS7353 is > 1 MΩ. Additionally, the same input bias current of about 0.6 µA appears at the input. Following the same precautions as stipulated with the dc-input mode of operation minimizes any potential issues.

Figure 61 shows the equivalent input circuit while in the dc + 250 mV shift mode of operation.

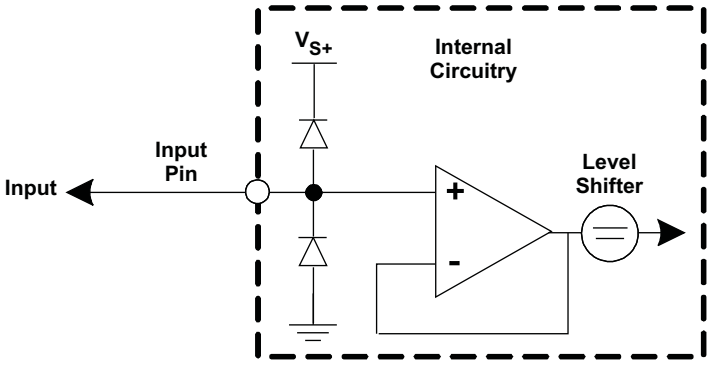


Figure 61. Equivalent DC + 250 mV Input Mode Circuit

INPUT MODES OF OPERATION – AC BIAS

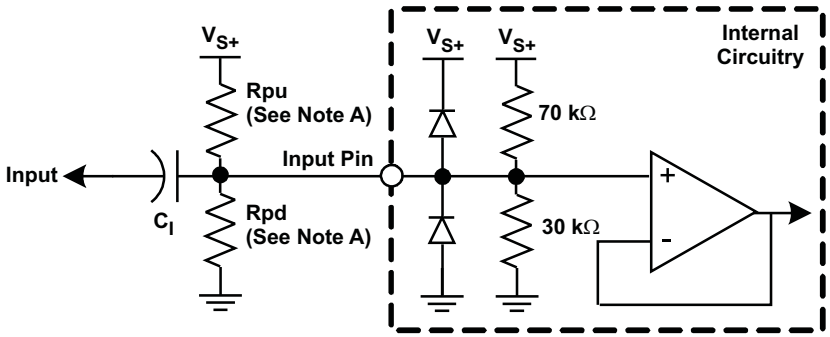
Other applications require an ac-coupled input. The ac coupling ensures that a dc input level does not alter, or clip, the resulting output video signal, and it also allows the THS7353 to re-establish its own dc-operating point. The first ac-coupling mode is the ac-bias mode where a simple internal dc-bias voltage is applied to the input signal on the THS7353 side of the external coupling capacitor.

The applied dc bias voltage is set internally by a simple resistor divider circuit as shown in Figure 62. The dc bias voltage is set to $V_{S+} \div 3.3$. With a 3.3-V power supply, the input bias voltage is nominally 1 V and with 5-V supply, the input bias voltage is nominally 1.5 V. The input impedance with this mode is approximately 21-kΩ. With a 1-µF input capacitor, it sets a high-pass corner frequency of about 7.6-Hz. If a lower frequency is desired, increasing the capacitor decreases the corner frequency proportionally. For example, using a 4.7-µF capacitor results in a 1.6-Hz high pass corner frequency, and results in lower droop (tilt). Using any capacitor value is acceptable for this mode of operation.

It is sometimes desirable to adjust the bias voltage to another level other than the one dictated by the internal resistors. There are two ways this is accomplished:

1. The first is to add an external resistor between the input pin and either the $+V_S$ or GND. This creates a new bias voltage equal to +Vs × [30 k / {30 k + (70 k || R_{PU})}] for raising the bias voltage, or +Vs × [(30 k || Rpd) / {(30 k || Rpd) + 70 k}] for reducing the bias voltage.
2. The second method to set the AC-Bias voltage is to use the Rpu and Rpd external resistors, but place the THS7353 in dc input bias mode. Since the dc mode is very high impedance, the resulting bias voltage is equal to +Vs × (Rpd / {Rpd + Rpu}).

This ac-bias mode is recommended for use with chroma (C'), P'_B, P'_R, U', V', and other nonsync signals.



NOTE: Use external pull-up and/or pull-down resistors if changing the AC-bias input voltage is desired.

Figure 62. Equivalent AC Bias Input Mode Circuit

INPUT MODES OF OPERATION – AC SYNC TIP CLAMP

The last input mode of operation is the ac with sync-tip-clamp (STC) which also requires a capacitor in series with the input. Note that while the term sync-tip-clamp is used throughout this document, the THS7353 is better termed as a dc restoration circuit based on the way this function is performed. This circuit is an active clamp circuit and not a passive diode clamp function. This function should be used when ac coupling is desired with signals that have sync signals embedded such as CVBS, Y', and G' signals.

The input to the THS7353 has an internal control loop which sets the lowest input applied voltage to clamp at approximately 250 mV. If the input signal tries to go below the 250-mV level, the internal control loop of the THS7353 sources up to 2 mA of current to increase the input voltage level on the THS7353 input side of the coupling capacitor. As soon as the voltage goes above the 250-mV level, the loop stops sourcing current.

One of the concerns about the sync-tip-clamp level is how the clamp reacts to a sync edge that has overshoot – common in VCR signals or reflections found in poor PCB layouts or poor cables. Ideally the STC should not react to the overshoot voltage of the input signal. Otherwise, this could result in clipping on the rest of the video signal because there may be too much increase of the bias voltage.

To help minimize this input signal overshoot problem, the patent-pending internal STC control loop in the THS7353 has an I^2C selectable low-pass filter as shown in Figure 63. This filter can be selected to be about 500 kHz, 2.5 MHz, or 5 MHz. The 500-kHz filter is useful when the THS7353's 5^{th}-order low pass filter is selected for 9-MHz operation. The effect of this filter is to slow down the response of the control loop so as not to clamp on the input overshoot voltage, but rather the flat portion of the sync signal when the ringing should be settled out. The 2.5-MHz filter is best suited for use in conjunction with the 16-MHz signal LPF to account for the faster sync times associated with the higher rate video signals. For HDTV signals, the 5-MHz STC filter should be selected to allow for the faster sync rates to properly set the clamp level. Any STC filter can be selected by the user regardless of the signal or system filter.

As a result of this selectable delay, the sync has an apparent voltage shift occurring between 150 ns and 2 µs after the sync falling edge – depending on the STC LPF. The amount of shift is dependant upon the amount of droop in the signal as dictated by the input capacitor and the STC input bias current selection. Because the sync is primarily for timing purposes with syncing occurring on the edge of the sync signal, this shift is transparent in most systems. Note that if the source signal is known to be good, selecting the 5-MHz STC LPF is recommended for all sources.

While this feature may not fully eliminate overshoot issues on the input signal in case of really bad overshoot and/or ringing, the STC system should help minimize improper clamping levels. As an additional method to help minimize this issue, an external capacitor (example: 10 pF to 47 pF) to ground in parallel with the external termination resistors can help filter overshoot problems.

It should be noted that this STC system is dynamic and does not rely upon timing in any way. It only depends on the voltage appearing at the input pin at any given point in time. The STC filtering helps minimize level shift problems associated with switching noises or very short spikes on the signal line. This helps ensure a robust STC system.

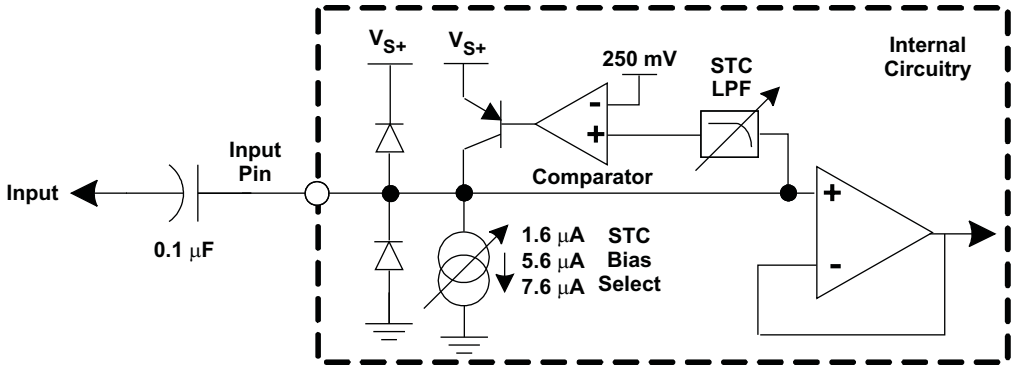


Figure 63. Equivalent AC Sync Tip Clamp Input Mode Circuit

When the ac sync-tip-clamp (STC) operation is used, there must also be some finite amount of discharge bias current. As previously described, if the input signal goes below the 250-mV clamp level, the internal loop of the THS7353 sources current to increase the voltage appearing at the input pin. As the difference between the signal level and the 250-mV reference level increases, the amount of source current increases proportionally – supplying up to 2-mA of current. Thus the time to re-establish the proper STC voltage can be fast. If the difference is small, then the source current is also small to account for the minor voltage droop.

But, what happens if the input signal goes above the 250-mV input level? The active video signal is always above this level and must not be altered in any way. But if the Sync level of the input signal is above this 250-mV level, then the internal discharge (sink) current reduces the ac-coupled bias signal to the proper 250-mV level.

This discharge current must not be large enough to alter the video signal appreciably or picture quality issues may arise. This is often seen by looking at the tilt (droop) of a constant luma signal being applied, and looking at the resulting output level. The associated change in luma level from the beginning of the video line to the end of the video line is the amount of line tilt (droop). The amount of tilt can be seen by the general formula:

$$I = C\ dV/dt$$

where I is the discharge current and C is the external coupling capacitor which is typically 0.1 µF. If the current (I) and the capacitor (C) are constant, then the tilt is governed by:

$$I/C = dV/dt$$

If the discharge current is small the amount of tilt is low which is good. But, the amount of time for the system to capture the sync signal could be too long. This is also termed *hum* rejection. Hum arises from the ac line voltage frequency of 50 Hz or 60 Hz which may have been inadvertently coupled into the video signal line. The value of the discharge current and the ac-coupling capacitor combine to dictate the hum rejection and the amount of line tilt.

Because many users have different thoughts as to the proper amount of hum rejection and line tilt, the THS7353 has incorporated a variable sink bias current selectable through the I^2C interface. The low bias mode selects about 1.6-µA of dc sink bias current for low line tilt. But, if more hum rejection is desired then selecting the mid bias mode increases the dc sink bias current to about 5.8 µA. For severe environments, the high bias mode has about 7.4 µA of dc sink bias current. This drawback to these higher bias modes is an increase in line tilt, but with an increase in hum rejection. The other method to change the hum rejection and line tilt is to change the input capacitor used. An increase in the capacitor from 0.1 µF to 0.22 µF decreases the hum rejection and line tilt by a factor of 2.2. A decrease of this input capacitor accomplishes the opposite effect. Note that the amplifier input bias current of nominally 0.6 µA has already been taken into account when stipulating the 1.6µA/5.8µA/7.4µA current sink values.

To ensure proper stability of the AC STC control loop, the source impedance must be less than 600-Ω and the input capacitor must be greater than 0.01 µF. Otherwise, there is a possibility of the control loop ringing. The ringing appears on the output of the THS7353. Similar to the dc modes of operation, many DACs and encoders use a resistor to establish the output voltage. These resistors are typically less than 300 Ω. Alternatively, if the source is from a video line, the line is terminated with a 75-Ω resistor which should always be in place. Thus, stability of the AC STC loop is ensured. But, if the source impedance looking from the THS7353 input perspective is high or open, then adding a 500-Ω or lower resistor to GND ensures proper operation of the THS7303.

If a MUX channel is not required in the system, then it is recommended to place a 75-Ω resistor to GND. This is not required, but it helps minimize any potential issues.

OUTPUT MODES OF OPERATION – DC COUPLED

The THS7353 incorporates a rail-to-rail output stage that can be used to drive the line directly without the need for large ac-coupling capacitors. This is shown in Figure 64. This offers the best line tilt and field tilt (or droop) performance since there is no ac coupling occurring. Keep in mind that if the input is ac coupled, then the resulting tilt due to the input ac coupling is still seen on the output regardless of the output coupling. The 70-mA output current drive capability of the THS7353 drives a 75-Ω load while keeping the output dynamic range as wide as possible.

One concern of dc coupling is if the line is terminated to ground. When the ac-bias input mode is selected, the output of the THS7353 is $+V_S \div 3.3$. This allows a dc current path to exist which results in a decreased high output voltage swing culminating in an increase in power dissipation of the THS7353. The THS7353 is designed to operate with a junction temperature of up to 125°C. Care must be taken to ensure that the junction temperature does not exceed this level, or long term reliability could suffer. Although this configuration adds less than 10 mW of power dissipation per channel, the overall low power dissipation of the THS7353 design minimizes potential thermal issues when using the TSSOP package at high ambient temperatures.

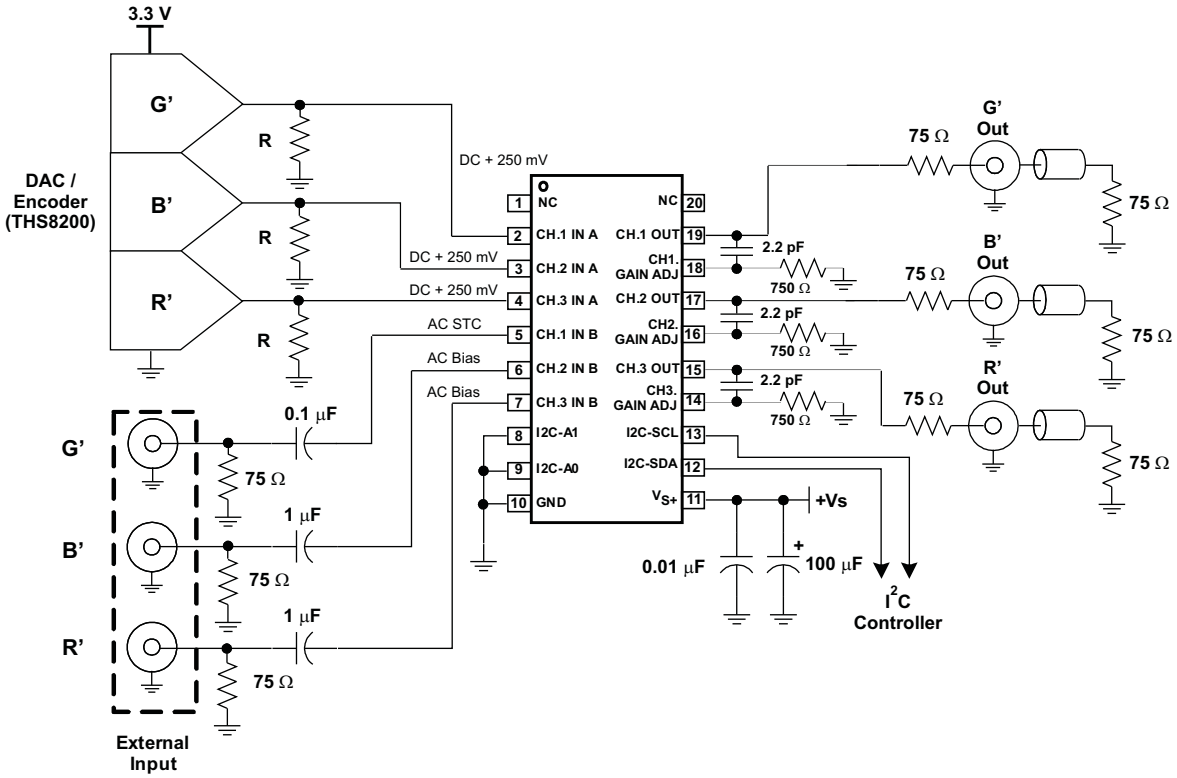


Figure 64. G'B'R' (R'G'B') System with 6-dB Gain and DC-Coupled Driving

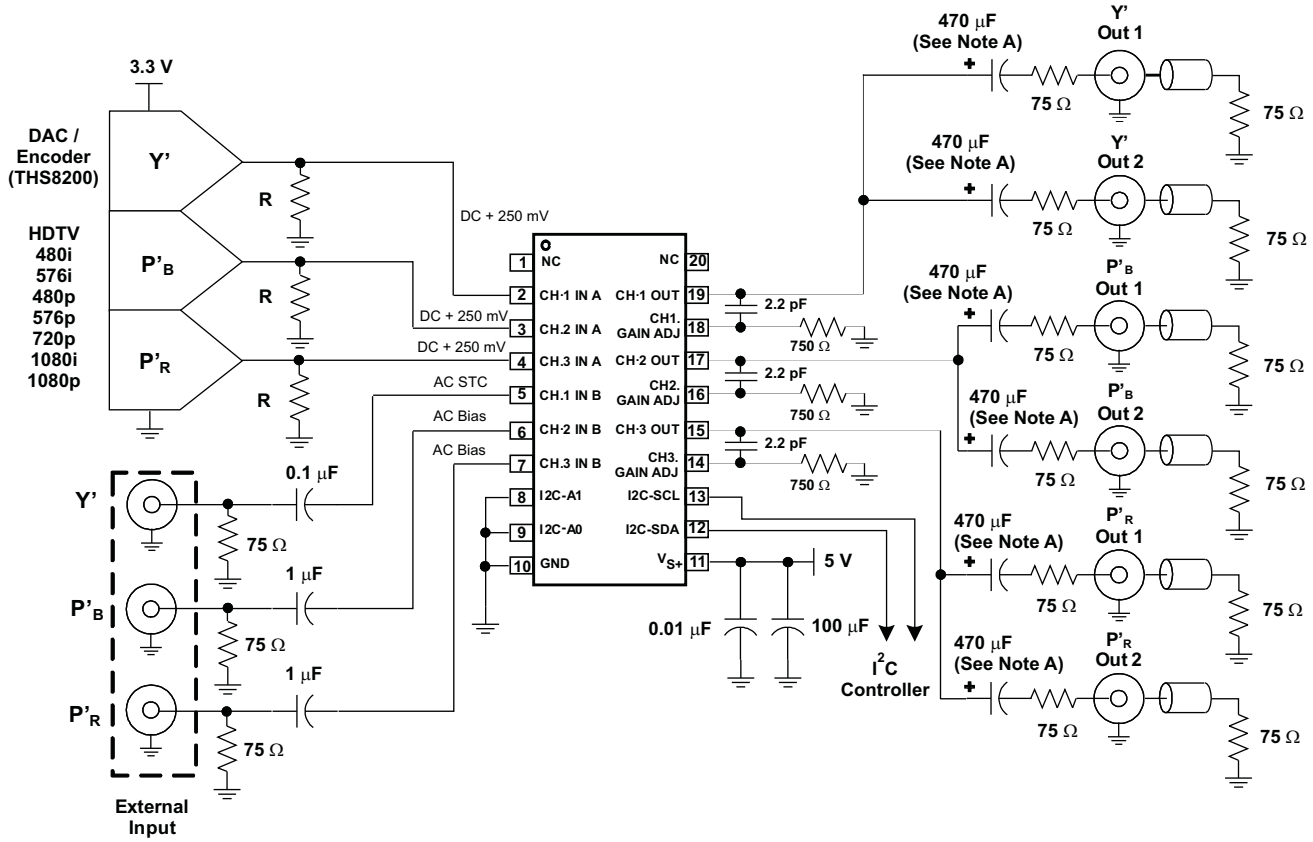
Note that the THS7353 drives the line with dc coupling regardless of the input mode of operation. The only caution is when driving capacitive loads. This capacitive loading includes both the PCB stray capacitance and possibly an ADC input capacitance which is typically between 5-pF and 10-pF. The THS7353 is designed to drive up to 15-pF loads without any issues. But, if the total capacitive loading is 20-pF or more, then it is recommended to place a series resistance at the output of the THS7353. The value of the resistor depends on the capacitive load and can vary from 10 Ω to 75 Ω. If the THS7353 is used to drive a video line, then the obvious use of a 75-Ω resistor ensures stability. Failure to isolate large capacitive loads may result in instabilities with the output buffer potentially causing ringing or oscillations to appear.

OUTPUT MODES OF OPERATION – AC COUPLED

A common method of coupling the video signal to an ADC or video decoder is with the use of a 0.1-µF to 1-µF decoupling capacitor. The low 0.8-Ω at 10-MHz output impedance of the THS7353 allows driving an ADC directly without worrying about possible *kick-back* current from the ADC. Additionally, the THS7353 can be used to drive a video line which is common when using a large capacitor. This large capacitor is typically between 220 µF and 1000 µF, although 470 µF is most common. This value of this capacitor must be this large to minimize the line tilt (droop) and/or field tilt associated with ac coupling as described previously in this document. Since the input impedance of an ADC or video decoder is high impedance, the coupling capacitor can be much smaller than a line's 150-Ω impedance.

AC coupling is done for several reasons, but the most common reason is to ensure full inter-operability voltage levels with the receiving system. This also eliminates possible ground loops, and ensures that regardless of the reference dc voltage used on the transmit side, the receive element (either the ADC or the video transmission line) re-establishes the dc-reference voltage to its own requirements.

Just like the dc output mode of operation discussed previously, each output should keep the capacitive loading below 20-pF. If the THS7353 is used to drive two video transmission lines, it is best to have each line use its own capacitor and resistor rather than sharing these components as shown in Figure 65.This helps ensure line-to-line dc isolation, and the potential problems as stipulated above. Using a single 1000-µF capacitor for 2-lines is possible, but there is a chance for ground loops and interference to be created between the two receivers.



A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-µF capacitor in parallel with these large capacitors.

Figure 65. Typical Y'P'$_B$P'$_R$ System Driving 2 AC-Coupled Video Lines

Due to the edge rates and frequencies of operation, it is recommended – but not required – to place a 0.1-µF to 0.01-µF capacitor in parallel with the large 220-µF to 1000-µF capacitors. These large value capacitors are most commonly aluminum electrolytic. It is known that these capacitors have significantly large equivalent series resistance (ESR), and their impedance at high frequencies is large due to the associated inductances involved with their construction. The small 0.1-µF to 0.01-µF capacitors help pass these high frequency (>1 MHz) signals with lower impedance than the large capacitors. This is especially true when HD and computer R'G'B' signals are being used. Their associated edge rates and frequency content can reach beyond 30-MHz for HD signals and can be over 100-MHz for R'G'B' signals – frequencies that typical aluminum electrolytic capacitors cannot pass effectively.

Although it is common to use the same capacitor values for all the video lines, the frequency bandwidth of the chroma signal in a S-Video system are not required to go as low or as high as the frequency of the luma channels. Thus, the capacitor values of the chroma line(s) can be smaller – such as 0.1 µF.

OUTPUT MODES OF OPERATION – GAIN ADJUST PIN

To expand the flexibility of the THS7353, a gain adjust pin is included for each channel. This pin allows the gain of the output buffer to be varied from 0-dB (1 V/V) to 14-dB (5 V/V) gain. This enables the user to adjust the gain to whatever is required for the system. For example, if a source signal is attenuated, then adding a resistor between the gain adjust pin and ground increases the channel gain according to Equation 1.

$$\text{Gain} = 1 + \frac{1\text{ k}}{250 + R_{(\text{external})}} \quad (1)$$

For a gain of 6-dB, a 750-Ω resistor should be added to the system. Note that while the internal resistor matching is very tight, less than ±1%, the absolute values of these resistors vary as much as ±10%. As such the overall gain varies even when using tight tolerance external components. For example, if the desired gain is to be 6 dB and a true 750-Ω external resistor is used, the overall gain is approximately 6 dB ± 0.33 dB.

One potential issue about this feature is that the dc bias point increases directly with the increase in gain. Thus, it can be possible for the dc operating point to saturate to the power supply. For example, if ac-bias is selected, the output dc operating point is about 1 V with a 3.3-V supply. But, if a gain of 14-dB is required, the dc operating point saturates to the positive rail as 1 V X 5 V/V = 5 V, well above the 3.3-V power supply.

One way to counteract this is to modify the bias point as shown in the *INPUT MODES OF OPERATION – AC BIAS* section of this application section. Another way to counteract this dc bias point increase is to use a capacitor in series with the Gain Adjust pin. This capacitor blocks the dc gain and maintains it at 0-dB. Thus, the signal gain can increase while the dc gain is only 1 – maintaining proper operation of the output amplifier. The only stipulation with doing this is the capacitor creates a high-pass filter with the -3-dB corner frequency equal to Equation 2. Thus, the capacitor value must be large enough to pass the desired range of frequencies.

$$\frac{1}{2\,\pi\,(R_{(\text{external})} + 250)\,C_{(\text{external})}} \quad (2)$$

One point that must not be neglected is that the output buffer amplifier is a voltage feedback (VFB) amplifier. VFB amplifiers have what is known as a gain-bandwidth (GBW) product. This means the -3-dB bandwidth of the amplifier is indirectly proportional to the gain resulting in a theoretical constant gain X bandwidth product. For the THS7353, the -3-dB frequency in bypass mode is about 150-MHz while in unity gain (0-dB). But, as the gain increases, the bandwidth decreases. In a gain of 2 V/V (6-dB), the bandwidth is about 80-MHz. In the maximum gain of 5 V/V (14 dB), the bandwidth is only about 30-MHz. Thus, there is interaction with the internal filters as it is a composite system. The filter attenuation is added with the output amplifier attenuation, resulting in a change in the overall system filter characteristics. Care must be taken when using high gains.

There are package parasitics and PCB parasitics in any system. Since the external gain adjustment is part of the feedback and gain system of the output amplifier, it is possible the parasitics can cause issues with the system. These issues can cause high frequency peaking to occur or even oscillations. Thus, it is recommended to place a small capacitor – 2.2 pF for example, directly between the Gain Adjust pin and the Output pin when not using the output in unity gain. In unity gain, the Gain Adjust pin should be tied directly to the output pin to ensure stability.

A benefit of the externally configured gain control is it allows for frequency gain manipulation. There are two main reasons to do this.

- The first reason is to account for skin-effect losses in cables. Skin-effect accounts for the high-frequency current flow at the edges of a conductor. This results in an increase of resistance as frequency increases. This high frequency resistance is proportional to the square-root of the frequency.
- For very short cable lengths, the skin effect can be generally ignored - especially for SD frequencies. But, if the cable length is greater than 10-meters for G'B'R' or HD signals, this effect can start to cause losses in high frequency signal amplitude. This would generally appear as a loss in sharpness on a video monitor.

One way to counter-act, or equalize, the skin-effect loss is to increase the gain of the amplifier at the same rate of attenuation. The difficult problem with equalization is that skin effect is a function of the square-root of the frequency. Hence, adding a simple RC zero network does not accurately equalize the loss. But, if combinations of RC zeroes spread throughout the frequency spectrum are used, such as the one shown in Figure 66, then a close approximation to skin-effect losses can be equalized out of the system. The amount of equalization is dependant on the length of the cable and the type of cable used. So, fixing the equalization to account for a long length of cable causes significant peaking issues when a short cable is used.

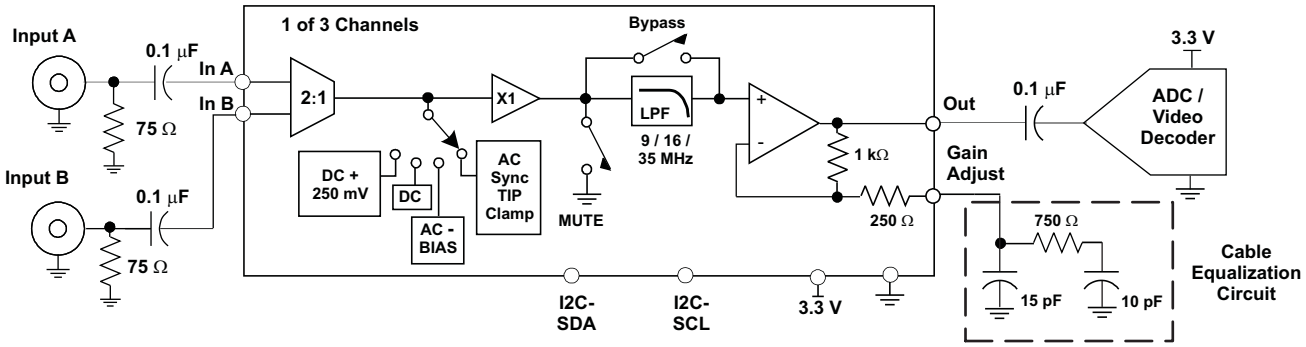


Figure 66. Skin-Effect Loss Compensation (Equalization) Input Buffer Configuration Example

Similar to skin-effect compensation, the other advantage of having control of the amplifier gain is for Sin-X/X compensation. DACs have a roll-off at high-frequencies approximating a Sin-X/X loss. This is dependant on the DAC, the sampling frequency, and the desired frequency of interest. Due to the numerous numbers of DACs and video encoders available, the Sin-X/X compensation must be adjusted depending on the system. An example of a dc-coupled Sin-X/X compensation circuit with a 6-dB gain is shown in Figure 67.

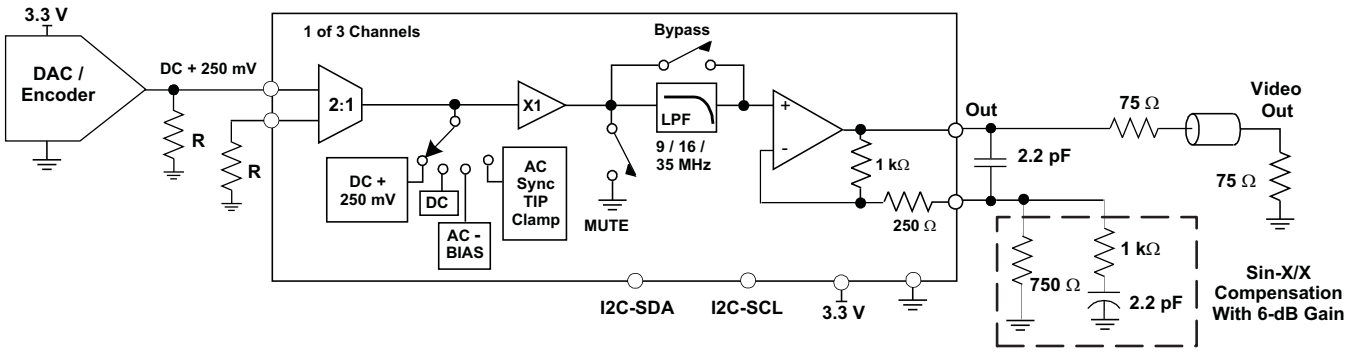


Figure 67. Sin-X/X Compensation with 6-dB Gain Output Buffer Configuration Example

LOW-PASS FILTER AND BYPASS MODES

Each channel of the THS7353 incorporates a 5th-Order Low-Pass Filter. These video anti-aliasing / reconstruction filters minimize the images from being passed onto the video decoder / ADC or to the line. Depending on the system design, failure to eliminate these images can cause picture quality problems due to aliasing of the data converter. Another benefit of the filter is to smooth out aberrations in the signal which some DACs can have if their own internal filtering is not good. This helps with picture quality and helps insure the signal meets video bandwidth requirements.

Each filter has a Butterworth characteristic. The benefit of the Butterworth response is the amplitude frequency response is flat with a relatively steep initial attenuation at the corner frequency. The problem is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in amplitude. An increase in group delay corresponds to a time domain pulse response that has overshoot and some ringing associated with the overshoot. Thus, the use of other type of filters such as elliptic or chebyshev are not recommended for video applications due to their very large group delay variations near the corner frequency. This results in significant overshoot or ringing on fast edge rates such as the sync signals or when a luma or color-difference signal changes from 0% to 100% or visa-versa. Ringing typically causes a display to have ghosting or fuzziness appear on the edges of a sharp transition. On the other hand, a Bessel filter has ideally flat group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Thus the Butterworth filter is a respectable compromise for both attenuation and group delay.

The THS7353 filter has a slightly lower group delay variation near the corner frequency compared to an ideal Butterworth filter. This results in a time domain pulse response which still has some overshoot, but not as much as a true Butterworth filter. Additionally, the initial rate of attenuation in the frequency response is not as fast as an ideal Butterworth response, but it is an acceptable initial rate of attenuation considering the pulse and group delay characteristic benefits.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature changes. To minimize temperature effects, the THS7353 uses thin-film metal resistors and high quality - low temperature coefficient capacitors found in the BiCom-3 process. The filters have been specified by design to account for process variations and temperature variations to maintain proper filter characteristics. Because resistor-to-resistor and capacitor-to-capacitor matching is very tight, the filter Q sensitivities are essentially eliminated. This maintains a low channel-to-channel time delay which is required for proper video signal performance.

The THS7353 filters have a nominal corner (-3 dB) frequency selectable at 9 MHz, 16 MHz, and 35 MHz along with a bypass mode. The 9-MHz filter is ideal for standard definition (SD) NTSC, PAL, and SECAM composite video (CVBS) signals. It is also useful for S-Video signals (Y'/C'), 480i / 576i $Y'P'_BP'_R$, G'B'R', and Y'U'V' video signals. The -3-dB corner frequency was designed to be 9 MHz to allow a maximally flat video signal while achieving over 40-dB of attenuation at 27 MHz – a common frequency between the ADC 2nd and 3rd Nyquist zones found in many video receivers. This is important because any signal appearing around this frequency can appear in the baseband due to aliasing effects of an analog to digital converter found in a receiver.

The 9-MHz filter frequency was chosen to account for process variations in the THS7353. To ensure the required video frequencies are not affected very much, the filter corner frequency must be high enough to allow for component variations. The other consideration is the attenuation must be large enough to ensure the anti-aliasing / reconstruction filtering is enough to meet the system demands. Thus, the selection of the filter frequencies was not chosen arbitrarily.

The 16-MHz filter was designed to pass 480p and 576p $Y'P'_BP'_R$ and G'B'R' video signals – sometimes referred as enhanced definition (ED). Additionally, this filter can be used to pass computer VGA signals with very flat frequency response in the video spectrum. The use the 16-MHz filter for SD signals ensures there is no amplitude aberrations, and to have an exceptional low group delay.

The 35-MHz filter is designed to pass high definition (HD) 720p and 1080i $Y'P'_BP'_R$ video signals along with G'B'R' (R'G'B') SVGA and XGA signals. If a 4:2:2 system is used, the $P'_BP'_R$ channels do not require the full bandwidth as required by the Y' channel. But, it is still recommended to use the same filter frequency of the Y' channel to match the group delay and timing of all 3 signals. Otherwise, extra delay compensation is required to minimize timing variations. This filter is also useful for passing 480p/576p signals with little amplitude or group delay variations.

The THS7353 bypass mode has a 150-MHz bandwidth (-3 dB) and a 300 V/μs slew rate to pass G'B'R' (R'G'B') SXGA and UXGA signals. This bypass mode is also useful for HDTV 1080p signals that require a 60-MHz video signal bandwidth.

The I^2C interface of the THS7353 allows each channel to be configured totally independent of the other channels. One of the benefits is that a multiple output encoder (or DAC) can be routed through one THS7353 with the proper input configuration and low-pass filter required regardless of the signal. This is useful for a portable system or in a low cost system where only one set (or two sets in parallel) is desired on the output of the system. An update of the I^2C commands changes the THS7353 channels. An example is shown in Figure 68 where the input MUX allows for one set of HDTV signals to be put into the THS7353, and then through an I^2C update, a SDTV set of signals is sent through the THS7353 with the proper input mode and low-pass filters.

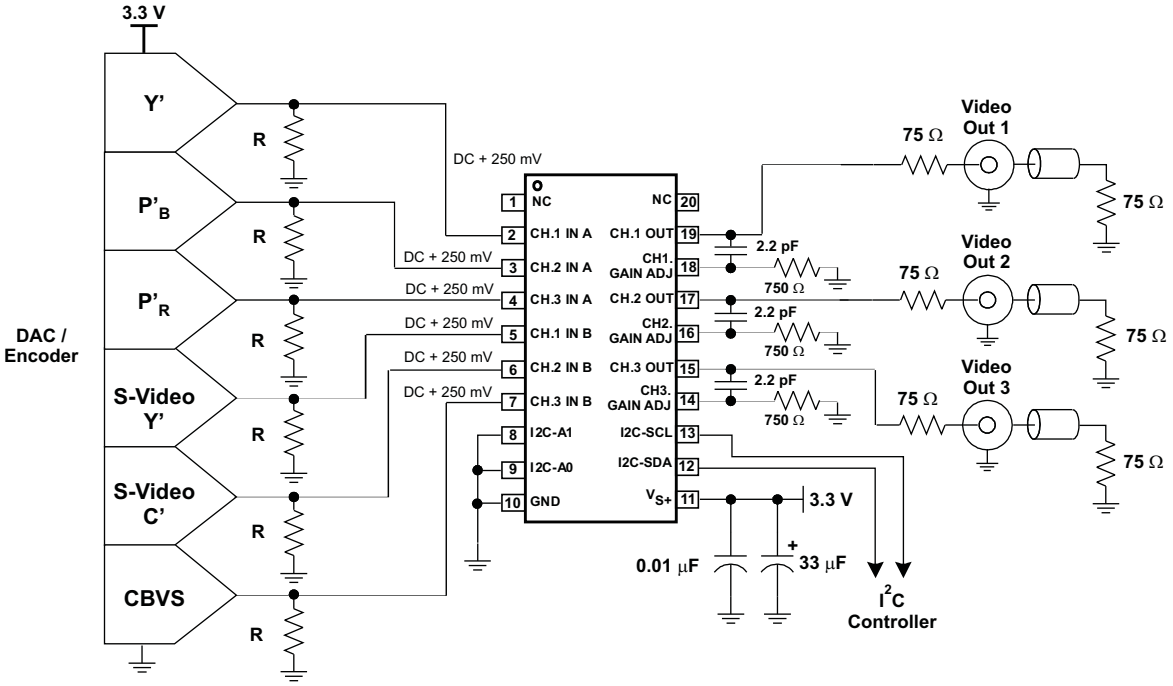
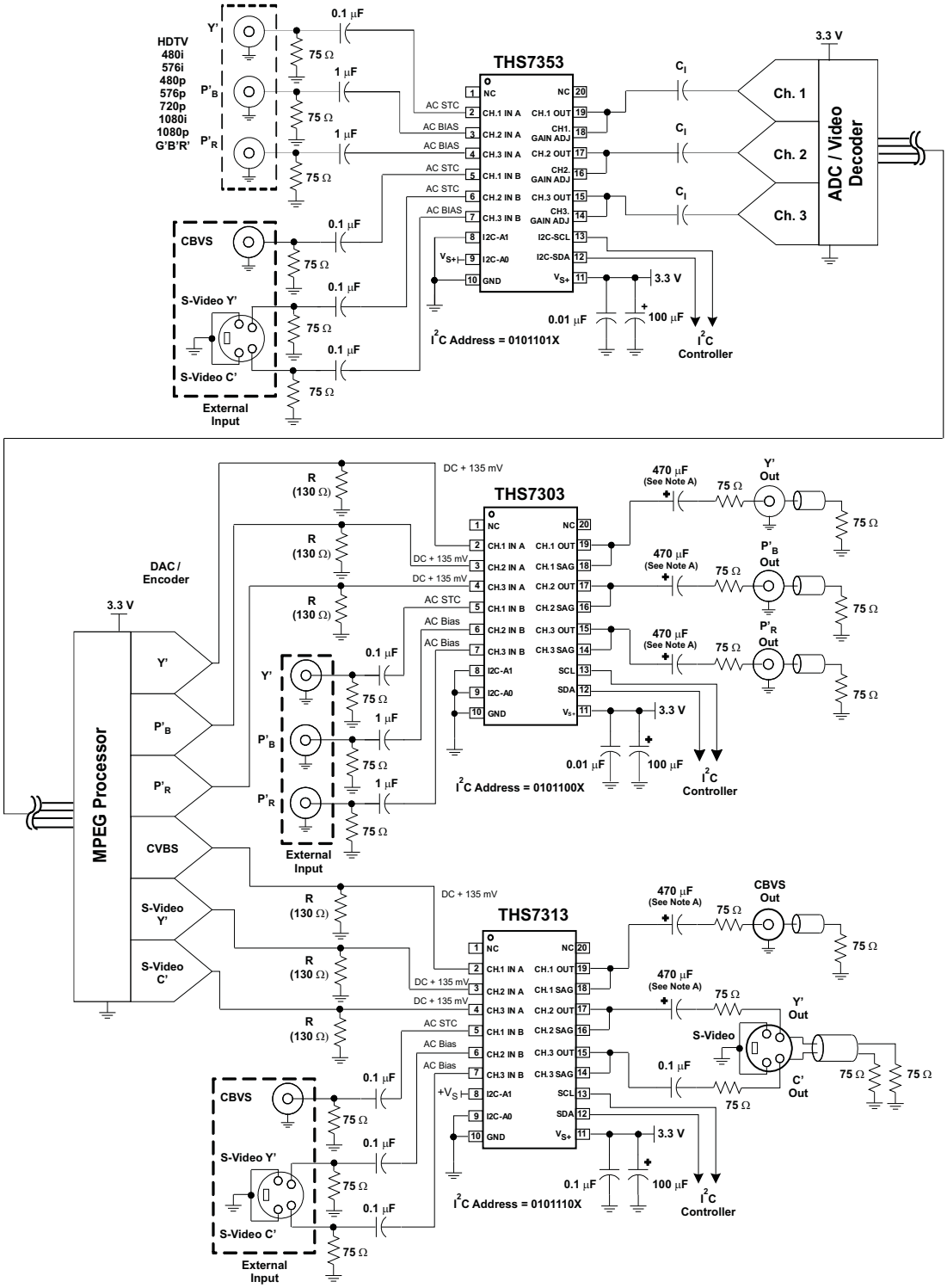


Figure 68. Typical EDTV/HDTV and SDTV Encoder DAC Driving a Single THS7353

Although the circuit of Figure 68 conserves space and cost, the re-use of the output connections may not be the best solution. For a complete system, the THS7353 can be used as an input buffer and the THS7313 (SLOS483) and THS7303 (SLOS479) are used as output buffers as shown in Figure 69. The THS7313 is targeted for SDTV signals and is limited to an 8-MHz filter. The THS7303 is a selectable SD/ED/HD line driver buffer. As the I^2C section discusses, it is easy to have both parts in one system as the I^2C address of each part can be one of four discrete addresses by the logic appearing on the I^2C-A1 and I^2C-A0 lines.



A. Due to the high frequency content of the video signal, it is recommended, but not required, to add a 0.01-µF capacitor in parallel with these large capacitors.

Figure 69. Typical SD/ED/HD System Interfacing with a THS7353, THS7303, and THS7313

I²C INTERFACE NOTES

The I²C interface is used to access the internal registers of the THS7353. I²C is a two-wire serial interface developed by Philips Semiconductor (see the I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device. The THS7353 works as a slave and supports the standard mode transfer (100 kbps) and fast mode transfer (400 kbps) as defined in the I²C-Bus specification. The THS7353 has been tested to be fully functional but not ensured with the high-speed mode (3.4 Mbps).

The basic I²C start and stop access cycles are shown in Figure 70.

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

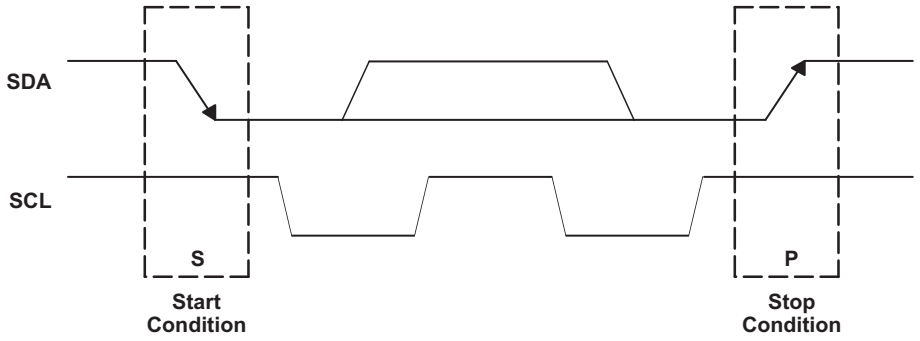


Figure 70. I²C Start and Stop Conditions

GENERAL I²C PROTOCOL

- The master initiates data transfer by generating a start condition. The start condition exist when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 70. All I²C-compatible devices should recognize a start condition.
- The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 71). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 72) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a communication link with a slave has been established.
- The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So, an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (See Figure 73).
- To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 70). This releases the bus and stops the communication link with the addressed slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

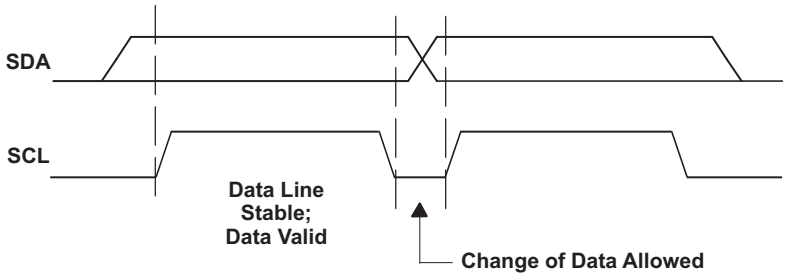


Figure 71. I²C Bit Transfer

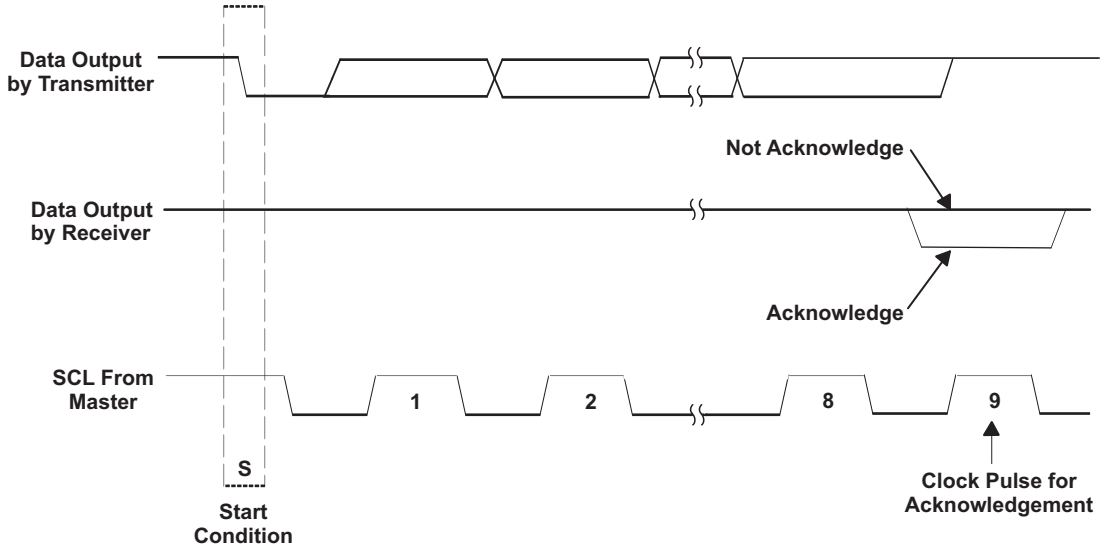


Figure 72. I²C Acknowledge

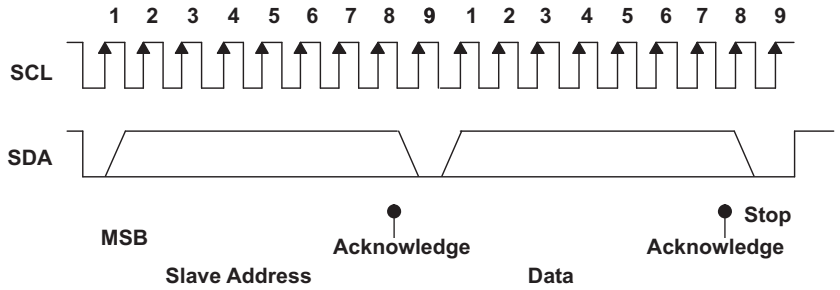


Figure 73. I²C Address and Data Cycles

During a write cycle, the transmitting device must not drive the SDA signal line during the acknowledge cycle, so that the receiving device may drive the SDA signal low. After each byte transfer following the address byte, the receiving device pulls the SDA line low for one SCL clock cycle. A stop condition is initiated by the transmitting device after the last byte is transferred. An example of a write cycle can be found in Figure 74 and Figure 75. Note that the THS7353 does not allow multiple write transfers to occur. See example section, *Writing to the THS7353* for more information.

During a read cycle, the slave receiver acknowledges the initial address byte if it decodes the address as its address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge (A) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 76 and Figure 77. Note that the THS7353 does not allow multiple read transfers to occur. See example section, *Reading from the THS7353* for more information.

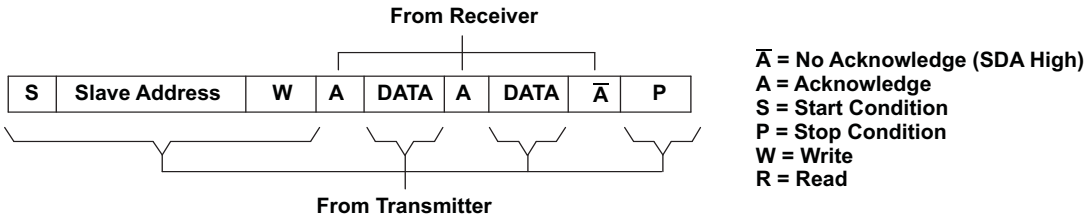


Figure 74. I²C Write Cycle

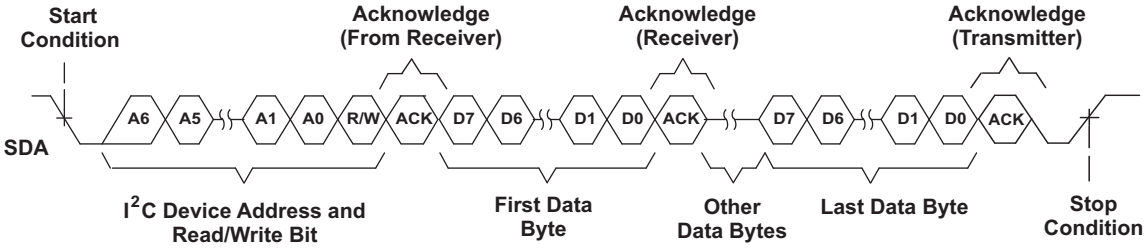


Figure 75. Multiple Byte Write Transfer

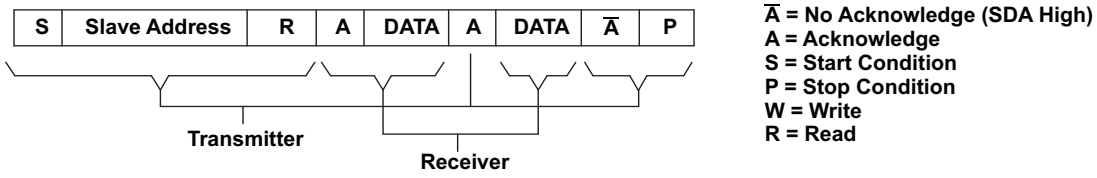


Figure 76. I²C Read Cycle

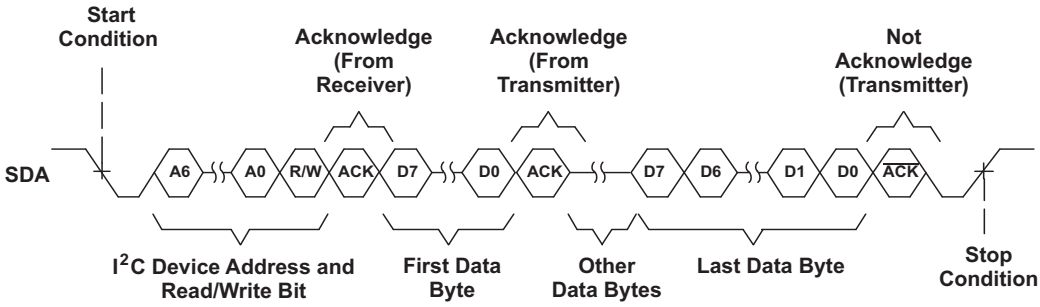


Figure 77. Multiple Byte Read Transfer

I²C DESIGN NOTES: ISSUES AND SOLUTIONS

The THS7353 requires some special attention to the I²C function that is usually not required. These are known design issues, but there are simple workarounds that allow the THS7353 to perform within any I²C system.

The first known I²C issue is with respect to the power-up condition. On power up, the THS7353 registers are in a random state from device to device. The registers remain in this random state until a valid write sequence is made to the THS7353. A total of nine bytes of data completely configure all channels of the THS7353. Therefore, configuring the THS7353 should be done on power-up of the system. Note that one such random state (acknowledge state or ACK) can be engaged. While ACK is engaged, the THS7353 pulls the SDA line low and the master cannot send data to any device on the I²C bus. To circumvent this state, at least one SCL cycle must be completed and then the acknowledge state disengages.

While one SCL cycle normally eliminates any issues, the internal FIFO buffer may have random bits internally to the THS7353. To completely clear all eight bits of this buffer, run eight cycles (or 8 bits or 1 byte) on the SCL line. While there are several different methods to run SCL cycles, the simplest is to have the master send a 00h code to the I²C bus on power-up, ignoring any ACK state. Note that the SCL cycle should occur only after the power-supply voltage of the THS7353 is at least 2.7 V. Failure to follow this step may cause the THS7353 to ignore the SCL cycles.

Another known issue with the I²C function is that the internal SDA and SCL buffers are susceptible to high-frequency noise. This noise can come from switch-mode power supplies, digital processors, or other high-frequency noise generators. While the THS7353 includes buffers with hysteresis on the front-end, these are placed after a low-gain CMOS buffer used as an ESD protection element. The noise susceptibility in real-world systems is very low; however, it can be an issue in some noisy or compact systems. The simple solution, which has shown to solve the issue, is to place a RC filter on each I²C line. Real-world results show that using a 100-Ω resistor in series on each SDA and SCL line along with a 22-pF capacitor from each SDA or SCL line to ground eliminates the noise susceptibility issue. These RC filters should be placed as close as possible to the THS7353 SDA and SCL input pins. Other solutions have shown that not using a series resistor and only using a larger value capacitor (such as 100 pF to 220 pF) has worked, but the RC solution is more robust.

One last real-world issue that has appeared relates to the value of the pull-up resistor on the SDA and SCL lines. While the standard allows for between 2 kΩ and 19 kΩ for this pull-up resistor, practice has shown that keeping this value lower works best. Typical values should be between 2 kΩ and 3.3 kΩ, with 2.7 kΩ being the most common.

SLAVE ADDRESS

Both the SDA and the SCL must be connected to a positive supply voltage via a pullup resistor. These resistors should comply with the I²C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The first 5 Bits (MSBs) of the address are factory preset to 01011. The next two bits of the THS7353 address are controlled by the logic levels appearing on the I²C-A1 and I²C-A0 pins. The I²C-A1 and I²C-A0 address inputs can be connected to V_{S+} for logic 1, GND for logic 0, or it can be actively driven by TTL/CMOS logic levels. The device address is set by the state of these pins and is not latched. Thus, a dynamic address control system can be used to incorporate several devices on the same system. Up to four THS7353 devices can be connected to the same I²C-Bus without requiring additional *glue* logic. Table 1 lists the possible addresses for the THS7353.

Table 1. THS7353 Slave Addresses

FIXED ADDRESS					SELECTABLE WITH ADDRESS PINS		READ/WRITE BIT
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 (A1)	Bit 1 (A0)	Bit 0
0	1	0	1	1	0	0	0
0	1	0	1	1	0	0	1
0	1	0	1	1	0	1	0
0	1	0	1	1	0	1	1
0	1	0	1	1	1	0	0
0	1	0	1	1	1	0	1
0	1	0	1	1	1	1	0
0	1	0	1	1	1	1	1

Channel Selection Register Description (Subaddress)

The THS7353 operates using only a single byte transfer protocol similar to Figure 74 and Figure 76. The internal subaddress registers and the functionality of each are found in Table 2. When writing to the device, it is required to send one byte of data to the corresponding internal subaddress. If control of all three channels is desired, then the master has to cycle through all the subaddresses (channels) one at a time, see the example section, *Writing to the THS7353* for the proper procedure of writing to the THS7353.

During a read cycle, the THS7353 sends the data in its selected subaddress (or channel) in a single transfer to the master device requesting the information. See the example section, *Reading from the THS7353* for the proper procedure on reading from the THS7353.

On power up, the THS7353 registers are in a random state from part-to-part. It remains in this random state until a valid write sequence is made to the THS7353. A total of 9 bytes of data completely configures all channels of the THS7353. As such, configuring the THS7353 should be done on power-up of the system. Note that one such random state (acknowledge state) can be engaged. To circumvent this state, have one SCL cycle run, and the acknowledge state disengages.

Table 2. THS7353 Channel Selection Register Bit Assignments

REGISTER NAME	BIT ADDRESS (b7b6b5....b0)
Channel 1	0000 0001
Channel 2	0000 0010
Channel 3	0000 0011

Channel Register Bit Descriptions

Each bit of the subaddress (channel selection) control register as described above allows the user to individually control the functionality of the THS7353. The benefit of this process allows the user to control the functionality of each channel independent of the other channels. The bit description is decoded in Table 3.

Table 3. THS7353 Channel Register Bit Decoder Table

BIT	FUNCTION	BIT VALUE(S)	RESULT
(MSB) 7, 6	STC Low Pass Filter Selection	0 0	500-kHz Filter – Useful for 9-MHz Video LPF
		0 1	2.5-MHz Filter – Useful for 16-MHz Video LPF
		1 0	5-MHz Filter – Useful for 35-MHz/Bypass Video LPF
		1 1	5-MHz Filter – Useful for 35-MHz/Bypass Video LPF
5	Input MUX Selection	0	Input A Select
		1	Input B Select
4 , 3	Low-Pass Filter Frequency Selection	0 0	9-MHz LPF – Useful for SDTV, S-Video, 480i/576i
		0 1	16-MHz LPF – Useful for EDTV 480p/576p and VGA
		1 0	35-MHz LPF – Useful for 720p, 1080i, and SVGA/XGA
		1 1	Bypass LPF – Useful for 1080p and SXGA/UXGA
2, 1, 0 (LSB)	Input Bias Mode Selection and Disable Control	0 0 0	Disable Channel – Conserves Power
		0 0 1	Channel On – Mute Function – No Output
		0 1 0	Channel On – DC Bias Select
		0 1 1	Channel On – DC Bias + 250 mV Offset Select
		1 0 0	Channel On – AC Bias Select
		1 0 1	Channel On – Sync Tip Clamp with low bias
		1 1 0	Channel On – Sync Tip Clamp with mid bias
		1 1 1	Channel On – Sync Tip Clamp with high bias

Bits 7 (MSB) and 6 – Controls the AC-Sync Tip Clamp Low Pass Filter function. If AC-STC mode is not used, this function is ignored.

Bit 5 – Controls the input MUX of the THS7353.

Bits 4 and 3 – Controls the 5^{th} order Low Pass Filter –3 dB corner frequency or the bypass mode of operation.

Bits 2, 1, and 0 (LSB) – Selects the input biasing of the THS7353 and the power-savings function. When sync-tip clamp is selected, the dc input sink bias current is also selectable.

EXAMPLE—WRITING TO THE THS7353

The proper way to write to the THS7353 is illustrated as follows:

An I^2C master initiates a write operation to the THS7353 by generating a start condition (S) followed by the THS7353 I^2C address (as shown below), in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving an acknowledge from the THS7353, the master presents the subaddress (channel) it wants to write consisting of one byte of data, MSB first. The THS7353 acknowledges the byte after completion of the transfer. Finally the master presents the data it wants to write to the register (channel) and the THS7353 acknowledges the byte. The I^2C master then terminates the write operation by generating a stop condition (P). Note that the THS7353 does not support multi-byte transfers. To write to all three channels – or registers – this procedure must be repeated for each register one series at a time (i.e., repeat steps 1 through 8 for each channel).

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each X Logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either Vs+ or GND.

Step 3	9
I^2C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C Write Channel Address (Master)	0	0	0	0	0	0	Addr	Addr

Where Addr is determined by the values shown in Table 2.

Step 5	9
I^2C Acknowledge (Slave)	A

Step 6	7	6	5	4	3	2	1	0
I^2C Write Data (Master)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the values shown in Table 3.

Step 7	9
I^2C Acknowledge (Slave)	A

Step 8	0
I^2C Stop (Master)	P

For Step 6, an example of the proper bit control for selecting Input B of the MUX, a 720p Y' channel signal with AC-STC lowest line tilt and shortest sync filter is 1111 0101.

EXAMPLE—READING FROM THE THS7353

The read operation consists of two phases. The first phase is the address phase. In this phase, an I^2C master initiates a write operation to the THS7353 by generating a start condition (S) followed by the THS7353 I^2C address, in MSB first bit order, followed by a 0 to indicate a write cycle. After receiving acknowledges from the THS7353, the master presents the subaddress (channel) of the register it wants to read. After the cycle is acknowledged (A), the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I^2C master initiates a read operation to the THS7353 by generating a start condition followed by the THS7353 I^2C address (as shown below for a read operation), in MSB first bit order, followed by a 1 to indicate a read cycle. After an acknowledge from the THS7353, the I^2C master receives one byte of data from the THS7353. After the data byte has been transferred from the THS7353 to the master, the master generates a not acknowledge followed by a stop. Similar to the Write function, to read all channels Steps 1 through 11 must be repeated for each and every channel desired.

THS7353 Read Phase 1:

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	0

Where each X Logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either V_{S+} or GND.

Step 3	9
I^2C Acknowledge (Slave)	A

Step 4	7	6	5	4	3	2	1	0
I^2C Read Channel Address (Master)	0	0	0	0	0	0	Addr	Addr

Where Addr is determined by the values shown in Table 2.

Step 5	9
I^2C Acknowledge (Slave)	A

Step 6	0
I^2C Start (Master)	P

THS7353 Read Phase 2:

Step 7	0
I^2C Start (Master)	S

Step 8	7	6	5	4	3	2	1	0
I^2C General Address (Master)	0	1	0	1	1	X	X	1

Where each X Logic state is defined by I^2C-A1 and I^2C-A0 pins being tied to either V_{S+} or GND.

Step 9	9
I^2C Acknowledge (Slave)	A

Step 10	7	6	5	4	3	2	1	0
I^2C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the Logic values contained in the Channel Register.

Step 11	9
I^2C Not-Acknowledge (Master)	$\overline{A}$

Step 12	0
I^2C Stop (Master)	P

Evaluation Module

To evaluate the THS7353, an evaluation module (EVM) is available. Because the THS7353 is controlled by the I^2C lines, additional control is required rather than simple switches. To keep the control as easy as possible, an USB-to-I^2C interface was designed onto the EVM. A computer running either Windows 2000 or XP is then connected to the EVM through the USB cable. A computer program interface allows graphical control of the THS7353 that allows both read and write functions to be performed. The EVM comes with a CD-ROM loaded with all the required software to install the command software on to the computer.

To program the THS7353, the user selects the channel, the filter, and the mode of operation, and selects the Execute button. The *Req Done* light on the computer screen is lit to confirm that the command was executed by the THS7353. The same procedure is done for each and every channel. To read the THS7353 registers, change the switch to *Read*, select the channel, and then select the Execute button. The resulting register content appears in hexadecimal code.

Note that the USB-to-I^2C interface circuitry must be powered by a 3.3-V supply only. Additionally, the I^2C circuitry section must be powered on either at the same time as the THS7353 or before power is applied to the THS7353. This is due to the reading of the EEPROM the TAS1020 device must complete to program its core. The yellow LED in the I^2C section is lit if the TAS1020 was programmed properly. If this LED is not lit, then cyclng the power should be done to reset the USB-to-I^2C TAS1020 chip.

Table 4 is a bill of materials, the board layout is found in Figure 78 through Figure 81.

Table 4. Bill Of Materials

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QUANTITY	MANUFACTURER'S PART NUMBER(1)	DISTRIBUTOR'S PART NUMBER
1	BEAD, FERRITE, 2.5A, 80 OHM	0805	FB1, FB2, FB3	3	(TDK) MPZ2012S331A	(DIGI-KEY) 445-1569-1-ND
2	CAP, 22uF, TAN, 6.3V, 10%, LO ESR	A	C30	1	(AVX) TPSA226K006R0900	(DIGI-KEY) 478-1754-1-ND
3	CAP, 100uF, TAN, 10V, 10%, LO ESR	C	C5	1	(AVX) TPSC107K010R0100	(DIGI-KEY) 478-1765-1-ND
4	OPEN	0805	C2, C3, C8, C11, C12, C14, C17, C21, C23, Z9, Z12, Z15	12		
5	CAP, 33pF, CERAMIC, 50V, NPO	0805	C31, C32	2	(AVX) 08055A330JAT2A	(DIGI-KEY) 478-1310-1-ND
6	CAP, 47pF, CERAMIC, 50V, NPO	0805	C27, C29	2	(AVX) 08055A470JAT2A	(DIGI-KEY) 478-1312-1-ND
7	CAP, 100pF, CERAMIC, 50V, NPO	0805	C34	1	(AVX) 08055A101JAT2A	(DIGI-KEY) 478-1316-1-ND
8	CAP, 1000pF, CERAMIC, 100V, NPO	0805	C33	1	(AVX) 08051A102JAT2A	(DIGI-KEY) 478-1290-1-ND
9	CAP, 0.01uF, CERAMIC, 100V, X7R	0805	C19, C28	2	(AVX) 08051C103KAT2A	(DIGI-KEY) 478-1358-1-ND
10	CAP, 0.1uF, CERAMIC, 50V, X7R	0805	C4, C6, C13, C22, C26, C43, C44, Z4	8	(AVX) 08055C104KAT2A	(DIGI-KEY) 478-1395-1-ND
11	CAP, 1uF, CERAMIC, 16V, X7R	0805	C18, C35, C36, C37, C38, C39, C40, C41, C42, Z5, Z6	11	(TDK) C2012X7R1C105K	(DIGI-KEY) 445-1358-1-ND
12	OPEN	0603	R47, R48, R49, R51	4		
13	RESISTOR, 0 OHM	0603	R1, R2, R3, R4, R6, R7, R19, R20, R23	9	(ROHM) MCR03EZPJ000	(DIGI-KEY) RHM0.0GCT-ND
14	RESISTOR, 2.74K OHM, 1/8W, 1%	0603	R41, R61	2	(ROHM) MCR03EZPFX2741	(DIGI-KEY) RHM2.7KHCT-ND
15	OPEN	0805	R9, R13, R15, R16, R21, R28, Z8, Z11, Z14	9		
16	RESISTOR, 0 OHM	0805	Z1, Z2, Z3, Z7, Z10, Z13	6	(ROHM) MCR10EZHJ000	(DIGI-KEY) RHM0.0ACT-ND
17	RESISTOR, 10 OHM, 1/8W, 1%	0805	R39, R44, R45, R52	4	(ROHM) MCR10EZHF10R0	(DIGI-KEY) RHM10.0CCT-ND
18	RESISTOR, 27.4 OHM, 1/8W, 1%	0805	R30, R31	2	(ROHM) MCR10EZHF27.4	(DIGI-KEY) RHM27.4CCT-ND

(1) Manufacturer's part numbers are used for test purposes only.

Table 4. Bill Of Materials (continued)

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QUANTITY	MANUFACTURER'S PART NUMBER(1)	DISTRIBUTOR'S PART NUMBER
19	RESISTOR, 75 OHM, 1/8W, 1%	0805	R5, R8, R10, R11, R12, R14, R17, R18, R22	9	(ROHM) MCR10EZHF75.0	(DIGI-KEY) RHM75.0CCT-ND
20	RESISTOR, 100 OHM, 1/8W, 1%	0805	R50	1	(ROHM) MCR10EZHF1000	(DIGI-KEY) RHM100CCT-ND
21	RESISTOR, 200 OHM, 1/8W, 1%	0805	R26, R27	2	(ROHM) MCR10EZHF2000	(DIGI-KEY) RHM200CCT-ND
22	RESISTOR, 649 OHM, 1/8W, 1%	0805	R33, R60	2	(ROHM) MCR10EZHF0649	(DIGI-KEY) RHM649CCT-ND
23	RESISTOR, 1.0K OHM, 1/8W, 1%	0805	R29	1	(ROHM) MCR10EZHF1001	(DIGI-KEY) RHM1.00KCCT-ND
24	RESISTOR, 1.5K OHM, 1/8W, 1%	0805	R32	1	(ROHM) MCR10EZHF1501	(DIGI-KEY) RHM1.50KCCT-ND
25	RESISTOR, 2.21K OHM, 1/8W, 1%	0805	R34, R35	2	(ROHM) MCR10EZHF2211	(DIGI-KEY) RHM2.21KCCT-ND
26	RESISTOR, 3.09K OHM, 1/8W, 1%	0805	R43	1	(ROHM) MCR10EZHF3091	(DIGI-KEY) RHM3.09KCCT-ND
27	RESISTOR, 10K OHM, 1/8W, 1%	0805	R24, R25, R40, R42	4	(ROHM) MCR10EZHF1002	(DIGI-KEY) RHM10.0KCCT-ND
28	RESISTOR, 20K OHM, 1/8W, 1%	0805	R46	1	(ROHM) MCR10EZHF2002	(DIGI-KEY) RHM20.0KCCT-ND
29	LED, GREEN	0805	D1	1	(LITE-ON) LTST-C171GKT	(DIGI-KEY) 160-1423-1-ND
30	LED, YELLOW	0805	D2	1	(LITE-ON) LTST-C171YKT	(DIGI-KEY) 160-1431-1-ND
31	IC, CONV, SERIAL TO USB		U3	1	(TI) TAS1020BPFB	(DIGI-KEY) TAS1020BPFB
32	IC, SERIAL, EEPROM, 64K	8-SOIC	U2	1	(MICROCHIP) 24LC64-I/SN	(DIGI-KEY) 24LC64-I/SN-ND
33	CRYSTAL, 6.00MHz., SMT	HCM49	X1	1	(CITIZEN) HCM49-6.000MABJT	(DIGI-KEY) 300-6112-1-ND
34	OPEN	SOT-23	U4, U5	2	(ZETEX) ZXMN6A07F	(DIGI-KEY) ZXMN6A07FCT-ND
35	JACK, BANANA RECEPTANCE, 0.25" DIA. HOLE		J4, J5, J16, J17	4	(SPC) 813	(NEWARK) 39N867
36	SWITCH, SMD GULL WING	4MM	S1	1	(BOURNS) 7914G-1-000E	(DIGI-KEY) 7914G-000ETR-ND
37	CONNECTOR, RCA, JACK, R/A		J1, J2, J12	3	(CUI) RCJ-32265	(DIGI-KEY) CP-1446-ND
38	CONNECTOR, USB, RTANG, FEMALE	B	J15	1	(ASSMANN) AU-Y1007	(DIGI-KEY) AE1085-ND
39	CONNECTOR, BNC, JACK, 75 OHM		J3, J6, J7, J8, J9, J10, J11, J13, J14	9	(AMPHENOL) 31-5329-72RFX	(NEWARK) 93F7554
40	HEADER, 0.1" CTRS, 0.025" SQ. PINS	2 POS.	JP1, JP2, JP3	3	(SULLINS) PZC36SAAN	(DIGI-KEY) S1011-36-ND
41	SHUNTS		JP1, JP2, JP3	3	(SULLINS) SSC02SYAN	(DIGI-KEY) S9002-ND
42	TEST POINT, RED		TP1, TP2, TP5, TP6, TP7	5	(KEYSTONE) 5000	(DIGI-KEY) 5000K-ND
43	TEST POINT, BLACK		TP3, TP4	2	(KEYSTONE) 5001	(DIGI-KEY) 5001K-ND
44	IC, THS7353		U1	1	(TI) THS7353PW	
45	STANDOFF, 4-40 HEX, 0.625" LENGTH			4	(KEYSTONE) 1808	(NEWARK) 89F1934
46	SCREW, PHILLIPS, 4-40, .250"			4	(BF) PMS 440 0031 PH	(DIGI-KEY) H343-ND
47	BOARD, PRINTED CIRCUIT			1	EDGE # 6473562 REV. A	

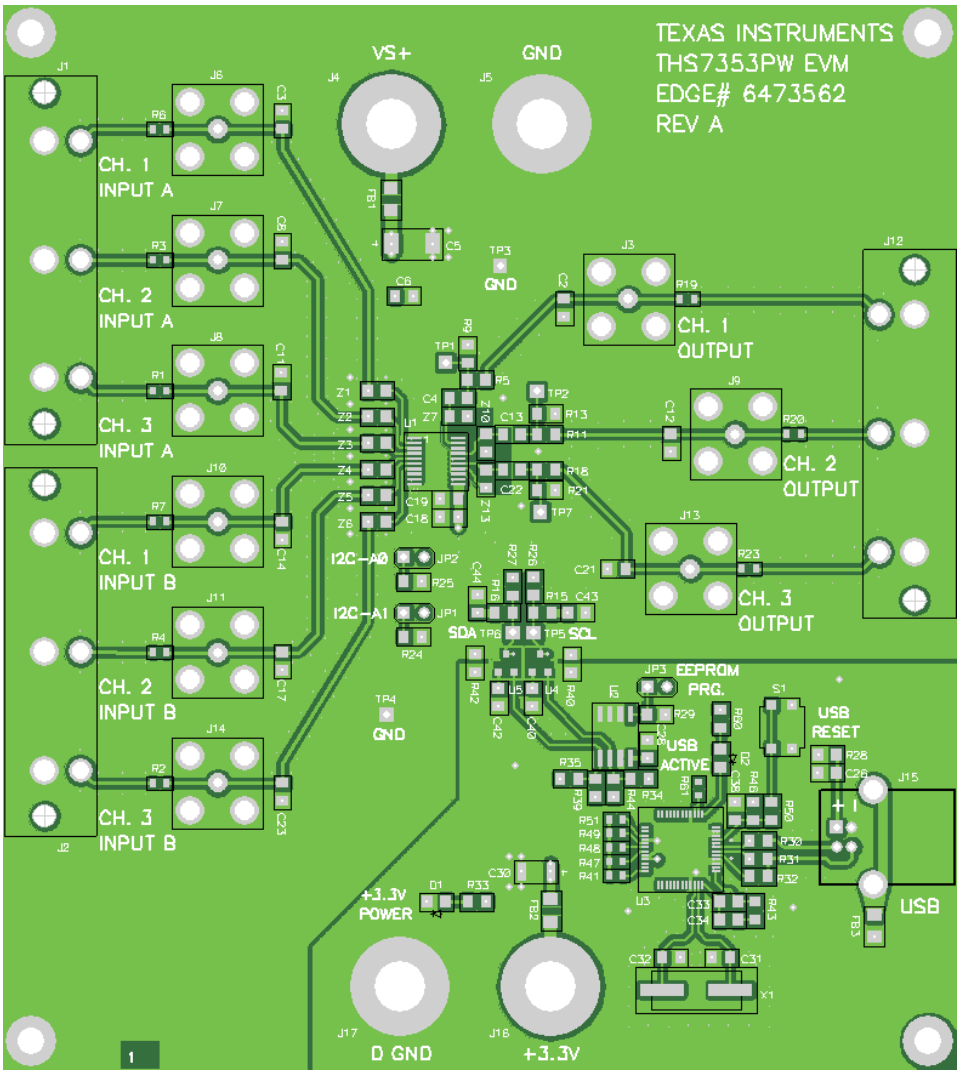


Figure 78. Top Layer: Signal Layer

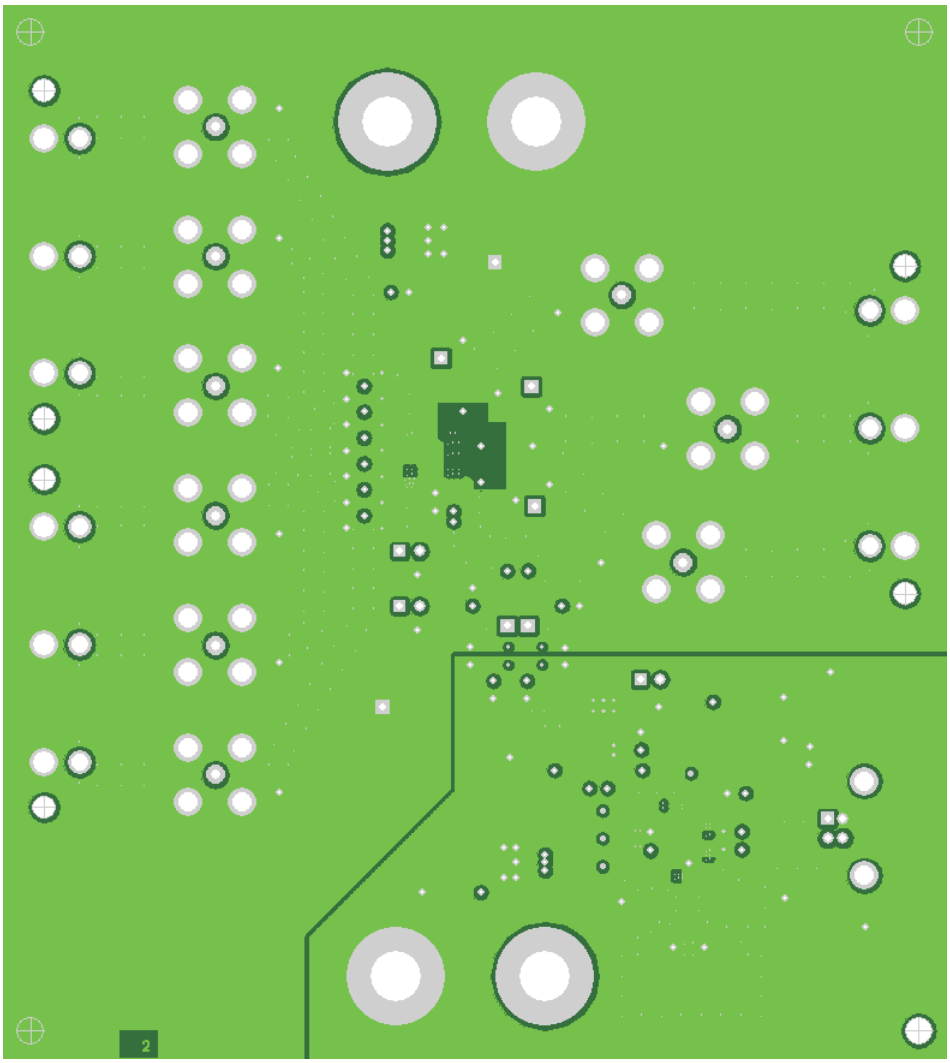


Figure 79. Layer Two: Ground Layer

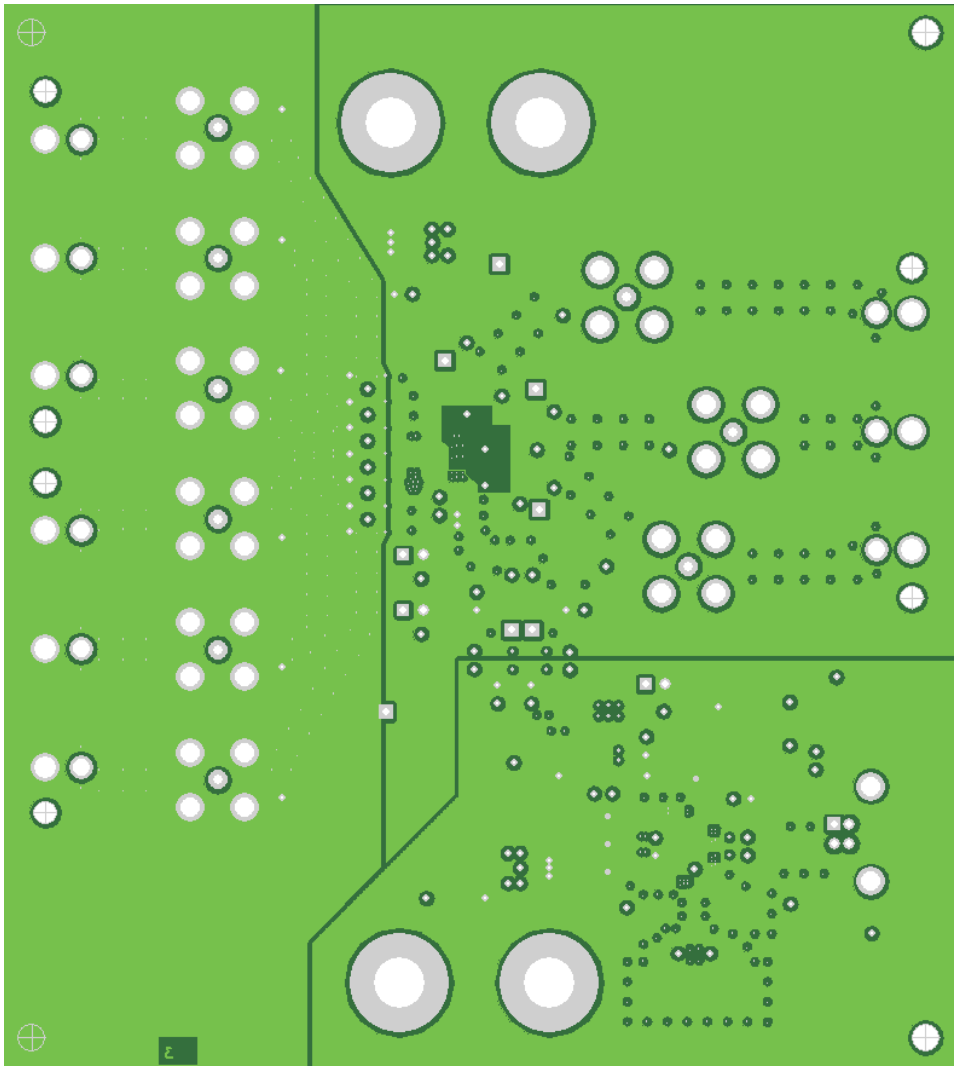


Figure 80. Layer Three: Power and Ground Layer

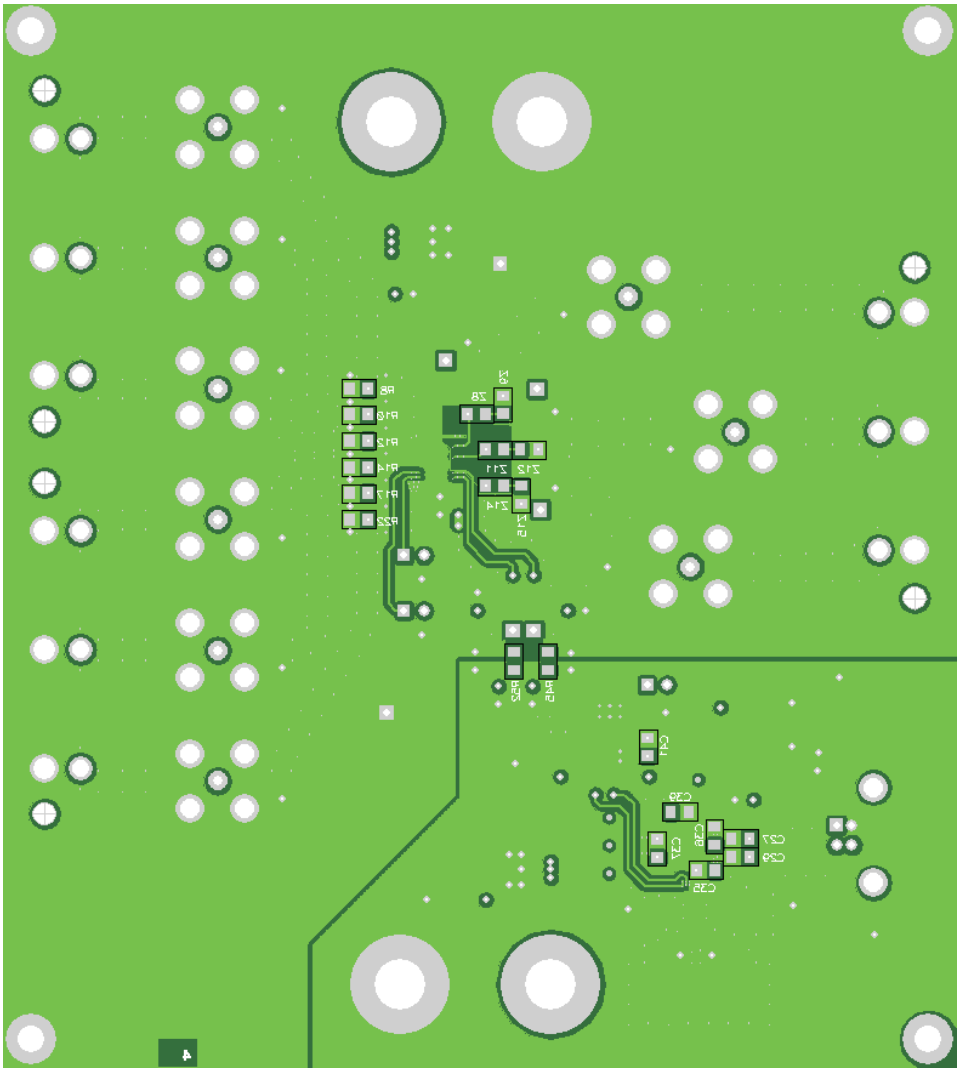


Figure 81. Bottom Layer: Signal Layer

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2010) to Revision B **Page**

- Added *I²C Design Notes: Issues and Solutions* section 37

Changes from Original (November, 2005) to Revision A **Page**

- Deleted *lead temperature* specifications from Absolute Maximum Ratings table 2
- Changed *bias output voltage* specification (bias = dc + 250 mV, V_I = 0 condition) values 4
- Added *Digital Characteristics* section and footnote (5) to Electrical Characteristics (3.3 V) 5
- Added *Digital Characteristics* section and footnote (5) to Electrical Characteristics (5 V) 7

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of (V_I) 0 V to 3 V, not to exceed VS+ or VS–, and the input voltage range (V_S) of 2.7 V to 5 V, and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +100°C. The EVM is designed to operate properly with certain components above +100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS7353PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS7353	Samples
THS7353PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS7353	Samples
THS7353PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	THS7353	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

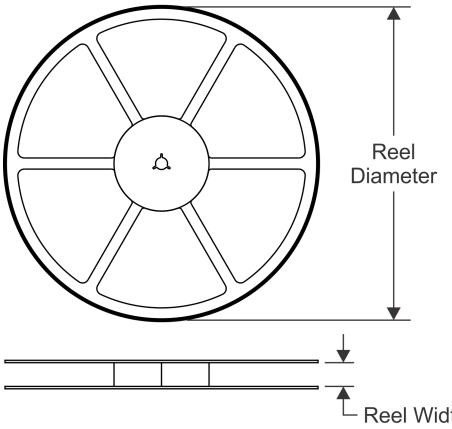
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

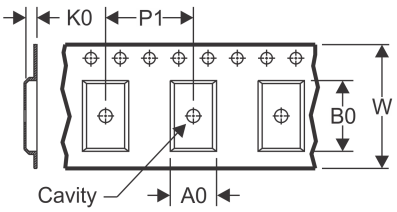
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

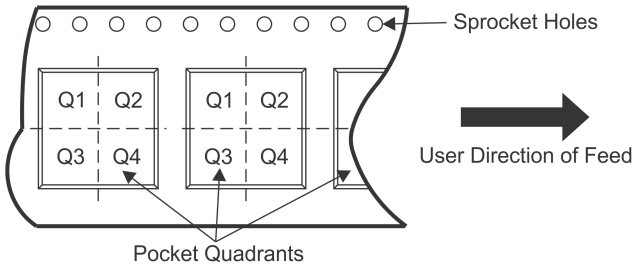


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

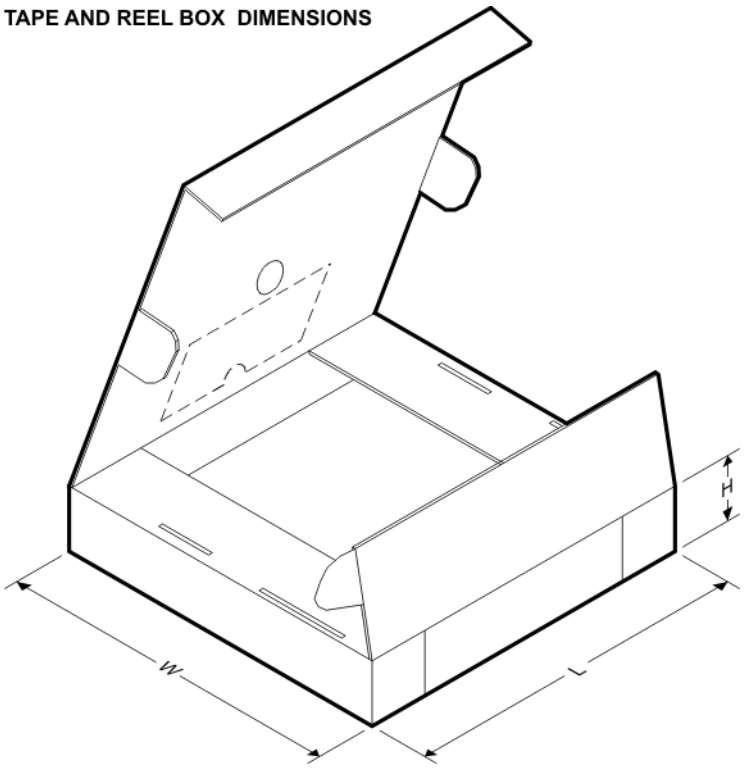
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7353PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

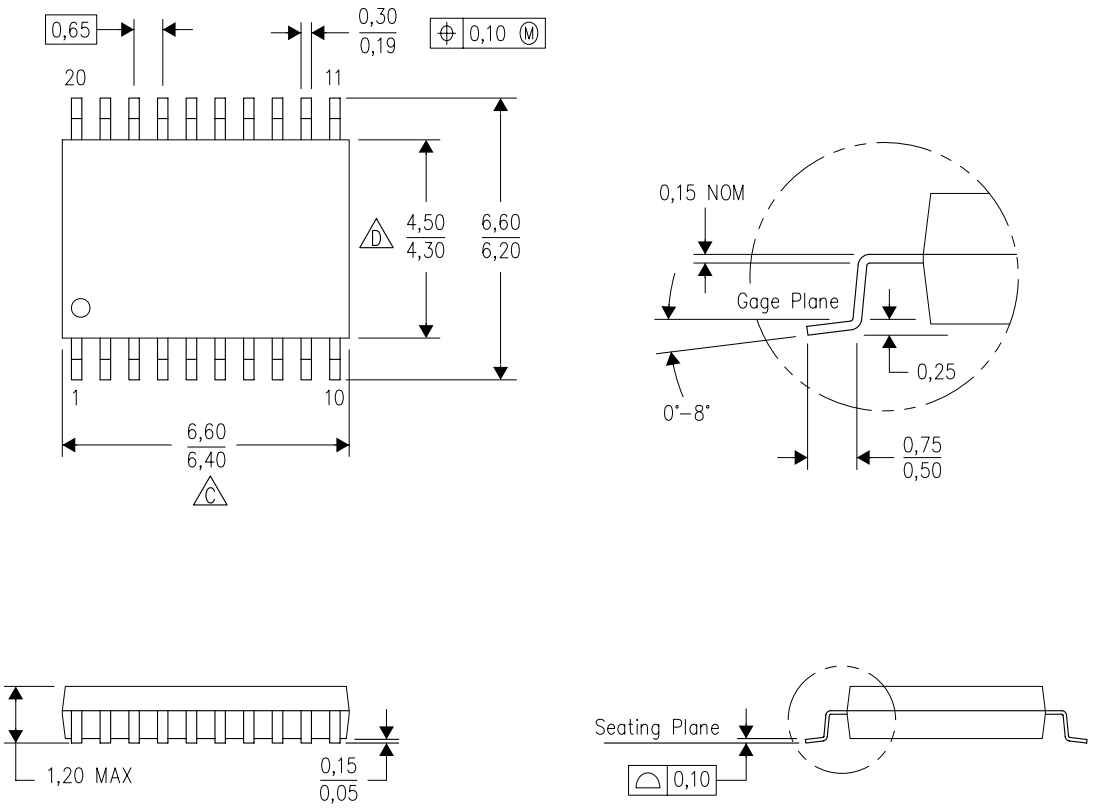
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7353PWR	TSSOP	PW	20	2000	350.0	350.0	43.0

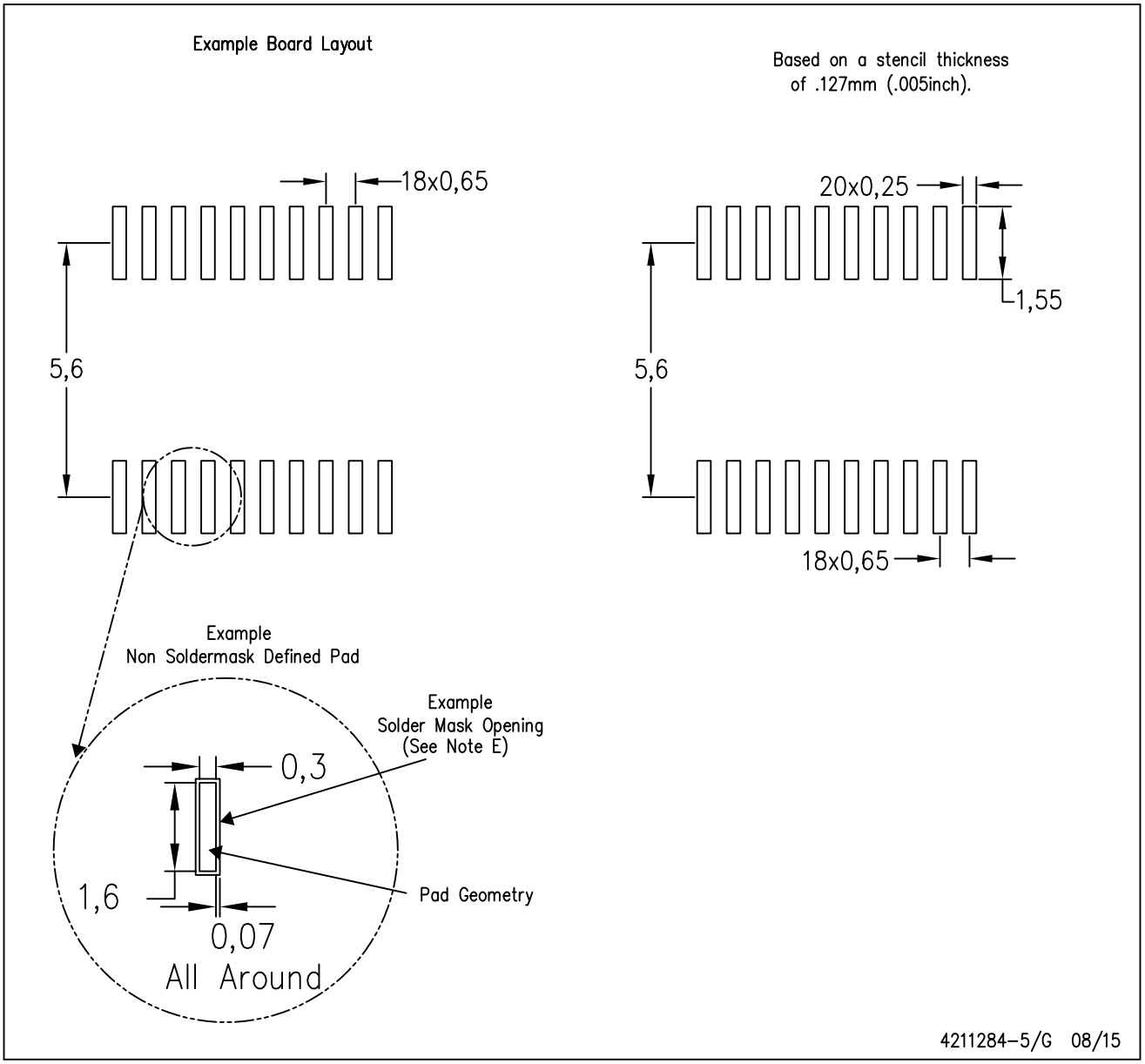
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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