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August 2016

FPF1203 / FPF1203L / FPF1204 / FPF12045
IntelliMAX™ Ultra-Small, Slew-Rate-Controlled Load Switch

Features

- 1.2 V to 5.5 V Input Voltage Operating Range
- Typical R_{ON}:
  - 45 mΩ at V_{IN}=5.5 V
  - 55 mΩ at V_{IN}=3.3 V
  - 90 mΩ at V_{IN}=1.8 V
  - 185 mΩ at V_{IN}=1.2 V
- Slew Rate Control with t_R:
  - FPF1203/FPF1203l/FPF1204: 100 µs
  - FPF12045: 2 µs
- Output Discharge Function on FPF1204 / 45
- Low <1.5 µA Quiescent Current
- ESD Protected: Above 7 kV HBM, 2 kV CDM
- GPIO / CMOS-Compatible Enable Circuitry
- 4-Bump, WLCSP 0.76 mm x 0.76 mm, 0.4 mm Pitch

Description

The FPF1203 / 03L / 04 / 45 are ultra-small integrated IntelliMAX™ load switches with integrated P-channel switch and analog control features. Integrated slew-rate control prevents inrush current and the resulting excessive voltage drop on the power rail. The input voltage range operates from 1.2 V to 5.5 V to provide power-disconnect capability for post-regulated power rails in portable and consumer products. The low shut-off current allows power designs to meet standby and off-power drain specifications.

The FPF120x are controlled by a logic input (ON pin) compatible with standard CMOS GPIO circuitry found on Field Programmable Gate Array (FPGA) embedded processors. The FPF120x are available in 0.76 mm x 0.76 mm 4-bump WLCSP.

Applications

- Mobile Devices and Smart Phones
- Portable Media Devices
- Tablet PCs
- Advanced Notebook, UMPC, MID
- Portable Medical Devices
- GPS and Navigation Equipment

Ordering Information

Part Number	Top Mark	Switch (Typical) at $3.3V_{IN}$	Output Discharge	ON Pin Activity	t_R	Package
FPF1203UCX	QL	55 mΩ	NA	Active HIGH	100 µs	4-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.76 mm x 0.76 mm, 0.4 mm Pitch
FPF1203LUCX	QP	55 mΩ	NA	Active LOW	100 µs	
FPF1204UCX	QM	55 mΩ	65 Ω	Active HIGH	100 µs	
FPF1204UCX_F013 (Amkor Assembly Only)	QM	55 mΩ	65 Ω	Active HIGH	100 µs	
FPF1204BUCX (Backside Laminate)	QM	55 mΩ	65 Ω	Active HIGH	100 µs	
FPF12045UCX	NC	55 mΩ	65 Ω	Active HIGH	2 µs	

Application Diagram

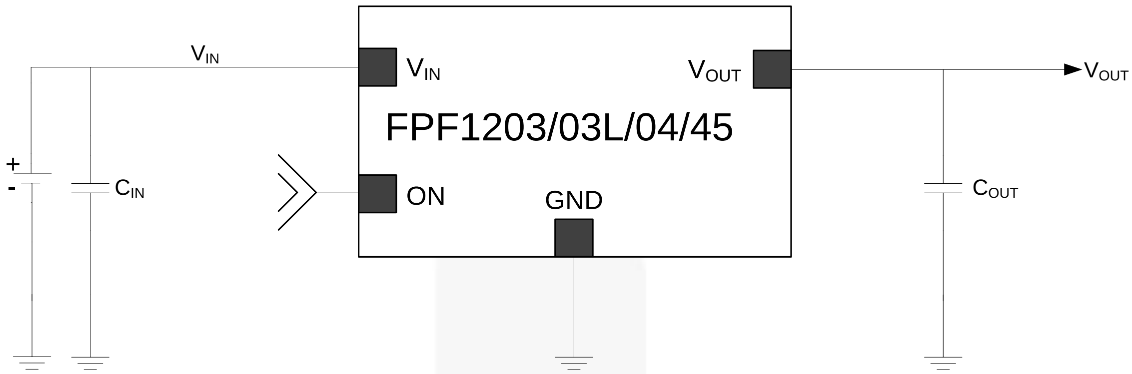


Figure 1. Typical Application

Functional Block Diagram

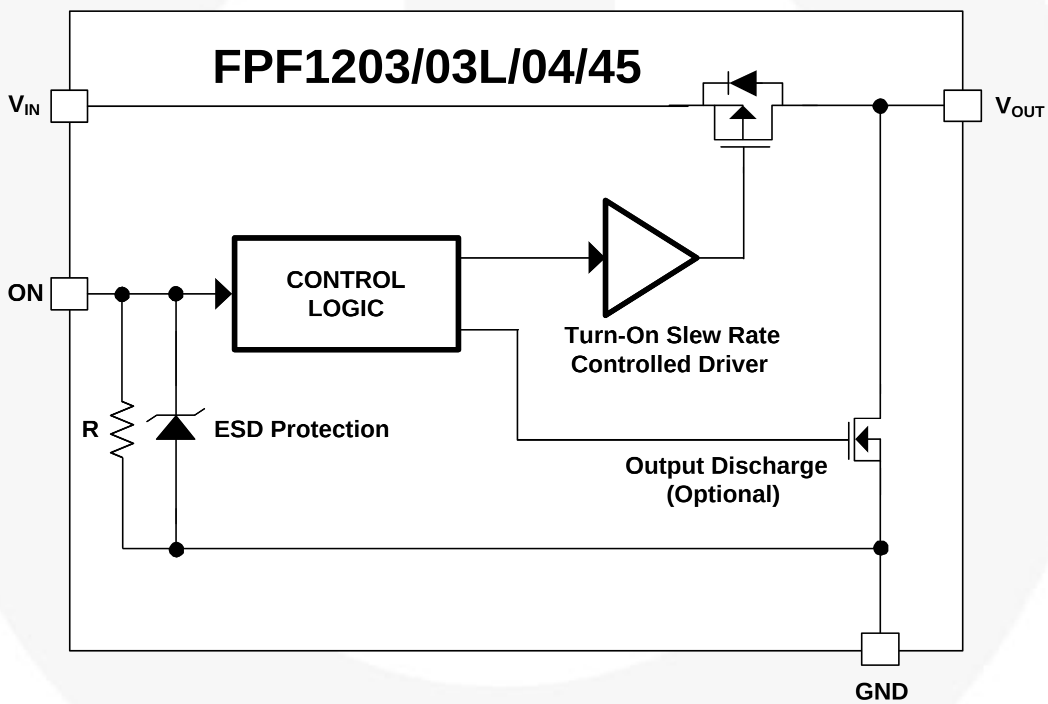


Figure 2. Functional Block Diagram (Output Discharge for FPF1204 / 45)

Pin Configurations

Figure 3. WLCSP Bumps Facing Down (Top View)

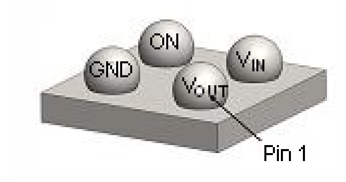


Figure 4. WLCSP Bumps Facing Up (Bottom View)

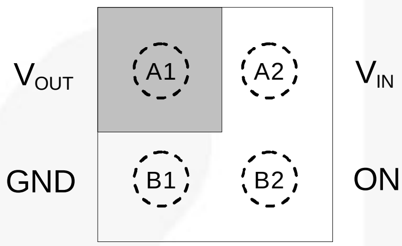


Figure 5. Pin Assignments (Top View)

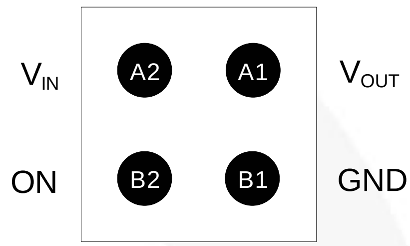


Figure 6. Pin Assignments (Bottom View)

Pin Definitions

Pin #	Name	Description
A1	V_{OUT}	Switch output
A2	V_{IN}	Supply input: input to the power switch
B1	GND	Ground
B2	ON	ON/OFF Control, active HIGH; FPF1203/04/45
B2	ON	ON/OFF Control, active LOW; FPF1203L

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

<table>
<tr><th>Symbol</th><th colspan="2">Parameter</th><th>Min.</th><th>Max.</th><th>Unit</th></tr>
<tr><td>V_{IN}</td><td colspan="2">V_{IN}, V_{OUT}, V_{ON} to GND</td><td>-0.3</td><td>6.0</td><td>V</td></tr>
<tr><td>I_{SW}</td><td colspan="2">Maximum Continuous Switch Current at Ambient Operating Temperature</td><td></td><td>2.2</td><td>A</td></tr>
<tr><td>P_D</td><td colspan="2">Power Dissipation at T_A=25°C</td><td></td><td>1.0</td><td>W</td></tr>
<tr><td>T_{STG}</td><td colspan="2">Storage Temperature Range</td><td>-65</td><td>+150</td><td>°C</td></tr>
<tr><td rowspan="2">Θ_{JA}</td><td rowspan="2">Thermal Resistance, Junction-to-Ambient</td><td>1S2P with One Thermal Via[1]</td><td></td><td>110</td><td rowspan="2">°C/W</td></tr>
<tr><td>1S2P without Thermal Via[2]</td><td></td><td>95</td></tr>
<tr><td rowspan="2">ESD</td><td rowspan="2">Electrostatic Discharge Capability[1,2]</td><td>Human Body Model, JESD22-A114</td><td>7</td><td></td><td rowspan="2">kV</td></tr>
<tr><td>Charged Device Model, JESD22-C101</td><td>2</td><td></td></tr>
</table>

Notes:
1. Measured using 2S2P JEDEC std. PCB.
2. Measured using 2S2P JEDEC PCB COLD PLATE Method.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Input Voltage	1.2	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

Electrical Characteristics

Unless otherwise noted, V_{IN}=1.2 V to 5.5 V and T_A=-40 to +85°C. Typical values are at V_{IN}=3.3 V and T_A=25°C.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
Basic Operation							
V_{IN}	Supply Voltage			1.2		5.5	V
$I_{Q(OFF)}$	Off Supply Current	FPF1203/04/45	V_{ON}=GND, V_{OUT}=Open, V_{IN}=5.5 V		0.1	1.0	µA
		FPF1203L	V_{ON}=$V_{IN,}$ V_{OUT}=Open, V_{IN}=5.5 V		1.0	2.0	
I_{SD}	Shutdown Current	FPF1203/04/45	V_{ON}=GND, V_{OUT}=GND		0.1	1.0	µA
		FPF1203L	V_{ON}=V_{IN}, V_{OUT}=GND		1.2	3.0	
I_Q	Quiescent Current	FPF1203/04/45	I_{OUT}=0 mA, $V_{ON=}$$V_{IN}$, =5.5 V		0.1	1.5	µA
		FPF1203L	I_{OUT}=0 mA, V_{ON}=GND, $V_{IN,}$ = 5.5 V				
R_{ON}	On Resistance		V_{IN}=5.5 V, I_{OUT}=200 mA, T_A=25°C		45	55(3)	mΩ
			V_{IN}=3.3 V, I_{OUT}=200 mA, T_A=25°C		55	65(3)	
			V_{IN}=1.8 V, I_{OUT}=200 mA, T_A=25°C		90	100(3)	
			V_{IN}=1.2 V, I_{OUT}=200 mA, T_A=25°C		185	220(3)	
			V_{IN}=1.8 V, I_{OUT}=200 mA, T_A=85°C(3)			105	
R_{PD}	Output Discharge $R_{PULL\ DOWN}$		V_{IN}=3.3 V, V_{ON}=OFF, I_{FORCE}=20 mA, T_A=25°C, FPF1204 / FPF12045		65	75	Ω
V_{IH}	On Input Logic HIGH Voltage		V_{IN}=1.2 V to 5.5 V	1.15			V
V_{IL}	On Input Logic LOW Voltage		V_{IN}=1.2 V to 5.5 V			0.65	V
R_{ON_PD}	Pull-Down Resistance at ON Pin		V_{IN}=1.2 V to 5.5 V		8.3		MΩ
I_{ON}	On Input Leakage		V_{ON}=V_{IN} or GND			1	µA
Dynamic Characteristics							
t_{DON}	Turn-On Delay(4)		V_{IN}=3.3 V, R_L=10 Ω, C_L=0.1 µF, T_A=25°C, FPF12045		70		µs
t_R	V_{OUT} Rise Time(4)				100		
t_{ON}	Turn-On Time(6)				170		
t_{DON}	Turn-On Delay(4)				2		
t_R	V_{OUT} Rise Time(4)				2		
t_{ON}	Turn-On Time(6)				4		
t_{DOFF}	Turn-Off Delay(4,5)		V_{IN}=3.3 V, R_L=10 Ω, C_L=0.1 µF, T_A=25°C, FPF1203L		0.5		µs
t_F	V_{OUT} Fall Time(4,5)				2.0		
t_{OFF}	Turn-Off Time(5,7)				2.5		
t_{DOFF}	Turn-Off Delay(4,5)		V_{IN}=3.3 V, R_L=500 Ω, C_L=0.1 µF, T_A=25°C, FPF1203L		6		µs
t_F	V_{OUT} Fall Time(4,5)				115		
t_{OFF}	Turn-Off Time(5,7)				121		
t_{DOFF}	Turn-Off Delay(4,5)		V_{IN}=3.3 V, R_L=10 Ω, C_L=0.1 µF, T_A=25°C, FPF1203		4.0		µs
t_F	V_{OUT} Fall Time(4,5)				2.9		
t_{OFF}	Turn-Off Time(5,7)				7.3		
t_{DOFF}	Turn-Off Delay(4,5)		V_{IN}=3.3 V, R_L=500 Ω, C_L=0.1 µF, T_A=25°C, FPF1203		6		µs
t_F	V_{OUT} Fall Time(4,5)				115		
t_{OFF}	Turn-Off Time(5,7)				121		

Continued on the following page…

Electrical Characteristics

Unless otherwise noted, V_{IN}=1.2 V to 5.5 V and T_A=-40 to +85°C. Typical values are at V_{IN}=3.3 V and T_A=25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{DOFF}	Turn-Off Delay(4,5)	V_{IN}=3.3 V, R_L=10 Ω, C_L=0.1 µF, T_A=25°C, FPF1204/45(5)		4.0		µs
t_F	V_{OUT} Fall Time(4,5)			2.5		
t_{OFF}	Turn-Off Time(5,7)			6.5		
t_{DOFF}	Turn-Off Delay(4,5)	V_{IN}=3.3 V, R_L=500Ω, C_L=0.1 µF, T_A=25°C, FPF1204/45(5)		6		µs
t_F	V_{OUT} Fall Time(4,5)			11		
t_{OFF}	Turn-Off Time(5,7)			17		

Notes:

3. This parameter is guaranteed by design and characterization; not production tested.
4. $t_{DON}/t_{DOFF}/t_R/t_F$ are defined in Figure 23.
5. Output discharge enabled during off-state.
6. $t_{ON}=t_R + t_{DON}$.
7. $t_{OFF}=t_F + t_{DOFF}$.

Typical Performance Characteristics

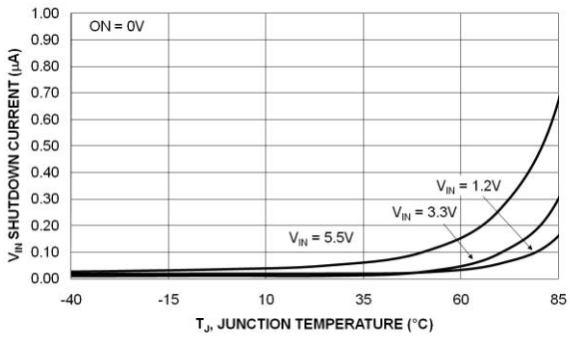


Figure 7. Shutdown Current vs. Temperature

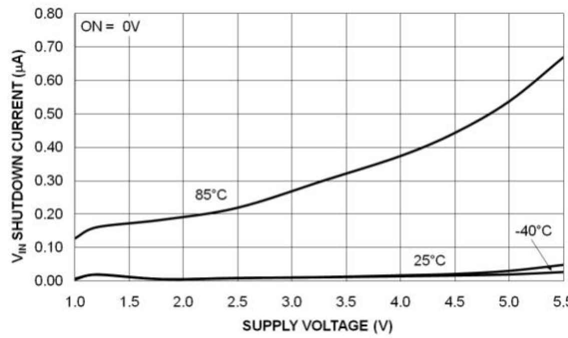


Figure 8. Shutdown Current vs. Supply Voltage

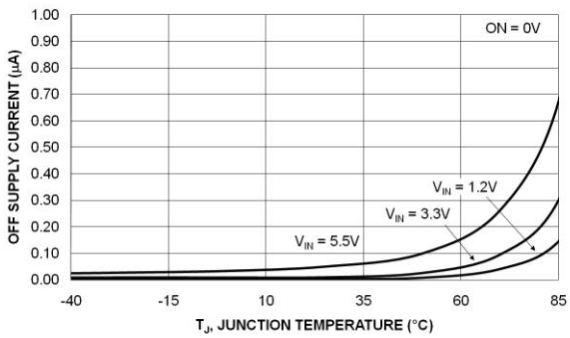


Figure 9. Off Supply Current vs. Temperature (V_{OUT} Floating)

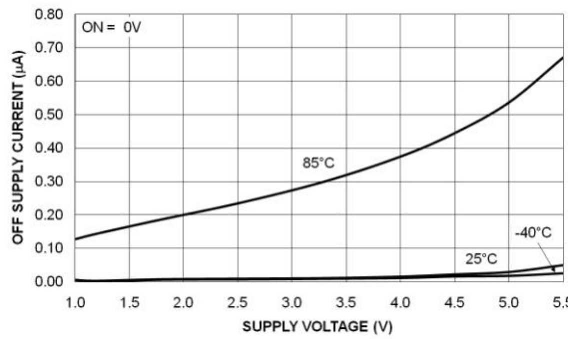


Figure 10. Off Supply Current vs. Supply Voltage (V_{OUT} Floating)

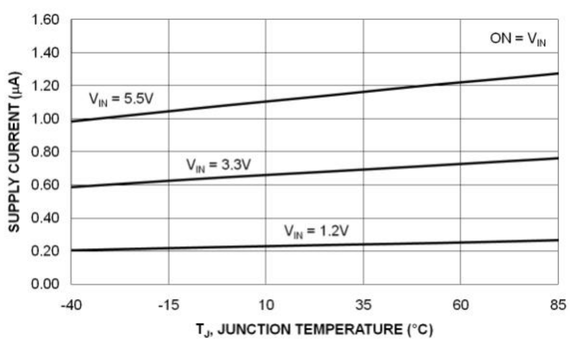


Figure 11. Quiescent Current vs. Temperature

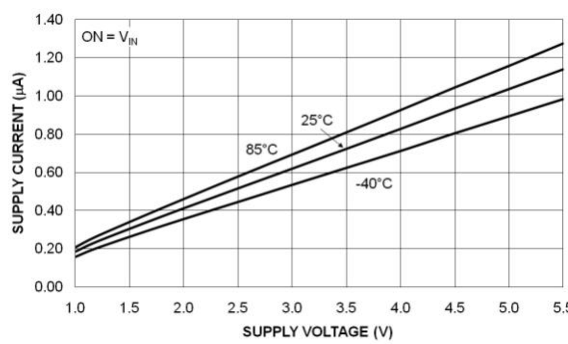


Figure 12. Quiescent Current vs. Supply Voltage

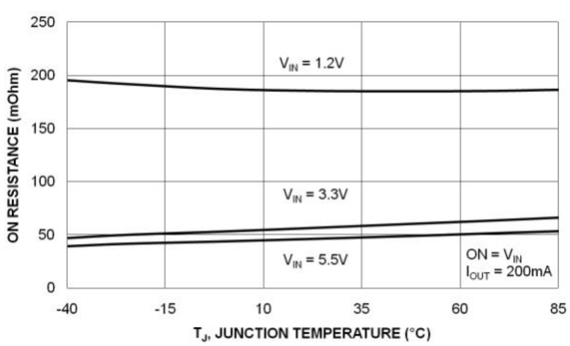


Figure 13. R_{ON} vs. Temperature

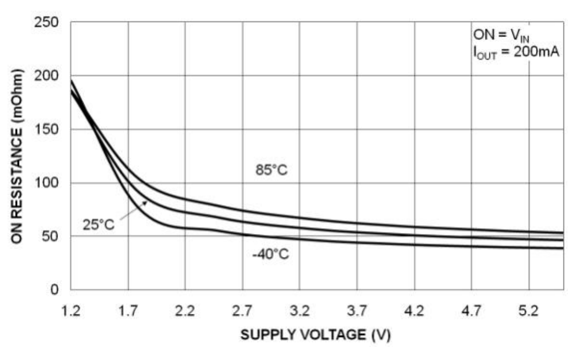


Figure 14. R_{ON} vs. Supply Voltage

Typical Performance Characteristics (Continued)

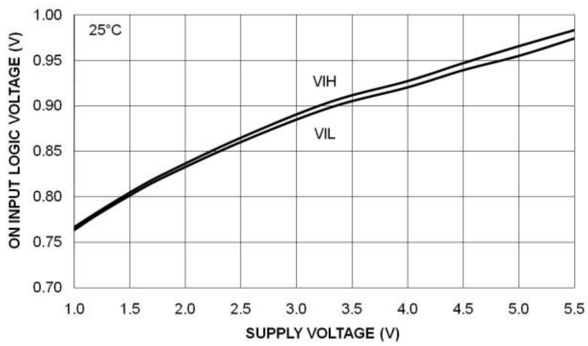


Figure 15. ON Pin Threshold vs. V_{IN}

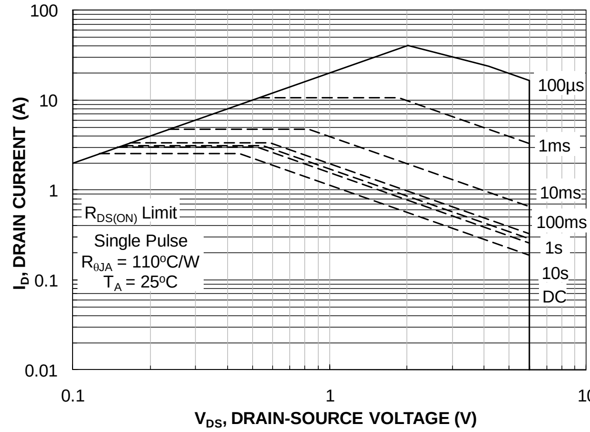


Figure 16. Drain Current vs. Drain-Source Voltage Safe Operating Area

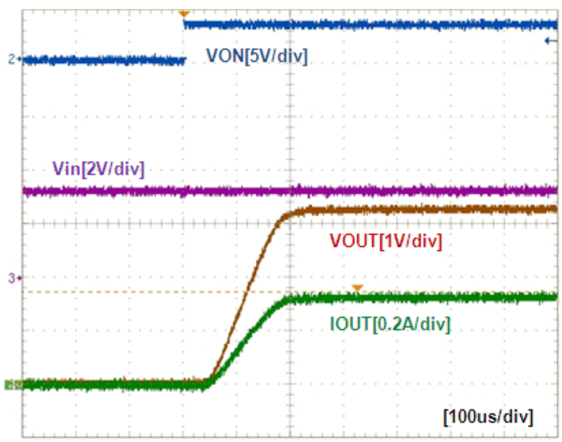


Figure 17. Turn-On Response – FPF1203 / 04
(V_{IN}=3.3 V, C_{IN}=1 µF, C_{OUT}=0.1 µF, R_L=10 Ω)

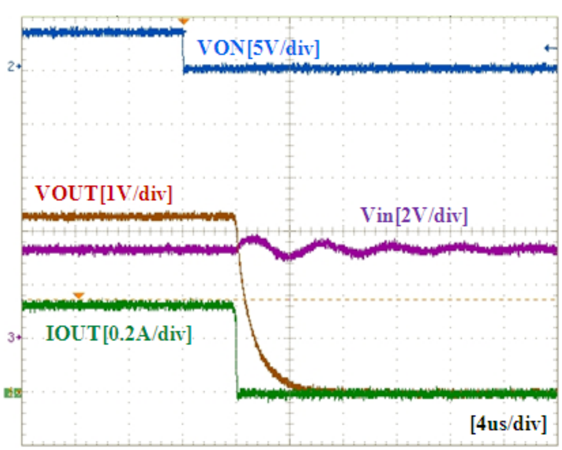


Figure 18. Turn-Off Response – FPF1203
(V_{IN}=3.3 V, C_{IN}=1 µF, C_{OUT}=0.1 µF, R_L=10 Ω)

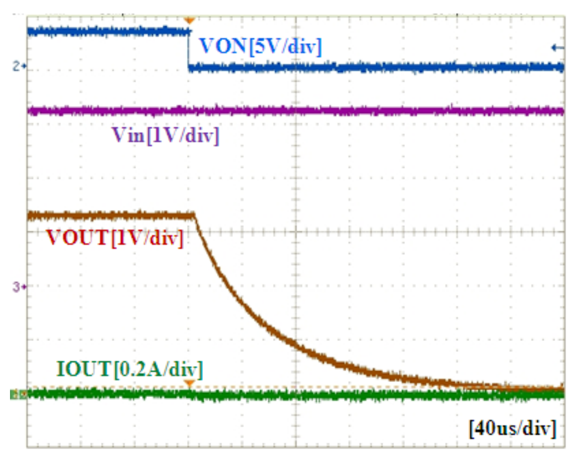


Figure 19. Turn-Off Response – FPF1203
(V_{IN}=3.3 V, C_{IN}=1 µF, C_{OUT}=0.1 µF, R_L=500 Ω)

Typical Performance Characteristics (Continued)

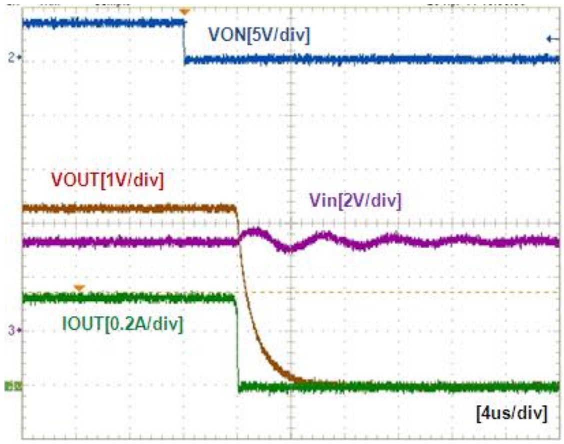


Figure 20. Turn-Off Response (V_{IN}=3.3 V, C_{IN}=1 µF, C_{OUT}=0.1 µF, R_L=10 Ω, FPF1204 / 45)

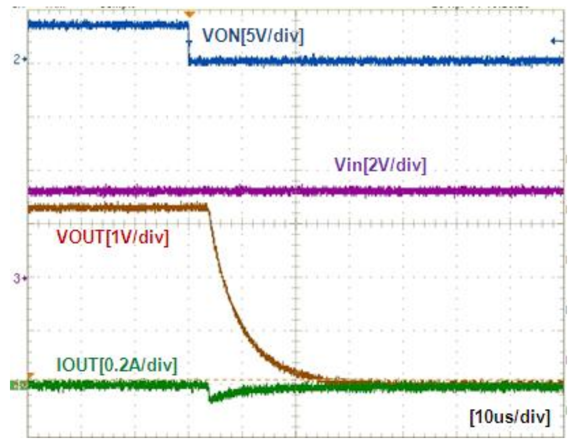


Figure 21. Turn-Off Response (V_{IN}=3.3 V, C_{IN}=1 µF, C_{OUT}=0.1 µF, R_L=500 Ω, FPF1204 / 45)

Operation and Application Description

The FPF1203 / 03L / 04 / 045 are low-R_{ON} P-channel load switches with controlled turn-on. The core of each device is a 55 mΩ P-channel MOSFET and controller capable of functioning over a wide input operating range of 1.2 to 5.5 V.

The FPF1204 / 45 contain a 65 Ω on-chip load resistor for quick output discharge when the switch is turned off.

The FPF12045 features a faster V_{OUT} Rise Time of 5 µs.

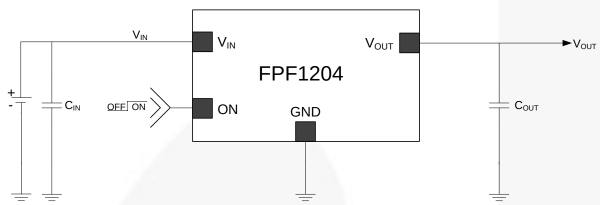


Figure 22. Typical Application

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between the V_{IN} and GND pins. A 1 µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher-value C_{IN} can be used to reduce the voltage drop in higher-current applications.

Output Capacitor

A 0.1 µF capacitor, C_{OUT}, should be placed between the V_{OUT} and GND pins. This capacitor prevents parasitic board inductance from forcing V_{OUT} below GND when the switch is on. C_{IN} greater than C_{OUT} is highly recommended. C_{OUT} greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

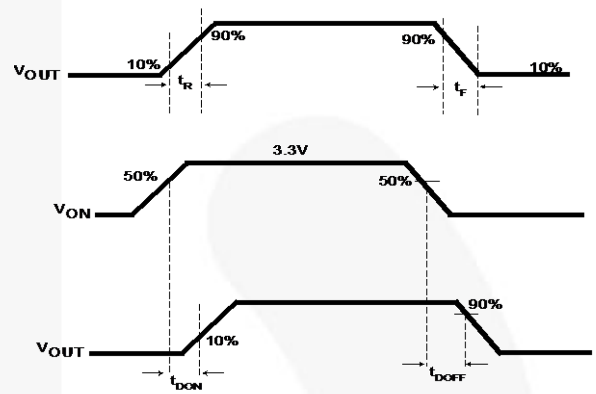


Figure 23. Timing Diagram for FPF1203/4/045

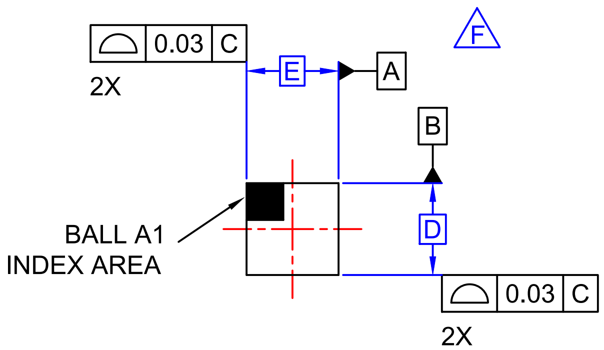
Board Layout

For best performance, traces should be as short as possible. To be most effective, input and output capacitors should be placed close to the device to minimize the effect of parasitic trace inductance on normal and short-circuit operation. Using wide traces or large copper planes for all pins (VIN, VOUT, ON, and GND) minimizes the parasitic electrical effects and the case-ambient thermal impedance. However, the VOUT pin should not connect directly to the battery source due to the discharge mechanism of the load switch.

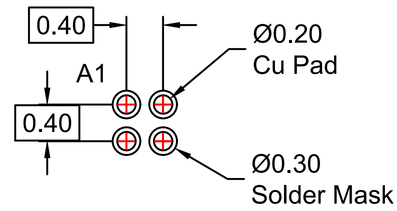
The table below pertains to the Packaging information on the following page.

Product Dimensions

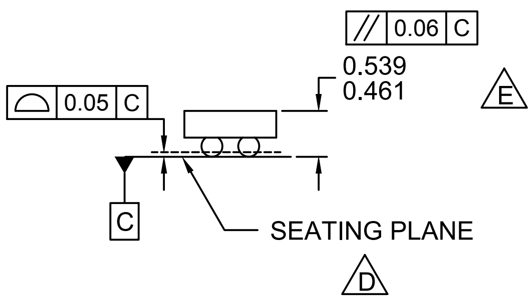
D	E	X	Y
760 µm ± 30 µm	760 µm ± 30 µm	0.180 mm± 0.018 µm	0.180 mm± 0.018 µm

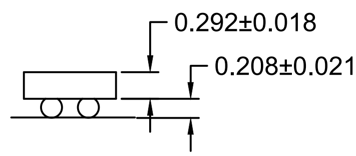


TOP VIEW

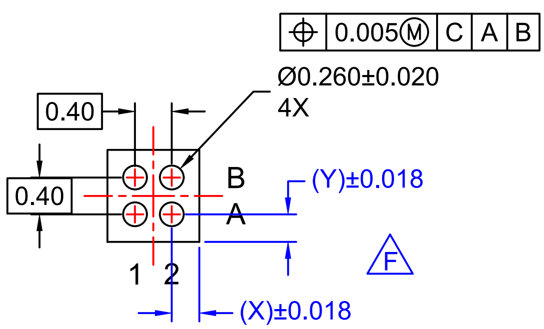


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 500 MICRONS ±39 MICRONS (461-539 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC004AFrev2.

FAIRCHILD™

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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