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# FPF1203 / FPF1203L / FPF1204 / FPF12045 IntelliMAX™ Ultra-Small, Slew-Rate-Controlled Load Switch

## Features

- 1.2 V to 5.5 V Input Voltage Operating Range
- Typical  $R_{ON}$ :
  - 45 m $\Omega$  at  $V_{IN}=5.5$  V
  - 55 m $\Omega$  at  $V_{IN}=3.3$  V
  - 90 m $\Omega$  at  $V_{IN}=1.8$  V
  - 185 m $\Omega$  at  $V_{IN}=1.2$  V
- Slew Rate Control with  $t_R$ :
  - FPF1203/FPF1203L/FPF1204: 100  $\mu$ s
  - FPF12045: 2  $\mu$ s
- Output Discharge Function on FPF1204 / 45
- Low <1.5  $\mu$ A Quiescent Current
- ESD Protected: Above 7 kV HBM, 2 kV CDM
- GPIO / CMOS-Compatible Enable Circuitry
- 4-Bump, WLCSP 0.76 mm x 0.76 mm, 0.4 mm Pitch

## Description

The FPF1203 / 03L / 04 / 45 are ultra-small integrated IntelliMAX™ load switches with integrated P-channel switch and analog control features. Integrated slew-rate control prevents inrush current and the resulting excessive voltage drop on the power rail. The input voltage range operates from 1.2 V to 5.5 V to provide power-disconnect capability for post-regulated power rails in portable and consumer products. The low shut-off current allows power designs to meet standby and off-power drain specifications.

The FPF120x are controlled by a logic input (ON pin) compatible with standard CMOS GPIO circuitry found on Field Programmable Gate Array (FPGA) embedded processors. The FPF120x are available in 0.76 mm x 0.76 mm 4-bump WLCSP.

## Applications

- Mobile Devices and Smart Phones
- Portable Media Devices
- Tablet PCs
- Advanced Notebook, UMPC, MID
- Portable Medical Devices
- GPS and Navigation Equipment

## Ordering Information

Part Number	Top Mark	Switch (Typical) at 3.3V <sub>IN</sub>	Output Discharge	ON Pin Activity	t <sub>R</sub>	Package
FPF1203UCX	QL	55 m $\Omega$	NA	Active HIGH	100 $\mu$ s	4-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.76 mm x 0.76 mm, 0.4 mm Pitch
FPF1203LUCX	QP	55 m $\Omega$	NA	Active LOW	100 $\mu$ s	
FPF1204UCX	QM	55 m $\Omega$	65 $\Omega$	Active HIGH	100 $\mu$ s	
FPF1204UCX_F013 (Amkor Assembly Only)	QM	55 m $\Omega$	65 $\Omega$	Active HIGH	100 $\mu$ s	
FPF1204BUCX (Backside Laminate)	QM	55 m $\Omega$	65 $\Omega$	Active HIGH	100 $\mu$ s	
FPF12045UCX	NC	55 m $\Omega$	65 $\Omega$	Active HIGH	2 $\mu$ s	

FPF1203 / FPF1203L / FPF1204 / FPF12045 — IntelliMAX™ Ultra-Small, Slew-Rate-Controlled Load Switch

### Application Diagram

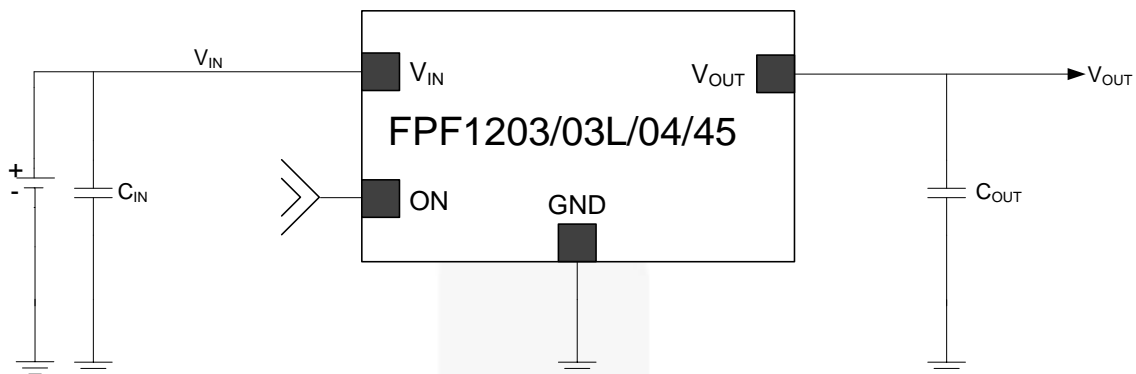


Figure 1. Typical Application

### Functional Block Diagram

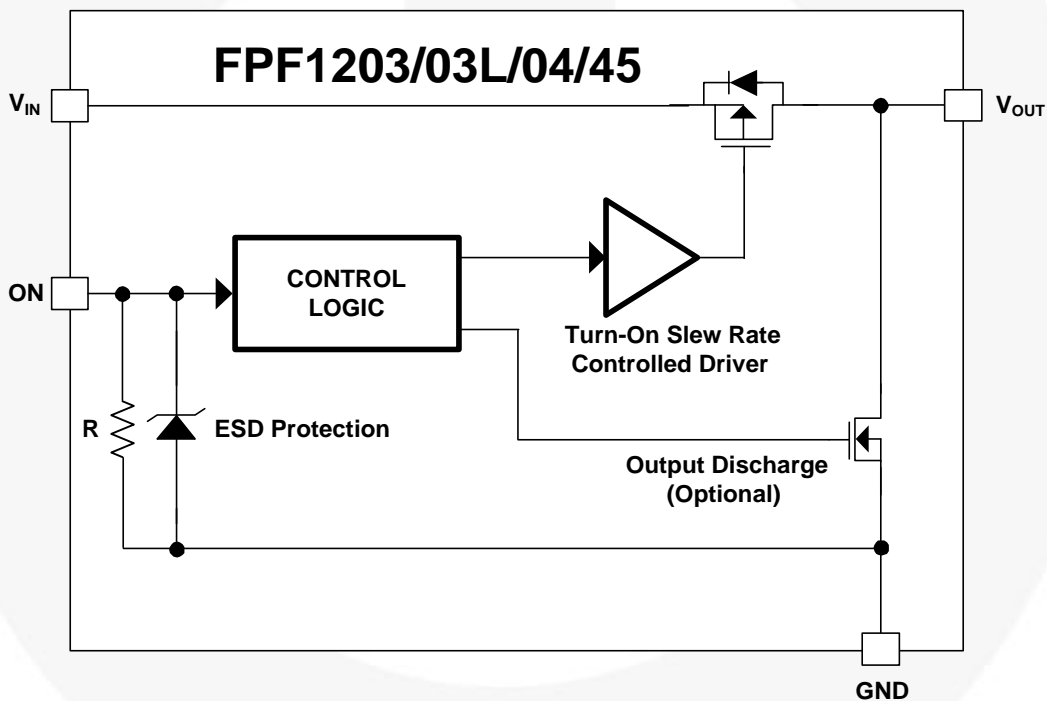


Figure 2. Functional Block Diagram (Output Discharge for FPF1204 / 45)

## Pin Configurations

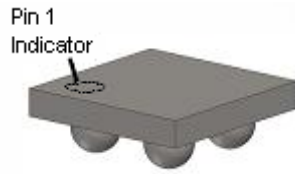


Figure 3. WLCSP Bumps Facing Down (Top View)

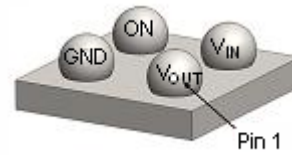


Figure 4. WLCSP Bumps Facing Up (Bottom View)

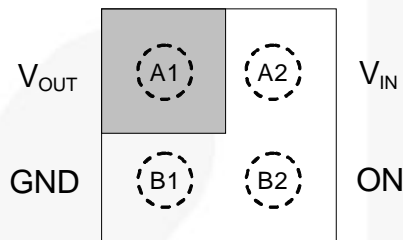


Figure 5. Pin Assignments (Top View)

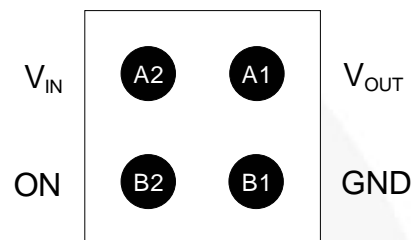


Figure 6. Pin Assignments (Bottom View)

## Pin Definitions

Pin #	Name	Description
A1	$V_{OUT}$	Switch output
A2	$V_{IN}$	Supply input: input to the power switch
B1	GND	Ground
B2	ON	ON/OFF Control, active HIGH; FPF1203/04/45
B2	ON	ON/OFF Control, active LOW; FPF1203L

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{IN}$	$V_{IN}$ , $V_{OUT}$ , $V_{ON}$ to GND	-0.3	6.0	V
$I_{SW}$	Maximum Continuous Switch Current at Ambient Operating Temperature		2.2	A
$P_D$	Power Dissipation at $T_A=25^\circ\text{C}$		1.0	W
$T_{STG}$	Storage Temperature Range	-65	+150	$^\circ\text{C}$
$\Theta_{JA}$	Thermal Resistance, Junction-to-Ambient	1S2P with One Thermal Via <sup>(1)</sup>	110	$^\circ\text{C/W}$
		1S2P without Thermal Via <sup>(2)</sup>	95	
ESD	Electrostatic Discharge Capability <sup>(1,2)</sup>	Human Body Model, JESD22-A114	7	kV
		Charged Device Model, JESD22-C101	2	

### Notes:

1. Measured using 2S2P JEDEC std. PCB.
2. Measured using 2S2P JEDEC PCB COLD PLATE Method.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{IN}$	Input Voltage	1.2	5.5	V
$T_A$	Ambient Operating Temperature	-40	+85	$^\circ\text{C}$

## Electrical Characteristics

Unless otherwise noted,  $V_{IN}=1.2\text{ V}$  to  $5.5\text{ V}$  and  $T_A=-40$  to  $+85^\circ\text{C}$ . Typical values are at  $V_{IN}=3.3\text{ V}$  and  $T_A=25^\circ\text{C}$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	
<b>Basic Operation</b>							
$V_{IN}$	Supply Voltage		1.2		5.5	V	
$I_{Q(OFF)}$	Off Supply Current	PPF1203/04/45	$V_{ON}=GND, V_{OUT}=Open, V_{IN}=5.5\text{ V}$		0.1	1.0	$\mu\text{A}$
		PPF1203L	$V_{ON}=V_{IN}, V_{OUT}=Open, V_{IN}=5.5\text{ V}$		1.0	2.0	
$I_{SD}$	Shutdown Current	PPF1203/04/45	$V_{ON}=GND, V_{OUT}=GND$		0.1	1.0	$\mu\text{A}$
		PPF1203L	$V_{ON}=V_{IN}, V_{OUT}=GND$		1.2	3.0	
$I_Q$	Quiescent Current	PPF1203/04/45	$I_{OUT}=0\text{ mA}, V_{ON}=V_{IN}, =5.5\text{ V}$		0.1	1.5	$\mu\text{A}$
		PPF1203L	$I_{OUT}=0\text{ mA}, V_{ON}=GND, V_{IN}, =5.5\text{ V}$				
$R_{ON}$	On Resistance		$V_{IN}=5.5\text{ V}, I_{OUT}=200\text{ mA}, T_A=25^\circ\text{C}$		45	55 <sup>(3)</sup>	m $\Omega$
			$V_{IN}=3.3\text{ V}, I_{OUT}=200\text{ mA}, T_A=25^\circ\text{C}$		55	65 <sup>(3)</sup>	
			$V_{IN}=1.8\text{ V}, I_{OUT}=200\text{ mA}, T_A=25^\circ\text{C}$		90	100 <sup>(3)</sup>	
			$V_{IN}=1.2\text{ V}, I_{OUT}=200\text{ mA}, T_A=25^\circ\text{C}$		185	220 <sup>(3)</sup>	
			$V_{IN}=1.8\text{ V}, I_{OUT}=200\text{ mA}, T_A=85^\circ\text{C}$ <sup>(3)</sup>			105	
$R_{PD}$	Output Discharge $R_{PULL\ DOWN}$		$V_{IN}=3.3\text{ V}, V_{ON}=OFF,$ $I_{FORCE}=20\text{ mA}, T_A=25^\circ\text{C},$ PPF1204 / PPF12045		65	75	$\Omega$
$V_{IH}$	On Input Logic HIGH Voltage		$V_{IN}=1.2\text{ V}$ to $5.5\text{ V}$	1.15			V
$V_{IL}$	On Input Logic LOW Voltage		$V_{IN}=1.2\text{ V}$ to $5.5\text{ V}$			0.65	V
$R_{ON\_PD}$	Pull-Down Resistance at ON Pin		$V_{IN}=1.2\text{ V}$ to $5.5\text{ V}$		8.3		M $\Omega$
$I_{ON}$	On Input Leakage		$V_{ON}=V_{IN}$ or GND			1	$\mu\text{A}$
<b>Dynamic Characteristics</b>							
$t_{DON}$	Turn-On Delay <sup>(4)</sup>	$V_{IN}=3.3\text{ V}, R_L=10\ \Omega, C_L=0.1\ \mu\text{F},$ $T_A=25^\circ\text{C}, \text{PPF12045}$			70	$\mu\text{s}$	
$t_R$	$V_{OUT}$ Rise Time <sup>(4)</sup>				100		
$t_{ON}$	Turn-On Time <sup>(6)</sup>				170		
$t_{DON}$	Turn-On Delay <sup>(4)</sup>				2		
$t_R$	$V_{OUT}$ Rise Time <sup>(4)</sup>				2		
$t_{ON}$	Turn-On Time <sup>(6)</sup>				4		
$t_{DOFF}$	Turn-Off Delay <sup>(4,5)</sup>	$V_{IN}=3.3\text{ V}, R_L=10\ \Omega, C_L=0.1\ \mu\text{F},$ $T_A=25^\circ\text{C}, \text{PPF1203L}$			0.5	$\mu\text{s}$	
$t_F$	$V_{OUT}$ Fall Time <sup>(4,5)</sup>				2.0		
$t_{OFF}$	Turn-Off Time <sup>(5,7)</sup>				2.5		
$t_{DOFF}$	Turn-Off Delay <sup>(4,5)</sup>	$V_{IN}=3.3\text{ V}, R_L=500\ \Omega, C_L=0.1\ \mu\text{F},$ $T_A=25^\circ\text{C}, \text{PPF1203L}$			6	$\mu\text{s}$	
$t_F$	$V_{OUT}$ Fall Time <sup>(4,5)</sup>				115		
$t_{OFF}$	Turn-Off Time <sup>(5,7)</sup>				121		
$t_{DOFF}$	Turn-Off Delay <sup>(4,5)</sup>	$V_{IN}=3.3\text{ V}, R_L=10\ \Omega, C_L=0.1\ \mu\text{F},$ $T_A=25^\circ\text{C}, \text{PPF1203}$			4.0	$\mu\text{s}$	
$t_F$	$V_{OUT}$ Fall Time <sup>(4,5)</sup>				2.9		
$t_{OFF}$	Turn-Off Time <sup>(5,7)</sup>				7.3		
$t_{DOFF}$	Turn-Off Delay <sup>(4,5)</sup>	$V_{IN}=3.3\text{ V}, R_L=500\ \Omega, C_L=0.1\ \mu\text{F},$ $T_A=25^\circ\text{C}, \text{PPF1203}$			6	$\mu\text{s}$	
$t_F$	$V_{OUT}$ Fall Time <sup>(4,5)</sup>				115		
$t_{OFF}$	Turn-Off Time <sup>(5,7)</sup>				121		

Continued on the following page...

## Electrical Characteristics

Unless otherwise noted,  $V_{IN}=1.2\text{ V}$  to  $5.5\text{ V}$  and  $T_A=-40$  to  $+85^\circ\text{C}$ . Typical values are at  $V_{IN}=3.3\text{ V}$  and  $T_A=25^\circ\text{C}$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{DOFF}$	Turn-Off Delay <sup>(4,5)</sup>	$V_{IN}=3.3\text{ V}$ , $R_L=10\ \Omega$ , $C_L=0.1\ \mu\text{F}$ , $T_A=25^\circ\text{C}$ , FPF1204/45 <sup>(5)</sup>		4.0		$\mu\text{s}$
$t_F$	$V_{OUT}$ Fall Time <sup>(4,5)</sup>			2.5		
$t_{OFF}$	Turn-Off Time <sup>(5,7)</sup>			6.5		
$t_{DOFF}$	Turn-Off Delay <sup>(4,5)</sup>	$V_{IN}=3.3\text{ V}$ , $R_L=500\ \Omega$ , $C_L=0.1\ \mu\text{F}$ , $T_A=25^\circ\text{C}$ , FPF1204/45 <sup>(5)</sup>		6		$\mu\text{s}$
$t_F$	$V_{OUT}$ Fall Time <sup>(4,5)</sup>			11		
$t_{OFF}$	Turn-Off Time <sup>(5,7)</sup>			17		

### Notes:

- This parameter is guaranteed by design and characterization; not production tested.
- $t_{DON}/t_{DOFF}/t_R/t_F$  are defined in Figure 23.
- Output discharge enabled during off-state.
- $t_{ON}=t_R + t_{DON}$ .
- $t_{OFF}=t_F + t_{DOFF}$ .

## Typical Performance Characteristics

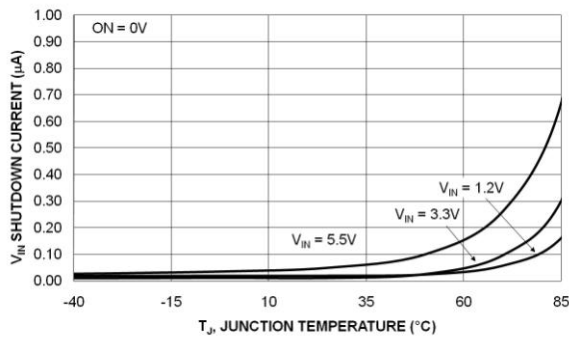


Figure 7. Shutdown Current vs. Temperature

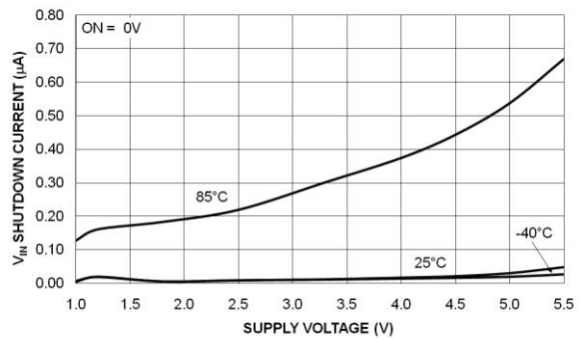


Figure 8. Shutdown Current vs. Supply Voltage

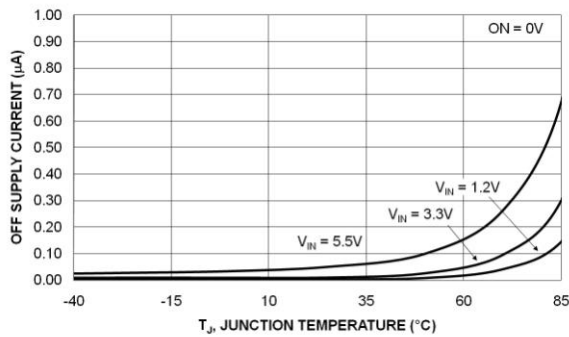


Figure 9. Off Supply Current vs. Temperature (V<sub>OUT</sub> Floating)

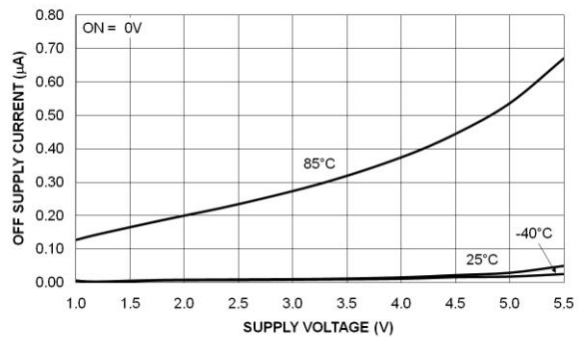


Figure 10. Off Supply Current vs. Supply Voltage (V<sub>OUT</sub> Floating)

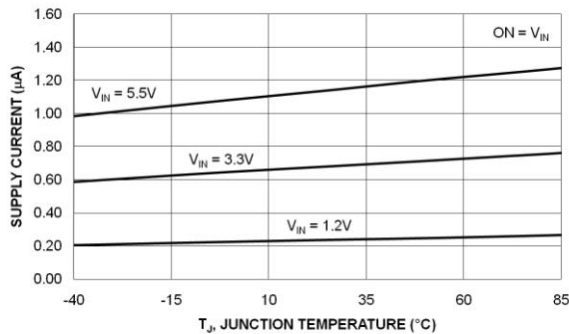


Figure 11. Quiescent Current vs. Temperature

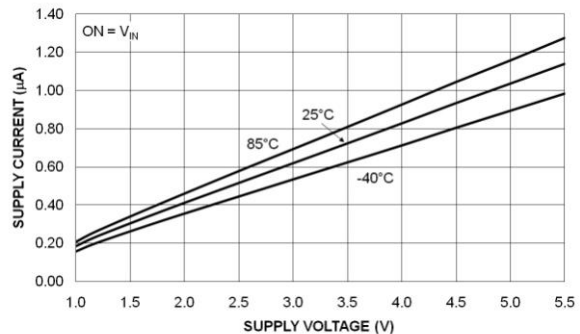


Figure 12. Quiescent Current vs. Supply Voltage

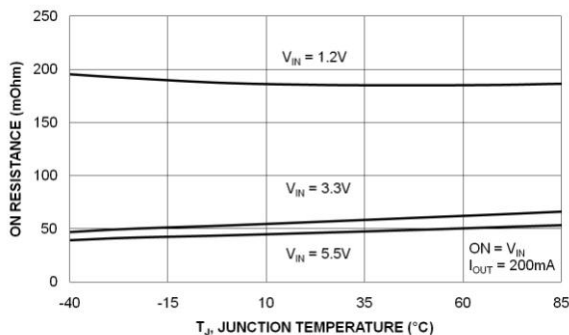


Figure 13. R<sub>ON</sub> vs. Temperature

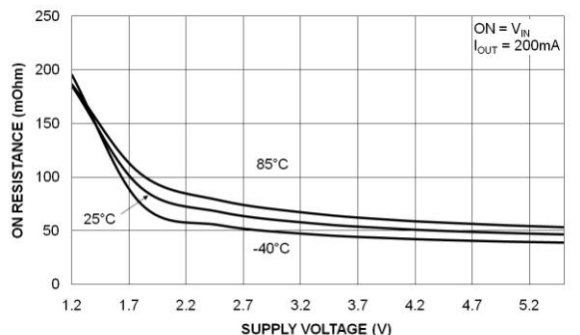


Figure 14. R<sub>ON</sub> vs. Supply Voltage



Typical Performance Characteristics (Continued)

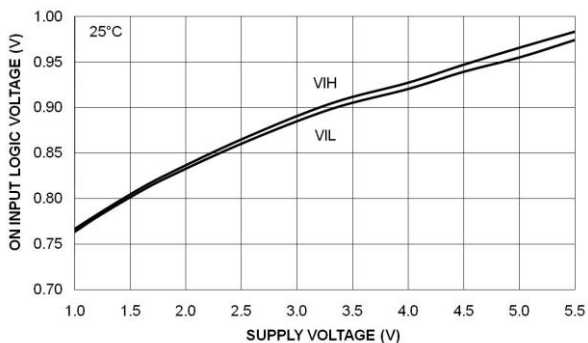


Figure 15. ON Pin Threshold vs.  $V_{IN}$

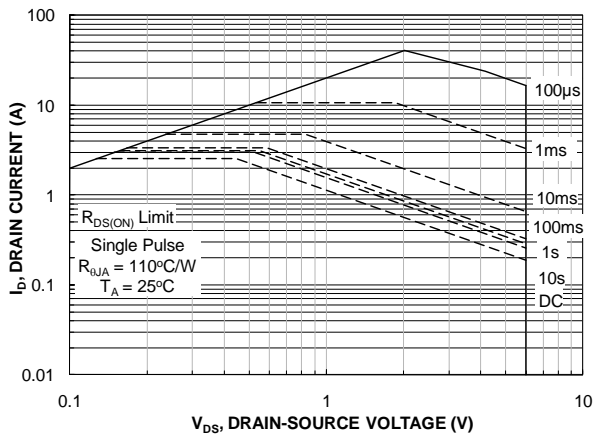


Figure 16. Drain Current vs. Drain-Source Voltage Safe Operating Area

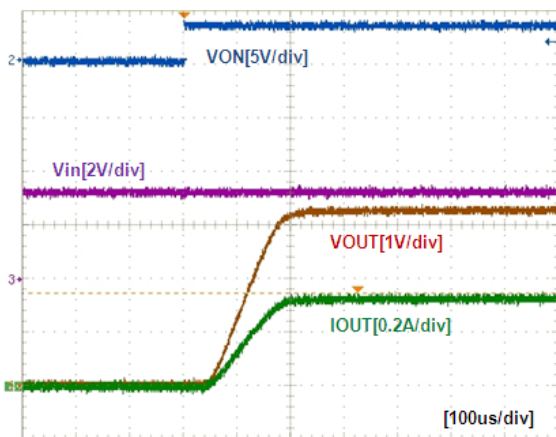


Figure 17. Turn-On Response – FPF1203 / 04 ( $V_{IN}=3.3\text{ V}$ ,  $C_{IN}=1\ \mu\text{F}$ ,  $C_{OUT}=0.1\ \mu\text{F}$ ,  $R_L=10\ \Omega$ )

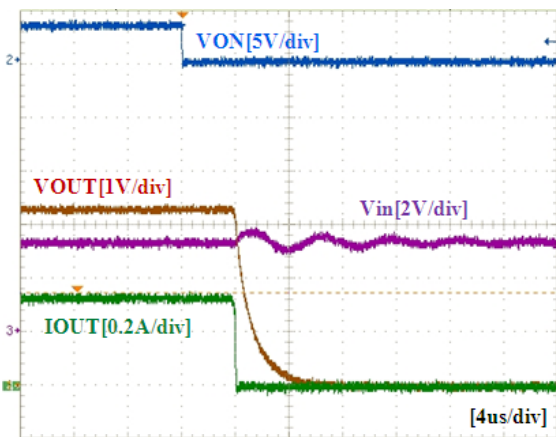


Figure 18. Turn-Off Response – FPF1203 ( $V_{IN}=3.3\text{ V}$ ,  $C_{IN}=1\ \mu\text{F}$ ,  $C_{OUT}=0.1\ \mu\text{F}$ ,  $R_L=10\ \Omega$ )

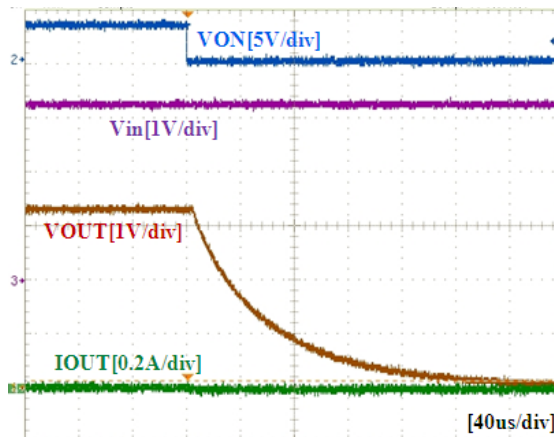


Figure 19. Turn-Off Response – FPF1203 ( $V_{IN}=3.3\text{ V}$ ,  $C_{IN}=1\ \mu\text{F}$ ,  $C_{OUT}=0.1\ \mu\text{F}$ ,  $R_L=500\ \Omega$ )

Typical Performance Characteristics (Continued)

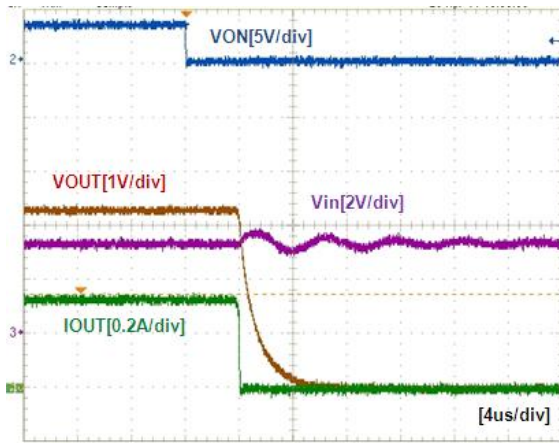


Figure 20. Turn-Off Response ( $V_{IN}=3.3\text{ V}$ ,  $C_{IN}=1\ \mu\text{F}$ ,  $C_{OUT}=0.1\ \mu\text{F}$ ,  $R_L=10\ \Omega$ , FPF1204 / 45)

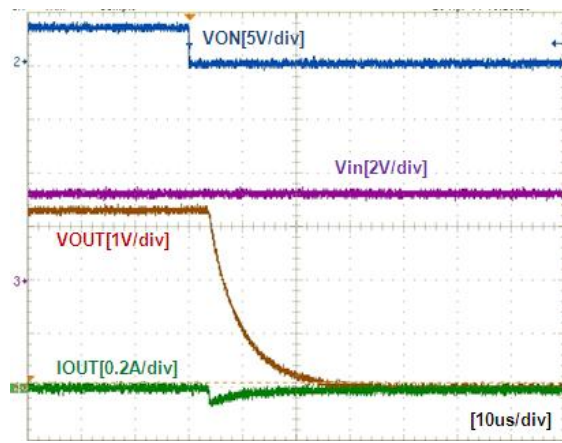


Figure 21. Turn-Off Response ( $V_{IN}=3.3\text{ V}$ ,  $C_{IN}=1\ \mu\text{F}$ ,  $C_{OUT}=0.1\ \mu\text{F}$ ,  $R_L=500\ \Omega$ , FPF1204 / 45)

## Operation and Application Description

The FPF1203 / 03L / 04 / 045 are low- $R_{ON}$  P-channel load switches with controlled turn-on. The core of each device is a 55 m $\Omega$  P-channel MOSFET and controller capable of functioning over a wide input operating range of 1.2 to 5.5 V.

The FPF1204 / 45 contain a 65  $\Omega$  on-chip load resistor for quick output discharge when the switch is turned off.

The FPF12045 features a faster  $V_{OUT}$  Rise Time of 5  $\mu$ s.

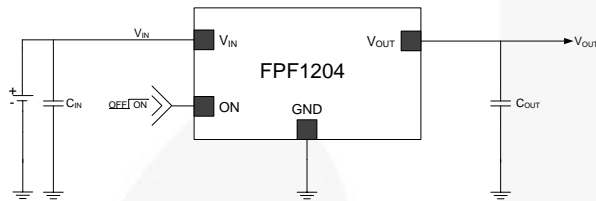


Figure 22. Typical Application

## Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between the  $V_{IN}$  and GND pins. A 1  $\mu$ F ceramic capacitor,  $C_{IN}$ , placed close to the pins is usually sufficient. Higher-value  $C_{IN}$  can be used to reduce the voltage drop in higher-current applications.

## Output Capacitor

A 0.1  $\mu$ F capacitor,  $C_{OUT}$ , should be placed between the  $V_{OUT}$  and GND pins. This capacitor prevents parasitic board inductance from forcing  $V_{OUT}$  below GND when the switch is on.  $C_{IN}$  greater than  $C_{OUT}$  is highly recommended.  $C_{OUT}$  greater than  $C_{IN}$  can cause  $V_{OUT}$  to exceed  $V_{IN}$  when the system supply is removed. This could result in current flow through the body diode from  $V_{OUT}$  to  $V_{IN}$ .

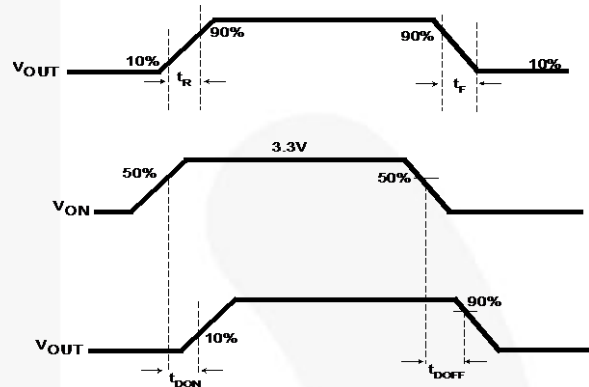


Figure 23. Timing Diagram for FPF1203/4/045

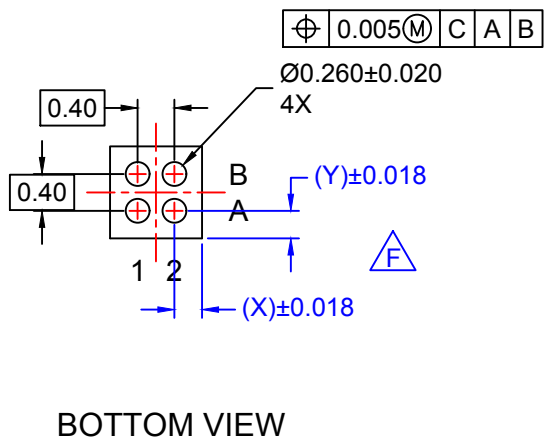
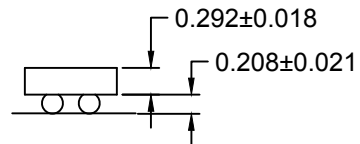
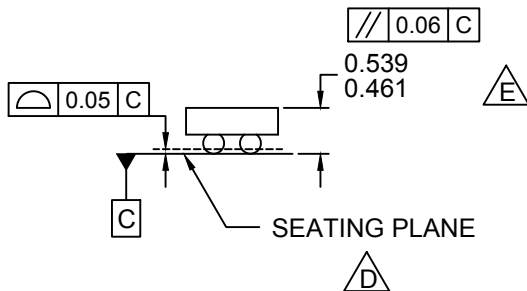
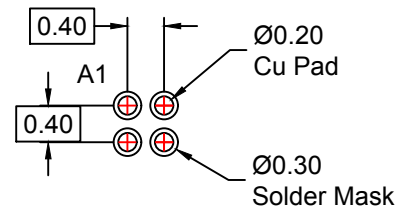
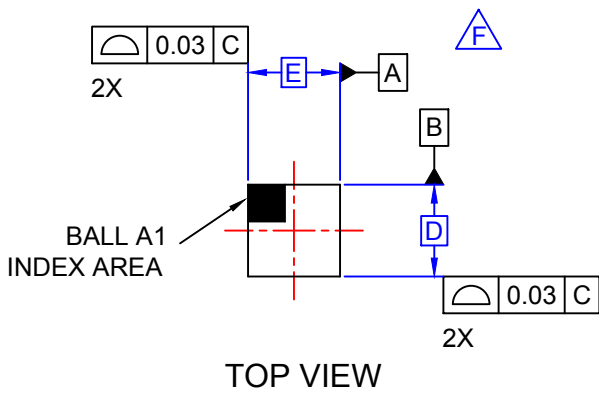
## Board Layout

For best performance, traces should be as short as possible. To be most effective, input and output capacitors should be placed close to the device to minimize the effect of parasitic trace inductance on normal and short-circuit operation. Using wide traces or large copper planes for all pins ( $V_{IN}$ ,  $V_{OUT}$ , ON, and GND) minimizes the parasitic electrical effects and the case-ambient thermal impedance. However, the  $V_{OUT}$  pin should not connect directly to the battery source due to the discharge mechanism of the load switch.

The table below pertains to the Packaging information on the following page.

## Product Dimensions

D	E	X	Y
760 $\mu$ m $\pm$ 30 $\mu$ m	760 $\mu$ m $\pm$ 30 $\mu$ m	0.180 mm $\pm$ 0.018 $\mu$ m	0.180 mm $\pm$ 0.018 $\mu$ m



### NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 500 MICRONS ±39 MICRONS (461-539 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILNAME: MKT-UC004AFrev2.



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