# LM4946 Boomer® Audio Power Amplifier Series Output Capacitor-Less Audio Subsystem with Programmable TI 3D

**Check for Samples: LM4946**

## FEATURES

- **I²C/SPI Control Interface**
- **I²C/SPI Programmable TI 3D Audio**
- **I²C/SPI Controlled 32 Step Digital Volume Control (-54dB to +18dB)**
- **Three Independent Volume Channels (Left, Right, Mono)**
- **Eight Distinct Output Modes**
- **WQFN and DSBGA Surface Mount Packaging**
- **"Click and Pop" Suppression Circuitry**
- **Thermal Shutdown Protection**
- **Low Shutdown Current (0.02uA, typ)**
- **RF Immunity Topology**

## APPLICATIONS

- **Mobile Phones**
- **PDAs**

## KEY SPECIFICATIONS

- **THD+N at 1kHz, 540mW into 8Ω BTL (3.3V) 1.0% (typ)**
- **THD+N at 1kHz, 35mW into 32Ω SE (3.3V) 1.0% (typ)**
- **Single Supply Operation (VDD) 2.7 to 5.5V**
- **I2C/SPI Single Supply Operation**
  - **WQFN 2.2 to 5.5V**
  - **DSBGA 1.7 to 5.5V**

## DESCRIPTION

The LM4946 is an audio power amplifier capable of delivering 540mW of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N, 35mW per channel of continuous average power into stereo 32Ω single-ended (SE) loads with 1% THD+N, or an output capacitor-less (OCL) configuration with identical specifications as the SE configuration, from a 3.3V power supply.

The LM4946 has three input channels: one pair for a two-channel stereo signal and the third for a differential single-channel mono input. The LM4946 features a 32-step digital volume control and eight distinct output modes. The digital volume control, 3D enhancement, and output modes (mono/SE/OCL) are programmed through a two-wire I²C or a three-wire SPI compatible interface that allows flexibility in routing and mixing audio channels.

The LM4946 is designed for cellular phone, PDA, and other portable handheld applications. It delivers high quality output power from a surface-mount package and requires only seven external components in the OCL mode (two additional components in SE mode).

## Typical Application

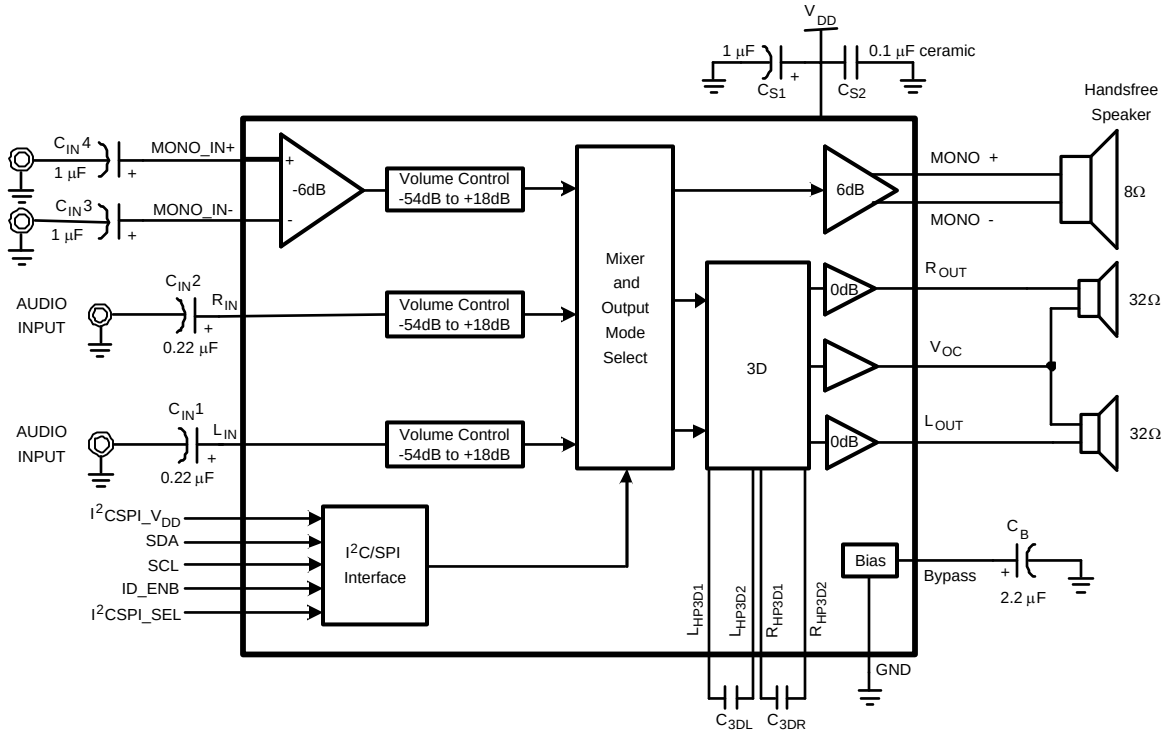



**Figure 1. Typical Audio Amplifier Application Circuit-Output Capacitor-less**

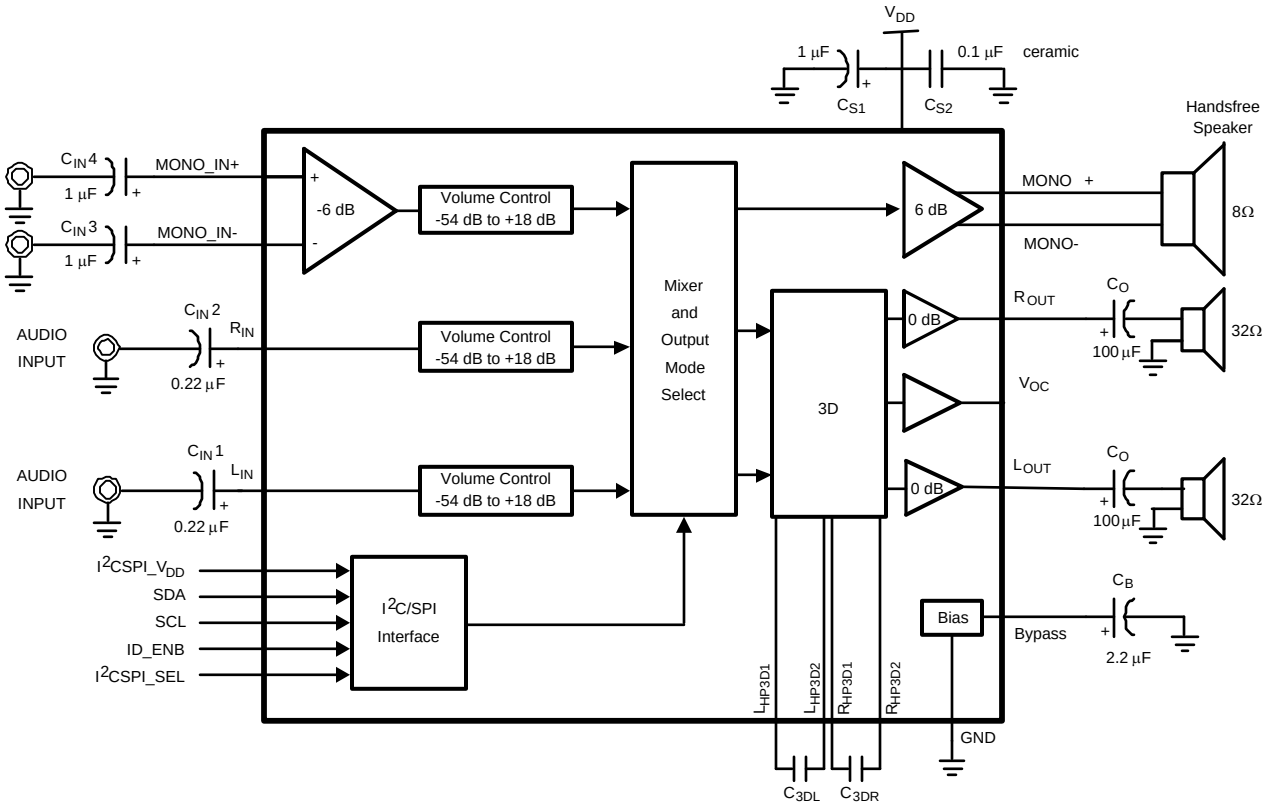



**Figure 2. Typical Audio Amplifier Application Circuit-Single Ended**

## Connection Diagram

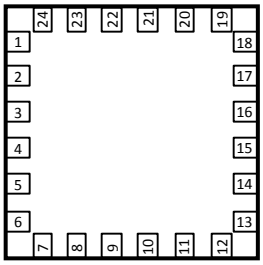



**Figure 3. 24 Lead WQFN Package (Top View)**

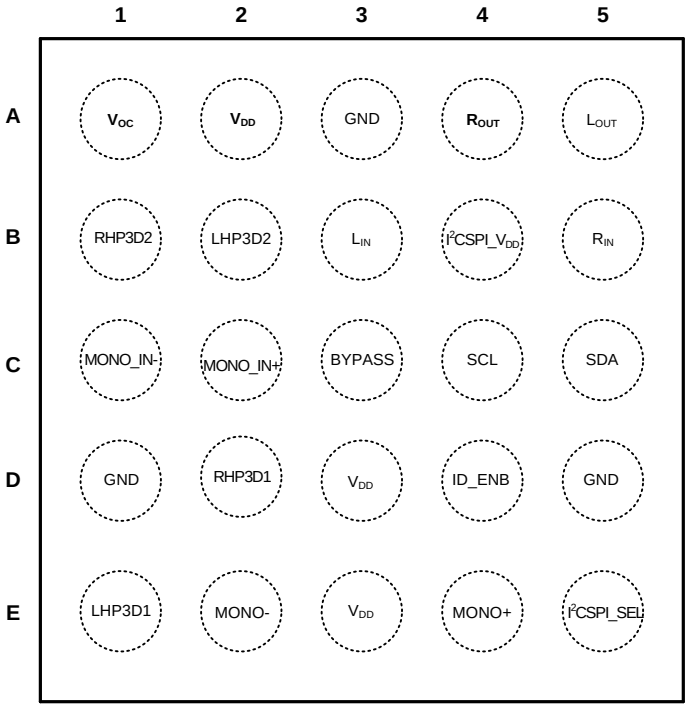



**Figure 4. 25 Bump DSBGA Package (Top View)**

## PIN DESCRIPTIONS

| Pin Number (WQFN) | Bump (DSBGA) | Name | Description |
|---|---|---|---|
| 1 | B2 | LHP3D2 | Left Headphone 3D Input 1 |
| 2 | A1 | $V_{OC}$ | Center Amplifier Output |
| 3 | A2 | $V_{DD}$ | Voltage Supply |
| 4 | A3 | GND | Ground |
| 5 | A4 | $R_{OUT}$ | Right Headphone Output |
| 6 | A5 | $L_{OUT}$ | Left Headphone Output |
| 7 | B4 | $I^2CSPI\_V_{DD}$ | $I^2C$ or SPI Interface Voltage Supply |
| 8 | B5 | $R_{IN}$ | Right Input Channel |
| 9 | B3 | $L_{IN}$ | Left Input Channel |
| 10 | C5 | SDA | Data |
| 11 | C4 | SCL | Clock |
| 12 | D5 | GND | Ground |
| 13 | D4 | ID_ENB | Address Identification/Enable Bar |
| 14 | E5 | $I^2CSPI\_SEL$ | $I^2C$ or SPI Select |
| 15 | E4 | MONO+ | Loudspeaker Output Positive |
| 16 | D3 | $V_{DD}$ | Voltage Supply |
| 17 | E2 | MONO- | Loudspeaker Output Negative |
| 18 | E1 | LHP3D1 | Left Headphone 3D Input 2 |
| 19 | D2 | RHP3D1 | Right Headphone 3D Input 1 |
| 20 | D1 | GND | Ground |
| 21 | C3 | BYPASS | Half-Supply Bypass |
| 22 | C1 | MONO_IN- | Loudspeaker Negative Input |
| 23 | C2 | MONO_IN+ | Loudspeaker Positive Input |
| 24 | B1 | RHP3D2 | Right Headphone 3D Input 2 |
|  | E3 | $V_{DD}$ | Voltage Supply |

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings(1)(2)

| | | |
|---|---|---|
| Supply Voltage | | 6.0V |
| Storage Temperature | | −65°C to +150°C |
| Input Voltage | | −0.3 to $V_{DD}$ +0.3 |
| ESD Susceptibility(3) | | 2.0kV |
| ESD Machine model(4) | | 200V |
| Junction Temperature | | 150°C |
| Soldering Information | Vapor Phase (60 sec.) | 215°C |
| | Infrared (15 sec.) | 220°C |
| Thermal Resistance(5) | $\theta_{JA}$ (typ) - RTW0024A | 46°C/W |
| | $\theta_{JA}$ (typ) - YFQ0025 | 49°C/W |

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human body model, 100pF discharged through a 1.5kΩ resistor.
(4) Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).
(5) The given $\theta_{JA}$ for an LM4946SQ mounted on a demonstration board with a 9$in^2$ area of 1oz printed circuit board copper ground plane.

## Operating Ratings

| | |
|---|---|
| Temperature Range | −40°C to 85°C |
| Supply Voltage ($V_{DD}$) | 2.7V ≤ $V_{DD}$ ≤ 5.5V |
| Supply Voltage ($I^2C$/SPI)(1) | $I^2CSPI\_V_{DD}$ ≤ $V_{DD}$ |
| WQFN | 2.2V ≤ $I^2CSPI\_V_{DD}$ ≤ 5.5V |
| DSBGA | 1.7V ≤ $I^2CSPI\_V_{DD}$ ≤ 5.5V |

(1) Refer to this table.

## Electrical Characteristics 3.3V[1][2]

The following specifications apply for $V_{DD}$ = 3.3V, $T_A$ = 25°C, all volume controls set to 0dB, unless otherwise specified.

| Symbol | Parameter | Conditions | LM4946 | | Units (Limits)[3] |
|---|---|---|---|---|---|
| | | | Typical[4] | Limits[5] | |
| $I_{DD}$ | Supply Current | Output Modes 2, 4, 6<br>$V_{IN}$ = 0V; No load,<br>SE Headphone | 3.25 | | mA |
| | | Output Modes 1, 3, 5, 7<br>$V_{IN}$ = 0V; No load,<br>SE Headphone | 5.65 | | mA |
| | | Output Modes 2, 4, 6<br>$V_{IN}$ = 0V; No load,<br>OCL Headphone | 4 | 6.5 | mA (max) |
| | | Output Modes 1, 3, 5,<br>$V_{IN}$ = 0V; No load,<br>OCL Headphone | 5 | | mA |
| | | Output Modes 7<br>$V_{IN}$ = 0V; No load,<br>OCL Headphone | 6.5 | 10.5 | mA (max) |
| $I_{SD}$ | Shutdown Current | Output Mode 0 | 0.02 | 1 | µA (max) |
| $V_{OS}$ | Output Offset Voltage | $V_{IN}$ = 0V, Mode 7<br>Mono | 12 | 50 | mV (max) |
| | | $V_{IN}$ = 0V, Mode 7<br>Headphones (Note 11) | 3 | 15 | |
| $P_O$ | Output Power | MONO $_{OUT}$; $R_L$ = 8Ω<br>THD+N = 1%; f = 1kHz, BTL, Mode 1 | 540 | 500 | mW (min) |
| | | $R_{OUT}$ and $L_{OUT}$; $R_L$ = 32Ω<br>THD+N = 1%; f = 1kHz, SE, Mode 4 | 35 | 30 | mW (min) |
| THD+N | Total Harmonic Distortion + Noise | $MONO_{OUT}$<br>f = 1kHz<br>$P_{OUT}$ = 250mW; $R_L$ = 8Ω, BTL, Mode 1 | 0.05 | | % |
| | | $R_{OUT}$ and $L_{OUT}$<br>f = 1kHz<br>$P_{OUT}$ = 12mW; $R_L$ = 32Ω, SE, Mode 4 | 0.015 | | % |
| $N_{OUT}$ | Output Noise | A-weighted,<br>inputs terminated to GND, output referred | | | |
| | | Speaker; Mode 1 | 17 | | µV |
| | | Speaker; Mode 3, 7 | 27 | | µV |
| | | Speaker; Mode 5 | 33 | | µV |
| | | Headphone; SE, Mode 2 | 8 | | µV |
| | | Headphone; SE, Mode 4, 7 | 8 | | µV |
| | | Headphone; SE, Mode 6 | 12 | | µV |
| | | Headphone; OCL, Mode 2 | 8 | | µV |
| | | Headphone; OCL, Mode 4, 7 | 9 | | µV |
| | | Headphone; OCL, Mode 6 | 12 | | µV |

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Datasheet min/max specifications are specified by design, test, or statistical analysis.
(4) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(5) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

## Electrical Characteristics 3.3V[1][2] (continued)

The following specifications apply for $V_{DD}$ = 3.3V, $T_A$ = 25°C, all volume controls set to 0dB, unless otherwise specified.

| Symbol | Parameter | Conditions | LM4946 | | Units (Limits)[3] |
|---|---|---|---|---|---|
| | | | Typical[4] | Limits[5] | |
| PSRR | Power Supply Rejection Ratio $MONO_{OUT}$ | $V_{RIPPLE}$ = 200m$V_{PP}$; f = 217Hz, $R_L$ = 8Ω<br>$C_B$ = 2.2µF, BTL<br>All audio inputs terminated to GND;<br>output referred | | | |
| | | BTL, Output Mode 1 | 76 | | dB |
| | | BTL, Output Mode 3, 7 | 65 | | dB |
| | | BTL, Output Mode 5 | 63 | | dB |
| | Power Supply Rejection Ratio $R_{OUT}$ and $L_{OUT}$ | $V_{RIPPLE}$ = 200m$V_{PP}$; f = 217Hz, $R_L$ = 32Ω<br>$C_B$ = 2.2µF,<br>All audio inputs terminated to GND<br>output referred | | | |
| | | SE, Output Mode 2 | 78 | | dB |
| | | SE, Output Mode 4,7 | 82 | | dB |
| | | SE, Output Mode 6 | 78 | | dB |
| | | OCL, Output Mode 2 | 84 | | dB |
| | | OCL, Output Mode 4, 7 | 78 | | dB |
| | | OCL, Output Mode 6 | 77 | | dB |
| | Volume Control Step Size Error | | ±0.2 | | dB |
| | Digital Volume Control Range | Maximum attenuation | -54 | –56<br>–52 | dB (max)<br>dB (min) |
| | | Maximum gain | 18 | 17.4<br>18.6 | dB (min)<br>dB (max) |
| | HP(SE) Mute Attenuation | Output Mode 1, 3, 5 | 96 | | dB |
| | MONO_IN Input Impedance<br>$R_{IN}$ and $L_{IN}$ Input Impedance | Maximum gain setting | 12.5 | 10<br>15 | kΩ (min)<br>kΩ (max) |
| | | Maximum attenuation setting | 110 | 90<br>130 | kΩ (min)<br>kΩ (max) |
| CMRR | Common-Mode Rejection Ratio | f = 217Hz, $V_{CM}$ = 1Vpp,<br>Mode 1, BTL, $R_L$ = 8Ω | 61 | | dB |
| | | f = 217Hz, $V_{CM}$ = 1Vpp,<br>Mode 2, $R_L$ = 32Ω | 66 | | |
| XTALK | Crosstalk | Headphone; $P_O$ = 12mW<br>f = 1kHz, OCL, Mode 4 | –54 | | dB |
| | | Headphone; $P_O$ = 12mW<br>f = 1kHz, SE, Mode 4 | –72 | | dB |
| $T_{WU}$ | Wake-Up Time from Shutdown | $C_B$ = 2.2µF, OCL | 100 | | ms |
| | | $C_B$ = 2.2µF, SE | 135 | | ms |

## Electrical Characteristics 5.0V[1][2]

The following specifications apply for $V_{DD}$ = 5.0V, $T_A$ = 25°C, all volume controls set to 0dB, unless otherwise specified.

| Symbol | Parameter | Conditions | LM4946 | | Units (Limits)[3] |
|---|---|---|---|---|---|
| | | | Typical[4] | Limits[5] | |
| $I_{DD}$ | Supply Current | Output Modes 2, 4, 6<br>$V_{IN}$ = 0V; No load<br>SE Headphone | 3.8 | | mA |
| | | Output Modes 1, 3, 5, 7<br>$V_{IN}$ = 0V; No Load,<br>SE Headphone | 6.6 | | mA |
| | | Output Modes 2, 4, 6<br>$V_{IN}$ = 0V; No load,<br>OCL Headphone | 4.6 | | mA |
| | | Output Modes 1, 3, 5<br>$V_{IN}$ = 0V; No Load,<br>OCL Headphone | 6 | | mA |
| | | Output Modes 7<br>$V_{IN}$ = 0V; No Load,<br>OCL Headphone | 7.4 | | mA |
| $I_{SD}$ | Shutdown Current | Output Mode 0 | 0.05 | | µA |
| $V_{OS}$ | Output Offset Voltage | $V_{IN}$ = 0V, Mode 7<br>Mono | 12 | | mV |
| | | $V_{IN}$ = 0V, Mode 7<br>Headphones | 3 | | |
| $P_O$ | Output Power | $MONO_{OUT}$; $R_L$ = 8Ω<br>THD+N = 1%; f = 1kHz, BTL, Mode 1 | 1.3 | | W |
| | | $R_{OUT}$ and $L_{OUT}$; $R_L$ = 32Ω<br>THD+N = 1%; f = 1kHz, SE, Mode 4 | 85 | | mW |
| THD+N | Total Harmonic Distortion + Noise | $MONO_{OUT}$, f = 1kHz<br>$P_{OUT}$ = 500mW; $R_L$ = 8Ω, BTL, Mode 1 | 0.05 | | % |
| | | $R_{OUT}$ and $L_{OUT}$, f = 1kHz<br>$P_{OUT}$ = 30mW; $R_L$ = 32Ω, SE, Mode 4 | 0.012 | | % |
| $N_{OUT}$ | Output Noise | A-weighted,<br>inputs terminated to GND, output referred | | | |
| | | Speaker; Mode 1 | 17 | | µV |
| | | Speaker; Mode 3, 7 | 27 | | µV |
| | | Speaker; Mode 5 | 33 | | µV |
| | | Headphone; SE, Mode 2 | 8 | | µV |
| | | Headphone; SE, Mode 4, 7 | 8 | | µV |
| | | Headphone; SE, Mode 6 | 12 | | µV |
| | | Headphone; OCL, Mode 2 | 8 | | µV |
| | | Headphone; OCL, Mode 4, 7 | 9 | | µV |
| | | Headphone; OCL, Mode 6 | 12 | | µV |
| PSRR | Power Supply rejection Ratio $MONO_{OUT}$ | $V_{RIPPLE}$ = 200m$V_{PP}$; f = 217Hz, $R_L$ = 8Ω<br>$C_B$ = 2.2µF, BTL<br>All audio inputs terminated to GND;<br>output referred | | | |
| | | BTL, Output Mode 1 | 69 | | dB |
| | | BTL, Output Mode 3, 7 | 60 | | dB |
| | | BTL, Output Mode 5 | 58 | | dB |

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Datasheet min/max specifications are specified by design, test, or statistical analysis.
(4) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(5) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

## Electrical Characteristics 5.0V[1][2] (continued)

The following specifications apply for $V_{DD}$ = 5.0V, $T_A$ = 25°C, all volume controls set to 0dB, unless otherwise specified.

| Symbol | Parameter | Conditions | LM4946 | | Units (Limits)[3] |
|---|---|---|---|---|---|
| | | | Typical[4] | Limits[5] | |
| PSRR | Power Supply Rejection Ratio $R_{OUT}$ and $L_{OUT}$ | $V_{RIPPLE}$ = 200m$V_{PP}$; f = 217Hz, $R_L$ = 32Ω $C_B$ = 2.2µF, BTL All audio inputs terminated to GND; output referred | | | |
| | | SE, Output Mode 2 | 75 | | dB |
| | | SE, Output Mode 4,7 | 75 | | dB |
| | | SE, Output Mode 6 | 72 | | dB |
| | | OCL, Output Mode 2 | 75 | | dB |
| | | OCL, Output Mode 4, 7 | 79 | | dB |
| | | OCL, Output Mode 6 | 72 | | dB |
| | Digital Volume Control Range | Maximum attenuation | -54 | -56<br>-52 | dB (max)<br>dB (min) |
| | | Maximum gain | 18 | 17.4<br>18.6 | dB (min)<br>dB (max) |
| | HP(SE) Mute Attenuation | Output Mode 1, 3, 5 | 96 | | dB |
| | MONO_IN Input Impedance $R_{IN}$ and $L_{IN}$ Input Impedance | Maximum gain setting | 12.5 | 10<br>15 | kΩ (min)<br>kΩ (max) |
| | | Maximum attenuation setting | 110 | 90<br>130 | kΩ (min)<br>kΩ (max) |
| CMRR | Common-Mode Rejection Ratio | f = 217Hz, $V_{CM}$ = 1Vpp, 0dB gain Mode 1, BTL, $R_L$ = 8Ω | 61 | | dB |
| | | f = 217Hz, $V_{CM}$ = 1Vpp, 0dB gain Mode 2, $R_L$ = 32Ω | 66 | | |
| XTALK | Crosstalk | Headphone; $P_O$ = 30mW, OCL, Mode 4 | –55 | | dB |
| | | Headphone; $P_O$ = 30mW, SE, Mode 4 | –72 | | dB |
| TWU | Wake-Up Time from Shutdown | $C_B$ = 2.2µF, OCL | 135 | | ms |
| | | $C_B$ = 2.2µF, SE | 180 | | ms |

## I²C/SPI WQFN/DSBGA[1][2]

The following specifications apply for $V_{DD}$ = 5.0V and 3.3V, $T_A$ = 25°C, 2.2V ≤ $I^2C$SPI_$V_{DD}$ ≤ 5.5V, unless otherwise specified.

| Symbol | Parameter | Conditions | LM4946[3] | | Units (Limits)[4] |
|---|---|---|---|---|---|
| | | | Typical[5] | Limits[6] [2] | |
| $t_1$ | $I^2C$ Clock Period | | | 2.5 | µs (min) |
| $t_2$ | $I^2C$ Data Setup Time | | | 100 | ns (min) |
| $t_3$ | $I^2C$ Data Stable Time | | | 0 | ns (min) |
| $t_4$ | Start Condition Time | | | 100 | ns (min) |
| $t_5$ | Stop Condition Time | | | 100 | ns (min) |
| $t_6$ | $I^2C$ Data Hold Time | | | 100 | ns (min) |
| $f_{SPI}$ | Maximum SPI Frequency | | | 1000 | kHz (max) |
| $t_{EL}$ | SPI ENB High Time | | | 100 | ns (min) |
| $t_{DS}$ | SPI Data Setup Time | | | 100 | ns (min) |
| $t_{ES}$ | SPI ENB Setup Time | | | 100 | ns (min) |

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) For LM4946 WQFN package, revised specification goes into effect starting with date code 79. Existing specification is per datasheet rev 1.0
(4) Datasheet min/max specifications are specified by design, test, or statistical analysis.
(5) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(6) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

## I²C/SPI WQFN/DSBGA(1)(2) (continued)

The following specifications apply for $V_{DD}$ = 5.0V and 3.3V, $T_A$ = 25°C, 2.2V ≤ $I^2CSPI\_V_{DD}$ ≤ 5.5V, unless otherwise specified.

| Symbol | Parameter | Conditions | LM4946(3) | | Units (Limits)(4) |
|---|---|---|---|---|---|
| | | | Typical(5) | Limits(6) (2) | |
| $t_{DH}$ | SPI Data Hold Time | | | 100 | ns (min) |
| $t_{EH}$ | SPI Enable Hold Time | | | 100 | ns (min) |
| $t_{CL}$ | SPI Clock Low Time | | | 500 | ns (min) |
| $t_{CH}$ | SPI Clock High Time | | | 500 | ns (min) |
| $V_{IH}$ | I²C/SPI Input Voltage High | | | 0.7x$I^2CSPI$ $V_{DD}$ | V (min) |
| $V_{IL}$ | I²C/SPI Input Voltage Low | | | 0.3x$I^2CSPI$ $V_{DD}$ | V (max) |

## I²C/SPI DSBGA only(1)(2)

The following specifications apply for $V_{DD}$ = 5.0V and 3.3V, $T_A$ = 25°C, 1.7V ≤ $I^2CSPI\_V_{DD}$ ≤ 2.2V, unless otherwise specified.

| Symbol | Parameter | Conditions | LM4946 | | Units (Limits)(3) |
|---|---|---|---|---|---|
| | | | Typical(4) | Limits(5) (2) | |
| $t_1$ | I²C Clock Period | | | 2.5 | µs (min) |
| $t_2$ | I²C Data Setup Time | | | 250 | ns (min) |
| $t_3$ | I²C Data Stable Time | | | 0 | ns (min) |
| $t_4$ | Start Condition Time | | | 250 | ns (min) |
| $t_5$ | Stop Condition Time | | | 250 | ns (min) |
| $t_6$ | I²C Data Hold Time | | | 250 | ns (min) |
| $f_{SPI}$ | Maximum SPI Frequency | | | 250 | kHz (max) |
| $t_{EL}$ | SPI ENB High Time | | | 250 | ns (min) |
| $t_{DS}$ | SPI Data Setup Time | | | 250 | ns (min) |
| $t_{ES}$ | SPI ENB Setup Time | | | 250 | ns (min) |
| $t_{DH}$ | SPI Data Hold Time | | | 250 | ns (min) |
| $t_{EH}$ | SPI Enable Hold Time | | | 250 | ns (min) |
| $t_{CL}$ | SPI Clock Low Time | | | 500 | ns (min) |
| $t_{CH}$ | SPI Clock High Time | | | 500 | ns (min) |
| $V_{IH}$ | I²C/SPI Input Voltage High | | | 0.7x$I^2CSPI$ $V_{DD}$ | V (min) |
| $V_{IL}$ | I²C/SPI Input Voltage Low | | | 0.25 x$I^2CSPI$ $V_{DD}$ | V (max) |

(1) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to the ground pin, unless otherwise specified.
(3) Datasheet min/max specifications are specified by design, test, or statistical analysis.
(4) Typical specifications are specified at +25°C and represent the most likely parametric norm.
(5) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

## Typical Performance Characteristics

**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, $P_O$ = 250mW**
**Mode 1, BTL, BW = 80kHz**

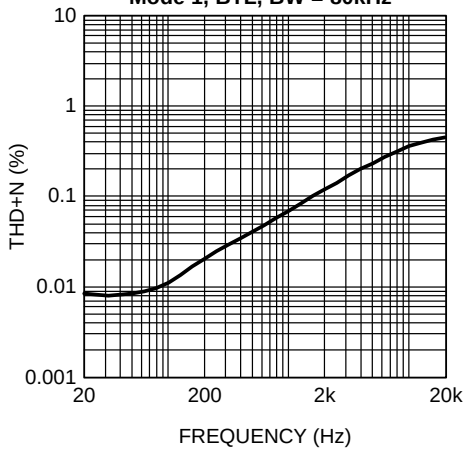



**Figure 5.**

**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, $P_O$ = 12mW**
**Mode 4, 7, OCL, BW = 80kHz**

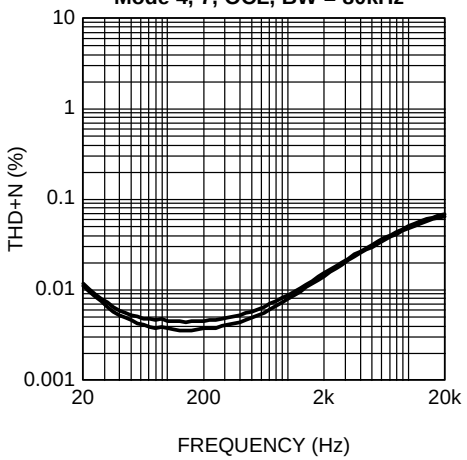



**Figure 6.**

**THD+N vs**
**Frequency $V_{DD}$ = 3.3V, $R_L$ = 32Ω, $P_O$ = 12mW**
**Mode 6, OCL, BW = 80kHz**

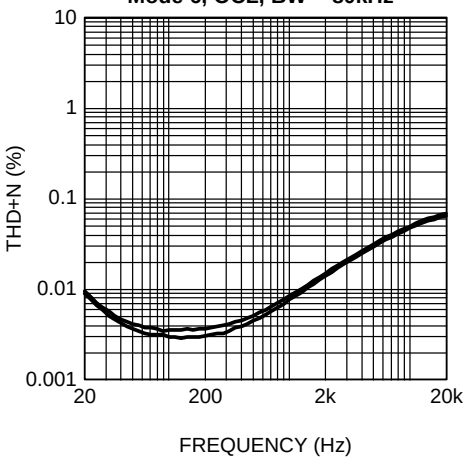



**Figure 7.**

**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, $P_O$ = 12mW**
**Mode 4, 7, SE, BW = 80kHz**

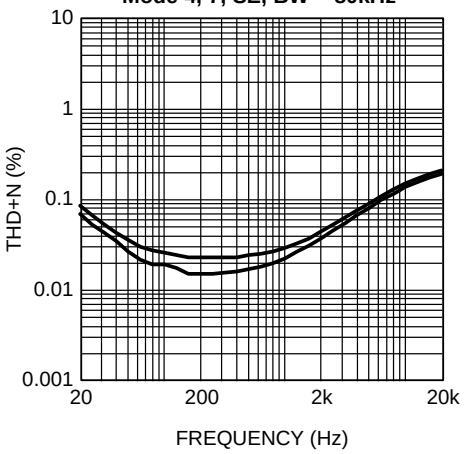



**Figure 8.**

**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, $P_O$ = 12mW**
**Mode 6, SE, BW = 80kHz**

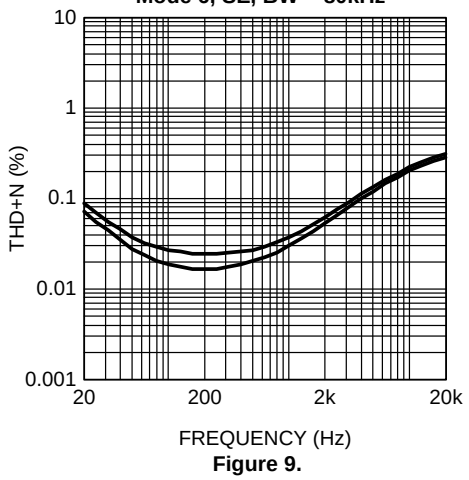



**Figure 9.**

**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, $P_O$ = 250mW**
**Mode 5, BTL, BW = 80kHz**

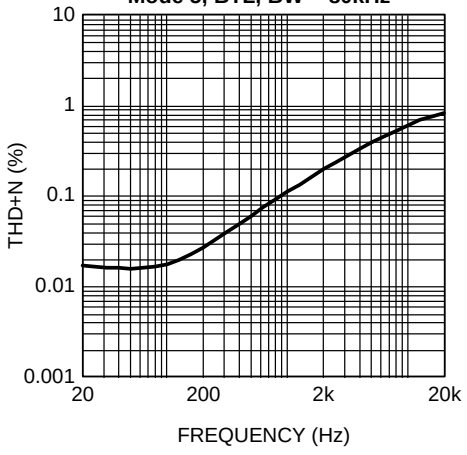



**Figure 10.**

## Typical Performance Characteristics (continued)

**THD+N vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 8Ω, $P_O$ = 500mW**
**Mode 1, BTL, BW = 80kHz**

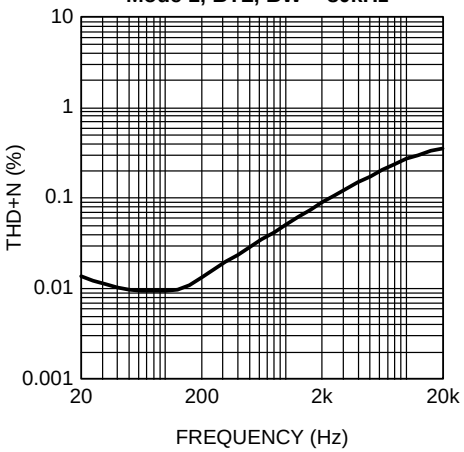



**Figure 11.**

**THD+N vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, $P_O$ = 30mW**
**Mode 4, 7, OCL, BW = 80kHz**

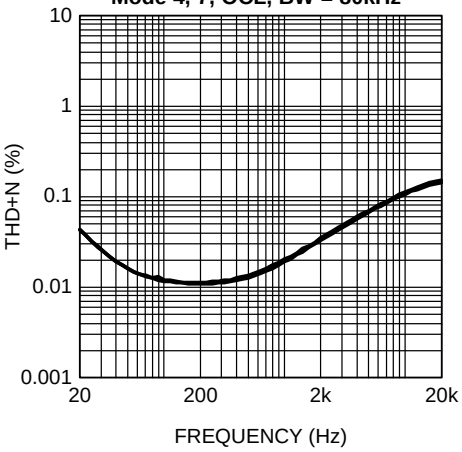



**Figure 12.**

**THD+N vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, $P_O$ = 30mW**
**Mode 4, 7, SE, BW = 80kHz**

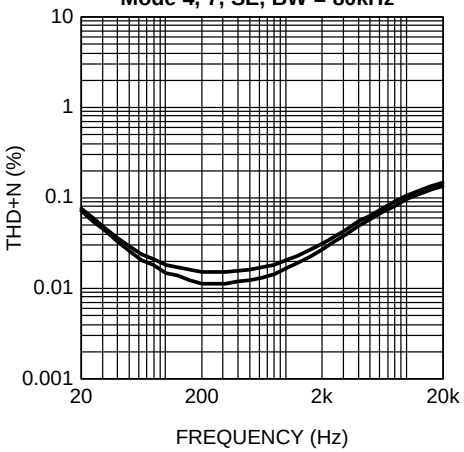



**Figure 13.**

**THD+N vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, $P_O$ = 30mW**
**Mode 6, OCL, BW = 80kHz**

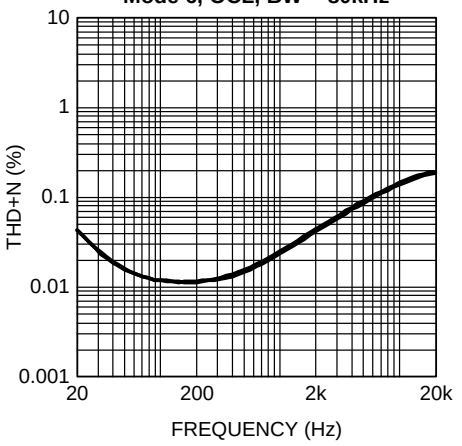



**Figure 14.**

**THD+N vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, $P_O$ = 30mW**
**Mode 6, SE, BW = 80kHz**

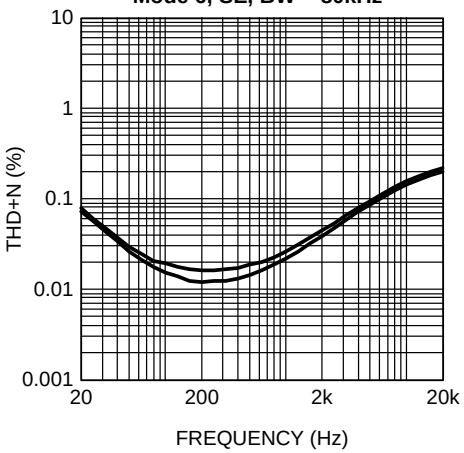



**Figure 15.**

**THD+N vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 8Ω, $P_O$ = 500mW**
**Mode 5, BTL**

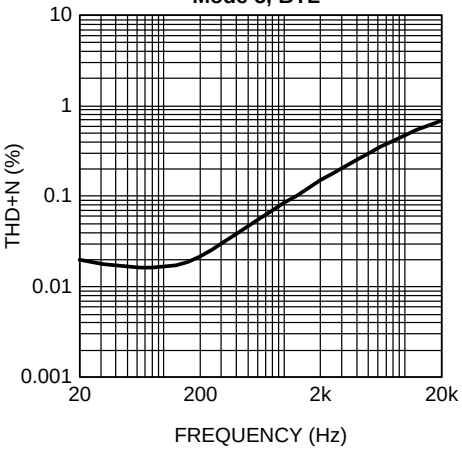



**Figure 16.**

## Typical Performance Characteristics (continued)

**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, $P_O$ = 12mW**
**Mode 2, OCL**

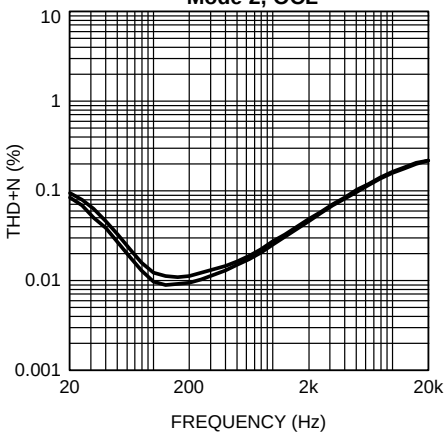



**Figure 17.**

**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, $P_O$ = 12mW**
**Mode 2, SE, BW = 80kHz**

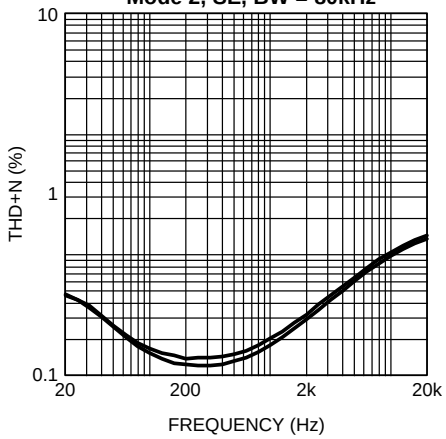



**Figure 18.**

**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, $P_O$ = 250mW**
**Mode 3, BTL**

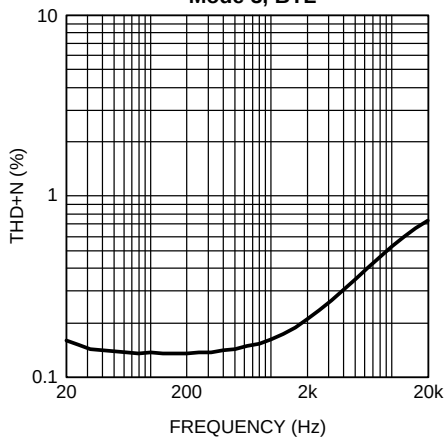



**Figure 19.**

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, f = 1kHz**
**Mode 1, BTL**

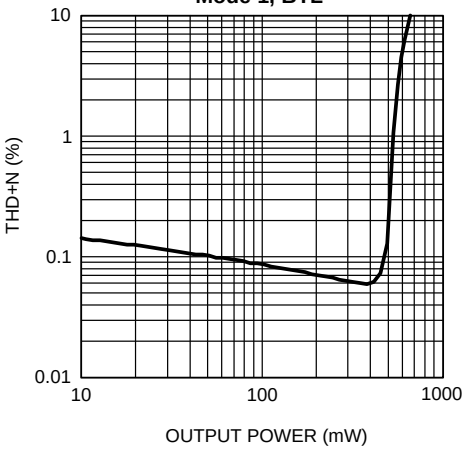



**Figure 20.**

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, f = 1kHz**
**Mode 5, BTL**

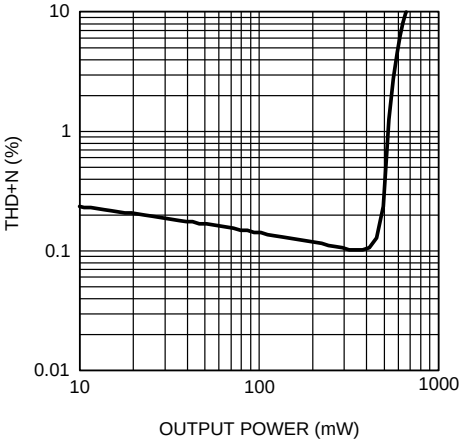



**Figure 21.**

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, f = 1kHz**
**Mode 4, 7, OCL**

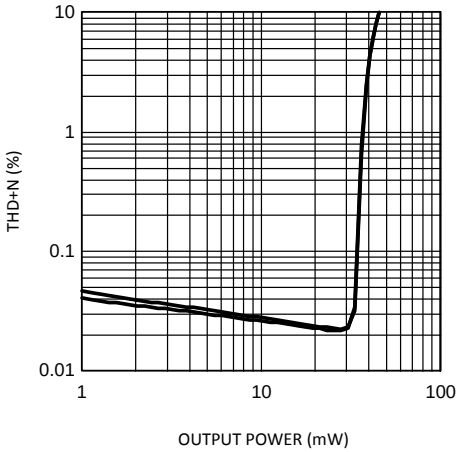



**Figure 22.**

## Typical Performance Characteristics (continued)

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, f = 1kHz**
**Mode 4, 7, SE**

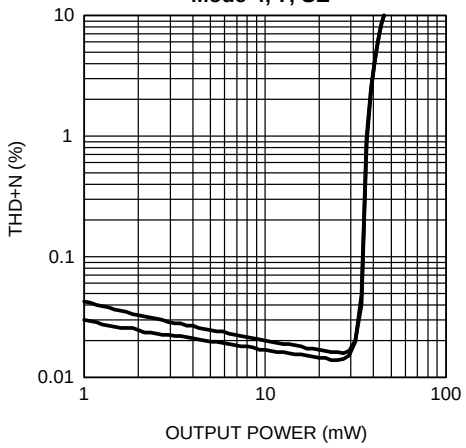



**Figure 23.**

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, f = 1kHz**
**Mode 6, SE**

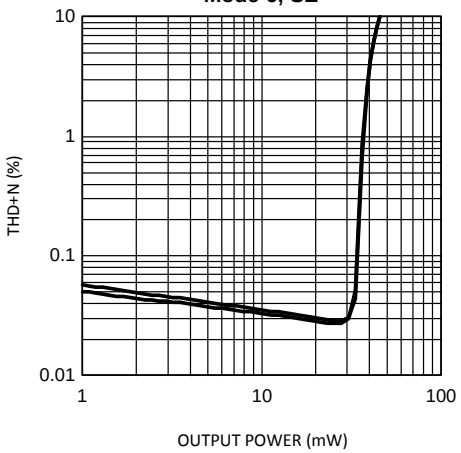



**Figure 24.**

**THD+N vs Output Power**
**$V_{DD}$ = 5V, $R_L$ = 8Ω, f = 1kHz**
**Mode 1, BTL**

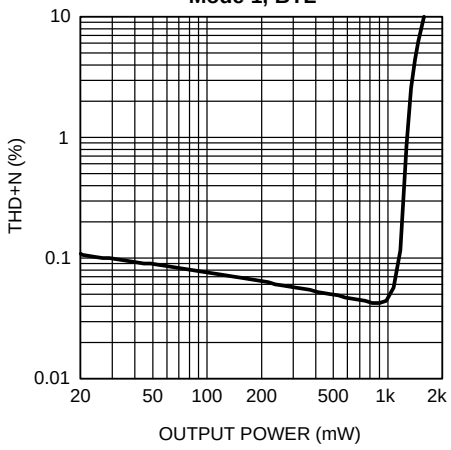



**Figure 25.**

**THD+N vs Output Power**
**$V_{DD}$ = 5V, $R_L$ = 8Ω, f = 1kHz**
**Mode 5, BTL**

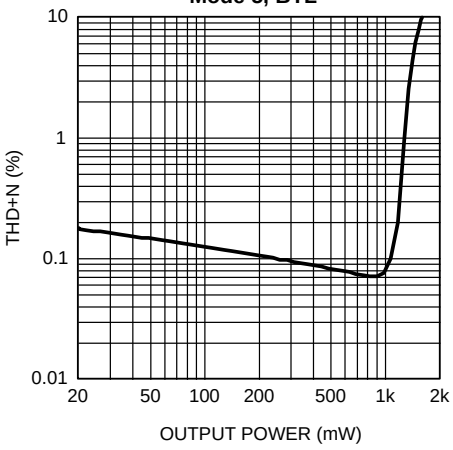



**Figure 26.**

**THD+N vs Output Power**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, f = 1kHz**
**Mode 4, 7, OCL**

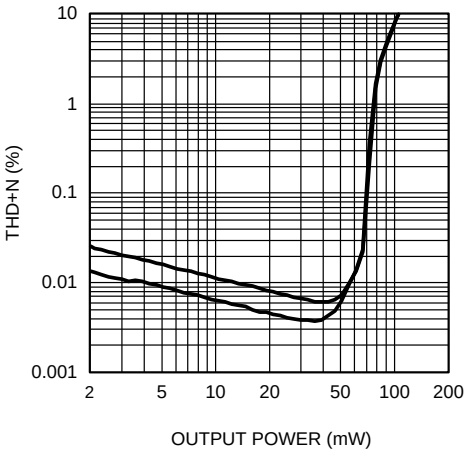



**Figure 27.**

**THD+N vs Output Power**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, f = 1kHz**
**Mode 4, 7, SE**

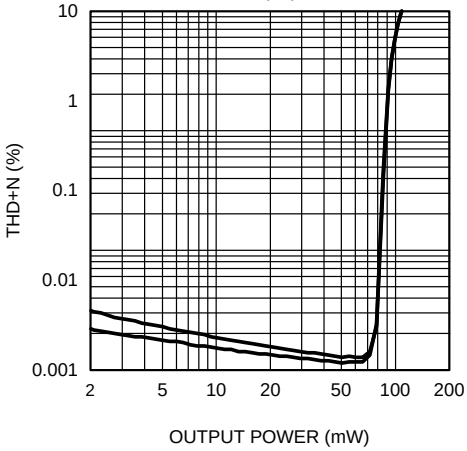



**Figure 28.**

## Typical Performance Characteristics (continued)

**THD+N vs Output Power**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, f = 1kHz**
**Mode 6, SE**

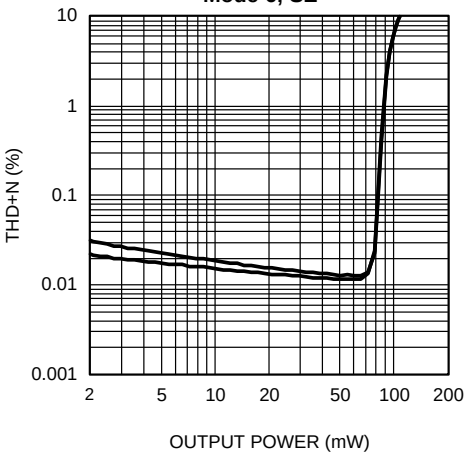



**Figure 29.**

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, f = 1kHz**
**Mode 6, Mono Input, OCL**

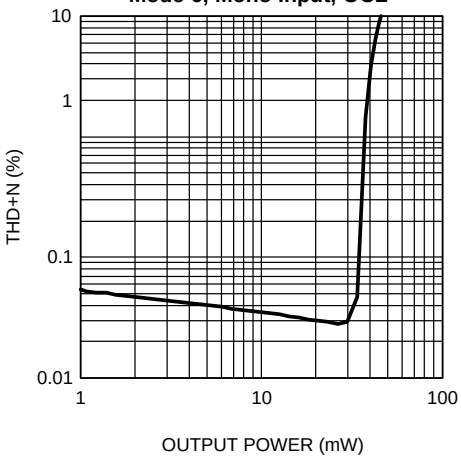



**Figure 30.**

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, f = 1kHz**
**Mode 6, Stereo Input, OCL**

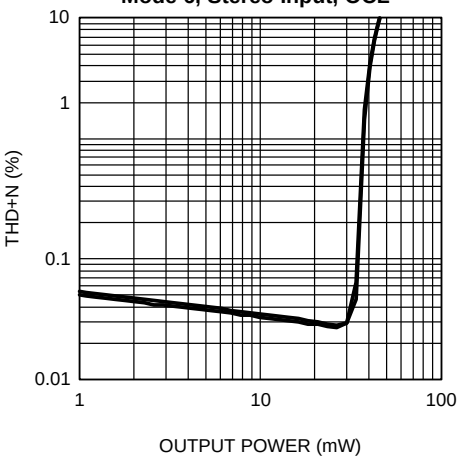



**Figure 31.**

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, f = 1kHz**
**Mode 2, OCL**

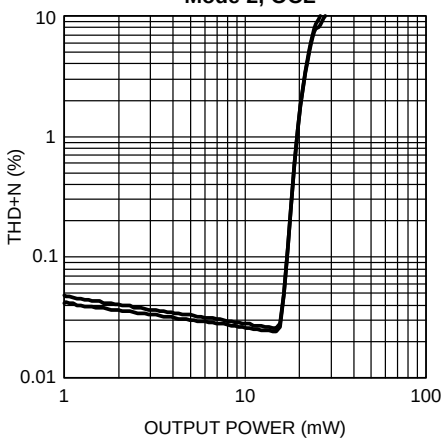



**Figure 32.**

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, f = 1kHz**
**Mode 2, SE**

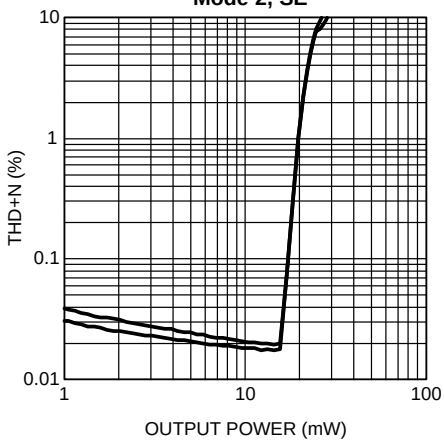



**Figure 33.**

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, f = 1kHz**
**Mode 3, BTL**

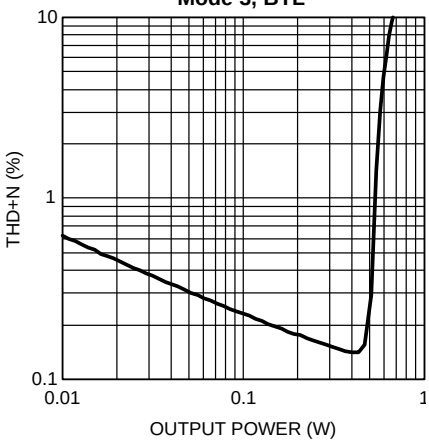



**Figure 34.**

## Typical Performance Characteristics (continued)

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, 0dB**
**Mode 4, 7, OCL**

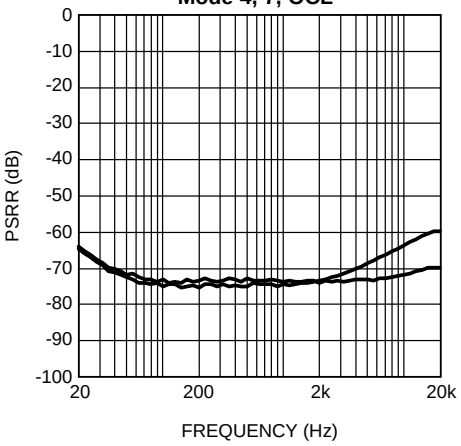



**Figure 35.**

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, 0dB**
**Mode 4, 7, SE**

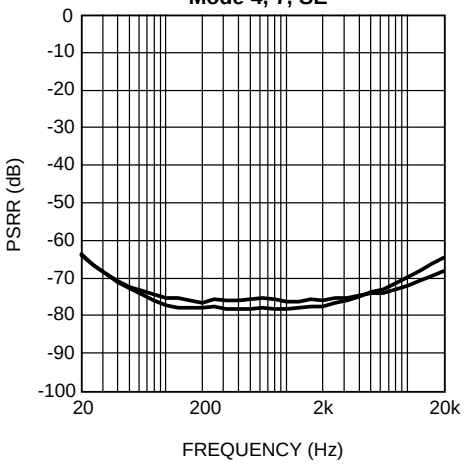



**Figure 36.**

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, 0dB**
**Mode 6, OCL**

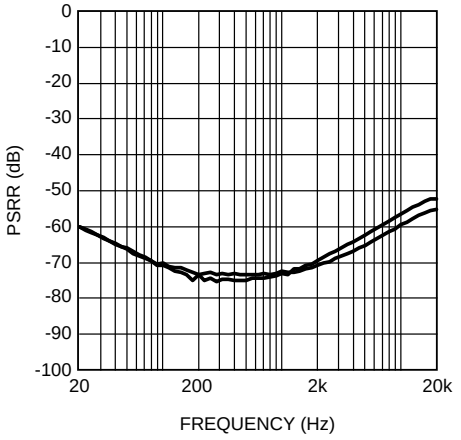



**Figure 37.**

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, 0dB**
**Mode 6, SE**

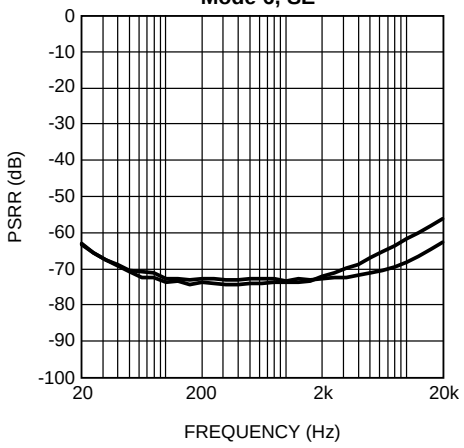



**Figure 38.**

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, 6dB**
**Mode 1, BTL**

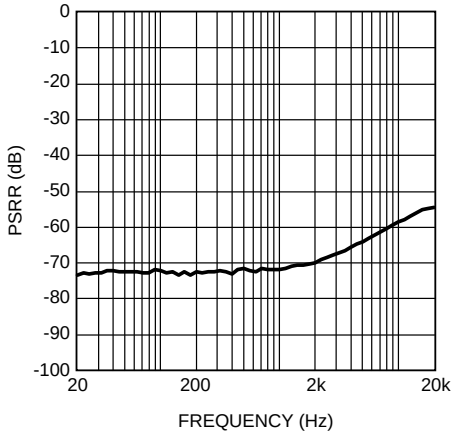



**Figure 39.**

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω**
**Mode 3, 7, BTL**

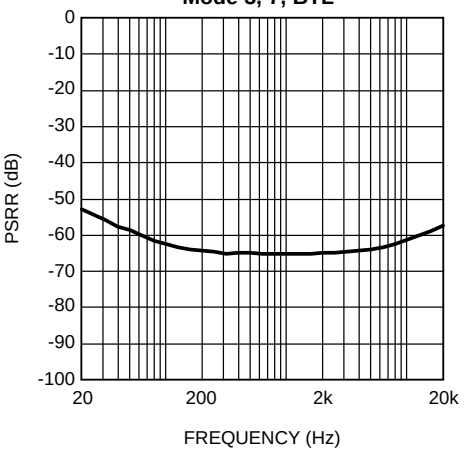



**Figure 40.**

## Typical Performance Characteristics (continued)

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω**
**Mode 2, OCL**

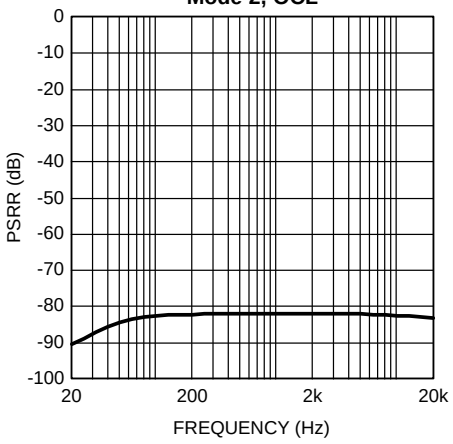



**Figure 41.**

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω**
**Mode 2, SE**

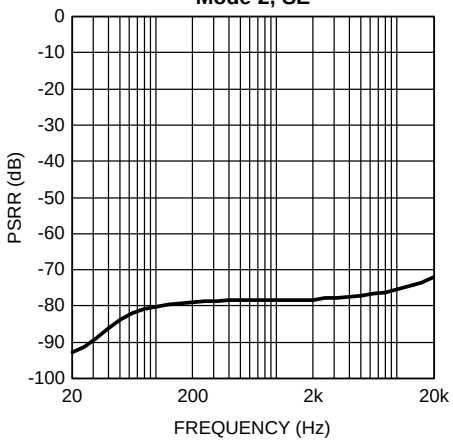



**Figure 42.**

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, 6dB**
**Mode 5, BTL**

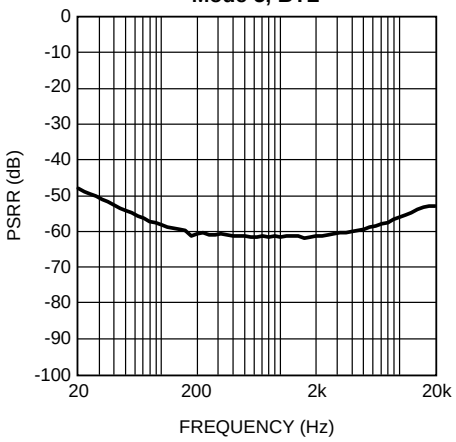



**Figure 43.**

**PSRR vs Supply Voltage**
**$R_L$ = 8Ω, 217Hz**
**Mode 1, BTL**

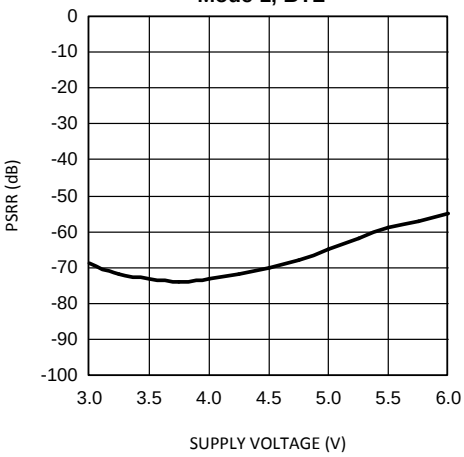



**Figure 44.**

**PSRR vs Supply Voltage**
**$R_L$ = 32Ω, 217Hz**
**Mode 4, OCL**

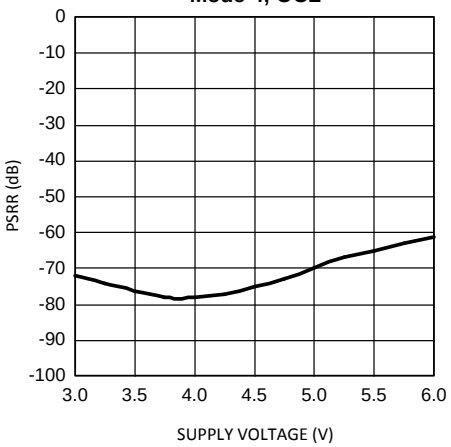



**Figure 45.**

**PSRR vs Supply Voltage**
**$R_L$ = 32Ω, 217Hz**
**Mode 4, SE**

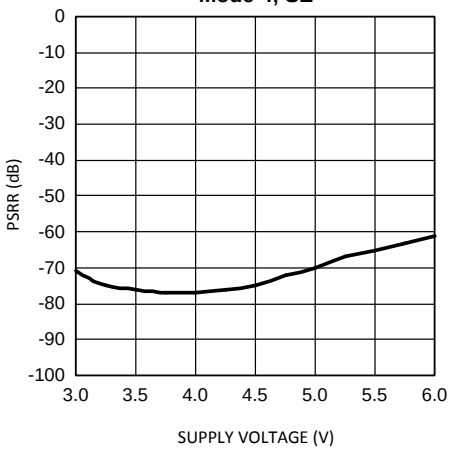



**Figure 46.**

## Typical Performance Characteristics (continued)

**Power Dissipation vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω**
**f = 1kHz, Mode 2, 4, 6, SE**

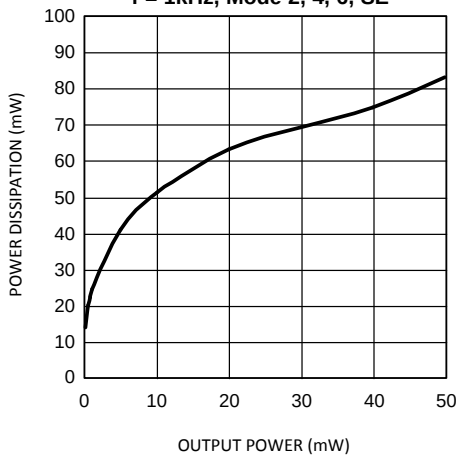



**Figure 47.**

**Power Dissipation vs Output Power**
**$V_{DD}$ = 5V, $R_L$ = 8Ω**
**f = 1kHz, Mode 1, 3, 5, BTL**

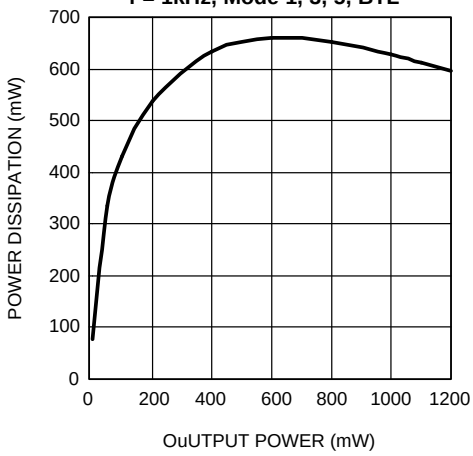



**Figure 48.**

**Power Dissipation vs Output Power**
**$V_{DD}$ = 5V, $R_L$ = 32Ω**
**f = 1kHz, Mode 2, 4, 6, OCL**

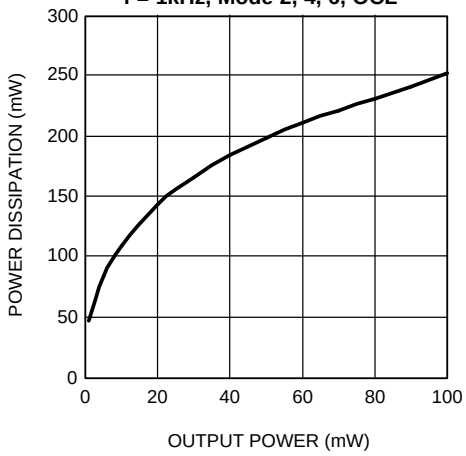



**Figure 49.**

**Power Dissipation vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, f = 1kHz,**
**Modes 1, 3, 5, BTL**

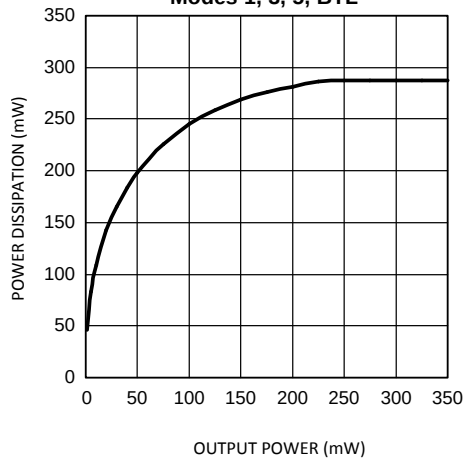



**Figure 50.**

**Power Dissipation vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, f = 1kHz,**
**Modes 2, 4, 6, OCL**

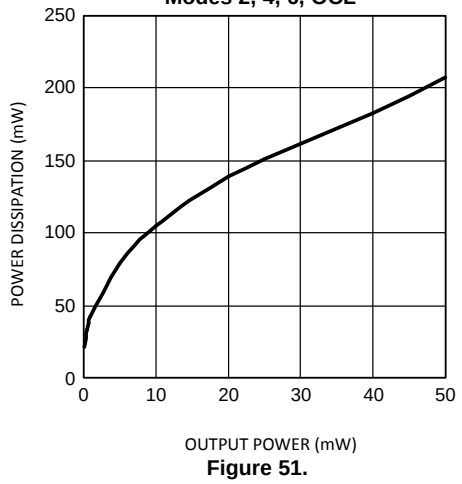



**Figure 51.**

**Power Dissipation vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, f = 1kHz,**
**Mode 7, OCL**

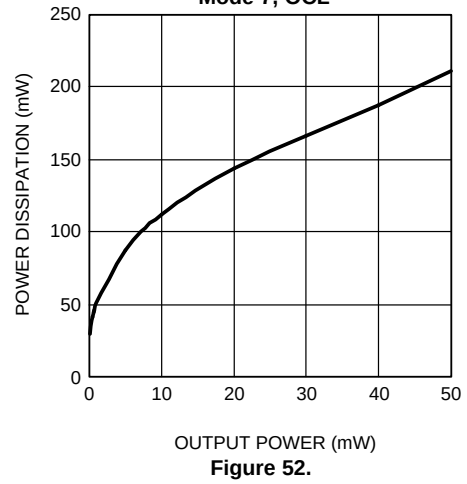



**Figure 52.**

## Typical Performance Characteristics (continued)

**Power Dissipation vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, f = 1kHz, Mode 7, SE**

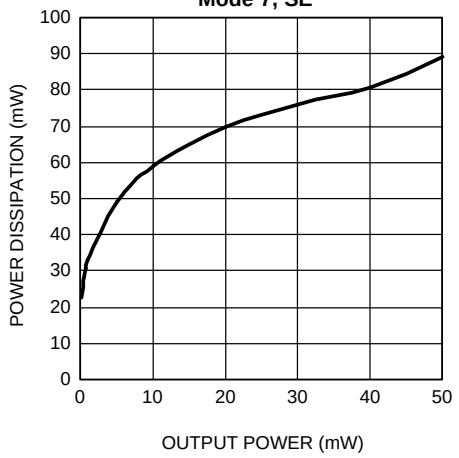



**Figure 53.**

**Crosstalk vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, $P_O$ = 12mW Right-Left, Mode 4, OCL**

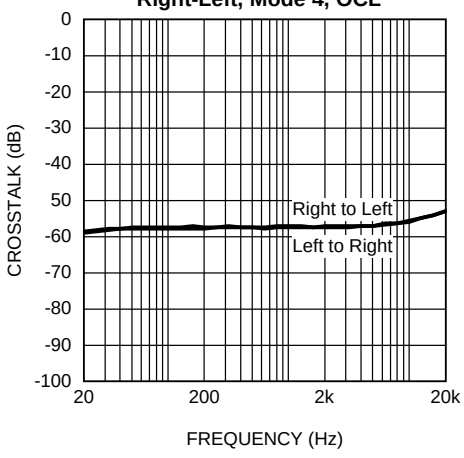



**Figure 54.**

**Crosstalk vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, $P_O$ = 30mW Left-Right, Mode 4, OCL**

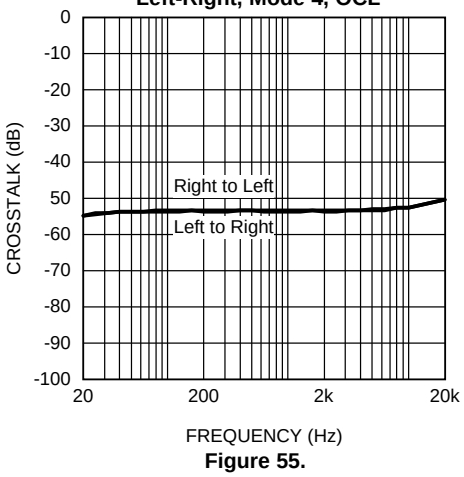



**Figure 55.**

**Crosstalk vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, $P_O$ = 12mW Mode 4, SE**

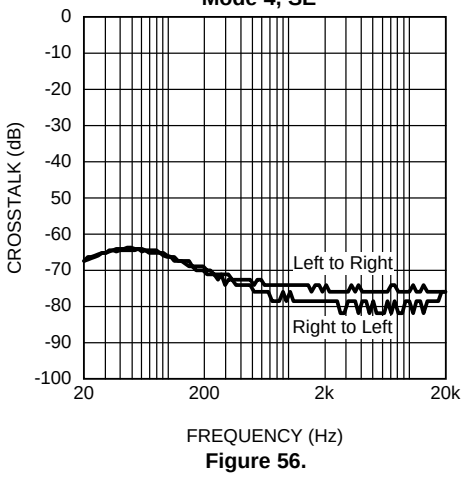



**Figure 56.**

**Crosstalk vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, $P_O$ = 30mW Mode 4, SE**

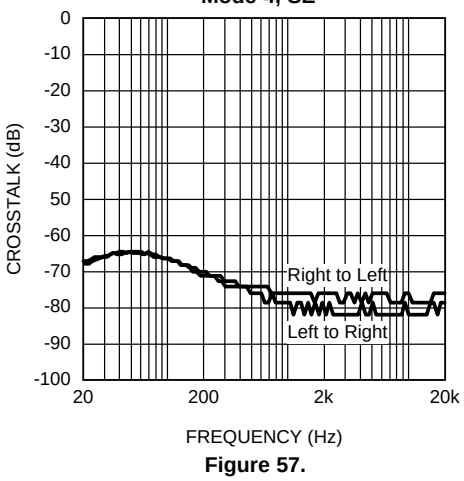



**Figure 57.**

**Supply Current vs Supply Voltage**
**No Load, Mode 7**

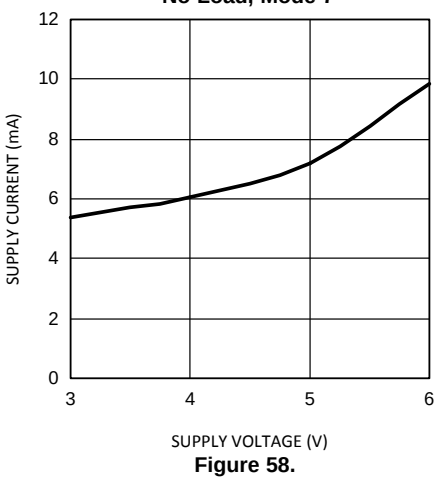



**Figure 58.**

## Typical Performance Characteristics (continued)

**Supply Current vs Supply Voltage**
**$V_{DD}$ = 3.3V, No Load, Modes 1, 3, 5**

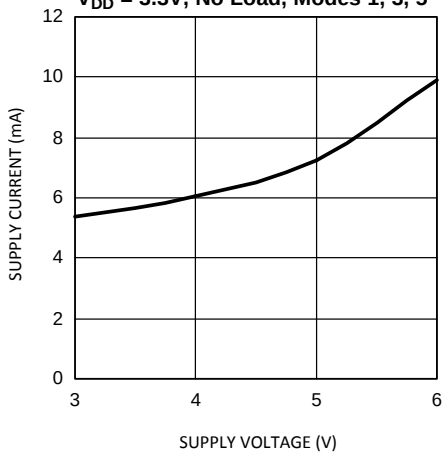



**Figure 59.**

**Supply Current vs Supply Voltage**
**No Load, Modes 2, 4, 6**

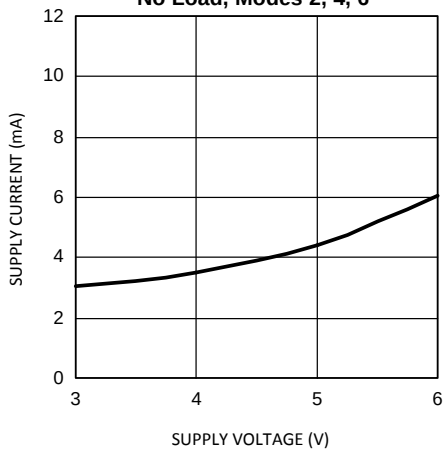



**Figure 60.**

**Output Power vs Supply Voltage**
**$R_L$ = 8Ω, f = 1kHz, Mono, Mode 1**

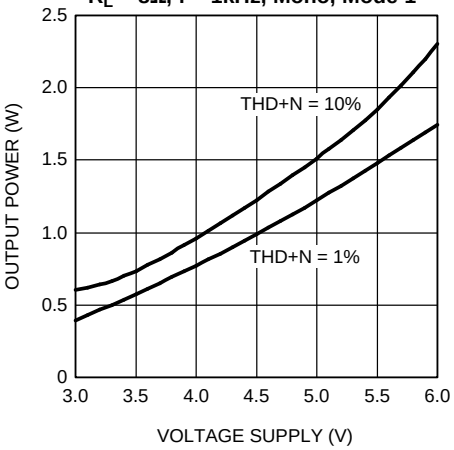



**Figure 61.**

**Output Power vs Supply Voltage**
**$R_L$ = 32Ω, f = 1kHz, OCL, Mode 4**

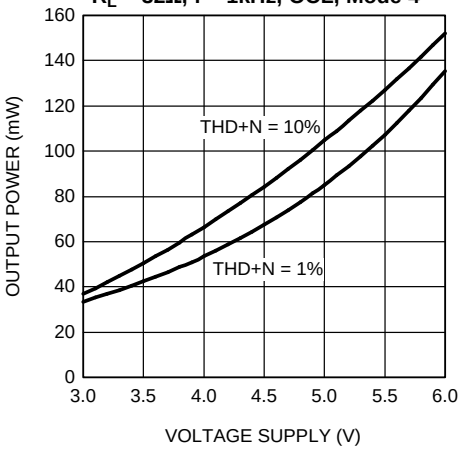



**Figure 62.**

# APPLICATION INFORMATION

## I²C PIN DESCRIPTION

SDA: This is the serial data input pin.

SCL: This is the clock input pin.

ID_ENB: This is the address select input pin.

I²CSPI_SEL: This is tied LOW for I²C mode.

## I²C COMPATIBLE INTERFACE

The LM4946 uses a serial bus which conforms to the I²C protocol to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I²C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4946.

The I²C address for the LM4946 is determined using the ID_ENB pin. The LM4946's two possible I²C chip addresses are of the form $111110X_10$ (binary), where $X_1$ = 0, if ID_ENB is logic LOW; and $X_1$ = 1, if ID_ENB is logic HIGH. If the I²C interface is used to address a number of chips in a system, the LM4946's chip address can be changed to avoid any possible address conflicts.

The bus format for the I²C interface is shown in Figure 63. The bus format diagram is broken up into six major sections:

1. The "start" signal is generated by lowering the data signal while the clock signal is HIGH. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own address.
2. The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is HIGH.

   For I²C interface operation, the I²CSPI_SEL pin needs to be tied LOW (and tied high for SPI operation).
3. After the last bit of the address bit is sent, the master releases the data line HIGH (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM4946 has received the address correctly, then it holds the data line LOW during the clock pulse. If the data line is not held LOW during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM4946.
4. The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable HIGH.
5. After the data byte is sent, the master must check for another acknowledge to see if the LM4946 received the data.

   If the master has more data bytes to send to the LM4946, then the master can repeat the previous two steps until all data bytes have been sent.
6. The "stop" signal ends the transfer. To signal "stop", the data signal goes HIGH while the clock signal is HIGH. The data line should be held HIGH when not in use.

## I²C INTERFACE POWER SUPPLY PIN (I²CSPI_$V_{DD}$)

The LM4946's I²C interface is powered up through the I²CSPI_$V_{DD}$ pin. The LM4946's I²C interface operates at a voltage level set by the I²C$V_{DD}$ pin which can be set independent to that of the main power supply pin $V_{DD}$. This is ideal whenever logic levels for the I²C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

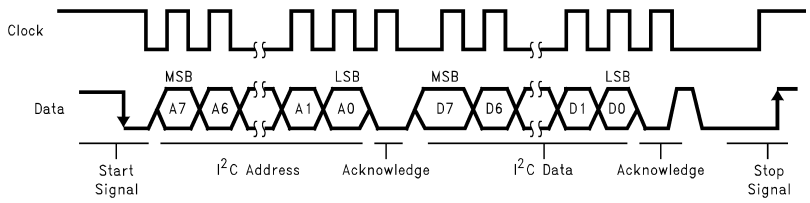



**Figure 63. I²C Bus Format**

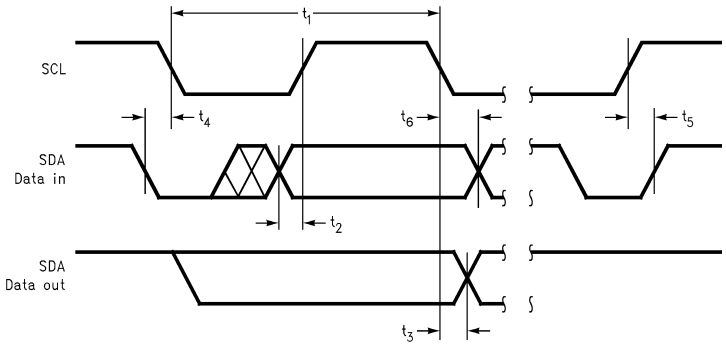



**Figure 64. I²C Timing Diagram**

## SPI DESCRIPTION

(For 2.2V ≤ I²CSPI_$V_{DD}$ ≤ 5.5V, see I2C/SPI WQFN/DSBGA for more information).

0. I²CSPI_SEL: This pin is tied HIGH for SPI mode.

1. The data bits are transmitted with the MSB first.

2. The maximum clock rate is 1MHz for the CLK pin.

3. CLK must remain HIGH for at least 500ns ($t_{CH}$ ) after the rising edge of CLK, and CLK must remain LOW for at least 500ns ($t_{CL}$) after the falling edge of CLK.

4. The serial data bits are sampled at the rising edge of CLK. Any transition on DATA must occur at least 100ns ($t_{DS}$) before the rising edge of CLK. Also, any transition on DATA must occur at least 100ns ($t_{DH}$) after the rising edge of CLK and stabilize before the next rising edge of CLK.

5.ID_ENB should be LOW only during serial data transmission.

6. ID_ENB must be LOW at least 100ns ($t_{ES}$ ) before the first rising edge of CLK, and ID_ENB has to remain LOW at least 100ns ($t_{EH}$) after the eighth rising edge of CLK.

7. If ID_ENB remains HIGH for more than 100ns before all 8 bits are transmitted then the data latch will be aborted.

8. If ID_ENB is LOW for more than 8 CLK pulses then only the first 8 data bits will be latched and activated when ID_ENB transitions to logic-high.

9. ID_ENB must remain HIGH for at least 100ns ($t_{EL}$ ) to latch in the data.

10. Coincidental rising or falling edges of CLK and ID_ENB are not allowed. If CLK is to be held HIGH after the data transmission, the falling edge of CLK must occur at least 100ns ($t_{CS}$) before ID_ENB transitions to LOW for the next set of data.

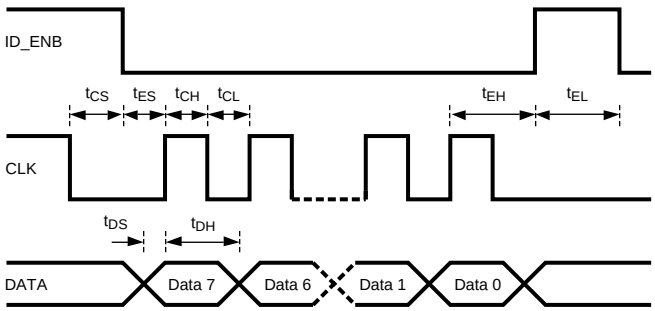



**Figure 65. SPI Timing Diagram**

**Table 1. Chip Address**

| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---|---|---|---|---|---|---|---|---|
| Chip Address | 1 | 1 | 1 | 1 | 1 | 0 | EC(1) | 0 |
| ID_ENB = 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| ID_ENB = 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

(1) EC — Externally Controlled

**Table 2. Control Registers(1)**

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Mode Control | 0 | 0 | 0 | 0 | OCL | MC2 | MC1 | MC0 |
| Programmable 3D | 0 | 1 | 0 | 0 | N3D3 | N3D2 | N3D1 | N3D0 |
| Mono Volume Control | 1 | 0 | 0 | MVC4 | MVC3 | MVC2 | MVC1 | MVC0 |
| Left Volume Control | 1 | 1 | 0 | LVC4 | LVC3 | LVC2 | LVC1 | LVC0 |
| Right Volume Control | 1 | 1 | 1 | RVC4 | RVC3 | RVC2 | RVC1 | RVC0 |

(1) Bits MVC0 — MVC4 control 32 step volume control for MONO input
Bits LVC0 — LVC4 control 32 step volume control for LEFT input
Bits RVC0 — RVC4 control 32 step volume control for RIGHT input
Bits MC0 — MC2 control 8 distinct modes
Bits N3D3, N3D2, N3D1, N3D0 control programmable 3D function
N3D0 turns the 3D function ON (N3D0 = 1) or OFF (N3D0 = 0), and N3D1 = 0 provides a “wider” aural effect or N3D1 = 1 a “narrower” aural effect
Bit OCL selects between SE with output capacitor (OCL = 0) or SE without output capacitors (OCL = 1). **Default is OCL = 0**

**Table 3. Programmable TI 3D Audio**

| | N3D3 | N3D2 |
|---|---|---|
| Low | 0 | 0 |
| Medium | 0 | 1 |
| High | 1 | 0 |
| Maximum | 1 | 1 |

**Table 4. Output Mode Selection(1)**

| Output Mode Number | MC2 | MC1 | MC0 | Handsfree Speaker Output | Right HP Output | Left HP Output |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | SD | SD | SD |
| 1 | 0 | 0 | 1 | $G_P$ X P | MUTE | MUTE |
| 2 | 0 | 1 | 0 | SD | $G_P$ X P/2 | $G_P$ X P/2 |
| 3 | 0 | 1 | 1 | 2 X ($G_L$ X L + $G_R$ X R) | MUTE | MUTE |
| 4 | 1 | 0 | 0 | SD | $G_R$ X R | $G_L$ X L |
| 5 | 1 | 0 | 1 | 2 X ($G_L$ X L + $G_R$ X R) + $G_P$ X P | MUTE | MUTE |
| 6 | 1 | 1 | 0 | SD | $G_R$ X R + $G_P$ X P/2 | $G_L$ X L + $G_P$ X P/2 |
| 7 | 1 | 1 | 1 | 2 X ($G_R$ X R + $G_L$ X L) | $G_R$ X R | $G_L$ X L |

(1) On initial POWER ON, the default mode is 000
P = Phone-in (Mono)
R = $R_{IN}$
L = $L_{IN}$
SD = Shutdown
MUTE = Mute Mode
$G_P$ = Phone In (Mono) volume control gain
$G_R$ = Right stereo volume control gain
$G_L$ = Left stereo volume control gain

**Table 5. Volume Control Table(1)**

| Volume Step | xVC4 | xVC3 | xVC2 | xVC1 | xVC0 | Gain,dB |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | –54.00 |
| 2 | 0 | 0 | 0 | 0 | 1 | –46.50 |
| 3 | 0 | 0 | 0 | 1 | 0 | –40.50 |
| 4 | 0 | 0 | 0 | 1 | 1 | –34.50 |
| 5 | 0 | 0 | 1 | 0 | 0 | –30.00 |
| 6 | 0 | 0 | 1 | 0 | 1 | –27.00 |
| 7 | 0 | 0 | 1 | 1 | 0 | –24.00 |
| 8 | 0 | 0 | 1 | 1 | 1 | –21.00 |
| 9 | 0 | 1 | 0 | 0 | 0 | –18.00 |
| 10 | 0 | 1 | 0 | 0 | 1 | –15.00 |
| 11 | 0 | 1 | 0 | 1 | 0 | –13.50 |
| 12 | 0 | 1 | 0 | 1 | 1 | –12.00 |
| 13 | 0 | 1 | 1 | 0 | 0 | –10.50 |
| 14 | 0 | 1 | 1 | 0 | 1 | –9.00 |
| 15 | 0 | 1 | 1 | 1 | 0 | –7.50 |
| 16 | 0 | 1 | 1 | 1 | 1 | –6.00 |
| 17 | 1 | 0 | 0 | 0 | 0 | –4.50 |
| 18 | 1 | 0 | 0 | 0 | 1 | –3.00 |
| 19 | 1 | 0 | 0 | 1 | 0 | –1.50 |
| 20 | 1 | 0 | 0 | 1 | 1 | 0.00 |
| 21 | 1 | 0 | 1 | 0 | 0 | 1.50 |
| 22 | 1 | 0 | 1 | 0 | 1 | 3.00 |
| 23 | 1 | 0 | 1 | 1 | 0 | 4.50 |
| 24 | 1 | 0 | 1 | 1 | 1 | 6.00 |
| 25 | 1 | 1 | 0 | 0 | 0 | 7.50 |
| 26 | 1 | 1 | 0 | 0 | 1 | 9.00 |
| 27 | 1 | 1 | 0 | 1 | 0 | 10.50 |
| 28 | 1 | 1 | 0 | 1 | 1 | 12.00 |
| 29 | 1 | 1 | 1 | 0 | 0 | 13.50 |
| 30 | 1 | 1 | 1 | 0 | 1 | 15.00 |
| 31 | 1 | 1 | 1 | 1 | 0 | 16.50 |
| 32 | 1 | 1 | 1 | 1 | 1 | 18.00 |

(1) x = M, L, or R
Gain / Attenuation is from input to output

## TI 3D ENHANCEMENT

The LM4946 features a stereo headphone, 3D audio enhancement effect that widens the perceived soundstage from a stereo audio signal. The 3D audio enhancement creates a perceived spatial effect optimized for stereo headphone listening. The LM4946 can be programmed for a “narrow” or “wide” soundstage perception. The narrow soundstage has a more focused approaching sound direction, while the wide soundstage has a spatial, theater-like effect. Within each of these two modes, four discrete levels of 3D effect that can be programmed: low, medium, high, and maximum (Table 2, Table 3), each level with an ever increasing aural effect, respectively. The difference between each level is 3dB.

The external capacitors, shown in Figure 66, are required to enable the 3D effect. The value of the capacitors set the cutoff frequency of the 3D effect, as shown by Equation 1 and Equation 2. Note that the internal 20kΩ resistor is nominal.

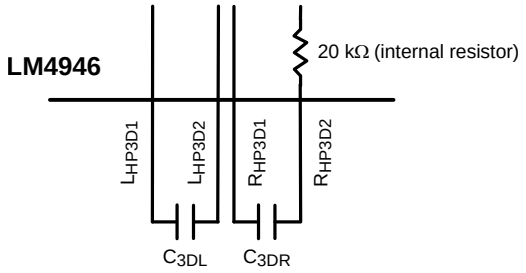



**Figure 66. External 3D Effect Capacitors**

$$f_{3DL(-3dB)} = 1 / 2\pi * 20k\Omega * C_{3DL} \quad (1)$$

$$f_{3DR(-3dB)} = 1 / 2\pi * 20k\Omega * C_{3DR} \quad (2)$$

Optional resistors $R_{3DL}$ and $R_{3DR}$ can also be added (Figure 67) to affect the -3dB frequency and 3D magnitude.

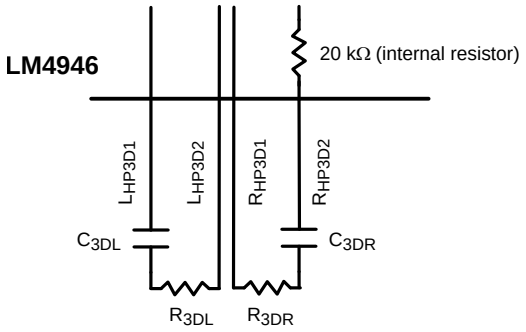



**Figure 67. External RC Network with Optional $R_{3DL}$ and $R_{3DR}$ Resistors**

$$f_{3DL(-3dB)} = 1 / 2\pi * (20k\Omega + R_{3DL}) * C_{3DL} \quad (3)$$

$$f_{3DR(-3dB)} = 1 / 2\pi * 20k\Omega + R_{3DR}) * C_{3DR} \quad (4)$$

ΔAV (change in AC gain) = 1 / 1 + M, where M represents some ratio of the nominal internal resistor, 20kΩ (see example below).

$$f_{3dB} (3D) = 1 / 2\pi (1 + M)(20k\Omega * C_{3D}) \quad (5)$$

$$C_{Equivalent} (new) = C_{3D} / 1 + M \quad (6)$$

**Table 6. Pole Locations**

| $R_{3D}$ (kΩ) (optional) | $C_{3D}$ (nF) | M | ΔAV (dB) | f-3dB (3D) (Hz) | Value of $C_{3D}$ to keep same pole location (nF) | new Pole Location (Hz) |
|---|---|---|---|---|---|---|
| 0 | 68 | 0 | 0 | 117 | | |
| 1 | 68 | 0.05 | –0.4 | 111 | 64.8 | 117 |
| 5 | 68 | 0.25 | –1.9 | 94 | 54.4 | 117 |
| 10 | 68 | 0.50 | –3.5 | 78 | 45.3 | 117 |
| 20 | 68 | 1.00 | –6.0 | 59 | 34.0 | 117 |

## PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 8Ω LOAD

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by an 8Ω load from 158.3mW to 156.4mW. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

## BRIDGE CONFIGURATION EXPLANATION

The LM4946 drives a load, such as a speaker, connected between outputs, MONO+ and MONO-.

This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between MONO- and MONO+ and driven differentially (commonly referred to as "bridge mode"). This results in a differential or BTL gain of:

$$A_{VD} = 2(R_f / R_i) = 2 \quad (7)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing MONO- and MONO+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

## POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM4946 has a pair of bridged-tied amplifiers driving a handsfree speaker, MONO. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation 8, assuming a 5V power supply and an 8Ω load, the maximum MONO power dissipation is 634mW.

$$P_{DMAX\text{-}SPKROUT} = 4(V_{DD})^2 / (2\pi^2 R_L)\text{: Bridge Mode} \quad (8)$$

The LM4946 also has a pair of single-ended amplifiers driving stereo headphones, $R_{OUT}$ and $L_{OUT}$. The maximum internal power dissipation for $R_{OUT}$ and $L_{OUT}$ is given by Equation 9 and Equation 10. From Equation 9 and Equation 10, assuming a 5V power supply and a 32Ω load, the maximum power dissipation for $L_{OUT}$ and $R_{OUT}$ is 40mW, or 80mW total.

$$P_{DMAX\text{-}LOUT} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (9)$$

$$P_{DMAX\text{-}ROUT} = (V_{DD})^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (10)$$

The maximum internal power dissipation of the LM4946 occurs when all three amplifiers pairs are simultaneously on; and is given by Equation 11.

$$P_{DMAX\text{-}TOTAL} = P_{DMAX\text{-}SPKROUT} + P_{DMAX\text{-}LOUT} + P_{DMAX\text{-}ROUT} \quad (11)$$

The maximum power dissipation point given by Equation 11 must not exceed the power dissipation given by Equation 12:

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (12)$$

The LM4946's $T_{JMAX}$ = 150°C. In the SQ package, the LM4946's $\theta_{JA}$ is 46°C/W. At any given ambient temperature $T_A$, use Equation 12 to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation 12 and substituting $P_{DMAX-TOTAL}$ for $P_{DMAX}$' results in Equation 13. This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4946's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX-TOTAL}\ \theta_{JA} \quad (13)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum mono power dissipation without exceeding the maximum junction temperature is approximately 121°C for the SQ package.

$$T_{JMAX} = P_{DMAX-TOTAL}\ \theta_{JA} + T_A \quad (14)$$

Equation 14 gives the maximum junction temperature $T_{JMAX}$. If the result violates the LM4946's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation 11 is greater than that of Equation 12, then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce $\theta_{JA}$. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the $\theta_{JA}$ is the sum of $\theta_{JC}$, $\theta_{CS}$, and $\theta_{SA}$. ($\theta_{JC}$ is the junction-to-case thermal impedance, $\theta_{CS}$ is the case-to-sink thermal impedance, and $\theta_{SA}$ is the sink-to-ambient thermal impedance). Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

## POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 1µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0µF tantalum bypass capacitor and a parallel 0.1µF ceramic capacitor connected between the LM4946's supply pin and ground. Keep the length of leads and traces that connect capacitors between the LM4946's power supply pin and ground as short as possible.

## SELECTING EXTERNAL COMPONENTS

### Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor ($C_i$ in Figure 1 & Figure 2). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

The internal input resistor ($R_i$), minimum 10kΩ, and the input capacitor ($C_i$) produce a high pass filter cutoff frequency that is found using Equation 15.

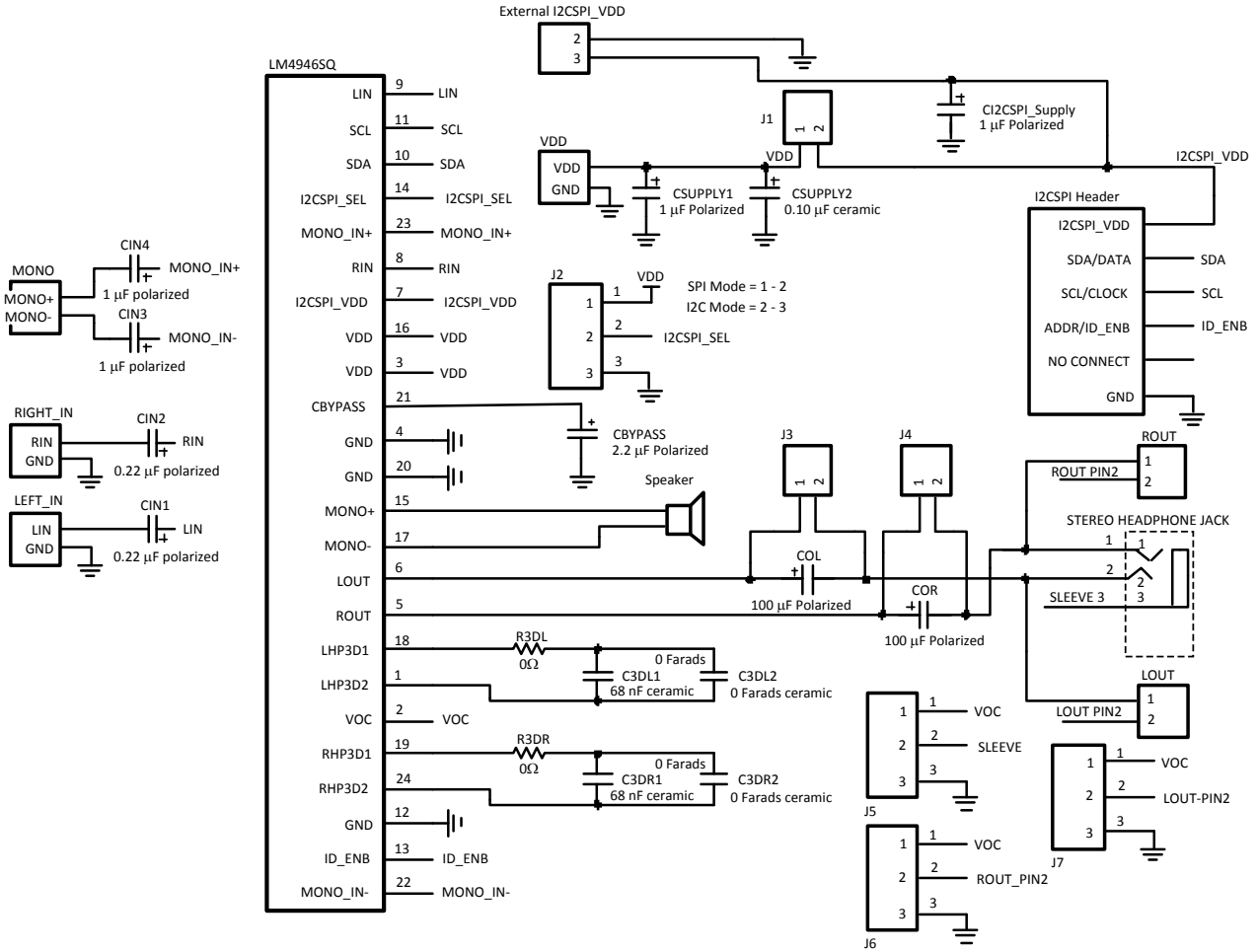
$$f_c = 1 / (2\pi R_i C_i) \quad (15)$$

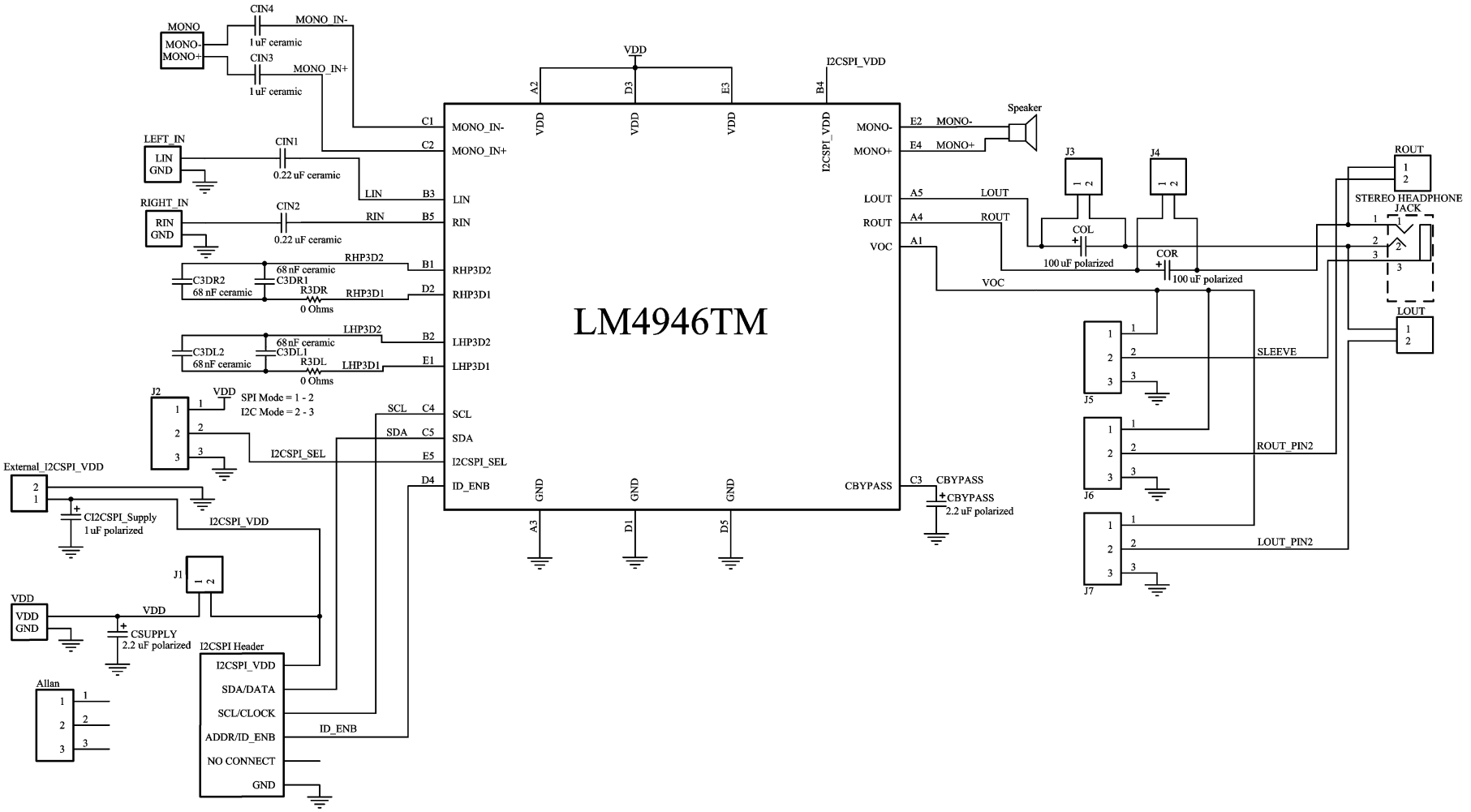
As an example when using a speaker with a low frequency limit of 150Hz, $C_i$, using Equation 15 is 0.106µF. The 0.22µF $C_i$ shown in Figure 1 allows the LM4946 to drive high efficiency, full range speaker whose response extends below 40Hz.

### Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of $C_B$, the capacitor connected to the BYPASS pin. Since $C_B$ determines how fast the LM4946 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4946's outputs ramp to their quiescent DC voltage (nominally $V_{DD}/2$), the smaller the turn-on pop. Choosing $C_B$ equal to 2.2µF along with a small value of $C_i$ (in the range of 0.1µF to 0.33µF), produces a click-less and pop-less shutdown function. As discussed above, choosing $C_i$ no larger than necessary for the desired bandwidth helps minimize clicks and pops. $C_B$'s value should be in the range of 7 to 10 times the value of $C_i$. This ensures that output transients are eliminated when power is first applied or the LM4946 resumes operation after shutdown.

## Demo Board Schematic Diagram





## REVISION HISTORY

| Rev | Date | Description |
|---|---|---|
| 1.0 | 01/23/06 | Initial release. |
| 1.1 | 03/05/07 | Added the YFQ0025XXX package. |
| 1.2 | 03/13/07 | Edited the 25–pin DSBGA connection diagram. |
| 1.3 | 04/24/07 | Added the I2C/SPI (1.7V 2.2V ) table. |
| 1.4 | 04/26/07 | Added the numerical values for the X1, X2, and X3 in the Physical Dimension section. |
| 1.5 | 05/02/07 | Text edits. Added the YFQ package. |
| 1.6 | 05/15/07 | Added the TM board schematic and input some text edits. |
| 1.7 | 05/16/07 | More text edits. |
| 1.8 | 06/06/07 | Added Note 11 and more text edits. |
| 1.9 | 07/31/07 | Edited the 5.0V EC table (MONO_IN Input Impedance and Rin/Lin Input Impedance). |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM4946SQ/NOPB | ACTIVE | WQFN | RTW | 24 | 1000 | Green (RoHS & no Sb/Br) | SN | Level-1-260C-UNLIM | -40 to 85 | L4946SQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

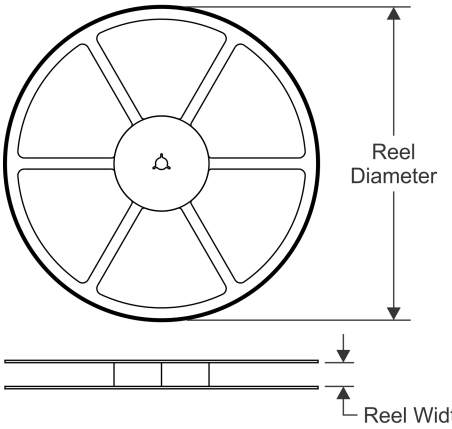
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

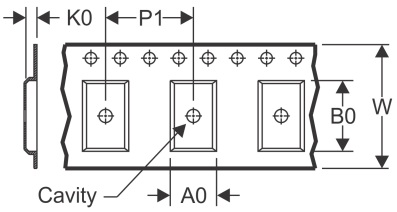
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

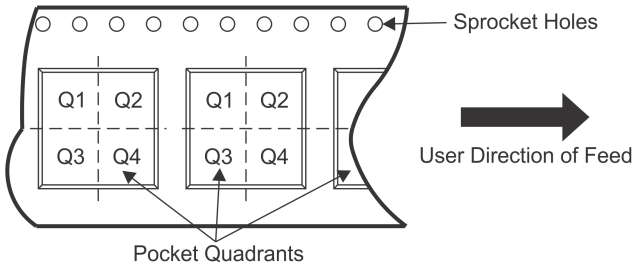



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

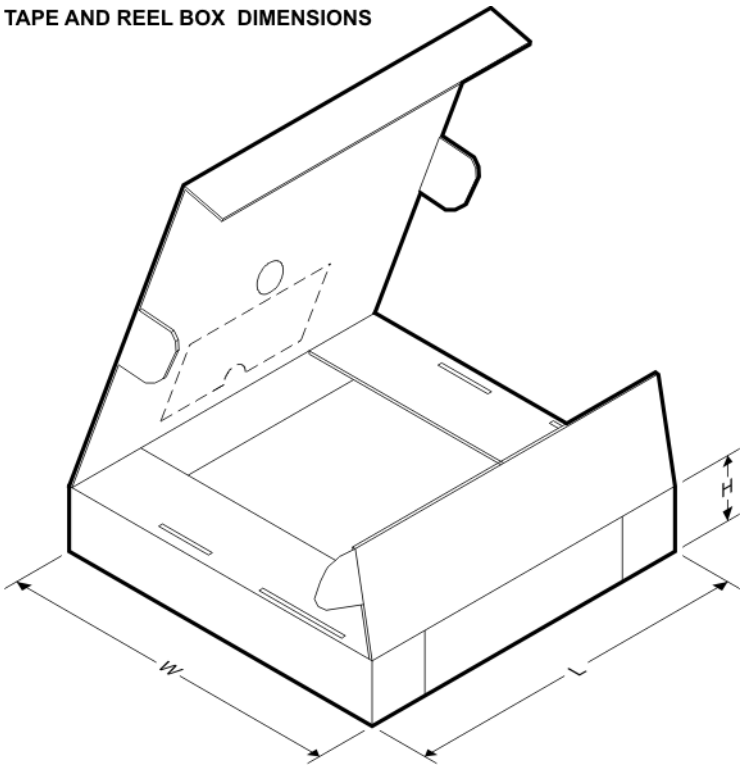
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM4946SQ/NOPB | WQFN | RTW | 24 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

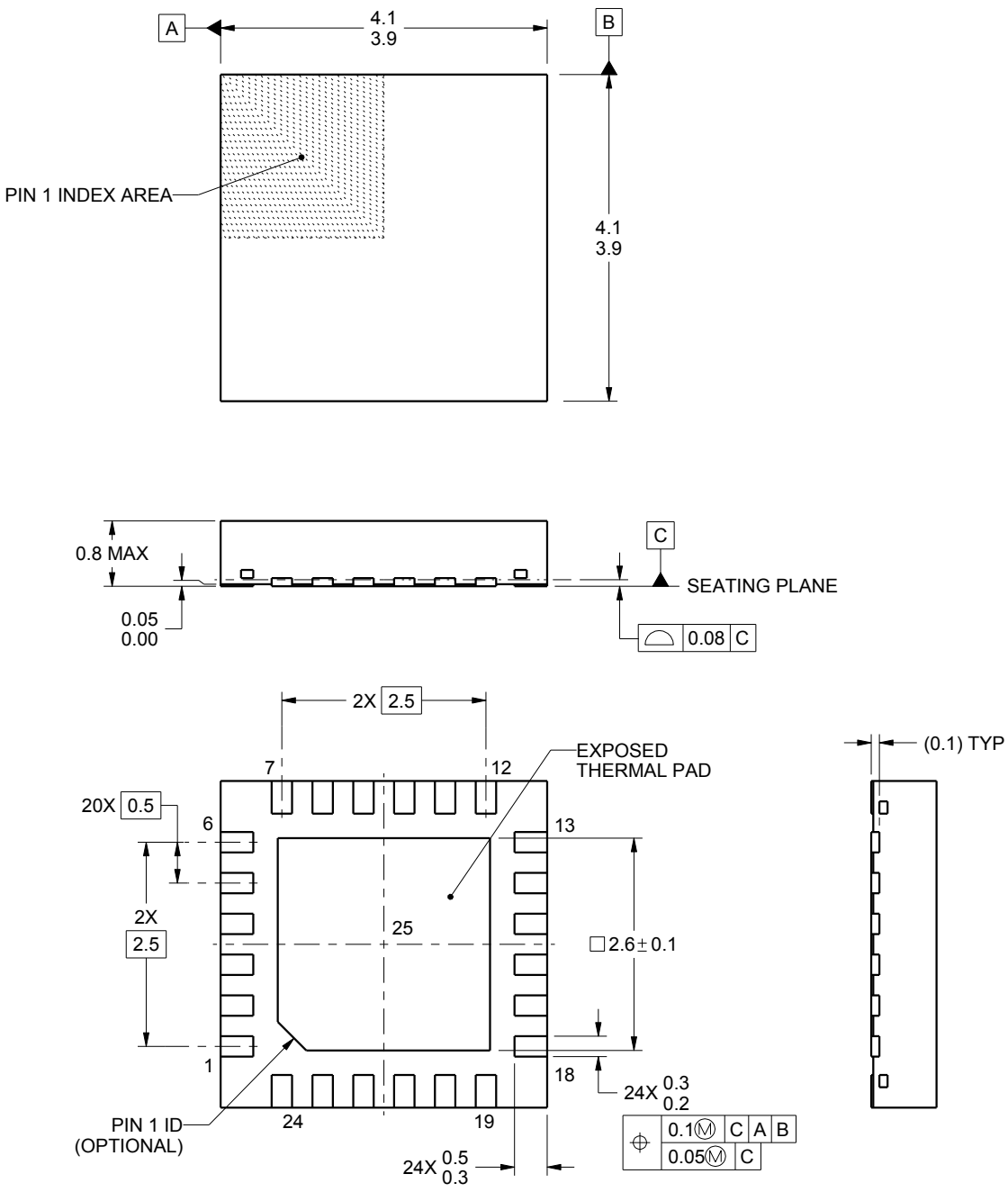
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM4946SQ/NOPB | WQFN | RTW | 24 | 1000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## RTW0024A

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

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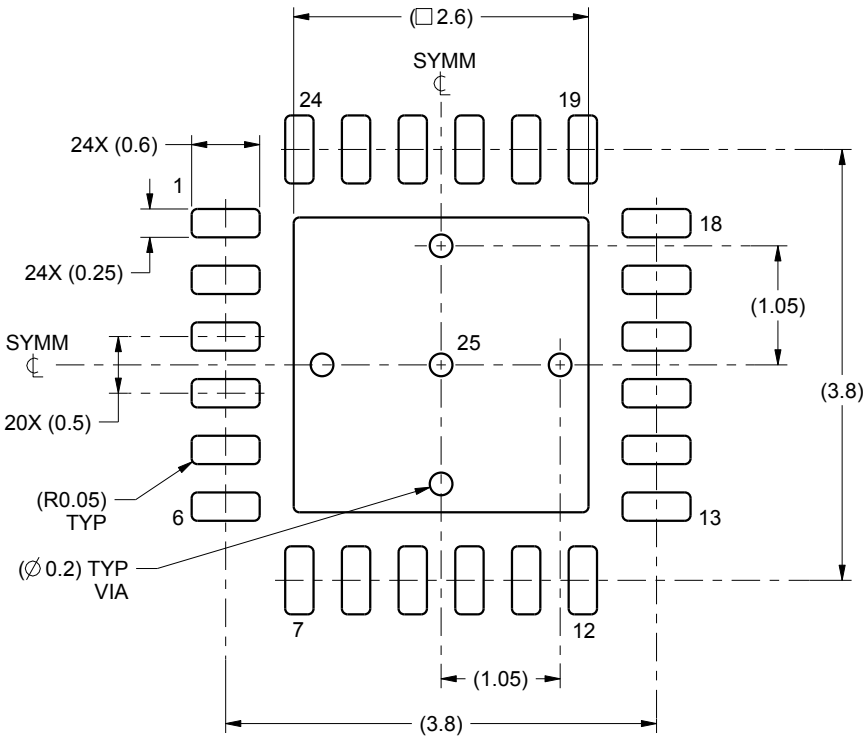
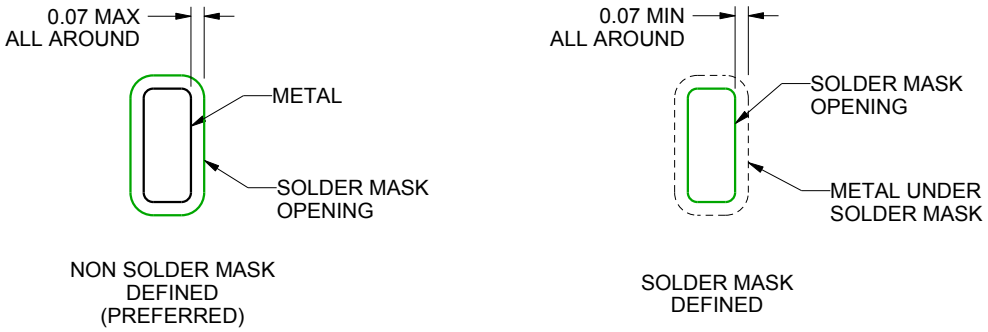
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:15X




SOLDER MASK DETAILS

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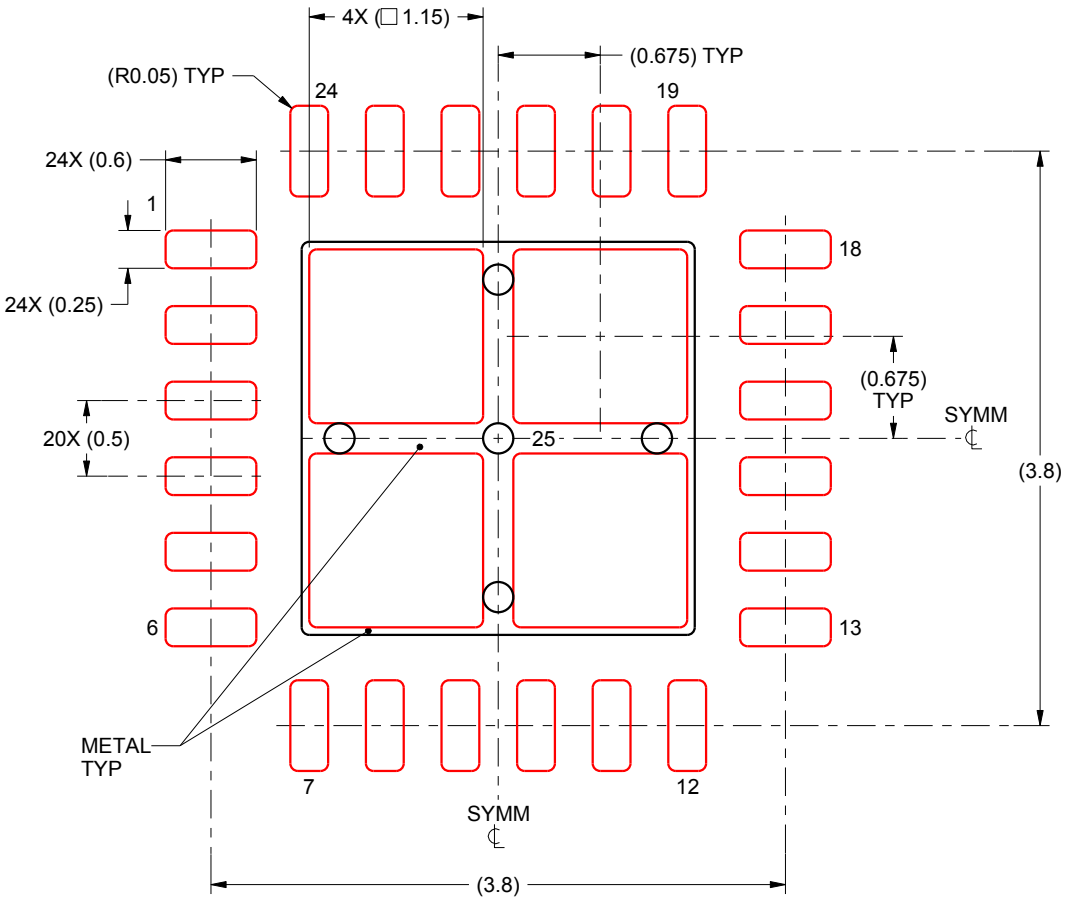
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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