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April 2014

NC7NZ14
TinyLogic® UHS Inverter with Schmitt Trigger Input

Features

- Ultra-High Speed: t_{PD} 3.7 ns (Typical) into 50 pF at 5 V V_{CC}
- High Output Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Power Down High Impedance Inputs/Outputs
- Over-Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Packages
- Space-Saving US8 Surface Mount Package

Description

The NC7NZ14 is a single inverter with Schmitt trigger input from Fairchild's Ultra-High Speed (UHS) series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range. The inputs and outputs are high-impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 7 V independent of V_{CC} operating voltage.

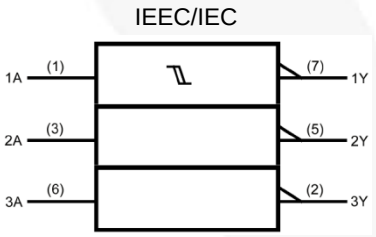

Figure 1. Logic Symbol

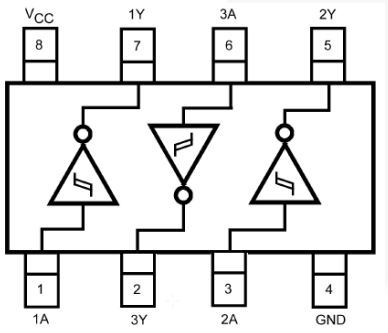

Figure 2. Connection Diagram (Top View)

Ordering Information

Part Number	Operating Temperature	Top Mark	Package	Packing Method
NC7NZ14K8X	-40 to +85°C	NZ14	8-Lead, US8, JEDEC MO-187, Variation CA 3.1 mm Wide	3000 Units on Tape & Reel
NC7NZ14L8X		P6	8-Lead MicroPak™, 1.6 mm Wide	5000 Units on Tape & Reel

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Pin Configurations

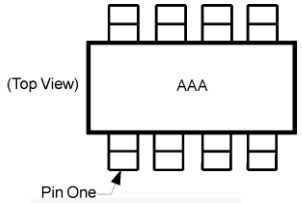


Figure 3. US8

Notes:
1. AAA represents product code top mark (see ordering table).
2. Orientation of top mark determines pin one location. Reading the top product code mark left to right, pin one is the lower left pin.

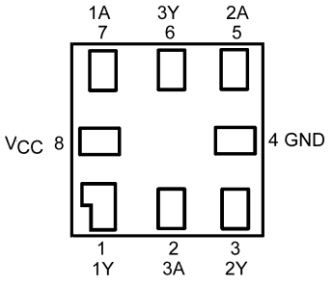


Figure 4. MicroPak™ (Top Through View)

Pin Definitions

Pin # US8	Pin # MicroPak™	Name	Description
1	7	1A	Input
2	6	3Y	Output
3	5	2A	Input
4	4	GND	Ground
5	3	2Y	Output
6	2	3A	Input
7	1	1Y	Output
8	8	V_{CC}	Supply Voltage

Function Table

Y= /A

Inputs	Output
A	**Y**
L	H
H	L

H = HIGH Logic Level

L = LOW Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	7.0	V
V_{IN}	DC Input Voltage		-0.5	7.0	V
V_{OUT}	DC Output Voltage		-0.5	7.0	V
I_{IK}	DC Input Diode Current	V_{IN} < -0.5 V		-50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < -0.5 V		-50	mA
		V_{OUT} > 6.0 V, V_{CC}=GND		+20	
I_{OUT}	DC Output Current			±50	mA
I_{CC} / I_{GND}	DC V_{CC} or Ground Current			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P_D	Power Dissipation at +85°C			250	mW
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charge Device Model, JEDEC:JESD22-C101			2000	

Recommended Operating Conditions[3]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
	Supply Voltage Data Retention		1.5	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		-40	+85	°C
θ_{JA}	Thermal Resistance	US8		250	°C/W
		Micropak™		400	

Note:

3. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A=+25°C			T_A=-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_P	Positive Threshold Voltage	1.65		0.70	1.10	1.50	0.70	1.50	
		2.30		1.00	1.40	1.80	1.00	1.80	
		3.00		1.30	1.75	2.20	1.30	2.20	
		4.50		1.90	2.45	3.10	1.90	3.10	
		5.50		2.20	2.90	3.60	2.20	3.60	
V_N	Negative Threshold Voltage	1.65		0.25	0.55	0.90	0.25	0.90	
		2.30		0.40	0.75	1.15	0.40	1.15	
		3.00		0.60	1.00	1.50	0.60	1.50	V
		4.50		1.00	1.43	2.00	1.00	2.00	
		5.50		1.20	1.70	2.30	1.20	2.30	
V_H	Hysteresis Voltage	1.65		0.15	0.54	1.00	0.15	1.00	
		2.30		0.25	0.65	1.10	0.25	1.10	
		3.00		0.40	0.77	1.20	0.40	1.20	V
		4.50		0.60	1.01	1.50	0.60	1.50	
		5.50		0.70	1.18	1.70	0.70	1.70	
V_{OH}	HIGH Level Output Voltage	1.65	$V_{IN}=V_{IL}$, I_{OH}=-100 µA	1.55	1.65		1.55		
		2.30		2.20	2.30		2.20		
		3.00		2.90	3.00		2.90		
		4.50		4.40	4.50		4.4		
		1.65	I_{OH}=-4 mA	1.29	1.52		1.29		V
		2.30	I_{OH}=-8 mA	1.90	2.15		1.90		
		3.00	I_{OH}=-16 mA	2.40	2.80		2.40		
		3.00	I_{OH}=-24 mA	2.30	2.68		2.30		
		4.50	I_{OH}=-32 mA	3.80	4.20		3.80		
V_{OL}	LOW Level Output Voltage	1.65	$V_{IN}=V_{IH}$, I_{OL}=100 µA		0.00	0.10		0.10	
		2.30			0.00	0.10		0.10	
		3.00			0.00	0.10		0.10	
		4.50			0.00	0.10		0.10	
		1.65	I_{OL}=4 mA		0.08	0.24		0.24	V
		2.30	I_{OL}=8 mA		0.10	0.30		0.30	
		3.00	I_{OL}=16 mA		0.15	0.40		0.40	
		3.00	I_{OL}=24 mA		0.22	0.55		0.55	
		4.50	I_{OL}=32 mA		0.22	0.55		0.55	
I_{IN}	Input Leakage Current	0 to 5.5	V_{IN}=5.5 V, GND			±0.1		±1.0	µA
I_{OFF}	Power Off Leakage Current	0	V_{IN} or V_{OUT}=5.5 V			1		10	µA
I_{CC}	Quiescent Supply Current	1.65 to 5.50	V_{IN}=5.5 V, GND			1.0		10	µA

AC Electrical Characteristics

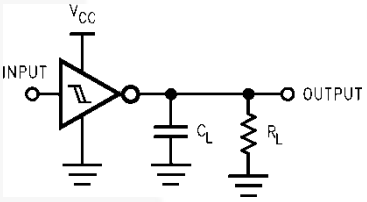
Symbol	Parameter	V_{CC} (V)	Conditions	T_A=+25°C			T_A=-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PLH}, t_{PHL}	Propagation Delay	1.80 ± 0.15	C_L=15 pF, R_L=1 MΩ	2.0	7.6	12.5	2.0	13.0	ns	Figure 5 Figure 6
		2.50 ± 0.20		1.0	5.0	9.0	1.0	9.5		
		3.30 ± 0.30		1.0	3.7	6.3	1.0	6.5		
		5.00 ± 0.50		0.5	3.1	5.2	0.5	5.5		
		3.30 ± 0.30	C_L=50 pF, R_L=500 Ω	1.5	4.4	7.2	1.5	7.5		Figure 5 Figure 6
		5.00 ± 0.50		0.8	3.7	5.9	0.8	6.2		
C_{IN}	Input Capacitance	0.00			2.5				pF	
C_{PD}	Power Dissipation Capacitance(4)	3.30			9				**pF**	Figure 7
		5.00			11					

Note:

4. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD}=(C_{PD})(V_{CC})(f_{IN})+(I_{CC}static)$.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°c	Unit
				Typ.	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L=50 pF, V_{IH}=5.0 V, V_{IL}=0 V	5.0	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}		5.0	-0.8	V



Note:

5. C_L includes load and stray capacitance; Input PRR=1.0 MHz; t_W=500 ns

Figure 5. AC Test Circuit

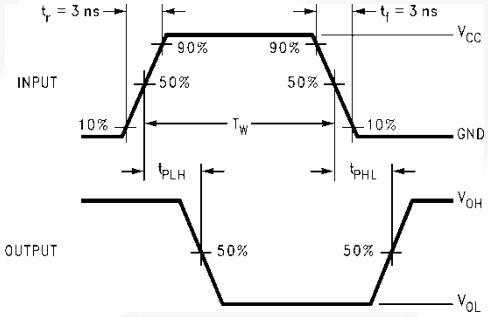
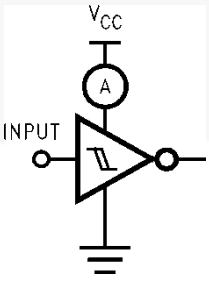


Figure 6. AC Waveforms



Note:

6. Input=AC Waveform; t_r=t_f=1.8 ns; PRR=10 MHz; Duty Cycle =50%.

Figure 7. I_{CCD} Test Circuit

Physical Dimensions

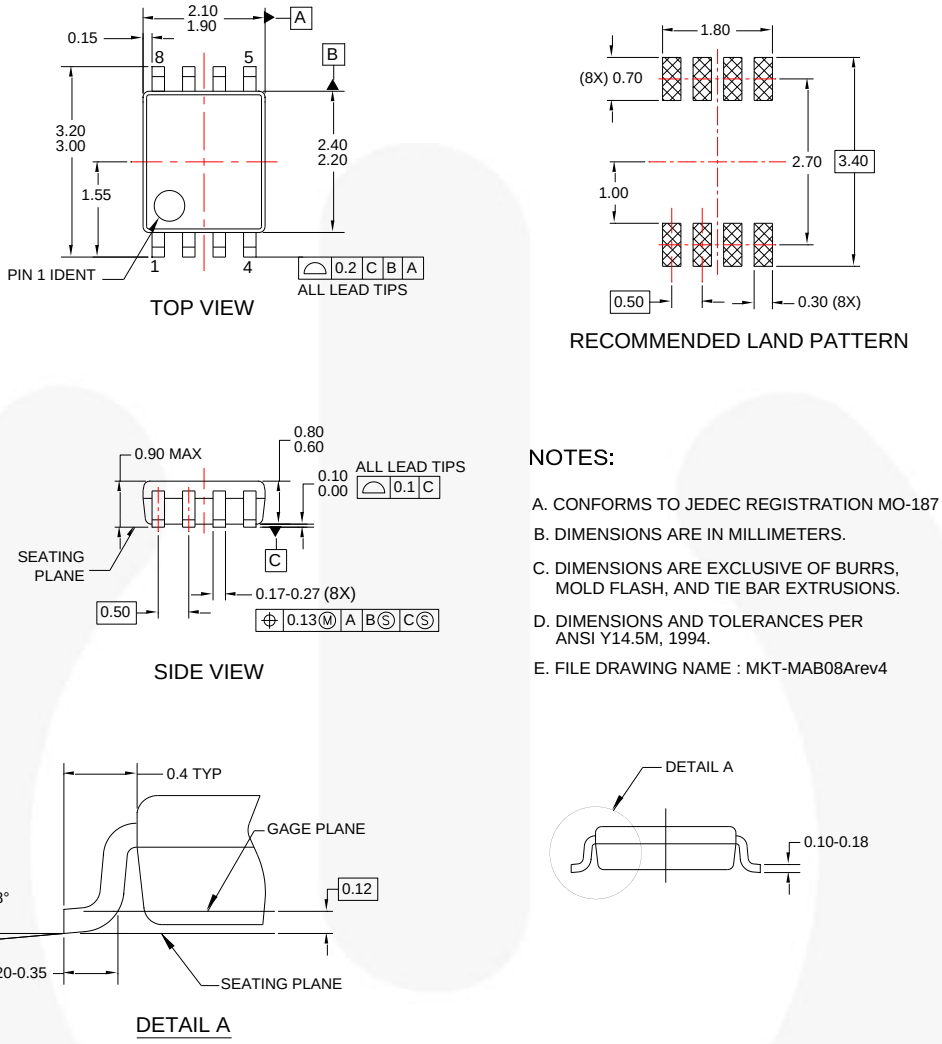


Figure 8. 8-Lead US8, JEDEC MO-187, Variation CA, 3.1 mm Wide

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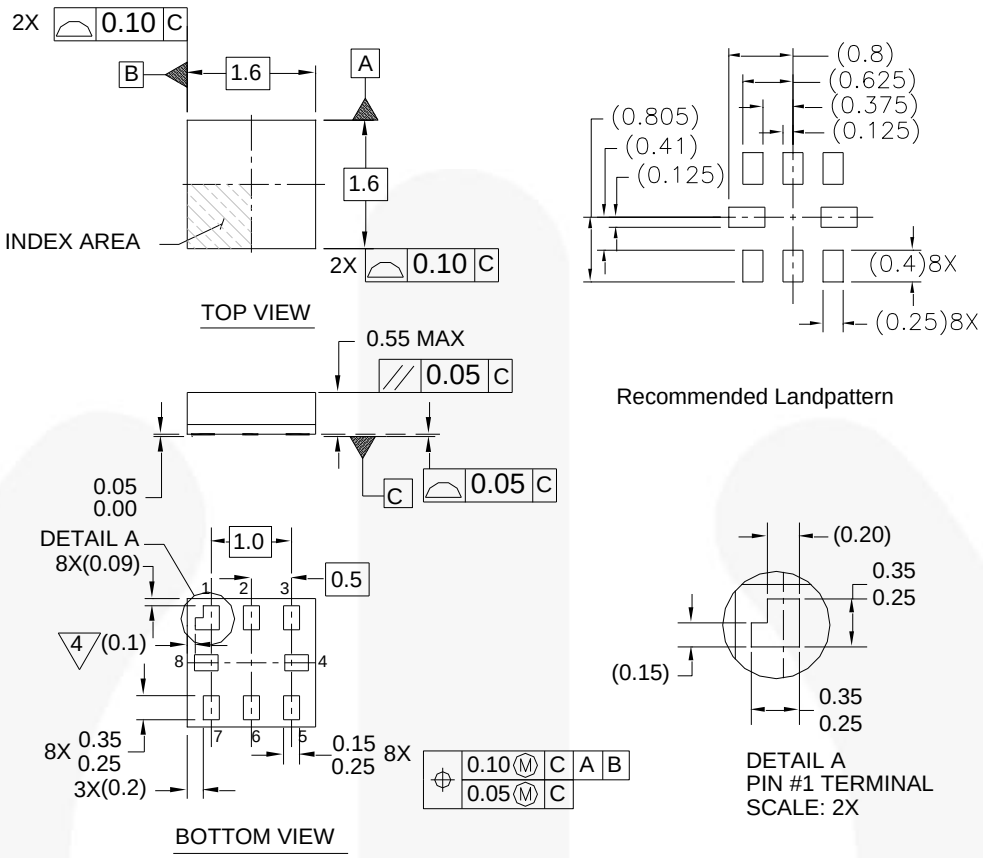
Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/packaging/US8_Pack_TNR.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
K8X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Figure 9. 8-Lead, MicroPak™, 1.0 mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L8X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I68

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