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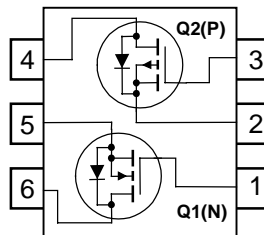
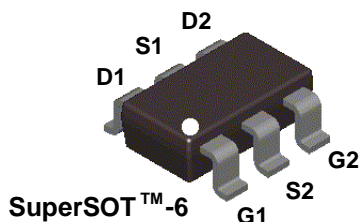
## Dual N & P-Channel Enhancement Mode Field Effect Transistor

### General Description

These dual N & P-Channel Enhancement Mode Field Effect Transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. These device is particularly suited for low voltage, low current, switching, and power supply applications.

### Features

- **Q1** 0.51 A, 60V.  $R_{DS(ON)} = 2 \Omega @ V_{GS} = 10 V$   
 $R_{DS(ON)} = 4 \Omega @ V_{GS} = 4.5 V$
- **Q2** -0.34 A, 60V.  $R_{DS(ON)} = 5 \Omega @ V_{GS} = -10 V$   
 $R_{DS(ON)} = 7.5 \Omega @ V_{GS} = -4.5 V$
- High saturation current
- High density cell design for low  $R_{DS(ON)}$
- Proprietary SuperSOT™-6 package: design using copper lead frame for superior thermal and electrical capabilities



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V <sub>DSS</sub>	Drain-Source Voltage	60	-60	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	±20	
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	0.51	-0.34	A
	– Pulsed	1.5	-1	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a)	0.96		W
	(Note 1b)	0.9		
	(Note 1c)	0.7		
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	60	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.01C	NDC7001C	7"	8mm	3000

### Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	Q1 60 Q2 -60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$ $I_D = -250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$	Q1 Q2	67 -57		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -48\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2		1 -1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	All		100	nA
$I_{GSSR}$	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	All		-100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	Q1	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	2.1	2.5	V
		Q2	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.9	-3.5	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	Q1	$I_D = 250\ \mu\text{A}, \text{Referenced. to } 25^\circ\text{C}$		-3.8		mV/°C
		Q2	$I_D = -250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$		3.2		
$R_{DS(on)}$	Static Drain-Source On-Resistance	Q1	$V_{GS} = 10\text{ V}, I_D = 0.51\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 0.35\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 0.51\text{ A}, T_J = 125^\circ\text{C}$		1 2 1.7	2 4 3.5	$\Omega$
		Q2	$V_{GS} = -10\text{ V}, I_D = -0.34\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -0.25\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -0.34\text{ A}, T_J = 125^\circ\text{C}$		1.2 1.5 1.9	5 7.5 10	
$I_{D(on)}$	On-State Drain Current	Q1	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$	1.5			A
		Q2	$V_{GS} = -10\text{ V}, V_{DS} = -10\text{ V}$	-1			
$g_{FS}$	Forward Transconductance	Q1	$V_{DS} = 10\text{ V}, I_D = 0.51\text{ A}$		380		mS
		Q2	$V_{DS} = -10\text{ V}, I_D = -0.34\text{ A}$		700		

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	Q1	For Q1: $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$		20		pF
		Q2			66		
$C_{oss}$	Output Capacitance	Q1	f = 1.0MHz		11		pF
		Q2		For Q2:		13	
$C_{riss}$	Reverse Transfer Capacitance	Q1	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}$ f = 1.0MHz		4.3		pF
		Q2			6		
$R_G$	Gate Resistance	Q1	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		11.2		$\Omega$
		Q2			11.2		

### Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	Q1	For Q1: $V_{DS} = 25\text{ V}, I_{DS} = 1\text{ A}$		2.8	5.6	ns
		Q2			3.2	6.4	
$t_r$	Turn-On Rise Time	Q1	$V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		8	16	ns
		Q2		For Q2:		10	
$t_{d(off)}$	Turn-Off Delay Time	Q1	$V_{DS} = -25\text{ V}, I_{DS} = -1\text{ A}$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		14	26	ns
		Q2			8	16	
$t_f$	Turn-Off Fall Time	Q1			4	8	ns
		Q2			1	2	
$Q_g$	Total Gate Charge	Q1	For Q1: $V_{DS} = 25\text{ V}, I_{DS} = 0.51\text{ A}$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		1.1	1.5	nC
		Q2			1.6	2.2	
$Q_{gs}$	Gate-Source Charge	Q1	For Q2: $V_{DS} = -25\text{ V}, I_{DS} = -0.35\text{ A}$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		0.2		nC
		Q2			0.3		
$Q_{gd}$	Gate-Drain Charge	Q1			0.4		nC
		Q2			0.3		

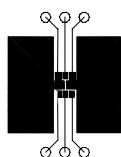
### Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

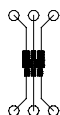
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>							
$I_S$	Maximum Continuous Drain–Source Diode Forward Current	Q1			0.51	A	
		Q2			-0.34		
$V_{SD}$	Drain–Source Diode Forward Voltage	Q1	$V_{GS} = 0\text{ V}, I_S = 0.51\text{ A}$ (Note 2)		0.8	1.2	V
		Q2	$V_{GS} = 0\text{ V}, I_S = -0.34\text{ A}$ (Note 2)		-0.8	-1.4	
$t_{rr}$	Diode Reverse Recovery Time	Q1	$I_F = 0.51\text{ A}, d_I/d_t = 100\text{ A}/\mu\text{s}$		18		nS
		Q2	$I_F = -0.34\text{ A}, d_I/d_t = 100\text{ A}/\mu\text{s}$		16		
$Q_{rr}$	Diode Reverse Recovery Charge	Q1	$I_F = 0.51\text{ A}, d_I/d_t = 100\text{ A}/\mu\text{s}$		16		nC
		Q2	$I_F = -0.34\text{ A}, d_I/d_t = 100\text{ A}/\mu\text{s}$		11		

**Notes:**

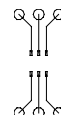
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $130^\circ\text{C}/\text{W}$  when mounted on a  $0.125\text{ in}^2$  pad of 2 oz. copper.



b)  $140^\circ\text{C}/\text{W}$  when mounted on a  $.005\text{ in}^2$  pad of 2 oz copper



c)  $180^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics: N-Channel

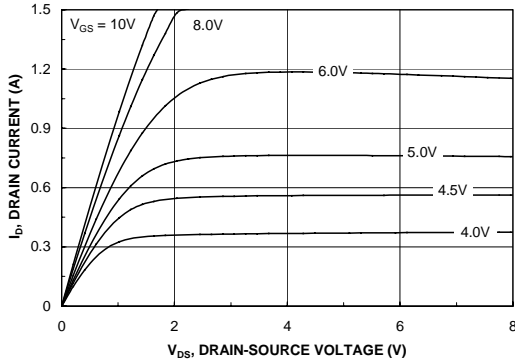


Figure 1. On-Region Characteristics.

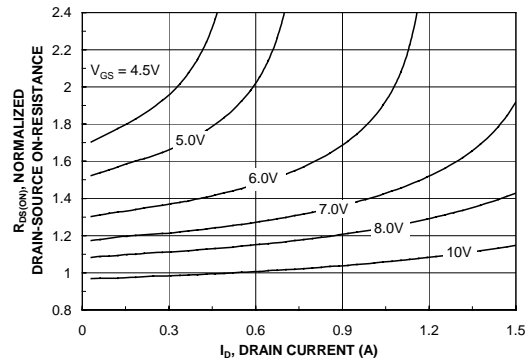


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

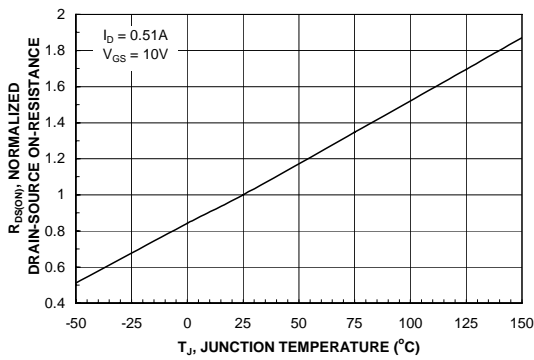


Figure 3. On-Resistance Variation with Temperature.

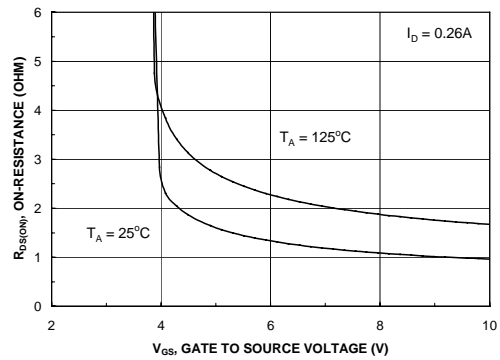


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

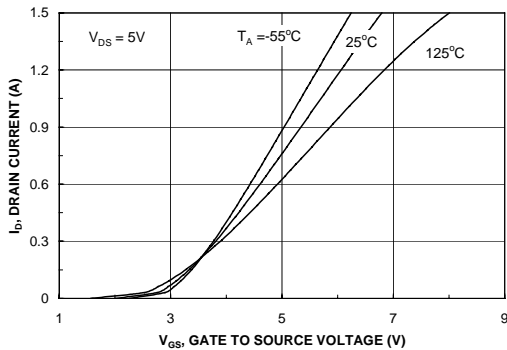


Figure 5. Transfer Characteristics.

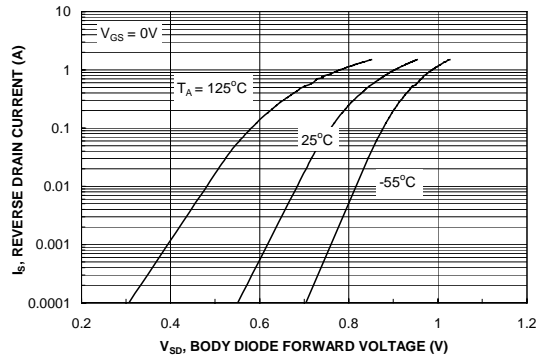
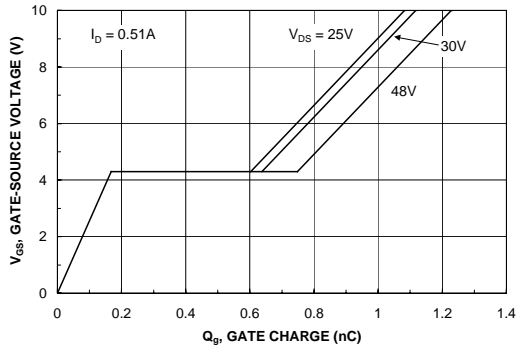
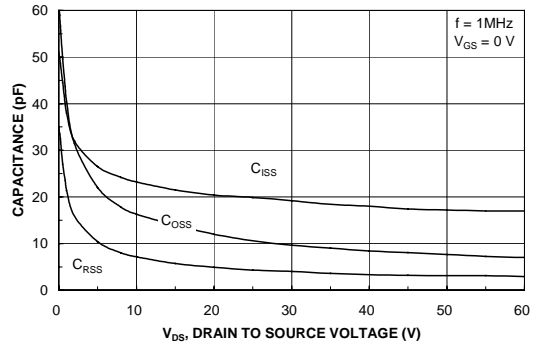


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

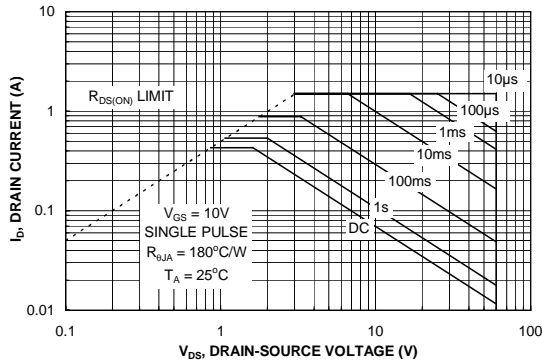
**Typical Characteristics: N-Channel** (continued)



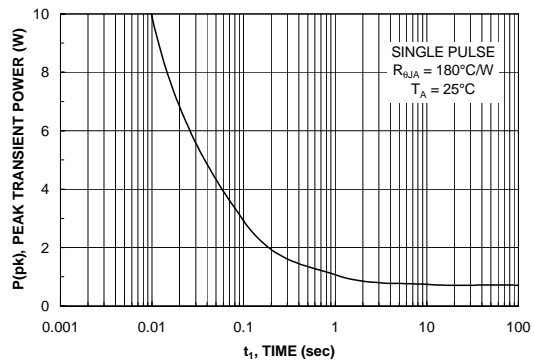
**Figure 7. Gate Charge Characteristics.**



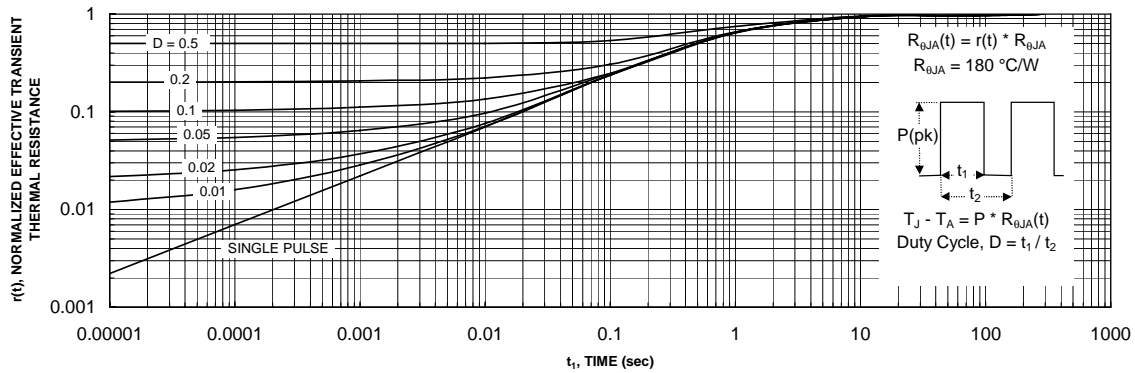
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 21. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

### Typical Characteristics: P-Channel

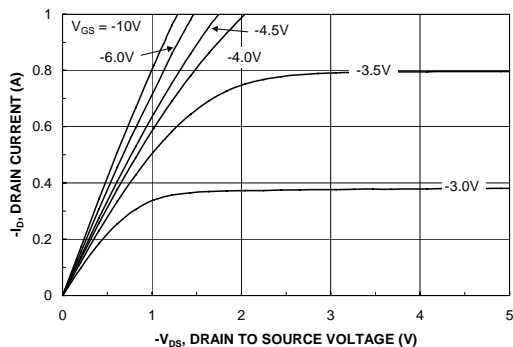


Figure 11. On-Region Characteristics.

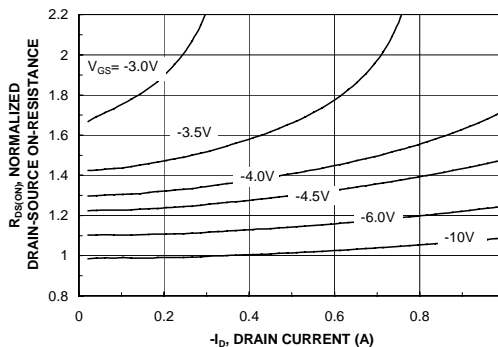


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

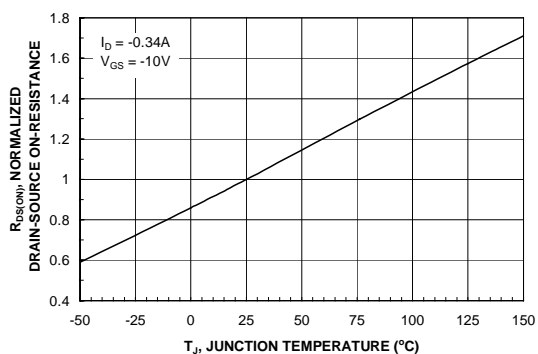


Figure 13. On-Resistance Variation with Temperature.

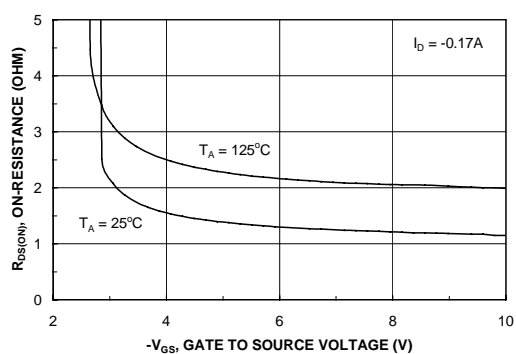


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

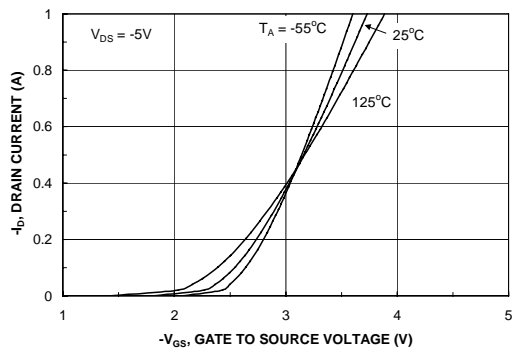


Figure 15. Transfer Characteristics.

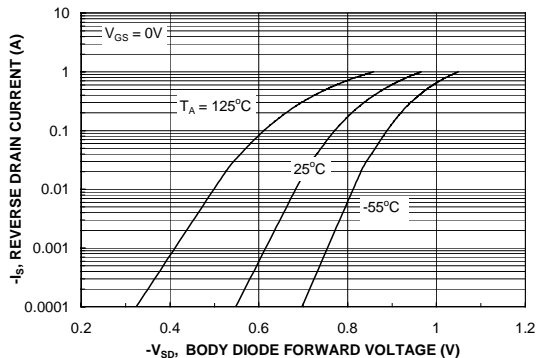
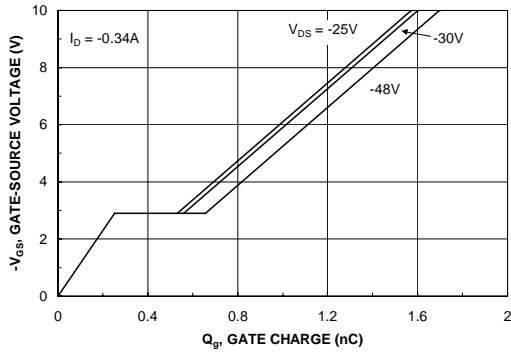
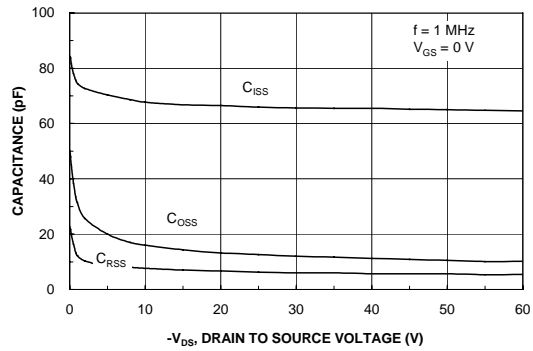


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

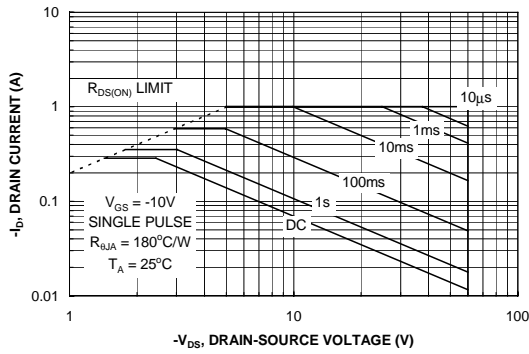
**Typical Characteristics: P-Channel** (continued)



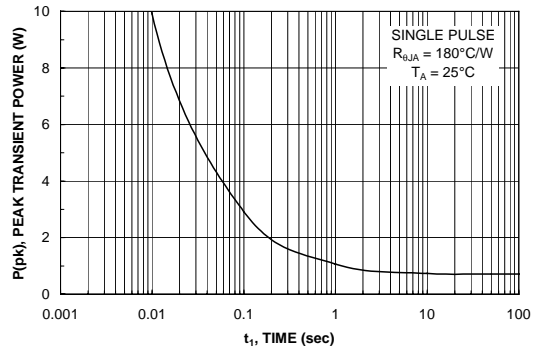
**Figure 17. Gate Charge Characteristics.**



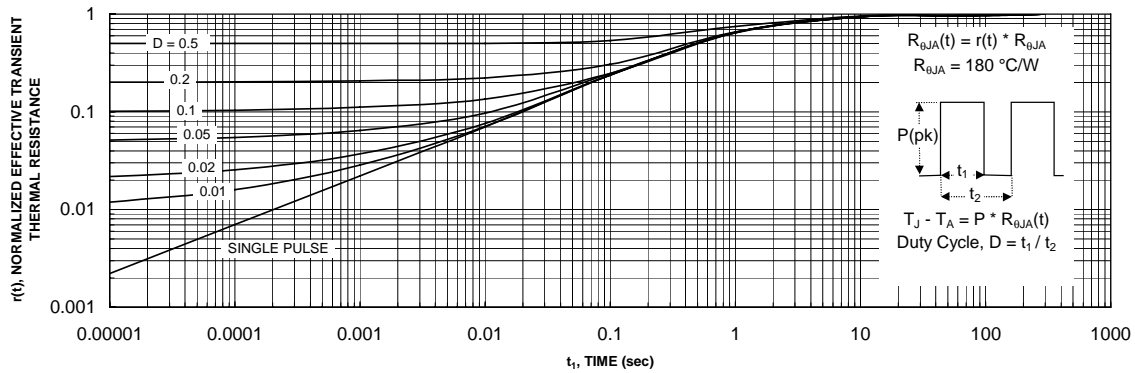
**Figure 18. Capacitance Characteristics.**



**Figure 19. Maximum Safe Operating Area.**



**Figure 20. Single Pulse Maximum Power Dissipation.**



**Figure 21. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



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