Enpirion® Power Datasheet ER2120QI 2A Synchronous Buck Regulator with Integrated MOSFETs

The Altera® Enpirion® ER2120QI is a synchronous buck controller with internal MOSFETs packaged in a small 4mmx4mm QFN package. The ER2120QI can support a continuous load of 2A and has a very wide input voltage range. With the switching MOSFETs integrated into the IC, the complete regulator footprint can be very small and provide a much more efficient solution than a linear regulator.

The ER2120QI is capable of stand-alone operation or it can be used in a master slave combination for multiple outputs that are derived from the same input rail. Multiple slave channels (up to six) can be synchronized. This method minimizes the EMI and beat frequencies effect with multi-channel operation.

The switching PWM controller drives two internal N-Channel MOSFETs in a synchronous-rectified buck converter topology. The synchronous buck converter uses voltage-mode control with fast transient response. The switching regulator provides a maximum static regulation tolerance of ±1% over line, load, and temperature ranges. The output is user-adjustable by means of external resistors down to 0.6V.

The output is monitored for undervoltage events. The switching regulator also has overcurrent protection. Thermal shutdown is integrated. The ER2120QI features a bi-directional Enable pin that allows the part to pull the enable pin low during fault detection.

POK delay for ER2120QI is 1ms typical (at 500kHz switching frequency).

Features

- Up to 2A Continuous Output Current
- Integrated MOSFETs for Small Regulator Footprint
- Adjustable Switching Frequency, 500kHz to 1.2MHz
- Tight Output Voltage Regulation, ±1% Over-temperature
- Wide Input Voltage Range, 5V ±10% or 5.5V to 14V
- Wide Output Voltage Range, from 0.6V
- Simple Single-Loop Voltage-Mode PWM Control Design
- Input Voltage Feed-Forward for Constant Modulator Gain
- Fast PWM Converter Transient Response
- Lossless $R_{DS(ON)}$ High Side and Low Side Overcurrent Protections
- Undervoltage Detection
- Integrated Thermal Shutdown Protection
- Power-Good Indication
- Adjustable Soft-Start
- Start-Up with Pre-Bias Output
- Pb-free (RoHS Compliant)

Applications

- FPGA power
- Point of Load Applications
- Graphics Cards
- ASIC Power Supplies
- Embedded Processor and I/O Supplies
- DSP Supplies

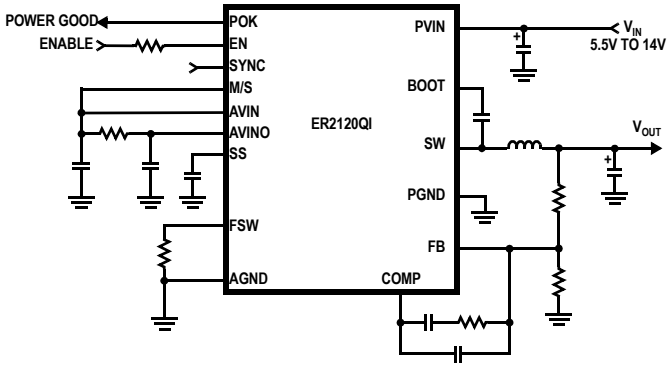


FIGURE 1. STAND-ALONE REGULATOR: V_{IN} 5.5V TO 14V

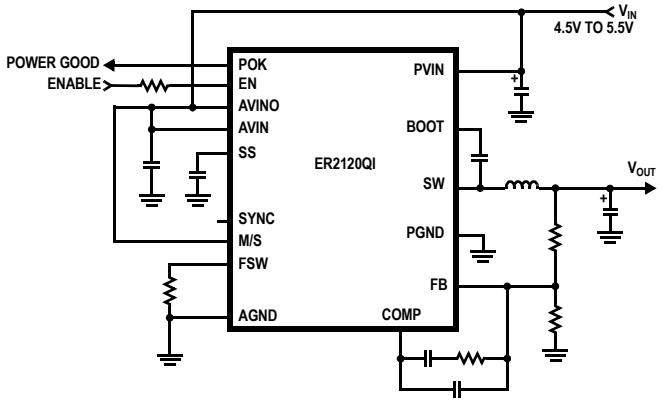


FIGURE 2. STAND-ALONE REGULATOR: V_{IN} 4.5V TO 5.5V

101 Innovation Drive
San Jose, CA 95134
www.altera.com

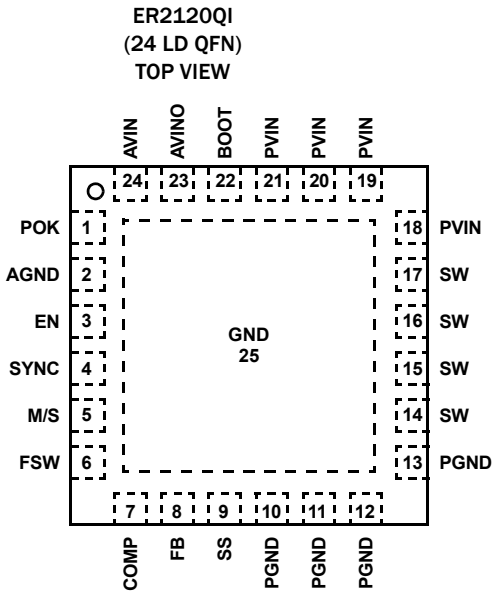
Ordering Information

PART NUMBER (Note 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ER2120QI (Notes 1, 3)	2120	-40 to +85	24 Ld 4x4 QFN	L24.4x4D
EVB-ER2120QI	Evaluation Board			

NOTES:

1. These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration



*See “Functional Pin Descriptions” beginning on page 13 for pin descriptions.

Typical Application Schematics

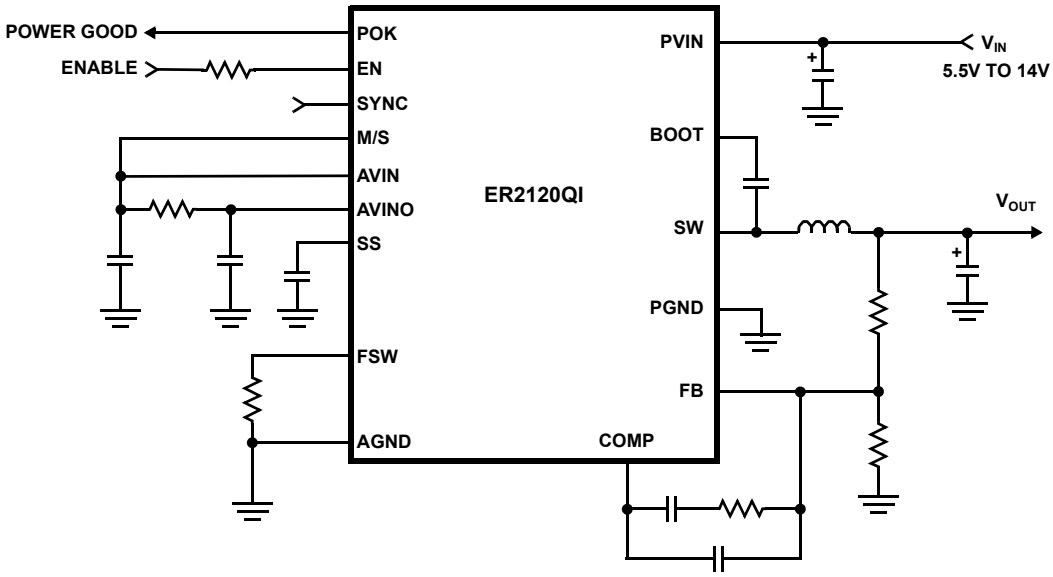


FIGURE 3. STAND-ALONE REGULATOR: V_{IN} 5.5V TO 14V

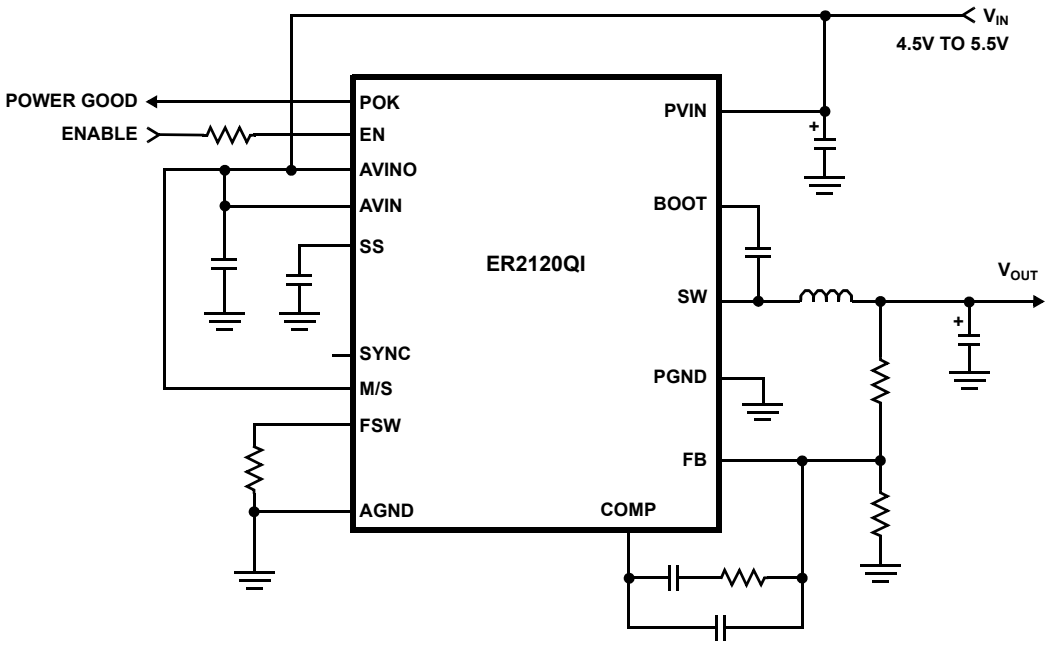
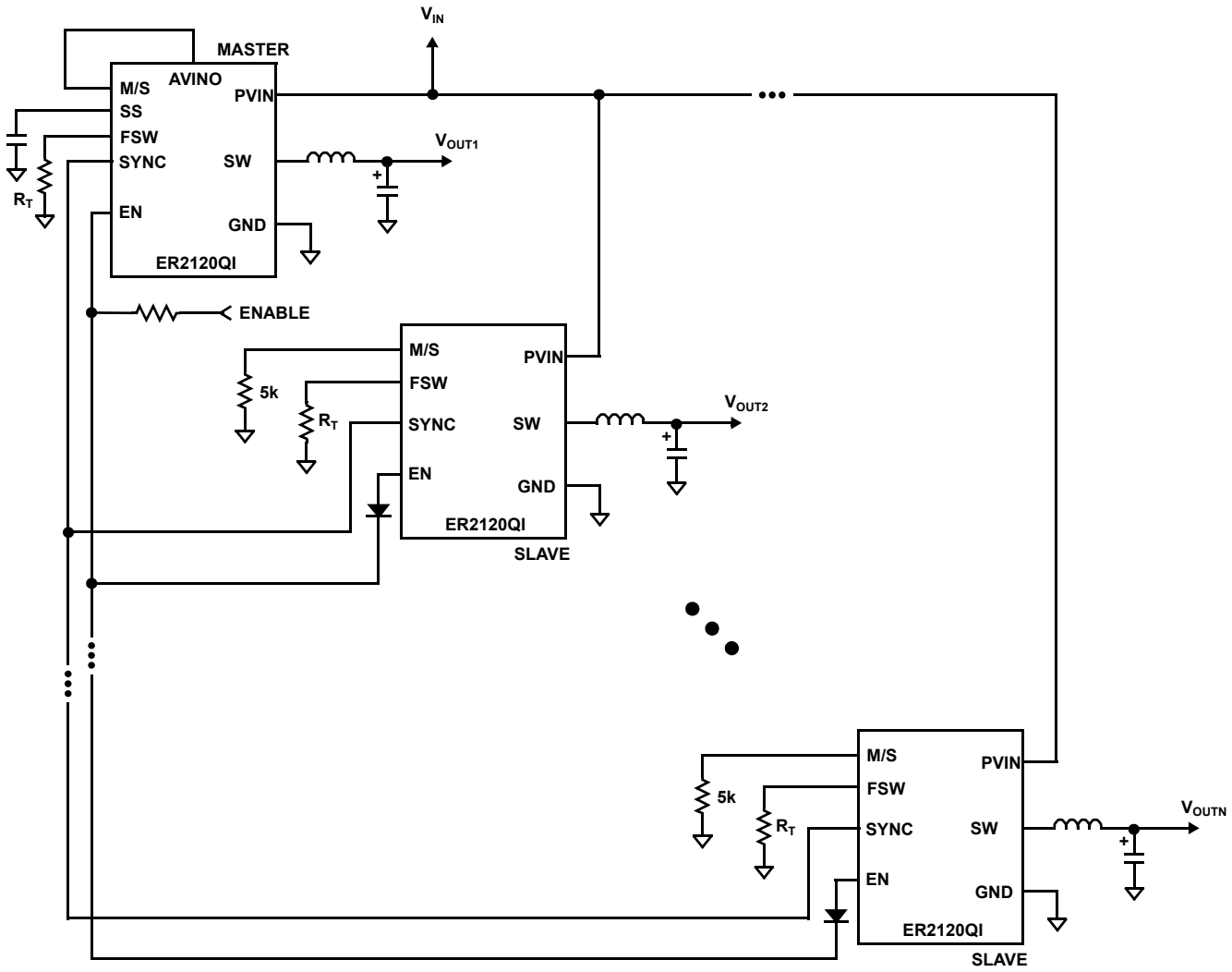


FIGURE 4. STAND-ALONE REGULATOR: V_{IN} 4.5V TO 5.5V

ER2120QI With Multiple Slaved Channels



Absolute Maximum Ratings

PVIN. . . . . GND - 0.3V to +16.5V
AVIN. . . . . GND - 0.3V to +6.0V
Absolute Boot Voltage, V_{BOOT} . . . . . +22.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{SW} . . . . . +6.0V
All other Pins . . . . . GND - 0.3V to AVIN + 0.3V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 2, 2)	38	2

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile. . . . . —

Recommended Operating Conditions

Supply Voltage on PVIN . . . . . 5.5V to 14V
Ambient Temperature Range . . . . . -40°C to +85°C
Junction Temperature Range . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Refer to "Block Diagram" and "Typical Application Schematics". Operating conditions unless otherwise noted: V_{IN} = 12V, or V_{AVIN} = 5V ±10%, T_A = -40°C to +85°C. Typical are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
V_{IN} SUPPLY						
PVIN Input Voltage Range		V_{IN}	**5.5** (Note 4)		**14** (Note 5)	V
		V_{IN} tied to V_{AVIN}	**4.5**		**5.5**	V
Input Operating Supply Current	I_Q	V_{FB} = 1.0V			**7**	mA
Input Standby Supply Current	I_{Q_SBY}	EN tied to GND, V_{IN} = 14V		1.25	**2**	mA
SERIES REGULATOR						
AVIN Voltage	V_{AVINO}	V_{IN} > 5.6V	**4.5**	5.0	**5.5**	V
Maximum Output Current	I_{AVINO}	V_{IN} = 12V	**50**			mA
AVIN Current Limit		V_{IN} = 12V, AVIN shorted to PGND		300		mA
POWER-ON RESET						
Rising AVIN POR Threshold			**4.2**	4.4	**4.49**	V
Falling AVIN POR Threshold			**3.85**	4.0	**4.10**	V
ENABLE						
Rising Enable Threshold Voltage	V_{EN_Rising}			2.7		V
Falling Enable Threshold Voltage	V_{EN_Fall}			2.3		V
Enable Sinking Current	I_{EN}				**500**	µA
OSCILLATOR						
PWM Frequency	f_{OSC}	R_T = 96kΩ	**400**	500	**600**	kHz
		R_T = 40kΩ	**960**	1200	**1440**	kHz
		FSW pin tied to AVIN		800		kHz
Ramp Amplitude	ΔV_{OSC}	V_{IN} = 14V		1.0		V
Ramp Amplitude	ΔV_{OSC}	V_{IN} = 5V		0.470		V
Modulator Gain	$V_{VIN}/\Delta V_{OSC}$	By Design		8		-
Maximum Duty Cycle	D_{MAX}	f_{OSC} = 500kHz	**88**			%
Maximum Duty Cycle	D_{MAX}	f_{OSC} = 1.2MHz	**76**			%

Electrical Specifications

Refer to “Block Diagram” and “Typical Application Schematics”. Operating conditions unless otherwise noted: V_{IN} = 12V, or V_{AVIN} = 5V ±10%, T_A = -40°C to +85°C. Typical are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}			0.600		V
System Accuracy			**-1.0**		**+1.0**	%
FB Pin Bias Current				±80	**±200**	nA
SOFT-START						
Soft-Start Current	I_{SS}		**20**	30	**40**	µA
Enable Soft-Start Threshold			**0.8**	1.0	**1.2**	V
Enable Soft-Start Threshold Hysteresis				12		mV
Enable Soft-Start Voltage High			**2.8**	3.2	**3.8**	V
ERROR AMPLIFIER						
DC Gain				88		dB
Gain-Bandwidth Product	GBWP			15		MHz
Maximum Output Voltage			**3.9**	4.4		V
Slew Rate	SR			5		V/µs
INTERNAL MOSFETS						
Upper MOSFET $R_{DS(ON)}$	r_{DS_UPPER}	V_{AVIN} = 5V		180		mΩ
Lower MOSFET $R_{DS(ON)}$	r_{DS_LOWER}	V_{AVIN} = 5V		90		mΩ
POK						
POK Threshold	V_{FB}/V_{REF}	Rising Edge Hysteresis 1%	**107**	111	**115**	%
		Falling Edge Hysteresis 1%	**86**	90	**93**	%
POK Rising Delay (Note 8)	t_{POK_DELAY}	f_{OSC} = 500kHz		1		ms
POK Leakage Current		V_{POK} = 5.5V			5	µA
POK Low Voltage	V_{POK}			0.10		V
POK Sinking Current	I_{POK}				**0.5**	mA
PROTECTION						
Positive Current Limit	I_{POC_peak}	IOC from PVIN to SW (Notes 6, 7) (T_A = 0°C to +85°C)	2.1	3.5	4.5	A
		IOC from PVIN to SW (Notes 6, 7) (T_A = -40°C to +0°C)	2.0	3.4	4.0	A
Negative Current Limit	I_{NOC_peak}	IOC from SW to PGND (Notes 6, 7) (T_A = 0°C to +85°C)	2.2	3.0	3.5	A
		IOC from SW to PGND (Notes 6, 7) (T_A = -40°C to +85°C)	1.9	2.8	3.7	A
Undervoltage Level	V_{FB}/V_{REF}		**76**	80	**84**	%
Thermal Shutdown Setpoint	T_{SD}			150		°C
Thermal Recovery Setpoint	T_{SR}			130		°C

Electrical Specifications

Refer to “Block Diagram” and “Typical Application Schematics”. Operating conditions unless otherwise noted: V_{IN} = 12V, or V_{AVIN} = 5V ±10%, T_A = -40°C to +85°C. Typical are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS

NOTES:

3. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
4. Minimum V_{IN} can operate below 5.5V as long as V_{AVIN} is greater than 4.5V.
5. Maximum V_{IN} can be higher than 14V voltage stress across the upper and lower do not exceed 15.5V in all conditions.
6. Circuit requires 150ns minimum on time to detect overcurrent condition.
7. Limits established by characterization and are not production tested.
8. POK Rising Delay is measured from the point where V_{OUT} reaches regulation to the point where POK rises. It does not include the external soft-start time. The POK Rising Delay specification is measured at 500kHz.

Typical Performance Curves

V_{IN} = 12V, V_{OUT} = 2.5V, I_O = 2A, f_{SW} = 500kHz, L = 4.7µH, C_{IN} = 20µF, C_{OUT} = 100µF + 22µF, T_A = +25° C, unless otherwise noted.

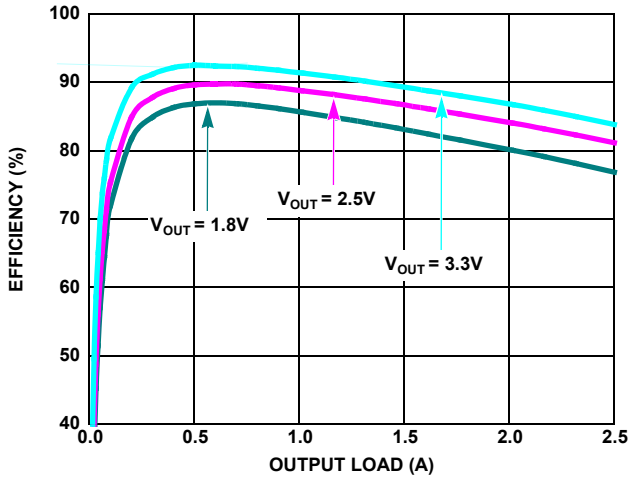


FIGURE 5. EFFICIENCY vs LOAD (V_{IN} = 5V)

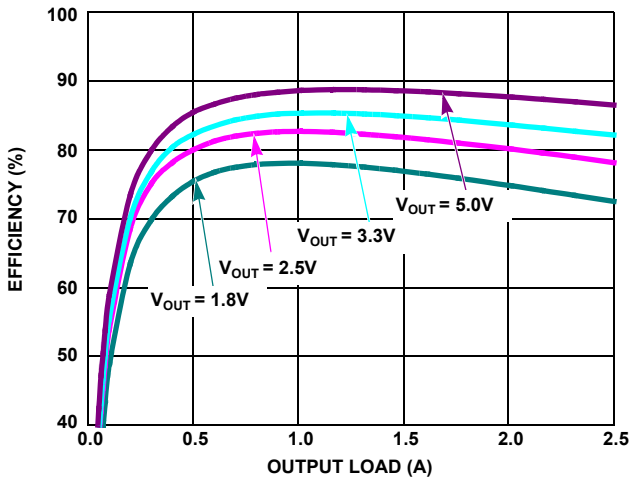


FIGURE 6. EFFICIENCY vs LOAD (V_{IN} = 12V)

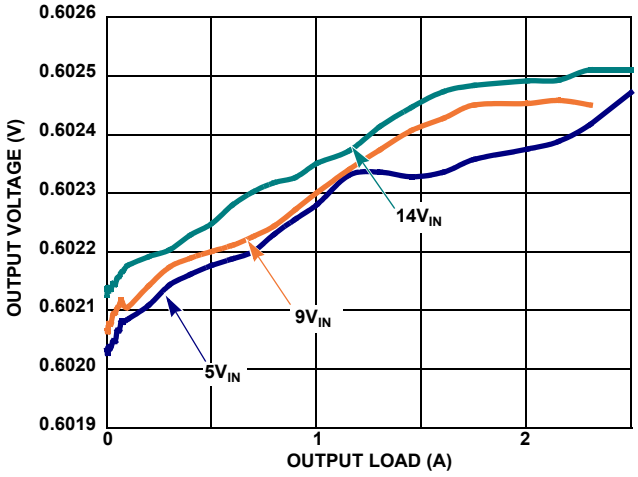


FIGURE 7. V_{OUT} REGULATION vs LOAD (V_{OUT} = 0.6V, 500kHz)

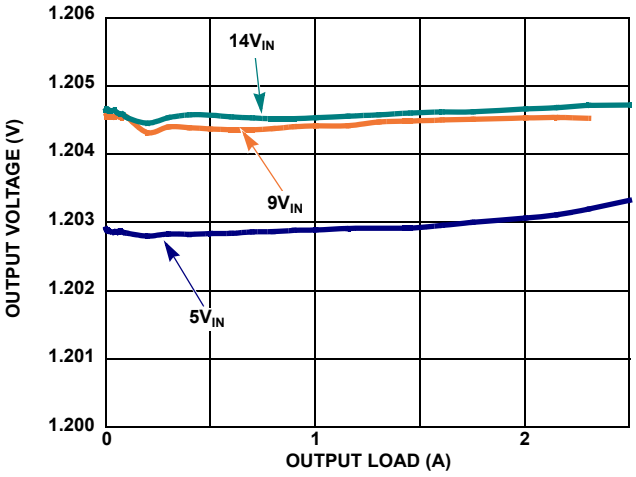


FIGURE 8. V_{OUT} REGULATION vs LOAD (V_{OUT} = 1.2V, 500kHz)

Typical Performance Curves

V_{IN} = 12V, V_{OUT} = 2.5V, I_O = 2A, f_{SW} = 500kHz, L = 4.7µH, C_{IN} = 20µF, C_{OUT} = 100µF + 22µF, T_A = +25° C, unless otherwise noted. **(Continued)**

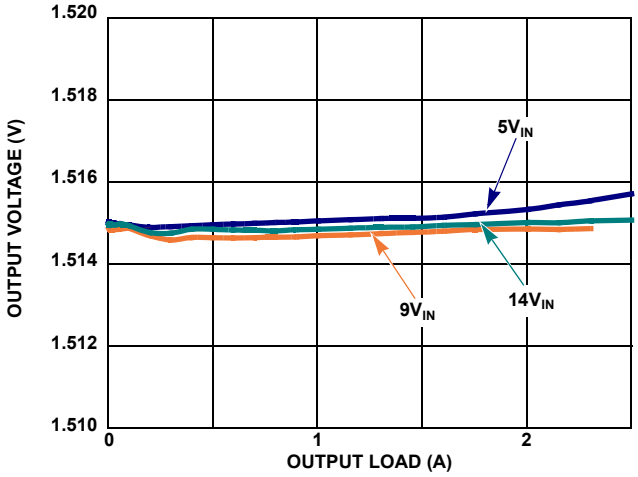


FIGURE 9. V_{OUT} REGULATION vs LOAD (V_{OUT} = 1.5V, 500kHz)

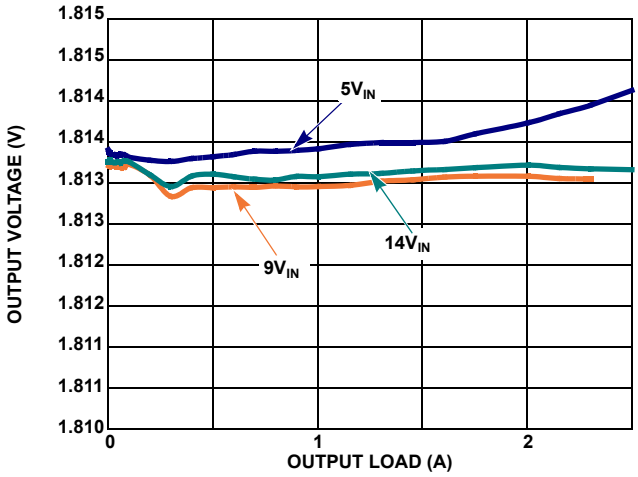


FIGURE 10. V_{OUT} REGULATION vs LOAD (V_{OUT} = 1.8V, 500kHz)

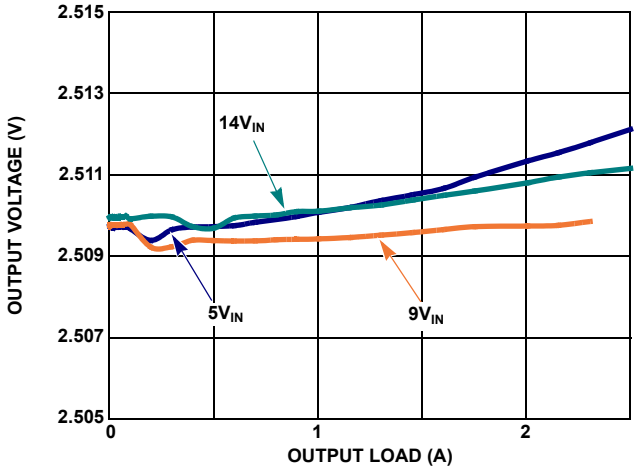


FIGURE 11. V_{OUT} REGULATION vs LOAD (V_{OUT} = 2.5V, 500kHz)

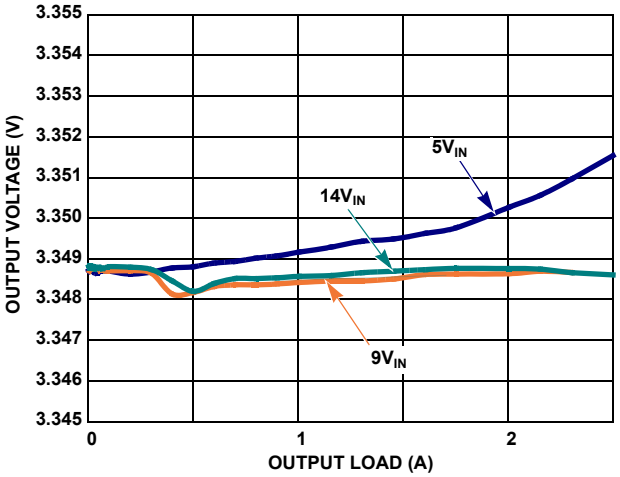


FIGURE 12. V_{OUT} REGULATION vs LOAD (V_{OUT} = 3.3V, 500kHz)

Typical Performance Curves

V_{IN} = 12V, V_{OUT} = 2.5V, I_O = 2A, f_{SW} = 500kHz, L = 4.7µH, C_{IN} = 20µF, C_{OUT} = 100µF + 22µF, T_A = +25° C, unless otherwise noted. **(Continued)**

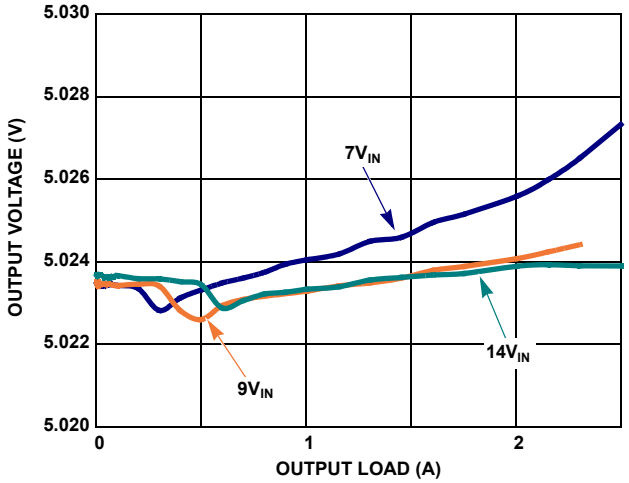


FIGURE 13. V_{OUT} REGULATION vs LOAD (V_{OUT} = 5V, 500kHz)

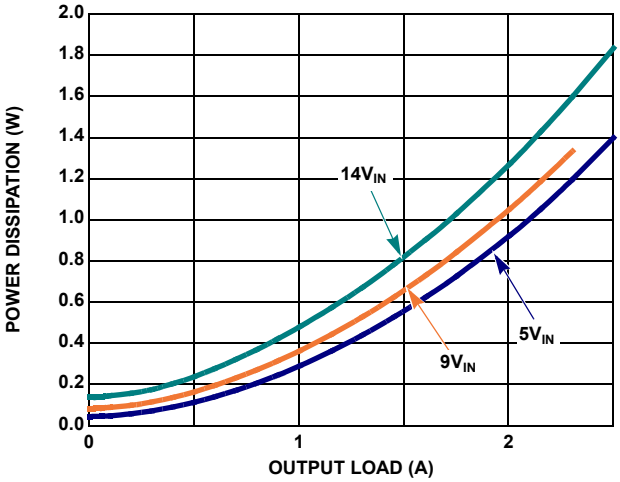


FIGURE 14. POWER DISSIPATION vs LOAD (V_{OUT} = 0.6V, 500kHz)

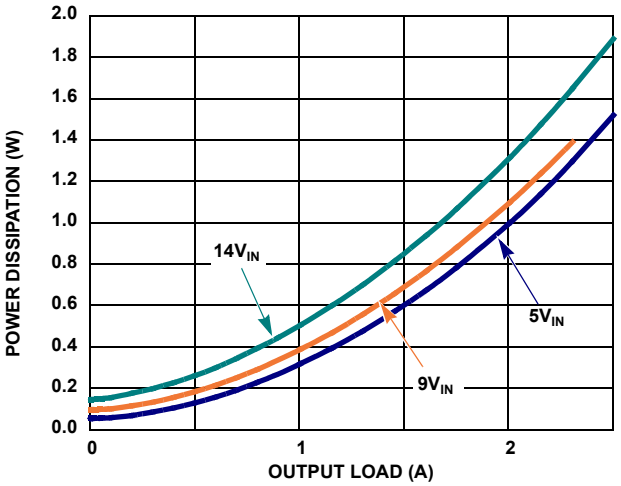


FIGURE 15. POWER DISSIPATION vs LOAD (V_{OUT} = 1.2V, 500kHz)

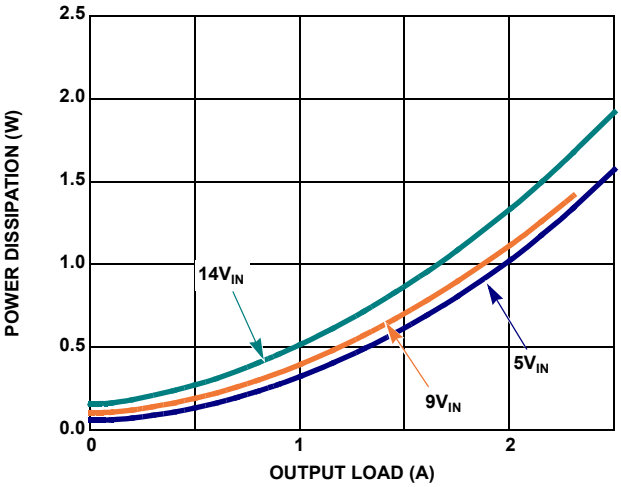


FIGURE 16. POWER DISSIPATION vs LOAD (V_{OUT} = 1.5V, 500kHz)

Typical Performance Curves

V_{IN} = 12V, V_{OUT} = 2.5V, I_O = 2A, f_{SW} = 500kHz, L = 4.7µH, C_{IN} = 20µF, C_{OUT} = 100µF + 22µF, T_A = +25° C, unless otherwise noted. **(Continued)**

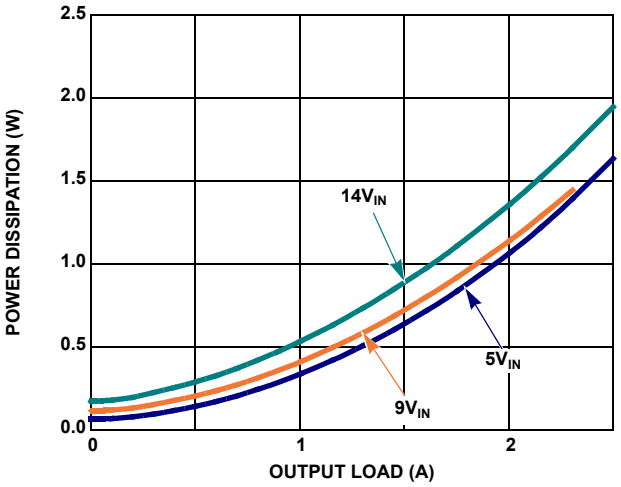


FIGURE 17. POWER DISSIPATION vs LOAD (V_{OUT} = 1.8V, 500kHz)

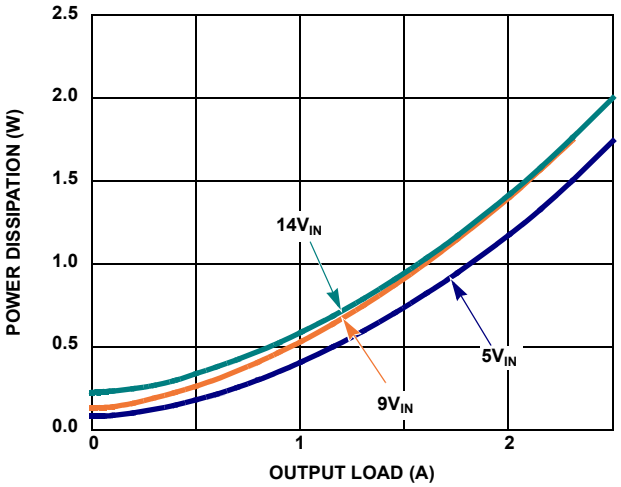


FIGURE 18. POWER DISSIPATION vs LOAD (VOUT = 2.5V, 500kHz)

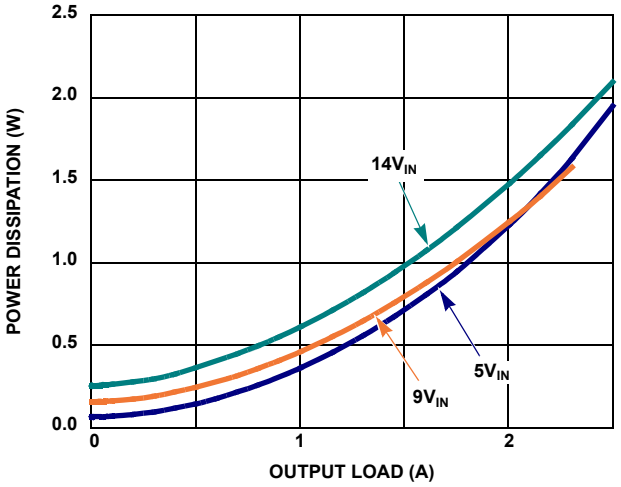


FIGURE 19. POWER DISSIPATION vs LOAD (V_{OUT} = 3.3V, 500kHz)

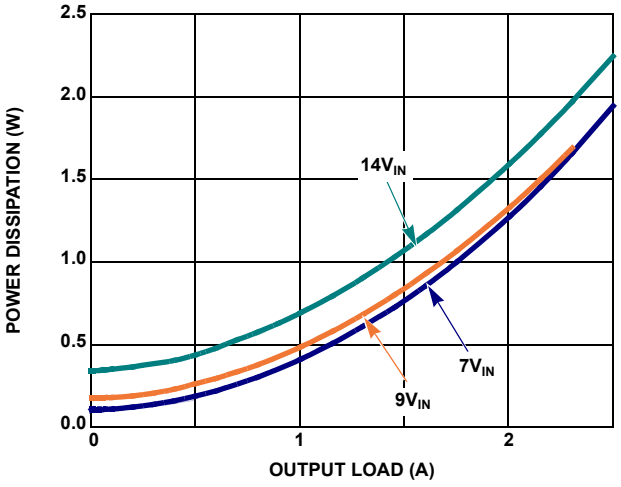


FIGURE 20. POWER DISSIPATION vs LOAD (V_{OUT} = 5V, 500kHz)

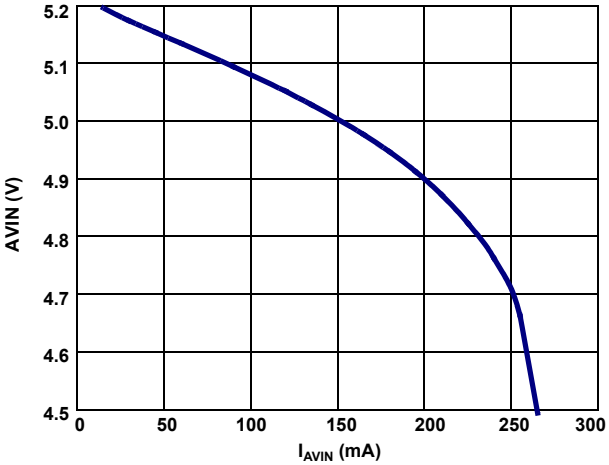


FIGURE 21. V_{AVIN} LOAD REGULATION

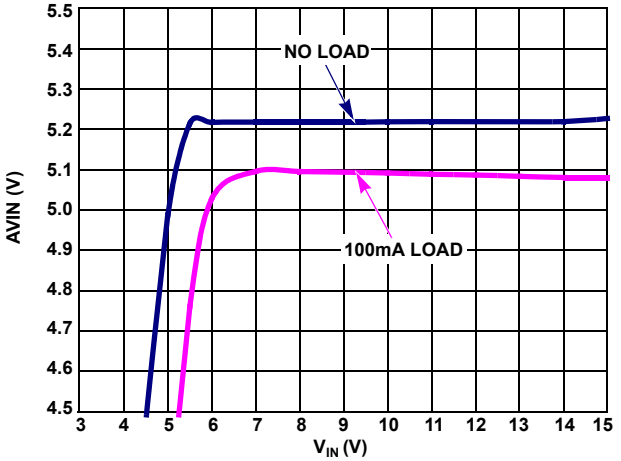


FIGURE 22. V_{AVIN} REGULATION vs V_{IN}

Typical Performance Curves

V_{IN} = 12V, V_{OUT} = 2.5V, I_O = 2A, f_{SW} = 500kHz, L = 4.7µH, C_{IN} = 20µF, C_{OUT} = 100µF + 22µF, T_A = +25° C, unless otherwise noted. **(Continued)**

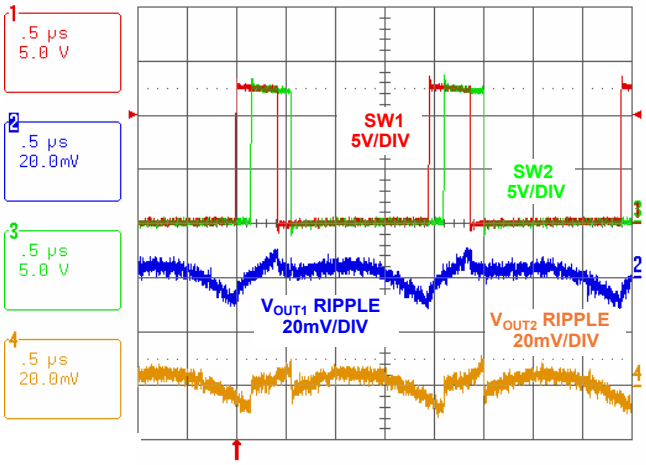


FIGURE 23. MASTER TO SLAVE OPERATION

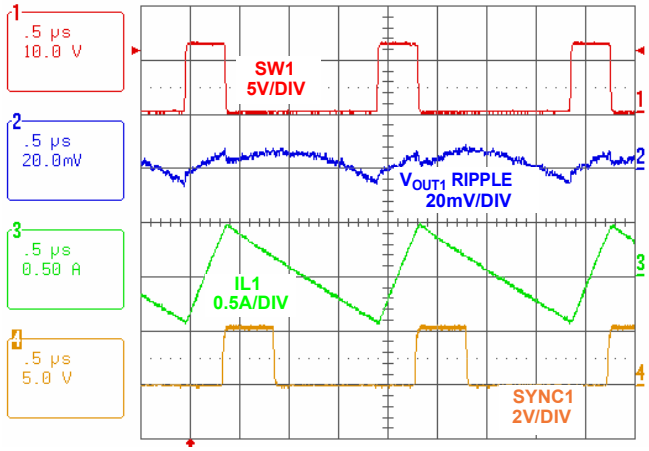


FIGURE 24. MASTER OPERATION AT NO LOAD

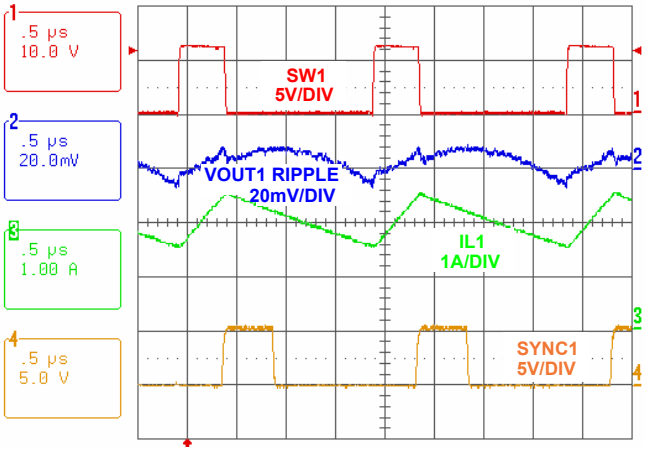


FIGURE 25. MASTER OPERATION WITH FULL LOAD

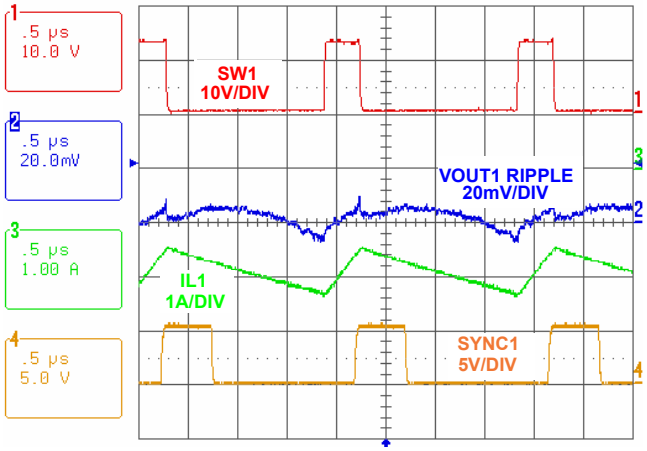


FIGURE 26. MASTER OPERATION WITH NEGATIVE LOAD

Typical Performance Curves

V_{IN} = 12V, V_{OUT} = 2.5V, I_O = 2A, f_{SW} = 500kHz, L = 4.7µH, C_{IN} = 20µF, C_{OUT} = 100µF + 22µF, T_A = +25° C, unless otherwise noted. **(Continued)**

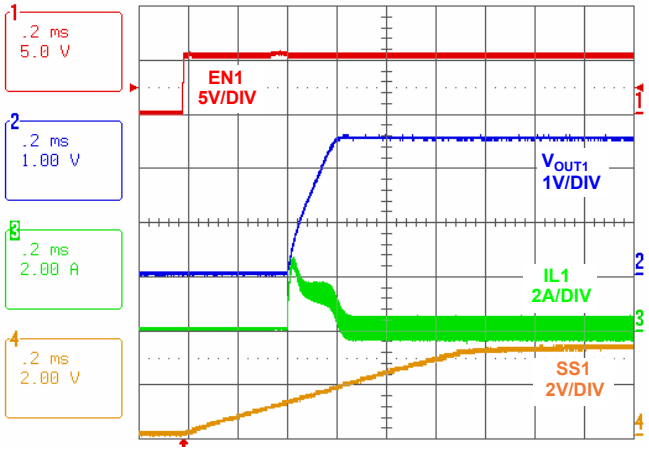


FIGURE 27. SOFT-START AT NO LOAD

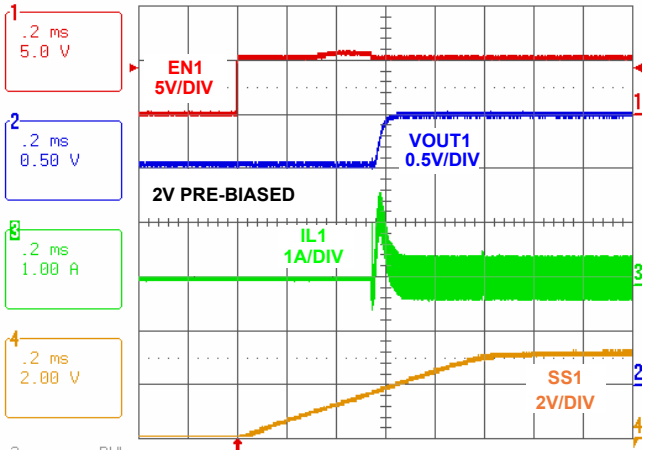


FIGURE 28. START-UP WITH PRE-BIASED

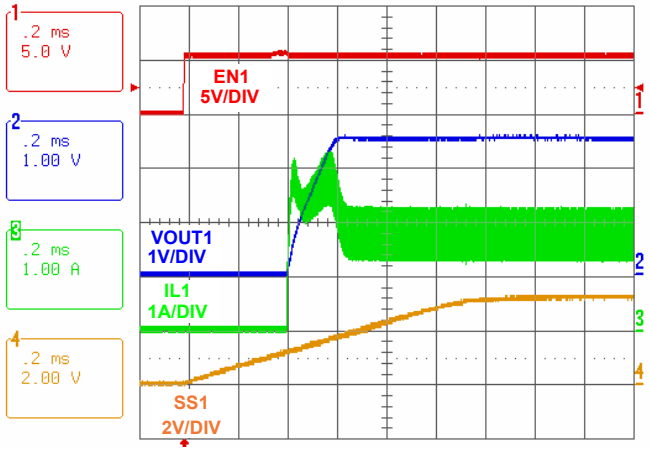


FIGURE 29. SOFT-START AT FULL LOAD

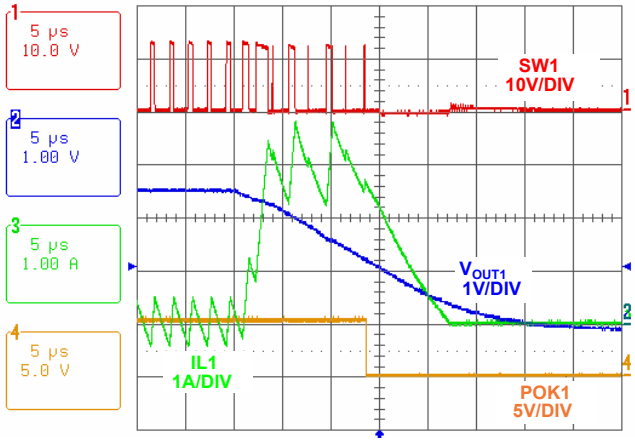


FIGURE 30. POSITIVE OUTPUT SHORT CIRCUIT

Typical Performance Curves

V_{IN} = 12V, V_{OUT} = 2.5V, I_O = 2A, f_{SW} = 500kHz, L = 4.7µH, C_{IN} = 20µF, C_{OUT} = 100µF + 22µF, T_A = +25° C, unless otherwise noted. **(Continued)**

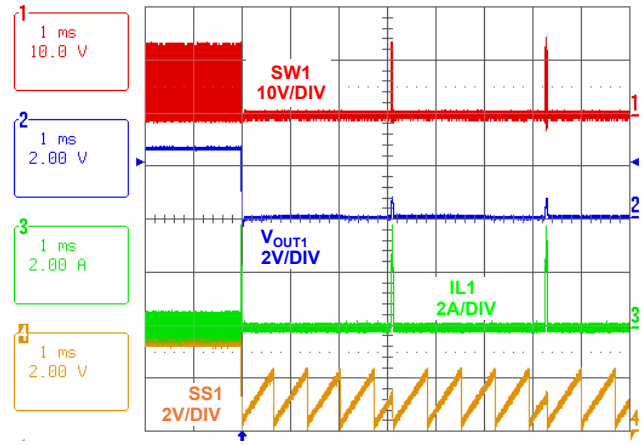


FIGURE 31. POSITIVE OUTPUT SHORT CIRCUIT (HICCUP MODE)

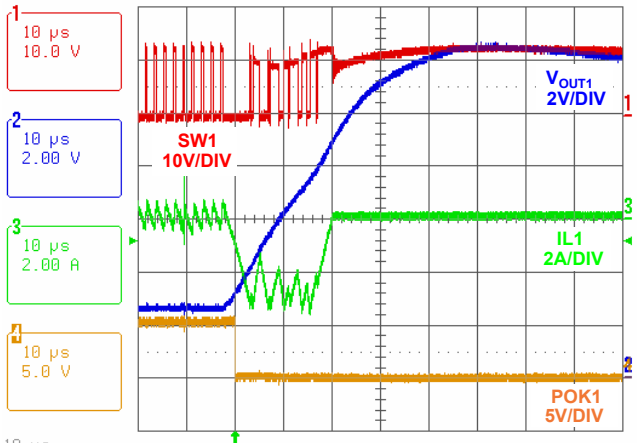


FIGURE 32. NEGATIVE OUTPUT SHORT CIRCUIT

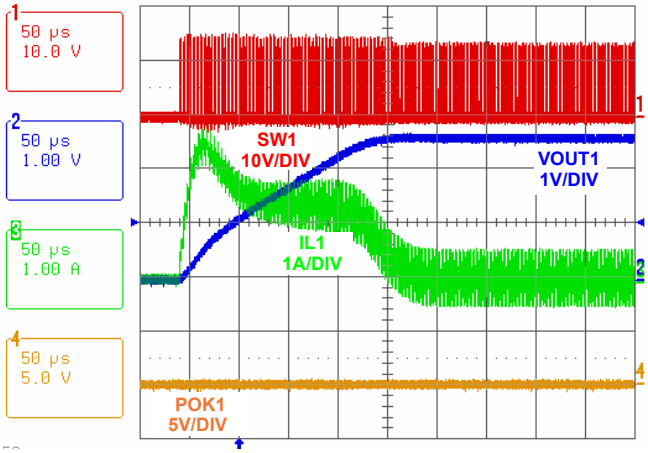


FIGURE 33. RECOVER FROM POSITIVE SHORT CIRCUIT

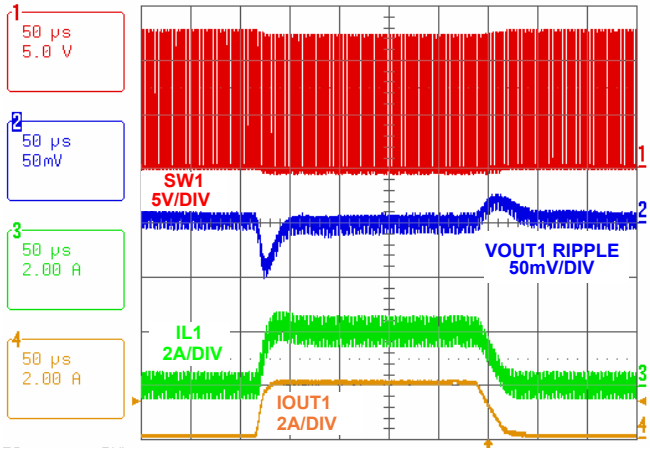


FIGURE 34. LOAD TRANSIENT

Functional Pin Descriptions

POK (Pin 1)

POK is an open drain output that pulls to low if the output goes out of regulation or a fault is detected. POK is equipped with a fixed delay upon output power-up. The POK Rising Delay specification is measured at 500 kHz from the point where V_{OUT} reaches regulation to the point where POK rises. This delay is reversely proportional to the switching frequency.

AGND (Pin 2)

The AGND terminal of the ER2120QI provides the return path for the control and monitor portions of the IC.

EN (Pin 3)

The Enable pin is a bi-directional pin. If the voltage on this pin exceeds the enable threshold voltage, the part is enabled. If a fault is detected, the EN pin is pulled low via internal circuitry for a duration of four soft-start periods. For automatic start-up, use 10kΩ to 100kΩ pull-up resistor connecting to AVIN.

SYNC (Pin 4)

SYNC is a bi-directional pin used to synchronize slave devices to the master device. As a master device, this pin outputs the clock signal to which the slave devices synchronize. As a slave device, this pin is an input to receive the clock signal from the master device.

If configured as a slave device, the ER2120QI is disabled if there is no clock signal from the master device on the SYNC pin.

Leave this pin unconnected if the IC is used in stand-alone operation.

M/S (Pin 5)

As a slave device, tie a 5kΩ resistor between the M/S pin and ground.

As a master or a stand-alone device, tie the M/S pin directly to the AVIN pin. Do not short the M/S pin to GND.

FSW (Pin 6)

The FSW pin provides oscillator switching frequency adjustment. By placing a resistor (R_T) from the FSW pin to GND, the switching frequency can be programmed as desired between 500kHz and 1.2MHz as shown in Equation 1.

$$R_T[k\Omega] = \frac{48000}{f_{OSC}[kHz]} \quad \textbf{(EQ. 1)}$$

Tying the FSW pin to the AVIN pin forces the switching frequency to 800kHz.

Using resistors with values below 40kΩ (1.2MHz) or with values higher than 97kΩ (500kHz) may damage the ER2120QI.

COMP (Pin 7) and FB (Pin 8)

The switching regulator employs a single voltage control loop. The FB pin is the negative input to the voltage loop error amplifier. The output voltage is set by an external resistor divider connected to FB. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. Loop compensation is achieved by connecting an AC network across the COMP pin and the FB pin. The FB pin is also monitored for undervoltage events.

SS (Pin 9)

Connect a capacitor from the SS pin to ground. This capacitor, along with an internal 30µA current source, sets the soft-start interval of the converter, t_{SS}, as shown in Equation 2.

$$C_{SS}[\mu F] = 50 \cdot t_{SS}[S] \quad \textbf{(EQ. 2)}$$

PGND (Pins 10-13)

The PGND pins are used as the ground connection of the power train.

SW (Pins 14-17)

The SW pins are the SW node connections to the inductor. These pins are connected to the source of the control MOSFET and the drain of the synchronous MOSFET.

PVIN (Pins 18-21)

Connect the input rail to the PVIN pins. These pins are the input to the regulator as well as the source for the internal linear regulator that supplies the bias for the IC.

It is recommended that the DC voltage applied to the PVIN pins does not exceed 14V. This recommendation allows for transient spikes and voltage ringing to occur while not exceeding Absolute Maximum Ratings.

BOOT (Pin 22)

The BOOT pin provides ground-referenced bias voltage to the upper MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive the internal N-channel MOSFET. The boot diode is included within the ER2120QI.

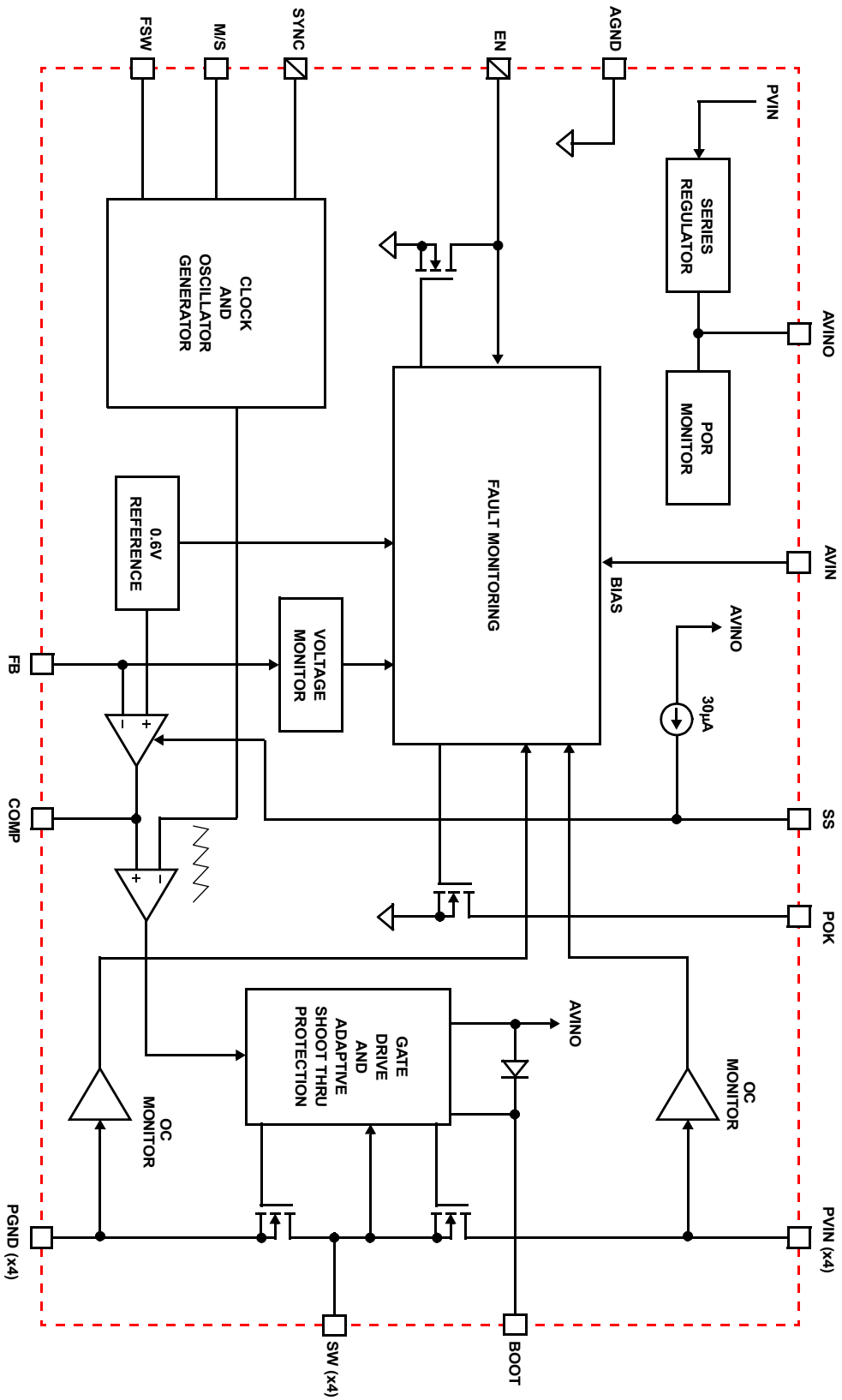
AVINO (Pin 23)

The AVINO pin is the output of the internal linear regulator that supplies the bias and gate voltage for the IC. A minimum 4.7µF decoupling capacitor is recommended.

AVIN (Pin 24)

The AVIN pin supplies the bias voltage for the IC. This pin should be tied to the AVINO pin through an RC low pass filter. A 10Ω resistor and 0.1µF capacitor are recommended.

Block Diagram



Functional Description

Initialization

The ER2120QI automatically initializes upon receipt of input power. The Power-On Reset (POR) function continuously monitors the voltage on the AVIN pin. If the voltage on the EN pin exceeds its rising threshold, then the POR function initiates soft-start operation after the bias voltage has exceeded the POR threshold.

Stand-alone Operation

The ER2120QI can be configured to function as a stand-alone single channel voltage mode synchronous buck PWM voltage regulator. The “Typical Application Schematics” on page 3 show the two configurations for stand-alone operation.

The internal series linear regulator requires at least 5.5V to create the proper bias for the IC. If the input voltage is between 5.5V and 15V, simply connect the PVIN pins to the input rail, and the series linear regulator creates the bias for the IC. The AVIN pin should be tied to a capacitor for decoupling.

If the input voltage is 5V ±10%, then tie the PVIN pins and the AVIN pin to the input rail. The ER2120QI uses the 5V rail as the bias. A decoupling capacitor should be placed as close as possible to the AVIN pin.

Multi-Channel (Master/Slave) Operation

The ER2120QI can be configured to function in a multi-channel system. “ER2120QI With Multiple Slaved Channels” on page 4 shows a typical configuration for the multi-channel system.

In the multi-channel system, each ER2120QI IC regulates a separate rail while sharing the same input rail. By configuring the devices in a master/slave configuration, the clocks of each IC can be synchronized.

There can only be one master IC in a multi-channel system. To configure an IC as the master, the M/S pin must be shorted to the AVIN pin. The SYNC pins of all the ER2120QI controller ICs in the multi-channel system must be tied together. The frequency set resistor value (R_T) used on the master device must be used on every slave device. Each slave device must have a 5kΩ resistor connecting it from M/S pin to ground.

The master device and all slave devices can have their EN pins tied to an enable “bus.” Since the EN pin is bi-directional, it allows for options on how each IC is tied to the enable bus. If the EN pin of any ER2120QI is tied directly to the enable bus, then that device is capable of disabling all the other devices that have their EN pins tied directly to the enable bus. If the EN pin of an ER2120QI is tied to the enable bus through a diode (anode tied to ER2120QI EN pin, cathode tied to enable bus), then the part does not disable other devices on the enable bus if it disables itself for any reason.

If the master device is disabled via the EN pin, it continues to send the clock signal from the SYNC pin. This allows slave devices to continue operating.

Fault Protection

The ER2120QI monitors the output of the regulator for overcurrent and undervoltage events. The ER2120QI also provides protection from excessive junction temperatures.

OVERCURRENT PROTECTION

The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through both the upper and lower MOSFETs.

Upon detection of any overcurrent condition, the upper MOSFET is immediately turned off and is not turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the Overcurrent Fault Counter is set to 1, and the Overcurrent Condition Flag is set from LOW to HIGH. If, on the subsequent cycle, another overcurrent condition is detected, the OC Fault Counter is incremented. If there are eight sequential OC fault detections, the regulator is shut down under an Overcurrent Fault Condition, and the EN pin is pulled LOW. An Overcurrent Fault Condition results, with the regulator attempting to restart in hiccup mode. The delay between restarts is four soft-start periods. At the end of the fourth soft-start wait period, the fault counters are reset, the EN pin is released, and soft-start is attempted again. If the overcurrent condition goes away prior to the OC Fault Counter reaching a count of four, the Overcurrent Condition Flag is set back to LOW.

If the Overcurrent Condition Flag is HIGH, the Overcurrent Fault Counter is less than four, and an undervoltage event is detected, the regulator shuts down immediately.

UNDERVOLTAGE PROTECTION

If the voltage detected on the FB pin falls 18% below the internal reference voltage, and if the overcurrent condition flag is LOW, then the regulator is shut down immediately under an Undervoltage Fault Condition, and the EN pin is pulled LOW. An Undervoltage Fault Condition results in the regulator attempting to restart in hiccup mode, with the delay between restarts being four soft-start periods. At the end of the fourth soft-start wait period, the fault counters are reset, the EN pin is released, and soft-start is attempted again.

THERMAL PROTECTION

If the ER2120QI IC junction temperature reaches a nominal temperature of +150°C, the regulator is disabled. The ER2120QI does not re-enable the regulator until the junction temperature drops below +130°C.

SHOOT-THROUGH PROTECTION

A shoot-through condition occurs when both the upper and lower MOSFETs are turned on simultaneously, effectively shorting the input voltage to ground. To protect from a shoot-through condition, the ER2120QI incorporates specialized circuitry, which ensures that the complementary MOSFETs are not ON simultaneously.

Application Guidelines

Operating Frequency

The ER2120QI can operate at switching frequencies from 500kHz to 1.2MHz. A resistor tied from the FSW pin to ground is used to program the switching frequency (Equation 3).

$$R_T[k\Omega] = \frac{48000}{f_{OSC}[kHz]} \quad \textbf{(EQ. 3)}$$

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier (see Figure 36).

The output voltage programming resistor, R_4, depends on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor is typically between 1kΩ and 10kΩ.

$$R_4 = \frac{R_1 \times 0.6V}{V_{OUT} - 0.6V} \quad \textbf{(EQ. 4)}$$

If the output voltage desired is 0.6V, then R_4 is left unpopulated.

Output Capacitor Selection

An output capacitor is required to filter the inductor current and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

The shape of the output voltage waveform during a load transient that represents the worst-case loading conditions ultimately determines the number of output capacitors and their type. When this load transient is applied to the converter, most of the energy required by the load is initially delivered from the output capacitors. This is due to the finite amount of time required for the inductor current to slew up to the level of the output current required by the load. This phenomenon results in a temporary dip in the output voltage. At the very edge of the transient, the Equivalent Series Inductance (ESL) of each capacitor induces a spike that adds on top of the existing voltage drop due to the Equivalent Series Resistance (ESR).

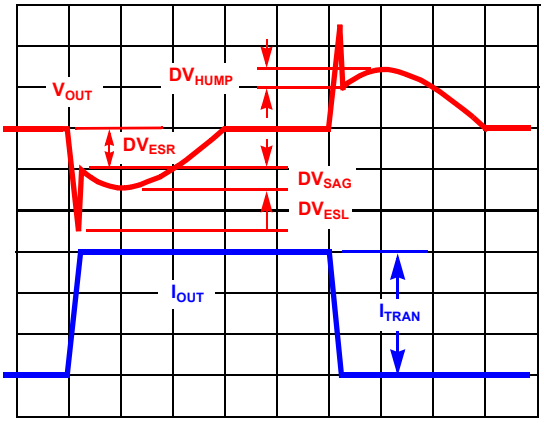


FIGURE 35. TYPICAL TRANSIENT RESPONSE

After the initial spike, attributable to the ESR and ESL of the capacitors, the output voltage experiences sag. This sag is a direct consequence of the amount of capacitance on the output.

During removal of the same output load, the energy stored in the inductor is dumped into the output capacitors. This energy dumping creates a temporary hump in the output voltage. This hump, as with the sag, can be attributed to the total amount of capacitance on the output. Figure 35 shows a typical response to a load transient.

The amplitudes of the different types of voltage excursions can be approximated using Equation 5.

$$\Delta V_{ESR} = ESR \bullet I_{tran} \qquad \Delta V_{ESL} = ESL \bullet \frac{dI_{tran}}{dt}$$

$$\Delta V_{SAG} = \frac{L_{out} \bullet I_{tran}^{2}}{C_{out} \bullet (V_{in} - V_{out})}$$

$$\Delta V_{HUMP} = \frac{L_{out} \bullet I_{tran}^{2}}{C_{out} \bullet V_{out}} \qquad \textbf{(EQ. 5)}$$

where: I_{tran} = Output Load Current Transient, and C_{out} = Total Output Capacitance.

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. The ESR and ESL typically are the major contributing factors in determining the output capacitance. The number of output capacitors can be determined by using Equation 6, which relates the ESR and ESL of the capacitors to the transient load step and the voltage limit (DVo):

$$\text{Number of Capacitors} = \frac{ESL \bullet \frac{dI_{tran}}{dt} + ESR \bullet I_{tran}}{\Delta V_{o}} \qquad \textbf{(EQ. 6)}$$

If DV_{SAG} or DV_{HUMP} is found to be too large for the output voltage limits, then the amount of capacitance may need to be increased. In this situation, a trade-off between output inductance and output capacitance may be necessary.

The ESL of the capacitors, which is an important parameter in the previous equations, is not usually listed in databooks. Practically, it can be approximated using Equation 7 if an Impedance vs Frequency curve is given for a specific capacitor:

$$ESL = \frac{1}{C(2 \bullet \pi \bullet f_{res})^{2}} \qquad \textbf{(EQ. 7)}$$

where f_{res} is the frequency at which the lowest impedance is achieved (resonant frequency).

The ESL of the capacitors becomes a concern when designing circuits that supply power to loads with high rates of change in the current.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and to minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current, and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by using Equation 8:

$$DI = \frac{VIN - VOUT}{F_{SW} \times L} \times \frac{VOUT}{VIN} \qquad DVOUT = DI \times ESR \qquad \text{(EQ. 8)}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter response time to a load transient.

One of the parameters limiting converter response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ER2120QI provides either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. Equation 9 gives the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{VIN - VOUT} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{VOUT} \qquad \text{(EQ. 9)}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst-case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst-case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high-frequency decoupling, and bulk capacitors to supply the current needed each time the upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of the upper MOSFET and the source of the lower MOSFET.

The important parameters for bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25x greater than the maximum input voltage, while a voltage rating of 1.5x is a conservative guideline. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately one-half the DC load current.

The maximum RMS current through the input capacitors can be closely approximated using Equation 10:

$$\sqrt{\frac{V_{OUT}}{V_{PVIN}} \times \left(I_{OUT_{MAX}}{}^2 \times \left(1 - \frac{V_{OUT}}{V_{PVIN}}\right) + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{L \times f_{OSC}} \times \frac{V_{OUT}}{V_{PVIN}} \right)^2 \right)} \qquad \text{(EQ. 10)}$$

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Feedback Compensation

Figure 36 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the reference voltage level. The error amplifier output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{PVIN} at the SW node. The PWM wave is smoothed by the output filter (L_O and C_O).

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC gain of the modulator is simply the input voltage (V_{PVIN}) divided by the
peak-to-peak oscillator voltage, DV_{OSC}. The ER2120QI incorporates a feed-forward loop that accounts for changes in the input voltage. This configuration maintains a constant modulator gain.

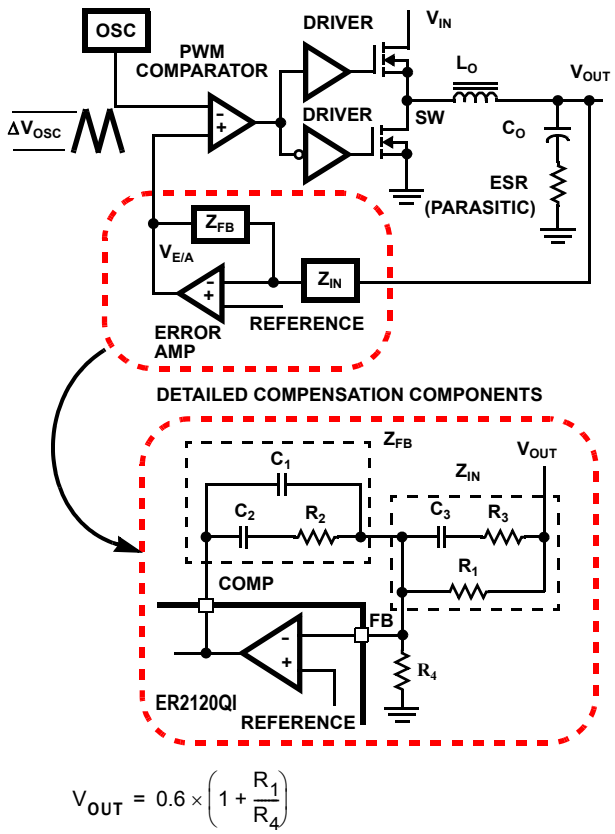


FIGURE 36. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN AND OUTPUT VOLTAGE SELECTION

Modulator Break Frequency Equations

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad f_{ESR} = \frac{1}{2\pi \times ESR \times C_O}$$

(EQ. 11)

The compensation network consists of the error amplifier (internal to the ER2120QI) and the impedance networks, Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. Equation 12 relates the compensation network's poles, zeros, and gain to the components (R_1, R_2, R_3, C_1, C_2 and C_3) in Figure 36. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R_2/R_1) for desired converter bandwidth.
2. Place first zero below filter's double pole (~75% F_{LC}).
3. Place second zero at filter's double pole.
4. Place first pole at ESR Zero.
5. Place second pole at half the switching frequency.
6. Check gain against error amplifier's open-loop gain.
7. Estimate phase margin; repeat if necessary.

Compensation Break Frequency Equations

$$f_{Z1} = \frac{1}{2\pi \times R_2 \times C_1} \qquad f_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$f_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad f_{P2} = \frac{1}{2\pi \times R_3 \times C_3}$$

(EQ. 12)

Figure 37 shows an asymptotic plot of the DC/DC converter gain vs frequency. The actual modulator gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 37. Using the guidelines provided should give a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The closed loop gain is constructed on the graph of Figure 37 by adding the modulator gain (in dB) to the compensation gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks, Z_{FB} and Z_{IN}, to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than +45°. Include worst-case component variations when determining phase margin.

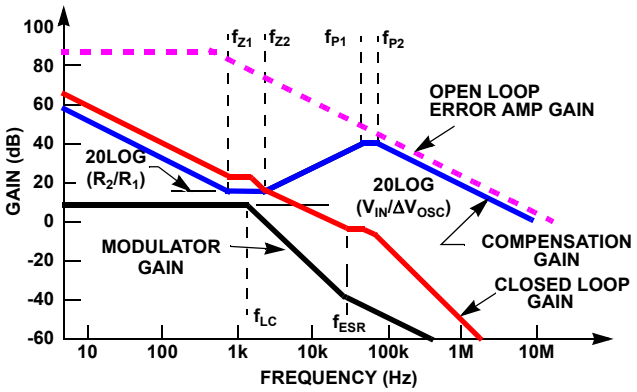


FIGURE 37. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently between 500kHz and 1.2MHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit board design minimize these voltage spikes.

As an example, consider the turn-off transition of the control MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the lower MOSFET. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide traces minimize the magnitude of voltage spikes.

There are two sets of critical components in the ER2120QI switching converter. The switching components are the most critical because they switch large amounts of energy and therefore tend to generate large amounts of noise. Next are the small signal components, which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 38 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer (usually a middle layer of the PC board) for a ground plane, and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane, and break this plane into smaller islands of common voltage levels. Keep the metal runs from the SW terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper-filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the GATE pins to the MOSFET gates should be kept short and wide enough to easily handle the 1A of drive current.

In order to dissipate heat generated by the internal V_{TT} LDO, the ground pad, pin 29, should be connected to the internal ground plane through at least five vias. This allows heat to move away from the IC and also ties the pad to the ground plane through a low impedance path.

The switching components should be placed close to the ER2120QI first. Minimize the length of connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between the upper and lower MOSFETs and the load. Make the PGND and the output capacitors as short as possible.

The critical small signal components include any bypass capacitors, feedback components, and compensation components. Place the PWM converter compensation components close to the FB and COMP pins. The feedback resistors should be located as close as possible to the FB pin, with vias tied straight to the ground plane as required.

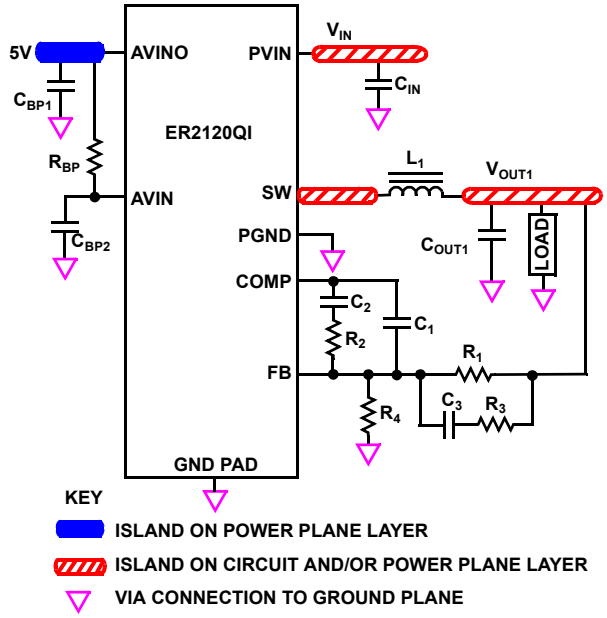


FIGURE 38. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Document Revision History

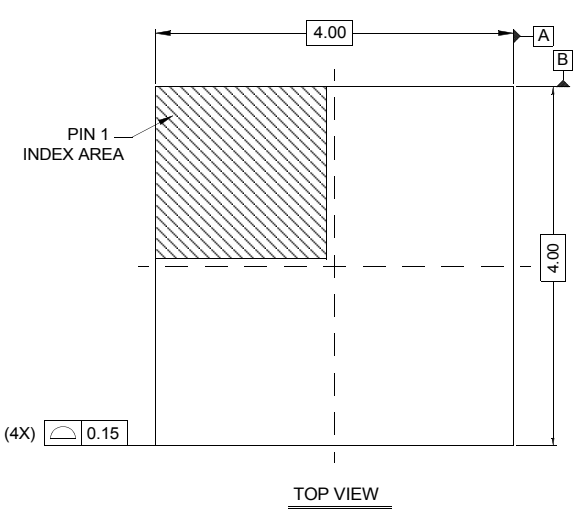
The table lists the revision history for this document.

Date	Version	Changes
March 2014	1.0	Initial release.

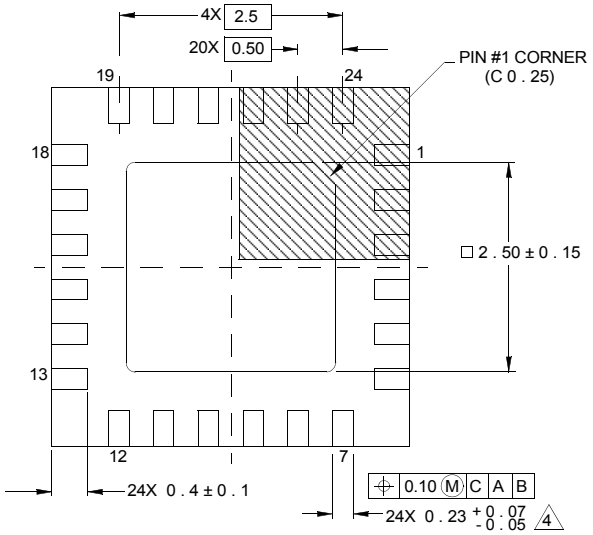
Package Outline Drawing

L24.4x4D

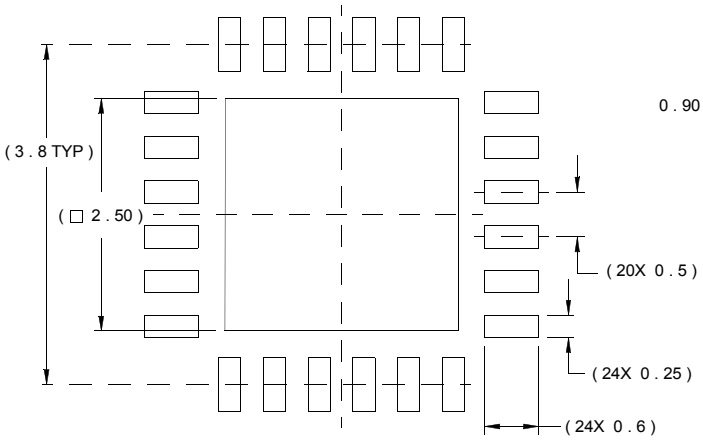
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE



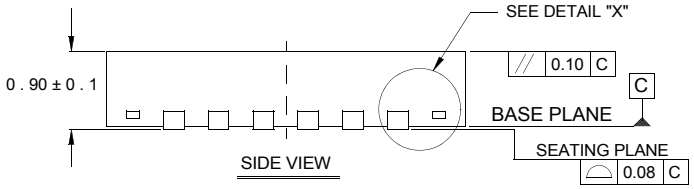
TOP VIEW



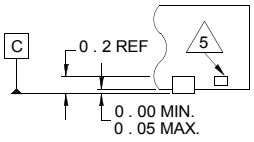
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.