

## DESCRIPTION

The MP5011 is a device designed to protect circuitry on the output (source) from transients on the input ( $V_{CC}$ ). It also protects the input from undesirable shorts and transients coming from the source.

At start up, the limited slew rate at the source limits the inrush current. A small capacitor at the dv/dt pin controls this slew rate. The dv/dt pin has an internal circuit that allows the customer to float this pin and still achieve a 1.4ms ramp time at the source.

The maximum load at the output is current-limited by using a sense MOSFET topology. An external resistor from the I-LIMIT pin to the source pin controls the magnitude of the current limit.

An internal charge pump drives the gate of the power device, allowing for the use of a DMOS power MOSFET with an ON resistance of just 44m $\Omega$ .

The device also includes protective features to protect the source against an input voltage that is outside the operating range.

## FEATURES

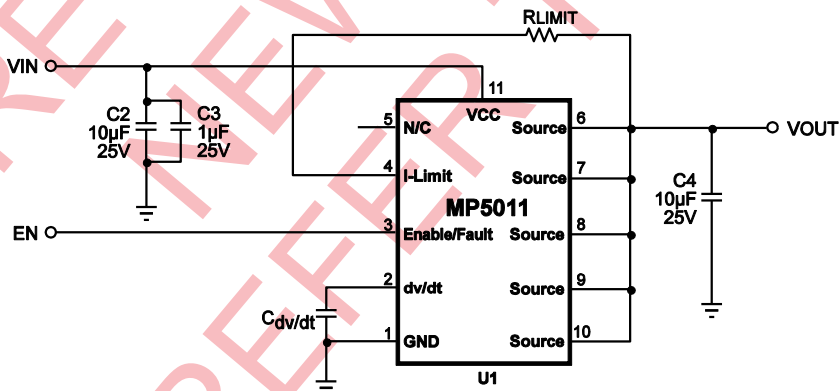
- Integrated 44m $\Omega$  Power MOSFET
- Enable/Fault Pin
- Adjustable Slew Rate for Output Voltage
- Adjustable Current Limit: 1A-5A
- Thermal Protection
- Over-Voltage Protection

## APPLICATIONS

- Hot Swap
- PC Cards
- Laptops

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## TYPICAL APPLICATION

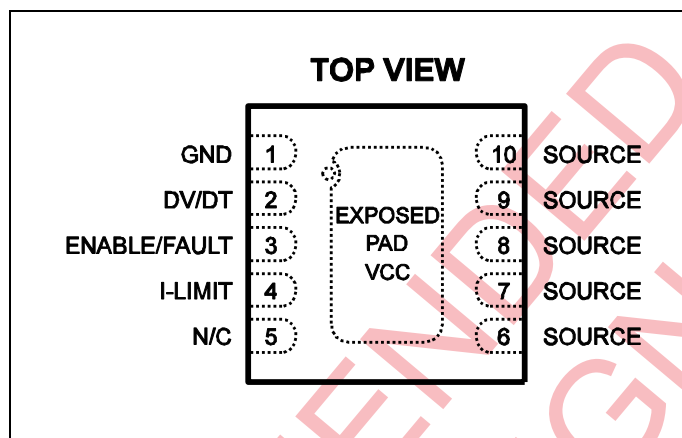


## ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5011DQ	QFN10 (3x3mm)	ACN

\* For Tape & Reel, add suffix -Z (e.g. MP5011DQ-Z);  
For RoHS Compliant Packaging, add suffix -LF (e.g. MP5011DQ-LF-Z)

## PACKAGE REFERENCE

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

$V_{CC}$ , SOURCE, I-LIMIT ..... -0.3V to 22V  
 $V_{CC}$ , SOURCE, I-LIMIT Transient (100ms) ... 25V  
 $dv/dt$ , ENABLE/FAULT ..... -0.3V to 6V  
 Storage Temperature ..... -65°C to +155°C  
 Continuous Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup>  
 ..... 2.5W  
 Operating Junction Temperature -40°C to 150°C

**Recommended Operating Conditions** <sup>(3)</sup>

Supply Voltage  $V_{IN}$  ..... 9V to 15V  
 Maximum Junction Temp. ( $T_J$ ) ..... 125°C

**Thermal Resistance** <sup>(4)</sup>  $\theta_{JA}$   $\theta_{JC}$ 

QFN10 (3x3mm) ..... 50 ..... 12 ... °C/W

**Notes:**

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J(\text{MAX})$ , the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7 4-layer board.

## ELECTRICAL CHARACTERISTICS

$V_{CC} = 12V$ ,  $R_{LIMIT}=15.4\Omega$ , Capacitive Load =  $100\mu F$ ,  $T_A=25^\circ C$ , unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power FET						
Delay Time	t <sub>DLY</sub>	Enabling of chip to I <sub>D</sub> =100mA with a 1A resistive load	0.1	0.15	0.2	ms
ON Resistance <sup>(5)</sup>	R <sub>DSon</sub>	T <sub>J</sub> =25°C		44	55	mΩ
		T <sub>J</sub> =80°C		52		
Off-State Output Voltage	V <sub>OFF</sub>	V <sub>CC</sub> =18Vdc, V <sub>ENABLE</sub> =0Vdc, R <sub>L</sub> = 500Ω			120	mV
Continuous Current	I <sub>D</sub>	0.5 in <sup>2</sup> pad,		4.2		A
		Minimum Copper, T <sub>A</sub> =80°C		2.3		
Thermal Latch						
Shutdown Temperature <sup>(5)</sup>	T <sub>SD</sub>		150	175	200	°C
Under/Over-Voltage Protection						
Output Clamping Voltage	V <sub>CLAMP</sub>	Overvoltage Protection V <sub>CC</sub> =17V	13.8	15	16.2	V
Under-Voltage Lockout	V <sub>UVLO</sub>	Turn on, Voltage going high	7.7	8.5	9.3	V
Under-Voltage Lockout Hysteresis	V <sub>HYST</sub>			0.80		V
Current Limit						
Hold Current <sup>(5)</sup>	I <sub>LIM-SS</sub>	R <sub>LIM</sub> =15.4Ω	3.8	4.5	5.2	A
Trip Current	I <sub>LIM-OL</sub>	R <sub>LIM</sub> =15.4Ω,		5.3		A
dv/dt Circuit						
Rise Time <sup>(6)</sup>	t <sub>r</sub>	Float dv/dt pin	0.8	1.4	2.0	ms
Enable/Fault						
Low Level Input Voltage	V <sub>IL</sub>	Output Disabled			0.5	V
Intermediate-Level Input Voltage	V <sub>I (INT)</sub>	Thermal Fault, Output Disabled	0.82	1.4	1.95	V
High-Level Input Voltage	V <sub>IH</sub>	Output Enabled	2.5			V
High-State Maximum Voltage	V <sub>I (MAX)</sub>			4.8		V
Low-Level Input Current (Sink)	I <sub>IL</sub>	V <sub>ENABLE</sub> =0V		-28	-50	μA
Maximum Fanout for Fault Signal		Total number of chips that can be connected for simultaneous shutdown			3	Units
Maximum Voltage on Enable/Fault Pin <sup>(7)</sup>	V <sub>MAX</sub>				VCC	V
Total Device						
Bias Current	I <sub>BIAS</sub>	Device Operational		1.5	2.0	mA
		Thermal Shutdown		0.4		
Minimum Operating Voltage for UVLO	V <sub>MIN</sub>	Enable<0.5V			5	V

## Notes:

5) Guaranteed by design.

6) Measured from 10% to 90%.

7) Maximum Input Voltage on Enable pin to be  $\leq 6.0V$  if  $V_{CC} \geq 6.0V$ , Maximum Input Voltage on Enable pin to be  $V_{CC}$  if  $V_{CC} \leq 6.0V$ .

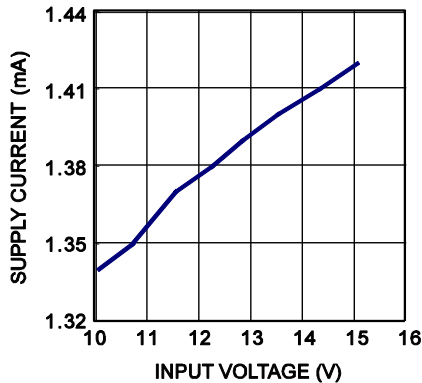
## PIN FUNCTIONS

Pin #	Name	Description
1	GND	Negative Input Voltage to the Device. This is used as the internal reference for the IC.
2	dv/dt	Slew Rate control. The internal dv/dt circuit controls the slew rate of the output voltage at turn-on. An internal capacitor allows the voltage to ramp up over 1.4ms. Use an external capacitor to increase the ramp time. If an additional time delay is not required, leave this pin open.
3	Enable/Fault	The Enable/Fault pin. A tri-state, bi-directional interface. It enables the output of the device when left floating, or disables the device when pulled to ground using an open-drain or open-collector device. In the event of a thermal fault, the voltage enters an intermediate state to signal a monitoring circuit that the device is in thermal shutdown. See text: "ENABLE/FAULT PIN".
4	I-Limit	Overload and Short-Circuit Current Set. Use a resistor between this pin and the Source pin to set the overload and short-circuit current limit levels.
5	NC	DO NOT CONNECT. Pin must be left floating.
6-10	SOURCE	Output. This pin is the source of the internal power FET and the output terminal of the IC.
Exposed Pad	V <sub>CC</sub>	Positive Input Voltage.

## TYPICAL PERFORMANCE CHARACTERISTICS

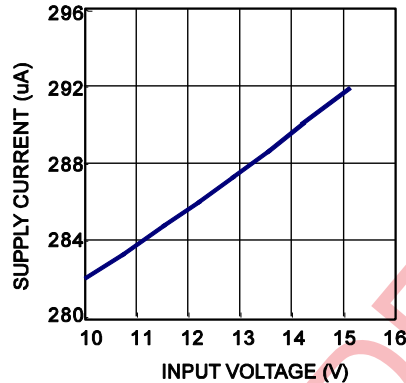
**Supply Current,  
Output Enabled vs.  
Input Voltage**

$V_{EN}=3.3V$ , no load



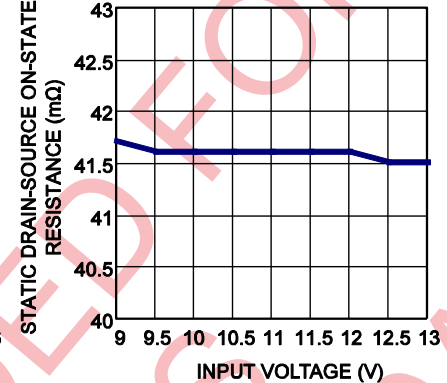
**Supply Current,  
Output Disabled vs.  
Input Voltage**

$V_{EN}=0V$

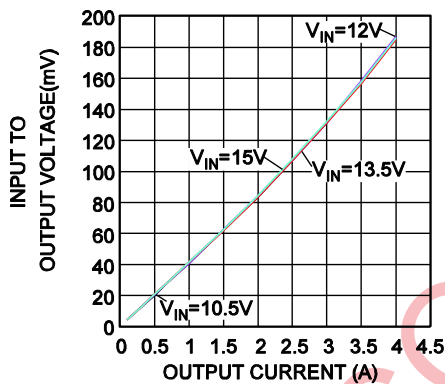


**Static Drain-Source  
On-State Resistance vs.  
Input Voltage**

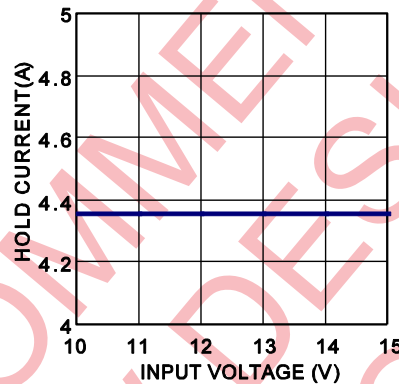
$I_{OUT}=1A$



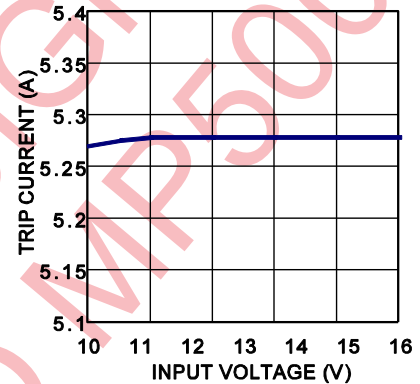
**Input to Output Voltage  
vs. Load Current**



**Hold Current vs.  
Input Voltage**

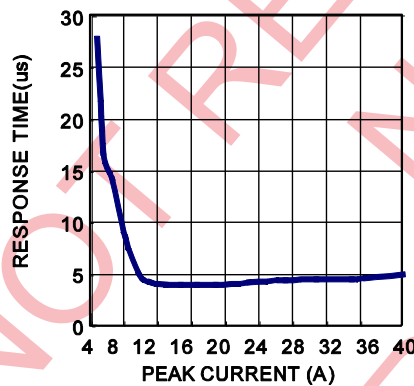


**Trip Current Vs.  
Input Voltage**

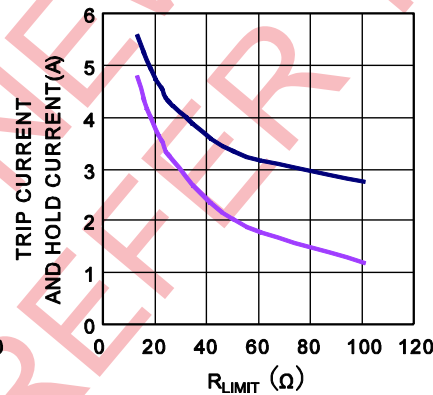


**Current Limit Response  
Vs. Peak Current**

no C<sub>OUT</sub>



**Trip Current  
and Hold Current vs.  
R<sub>LIMIT</sub>**

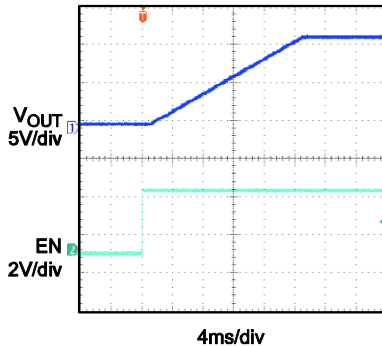


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$ ,  $V_{EN} = 3.3V$ ,  $R_{LIMIT} = 15.4\Omega$ ,  $C_{OUT} = 10\mu F$ ,  $C_{dv/dt} = 1nF$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

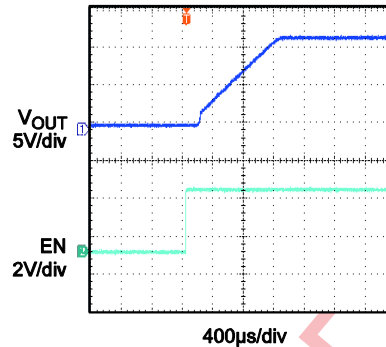
### Turn On Delay and Rise Time with 1 $\mu F$ Load

$C_{OUT} = 1\mu F$ , no load,  $C_{dv/dt} = 1nF$



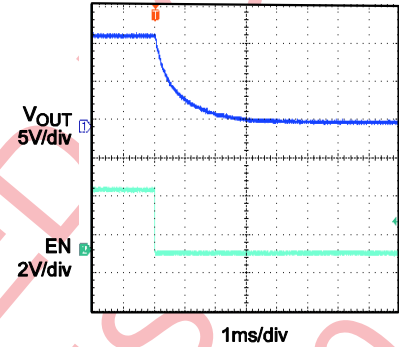
### Turn On Delay and Rise Time with 1 $\mu F$ Load

$C_{OUT} = 1\mu F$ , no load, no  $C_{dv/dt}$



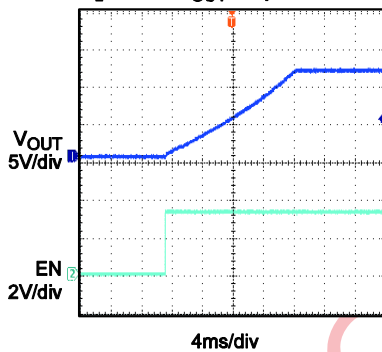
### Turn Off Delay and Fall Time with 1 $\mu F$ Load

$C_{OUT} = 1\mu F$ , no load,  $C_{dv/dt} = 1nF$



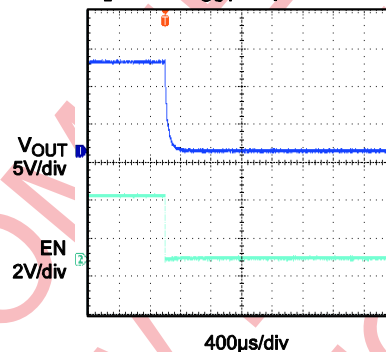
### Turn On Delay and Rise Time with 10 $\mu F$ Load

$R_L = 3.9\Omega$ ,  $C_{OUT} = 10\mu F$

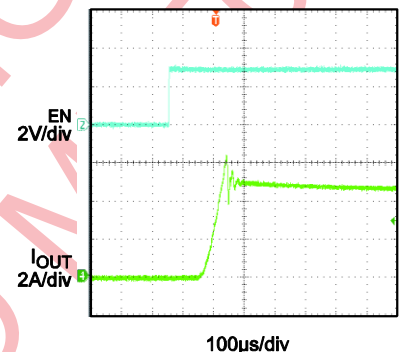


### Turn Off Delay and Fall Time with 10 $\mu F$ Load

$R_L = 3.9\Omega$ ,  $C_{OUT} = 10\mu F$

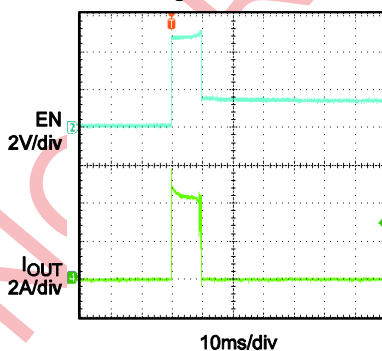


### Short Circuit Current Device Enabled into Short

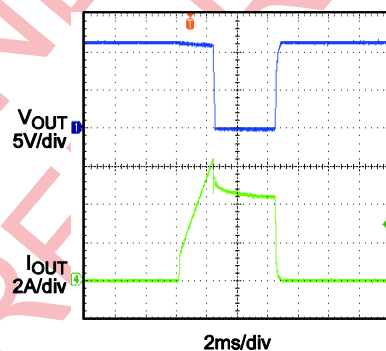


### Short Circuit Current Device Enabled into Short and Thermal Shut Down

EN floating

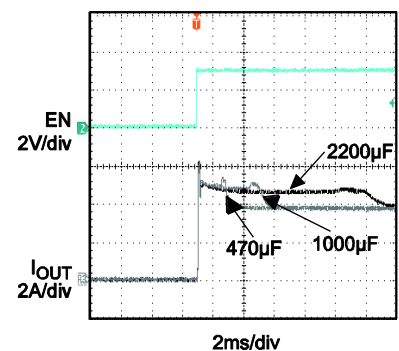


### Trip Current with Ramped Load on Enabled Device



### Inrush Current with Different Load Capacitance

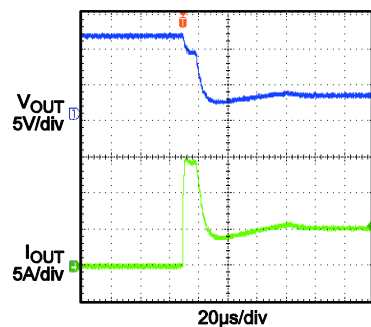
$R_L = 3\Omega$ , no  $C_{dv/dt}$ , EN floating



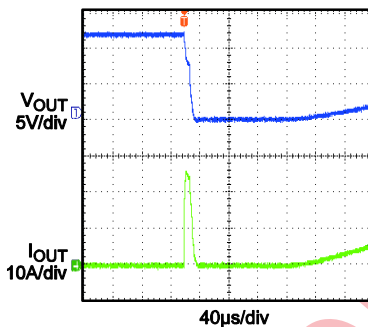
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$ ,  $V_{EN}=3.3V$ ,  $R_{LIMIT}=15.4\Omega$ ,  $C_{OUT}=10\mu F$ ,  $C_{dv/dt}=1nF$ ,  $T_A=25^\circ C$ , unless otherwise noted.

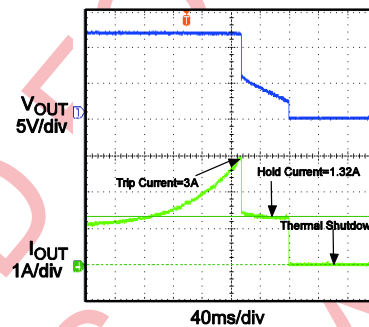
**0.66 $\Omega$  Load**  
Connected to Enabled Device



**0.33 $\Omega$  Load**  
Connected to Enabled Device



**Current Limit**  
 $R_{LIMIT}=100\Omega$





## BLOCK DIAGRAM

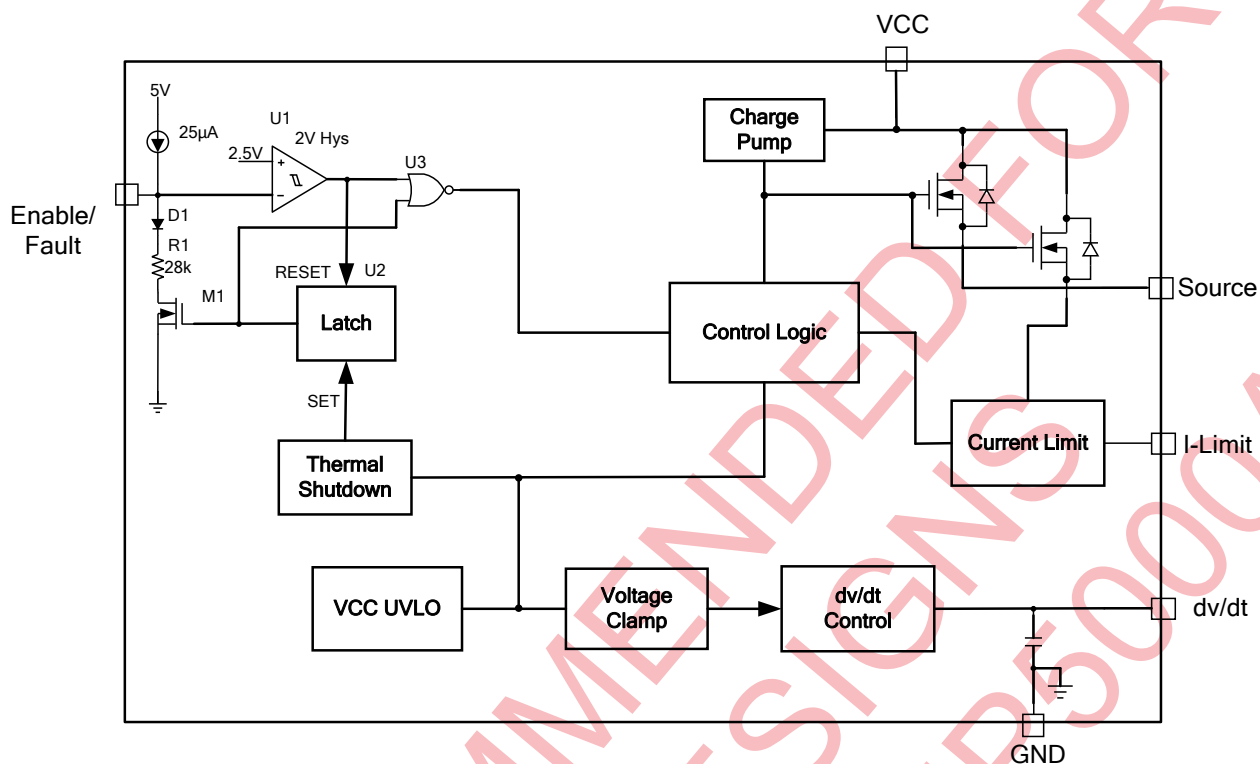


Figure 1: Functional Block Diagram



## OPERATION

### Current Limit

The current limit is a function of the external current limit resistor.

**Table 1: Current Limit vs. Current Limit Resistor (VCC=12V)**

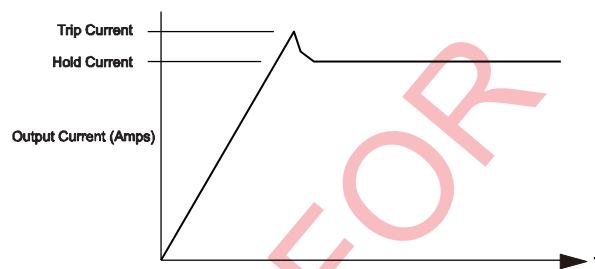
Current Limit Resistor ( $\Omega$ )	15.4	50	100
Trip Current (A)	5.3	3.4	2.8
Hold Current (A)	4.5	2.1	1.2

If a short is present or the load reaches the trip current—the minimum threshold current to trigger over-current protection (OCP)—when the part is active, the part switches into to a constant-current (hold) mode (CCM). The device shuts down only if the over-current condition remains for long enough to trigger thermal protection.

However, when the part is powered up by  $V_{CC}$  or EN, the load current should be smaller than the current. Otherwise, the part will not completely turn on.

In a typical application using a current limit resistor of  $15.4\Omega$ , the trip current is 5.3A and the hold current is 4.5A. If the device is in its normal operating state and passing 2.0A it will need to dissipate only 176mW with a very low ON resistance of  $44m\Omega$ . For a package dissipation of  $50^\circ\text{C}/\text{Watt}$ , the temperature rise will only be  $+9^\circ\text{C}$ ; with  $25^\circ\text{C}$  ambient temperature, this amounts to a total package temperature of  $34^\circ\text{C}$ .

In the case of a short-circuit condition, the device now has 12V across it and the hold current clamps at 4.5A and therefore must dissipate 44W. At  $50^\circ\text{C}/\text{watt}$ , the temperature rises above the MP5011 thermal protection ( $175^\circ\text{C}$ ) if left unchecked and device shutdown allows the temperature to drop below a hysteresis level. Use an appropriate heat sink if the device is intended to supply the hold current and not shutdown. Without a heat sink, maintain the hold current below 250mA at  $25^\circ\text{C}$  and below 150mA at  $85^\circ\text{C}$  to prevent the device from activating the thermal shutdown feature.



**Figure 2**

### Rise Time

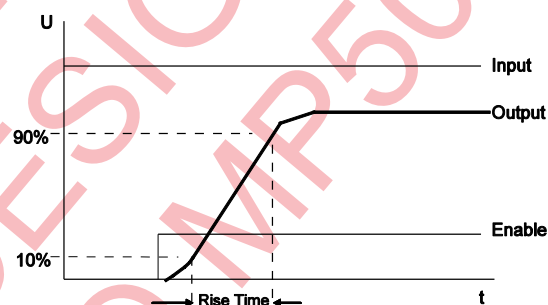
The rise time is a function of the capacitor ( $C_{dv/dt}$ ) on the  $dv/dt$  pin.

**Table 2: Rise Time vs.  $C_{dv/dt}$**

$C_{dv/dt}$	None	33pF	470pF	1nF
Rise Time (Typ) (ms)	1.4	2.0	11.6	22.5

\* Notes: Rise Time =  $K_{RT} \cdot (50pF + C_{dv/dt})$ ,  $K_{RT} = 22E6$

The rise time is measured by from 10% to 90% of output voltage.



**Figure 3**

### Enable / Fault Pin

The Enable/Fault pin is a bi-directional, three-level I/O with a weak pull-up current (typically  $25\mu\text{A}$ ). There are three levels: low, mid, and high. It enables/disables the part and relays fault information.

When the Enable/Fault pin is an input:

1. Low and mid levels disable the part.
2. Low clears the fault flag in addition to disabling the part.
3. High enables the part (if the fault flag is clear).

When the Enable/Fault pin is an output:

1. The pull-up current (if not overridden) allows for a “wired NOR” pull up to enable the part.
2. An under-voltage causes a low on the Enable/Fault pin, and clears the fault flag. A thermal fault causes a mid level on the Enable/Fault pin, and sets the fault flag.

The Enable/Fault line must be above the mid level for the output to be turned on.

The fault flag is an internal flip-flop that can be set or reset under various conditions:

1. Thermal Shutdown: set fault flag
2. Under-Voltage: reset fault flag

3. Low Voltage on Enable/Fault Pin: reset fault flag
4. Mid Voltage on Enable/Fault Pin: no effect

Under a fault, the Enable/Fault pin goes to the mid level.

There are four types of faults, and each fault has a direct and indirect effect on the Enable/Fault pin and the internal fault flag.

In a typical application there are one or more MP5011 chips in a system. Typically, tie the Enable/Fault lines together.

**Table 3: Fault Function Influence in Application**

Fault description	Internal action	Effect on Fault Pin	Effect on Flag	Effect on secondary Part
Short/Over Current	Limit current	none	None	none
Under-Voltage	Output turns off	Internally drives Enable/Fault pin to Logic low	Flag resets	Secondary part output disabled, and fault flag resets.
Over-Voltage	Limit output voltage	None	None	None
Thermal Shutdown	Shutdown part. The part is latched off until a UVLO or externally driven to ground.	Internally drives Enable/Fault pin to mid level	Flag sets	Secondary-part output disabled.

### Under-Voltage Lockout Operation

If the supply (input) is below the UVLO threshold, the output is disabled, and the fault line is driven low.

When the supply goes above the UVLO threshold, the output is enabled and the fault line releases. When the fault line releases, a 25μA current source pulls it high without the need for an external pull up resistor. The pull-up voltage has a 5V limit.

### Thermal Protection

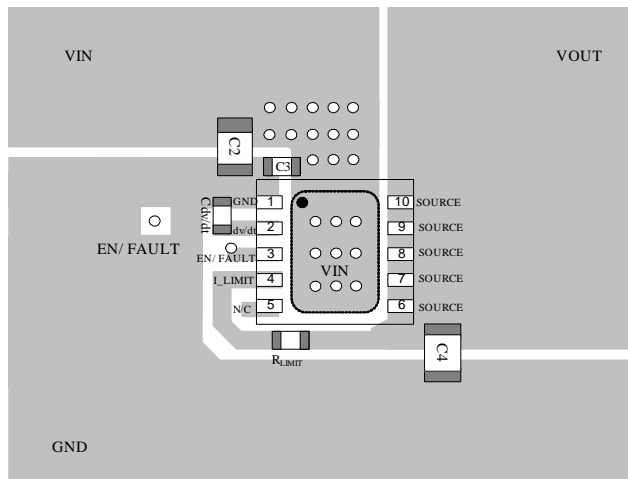
In the presence of a thermal protection fault, the output is disabled and the fault line is driven to the mid level. The thermal fault condition latches—the fault flag is set—and the part remains latched off until the fault (enable) line goes low. Cycling the power below the UVLO threshold also resets the fault flag.

## PCB LAYOUT

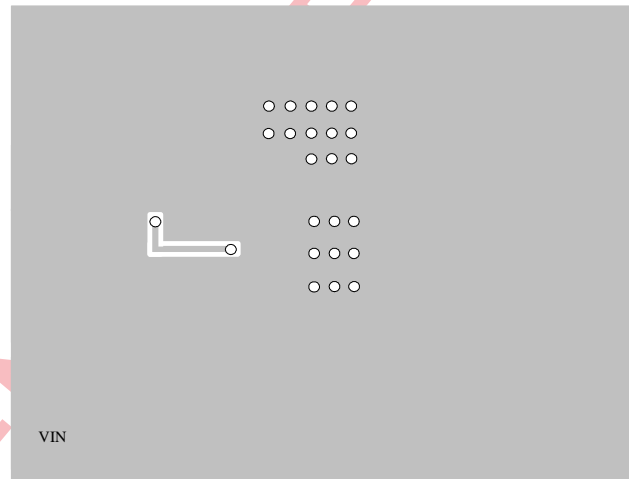
Please follow these guidelines use Figure 4 below figure reference to design for stable operation:

- Place  $R_{\text{limit}}$  close to the  $I_{\text{Limit}}$  pin,  $C_{\text{dv/dt}}$  close to the dv/dt pin and the input capacitor close to the  $V_{\text{CC}}$  pin.

- Float the NC pin.
- Add vias for the thermal pad and use large copper surfaces for  $V_{\text{CC}}$  and source to achieve better thermal performance.



**Top Layer**

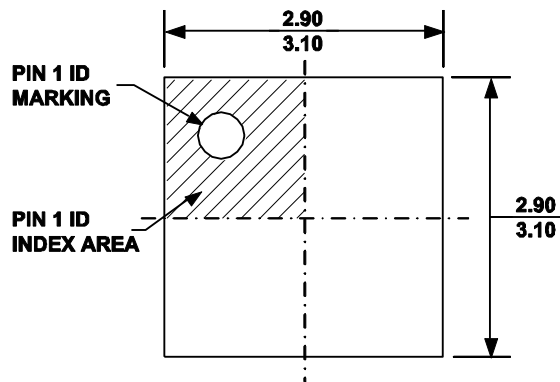


**Bottom Layer**

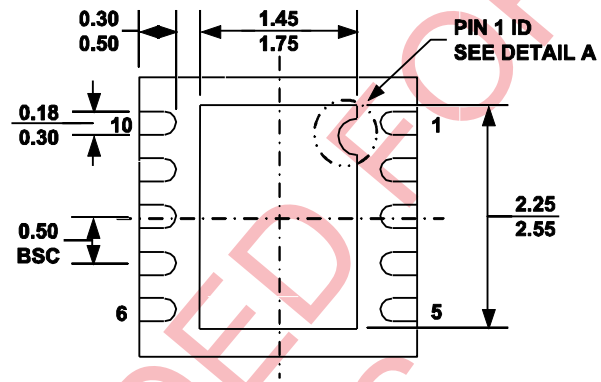
**Figure 4: PCB Layout**

## PACKAGE INFORMATION

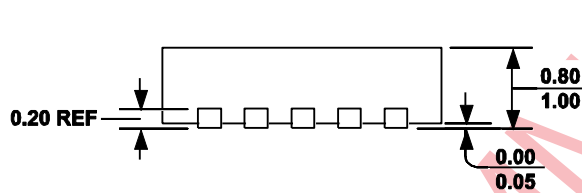
### QFN10 (3 x 3mm)



**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**

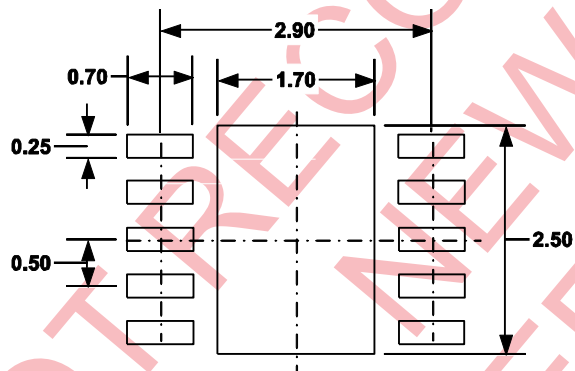
**PIN 1 ID OPTION A  
R0.20 TYP.**



**PIN 1 ID OPTION B  
R0.20 TYP.**



**DETAIL A**



**RECOMMENDED LAND PATTERN**

#### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
- 5) DRAWING IS NOT TO SCALE.

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