LM95214 Quad Remote Diode and Local Temperature Sensor With SMBus Interface

1 Features

- Accurately Senses Die Temperature of 4 Remote ICs or Diode Junctions and Local Temperature
- Local Temperature Accuracy ±2.0°C (Maximum)
- Remote Diode Temperature Accuracy ±1.1°C (Maximum)
- Supply Voltage: 3 V to 3.6 V
- Average Supply Current (1-Hz Conversion Rate) 0.57 mA (Typical)
- Programmable Digital Filters and Analog Front-End Filter
- 0.125°C LSB Temperature Resolution
- 0.03125°C LSB Remote Temperature Resolution With Digital Filter Enabled
- Signed Format: +127.875°C/–128°C Remote Range
- Unsigned Format: 0°C/255°C Remote Range
- Remote Diode Fault Detection, Model Selection, and Offset Correction
- Mask and Status Register Support
- 3 Programmable $\overline{\text{TCRIT}}$ Outputs With Programmable Shared Hysteresis and Fault-Queue
- Programmable Conversion Rate and Shutdown Mode One-Shot Conversion Control
- SMBus 2.0 Compatible Interface, Supports TIMEOUT
- Three-Level Address Pin

2 Applications

- MCU, GPU, ASIC, FPGA, DSP, and CPU Temperature Monitoring
- Telecommunication Equipment
- Servers and Personal Computers
- Cloud Ethernet Switches
- Secure Data Centers
- Highly Integrated Medical Systems
- Precision Instruments and Test Equipment
- LED Lighting Thermal Control
- Office Electronics
- Electronic Test Equipment
- Processor and Computer System Thermal Management

3 Description

The LM95214 device is an 11-bit digital temperature sensor with a 2-wire System Management Bus (SMBus) interface that can very accurately monitor the temperature of four remote diodes as well as its own temperature. The four remote diodes can be external devices such as microprocessors, graphics processors that target the ideality of a 2N3904 transistor or diode-connected 2N3904s.

The LM95214 reports temperature in two different formats for +127.875°C/–128°C range and 0°C/255°C range. The LM95214 $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ outputs are triggered when any unmasked channel exceeds its corresponding programmable limit and can be used to shutdown the system, to turn on the system fans or as a microcontroller interrupt function. The current status of the $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, and $\overline{\text{TCRIT3}}$ pins can be read back from the status registers. Mask registers are available for further control of the $\overline{\text{TCRIT}}$ outputs.

Two LM95214 remote temperature channels have programmable digital filters while the other two remote channels use a fault-queue to minimize unwanted $\overline{\text{TCRIT}}$ events when temperature spikes are encountered.

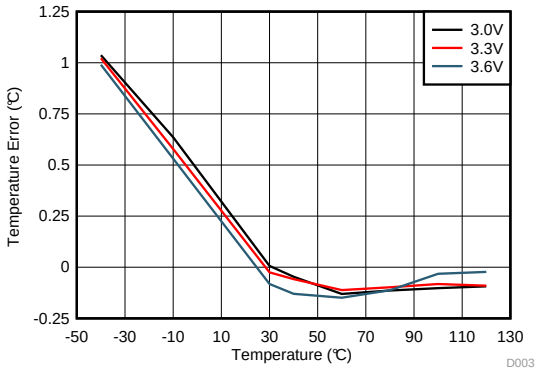
For optimum flexibility and accuracy, each LM95214 channel includes registers for offset correction. A three-level address pin allows connection of up to 3 LM95214s to the same SMBus master. The LM95214 includes power saving functions such as: programmable conversion rate, shutdown mode, and disabling of unused channels.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM95214	WSON (14)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Remote 1 Temperature Error, T_A=T_D



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2013) to Revision B — **Page**

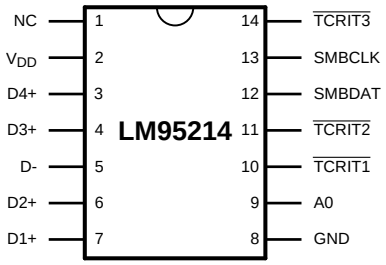
- *Added Device Information* table, Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Specification* section, *Detailed Description* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Original (March 2013) to Revision A — **Page**

- Changed layout of National Data Sheet to TI format ... 43

5 Pin Configuration and Functions

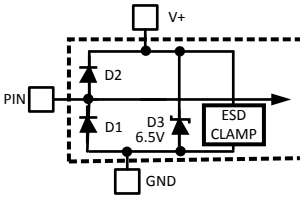
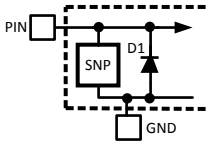
NHL Package
14-Pin WSON
Top View



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	NC	No Connect Not connected. May be left floating, connected to GND or V_{DD}.
2	V_{DD}	Positive Supply Voltage Input DC Voltage from 3.0 V to 3.6 V. V_{DD} must be bypassed with a 0.1-µF capacitor in parallel with 100 pF. The 100-pF capacitor must be placed as close as possible to the power supply pin. Noise must be kept below 200 mVp-p, a 10-µF capacitor may be required to achieve this.
3	D4+	Diode Current Source Fourth Diode Anode. Connected to remote discrete diode-connected transistor junction or to the diode-connected transistor junction on a remote IC whose die temperature is being sensed. A capacitor is not required between D4+ and D–. A 100 pF capacitor between D4+ and D– can be added and may improve performance in noisy systems. Float this pin if this thermal diode is not used.
4	D3+	Diode Current Source Third Diode Anode. Connected to remote discrete diode-connected transistor junction or to the diode-connected transistor junction on a remote IC whose die temperature is being sensed. A capacitor is not required between D3+ and D–. A 100-pF capacitor between D3+ and D– can be added and may improve performance in noisy systems. Float this pin if this thermal diode is not used.
5	D−	Diode Return Current Sink All Diode Cathodes. Common D– pin for all four remote diodes.
6	D2+	Diode Current Source Second Diode Anode. Connected to remote discrete diode-connected transistor junction or to the diode-connected transistor junction on a remote IC whose die temperature is being sensed. A capacitor is not required between D2+ and D–. A 100-pF capacitor between D2+ and D– can be added and may improve performance in noisy systems. Float this pin if this thermal diode is not used.
7	D1+	Diode Current Source First Diode Anode. Connected to remote discrete diode-connected transistor junction or to the diode-connected transistor junction on a remote IC whose die temperature is being sensed. A capacitor is not required between D1+ and D–. A 100-pF capacitor between D1+ and D– can be added and may improve performance in noisy systems. Float this pin if this thermal diode is not used.
8	GND	Power Supply Ground -- System low noise ground.
9	A0	Digital Input SMBus slave address select pin. Selects one of three addresses. Can be tied to V_{DD}, GND, or to the middle of a resistor divider connected between V_{DD} and GND.
10	$\overline{\text{TCRIT1}}$	Digital Output, Open-Drain Critical temperature output 1. Requires pullup resistor. Active *LOW*.
11	$\overline{\text{TCRIT2}}$	Digital Output, Open-Drain Critical temperature output 2. Requires pullup resistor. Active *LOW*.
12	SMBDAT	SMBus Bidirectional Data Line, Open-Drain Output From and to Controller; may require an external pullup resistor
13	SMBCLK	SMBus Clock Input From Controller; may require an external pullup resistor
14	$\overline{\text{TCRIT3}}$	Digital Output, Open-Drain Critical temperature output 3. Requires pullup resistor. Active *LOW*.

Table 1. ESD Protection

PIN NO.	LABEL	CIRCUIT	CIRCUITS FOR PIN ESD PROTECTION STRUCTURE
1	NC	–	
2	V_{DD}	A	
3	D4+	A	
4	D3+	A	
5	D-	A	
6	D2+	A	
7	D1+	A	**Circuit A**
8	GND	–	
9	A0	B	
10	$\overline{\text{TCRIT1}}$	B	
11	$\overline{\text{TCRIT2}}$	B	
12	SMBDAT	B	
13	SMBCLK	B	
14	$\overline{\text{TCRIT2}}$	B	**Circuit B**

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

	MIN	MAX	UNIT
Supply voltage	–0.3	6	V
Voltage at SMBDAT, SMBCLK, $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, $\overline{\text{TCRIT3}}$	–0.5	6	V
Voltage at other pins	–0.3	V_{DD} + 0.3	V
D− Input current		±1	mA
Input current at all other pins (4)		±5	mA
Package input current (4)		30	mA
SMBDAT, $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, $\overline{\text{TCRIT3}}$ output sink current		10	mA
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Soldering process must comply with reflow temperature profile specifications. Refer to http://www.ti.com/packaging
(3) Reflow temperature profiles are different for packages containing lead (Pb) than for those that do not.
(4) When the input voltage (V_I) at any pin exceeds the power supplies (V_I < GND or V_I > V_{DD}), the current at that pin must be limited to 5 mA. Parasitic components and or ESD protection circuitry are shown in the table below for the LM95214's pins.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge (1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±1000	
		Machine Model	±200	

(1) Human-body model, 100-pF discharged through a 1.5-kΩ resistor. Machine model, 200-pF discharged directly into each pin. Charged-device model (CDM) simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Operating temperature	–40		140	°C
Supply voltage (V_{DD})	3		3.6	V

6.4 Thermal Information

THERMAL METRIC(1)		LM95214 NHL (WSON) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: Temperature-to-Digital Converter

minimum and maximum specifications are over –40°C to +125°C and V+ = +3 V to 3.6 V (unless otherwise noted); typical specifications are at $T_A = T_J = 25°C$ and V+ = 3.3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temperature error using local diode	T_A = –40°C to +125°C, (1)	–2	±1	+2	°C
Temperature error using an MMBT3904 transistor remote diode(2)	T_A = +25°C to +85°C T_D = +60°C to +100°C	–1.1		+1.1	°C
	T_A = +25°C to +85°C T_D = –40°C to +125°C	–1.3		+1.3	°C
	T_A = –40°C to +85°C T_D = –40°C to +125°C	–3		+3	°C
	T_A = –40°C to +85°C T_D = 125°C to +140°C	–3.3		+3.3	°C
Local diode measurement resolution			11		Bits
			0.125		°C
Remote diode measurement resolution	Digital filter off		11		Bits
			0.125		°C
	Digital filter on (Remote Diodes 1 and 2 only)		13		Bits
			0.03125		°C
Conversion time of all temperatures at the fastest setting(3)	All channels are enabled in default state		1100	1210	ms
	1 external channel		31	34	ms
	Local only		30	33	ms
Quiescent current (4)	SMBus inactive, 1-Hz conversion rate, channels in default state		570	800	µA
	Shutdown		360		µA
D− Source voltage			0.4		V
Remote diode source current	High level		160	230	µA
	Low level		10		

(1) Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the LM95214 and the thermal resistance. See under *Recommended Operating Conditions* table for the thermal resistance to be used in the self-heating calculation.
(2) The accuracy of the LM95214CISD is ensured when using a typical MMBT3904 diode-connected transistor. For further information on other thermal diodes see applications Diode Non-Ideality.
(3) This specification is provided only to indicate how often temperature data is updated. The LM95214 can be read at any time without regard to conversion state (and will yield last conversion result).
(4) Quiescent current will not increase substantially with an SMBus communication.

Electrical Characteristics: Temperature-to-Digital Converter (continued)

minimum and maximum specifications are over –40°C to +125°C and V+ = +3 V to 3.6 V (unless otherwise noted); typical specifications are at $T_A = T_J = 25°C$ and V+ = 3.3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-On reset threshold	Measured on V_{DD} input, falling edge	1.6		2.8	V
$\overline{\text{TCRIT1}}$ pin temperature threshold	Default diodes 1 and 2 only	110			°C
$\overline{\text{TCRIT2}}$ pin temperature threshold	Default all channels	85			°C
$\overline{\text{TCRIT3}}$ pin temperature threshold	Default diodes 3 and 4 only	85			°C

6.6 Logic Electrical Characteristics: Digital DC Characteristics

Unless otherwise noted all limits are specified for V_{DD} = +3 Vdc to 3.6 Vdc, $T_A = T_J$ = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SMBDAT, SMBCLK INPUTS						
$V_{IN(1)}$	Logical 1 input voltage		2.1			V
$V_{IN(0)}$	Logical 0 input voltage				0.8	V
$V_{IN(HYST)}$	SMBDAT and SMBCLK digital input hysteresis		400			mV
$I_{IN(1)}$	Logical 1 input current	$V_{IN} = V_{DD}$	0.005		10	µA
$I_{IN(0)}$	Logical 0 input current	V_{IN} = 0 V	−0.005		–10	µA
C_{IN}	Input capacitance		5			pF
A0 DIGITAL INPUT						
V_{IH}	Input high voltage		0.90 × V_{DD}			V
V_{IM}	Input middle voltage		0.43 × V_{DD}		0.57 × V_{DD}	V
						V
V_{IL}	Input low voltage				0.10 × V_{DD}	V
$I_{IN(1)}$	Logical 1 input current	$V_{IN} = V_{DD}$	$V_{IN} = V_{DD}$	–0.005	–10	µA
$I_{IN(0)}$	Logical 0 input current	V_{IN} = 0 V	V_{IN} = 0 V	0.005	10	µA
C_{IN}	Input capacitance			5		pF
SMBDAT, $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, $\overline{\text{TCRIT3}}$ DIGITAL OUTPUTS						
I_{OH}	High level output current	$V_{OH} = V_{DD}$			10	µA
$V_{OL(SMBDAT)}$	SMBus low level output voltage	I_{OL} = 4 mA	0.4			V
		I_{OL} = 6 mA			0.6	V
$V_{OL(\overline{\text{TCRIT}})}$	$\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, $\overline{\text{TCRIT3}}$ low level output voltage	I_{OL} = 6 mA			0.4	V
C_{OUT}	Digital output capacitance			5		pF

6.7 Switching Characteristics: SMBus Digital

Unless otherwise noted, these specifications apply for V_{DD}=+3.0 Vdc to +3.6 Vdc, C_L (load capacitance) on output lines = 80 pF, $T_A = T_J$ = +25°C.

The switching characteristics of the LM95214 fully meet or exceed the published specifications of the SMBus version 2.0. The following parameters are the timing relationships between SMBCLK and SMBDAT signals related to the LM95214. They adhere to but are not necessarily the SMBus bus specifications.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus clock frequency		10		100	kHz
t_{LOW}	SMBus clock low time	from $V_{IN(0)}$max to $V_{IN(0)}$max	4.7			µs
					25	ms
t_{HIGH}	SMBus clock high time	from $V_{IN(1)}$min to $V_{IN(1)}$min	4.0			µs
$t_{R,SMB}$	SMBus rise time	See (1)	1			µs
$t_{F,SMB}$	SMBus fall time	See (2)	0.3			µs
t_{OF}	Output fall time	C_L = 400 pF, I_O = 3 mA (2)			250	ns
$t_{TIMEOUT}$	SMBDAT and SMBCLK time low for reset of serial interface		25		35	ms
$t_{SU;DAT}$	Data in setup time to SMBCLK high		250			ns
$t_{HD;DAT}$	Data out stable after SMBCLK low		300		1075	ns
$t_{HD;STA}$	Start condition SMBDAT low to SMBCLK low (Start condition hold before the first clock falling edge)		100			ns
$t_{SU;STO}$	Stop condition SMBCLK high to SMBDAT low (Stop condition setup)		100			ns
$t_{SU;STA}$	SMBus repeated start-condition setup time, SMBCLK high to SMBDAT low		0.6			µs
t_{BUF}	SMBus free time between stop and start conditions		1.3			µs

(1) The output rise time is measured from ($V_{IN(0)}$max − 0.15 V) to ($V_{IN(1)}$min + 0.15 V).
(2) The output fall time is measured from ($V_{IN(1)}$min + 0.15 V) to ($V_{IN(0)}$max − 0.15 V).

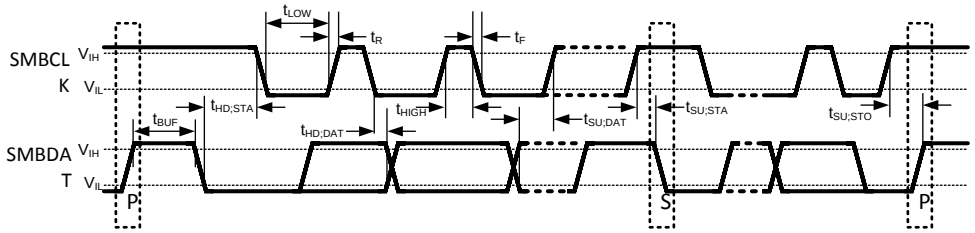


Figure 1. SMBus Communication

6.8 Typical Characteristics

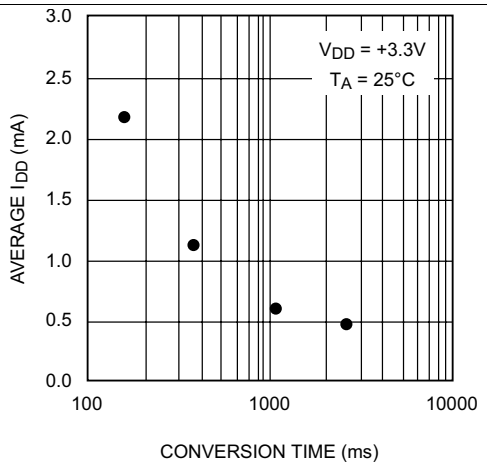


Figure 2. Conversion Rate Effect on Average Power Supply Current

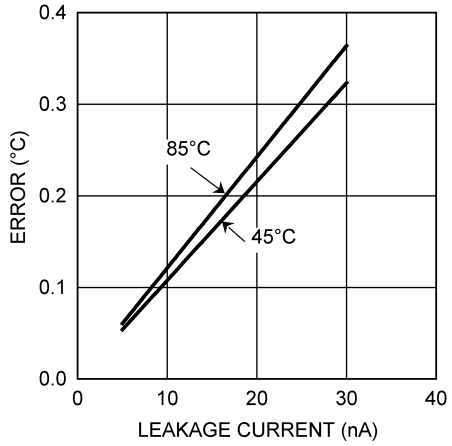


Figure 3. Thermal Diode Capacitor or PCB Leakage Current Effect on Remote Diode Temperature Reading

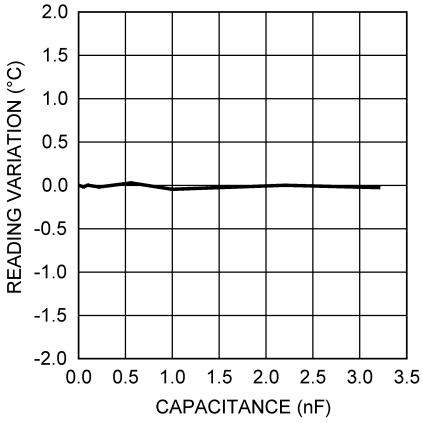


Figure 4. Remote Temperature Reading Sensitivity to Thermal Diode Filter Capacitance

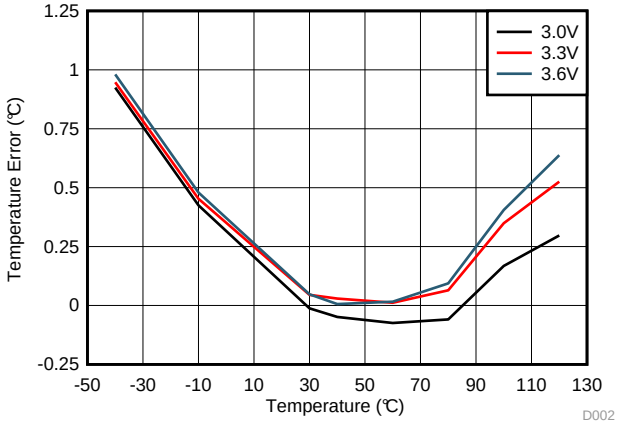


Figure 5. Local Temperature Error, $T_A = T_D$

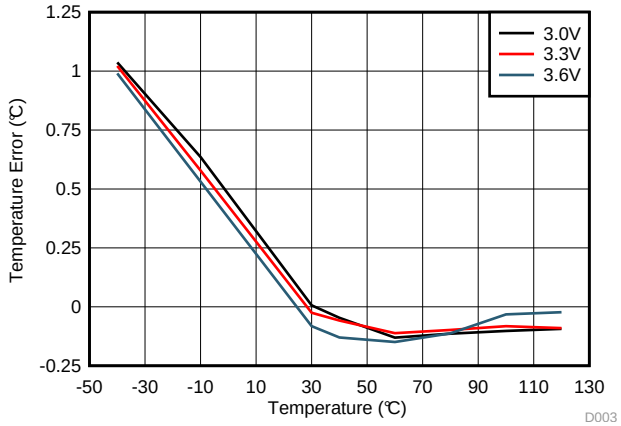


Figure 6. Remote 1 Temperature Error, $T_A = T_D$

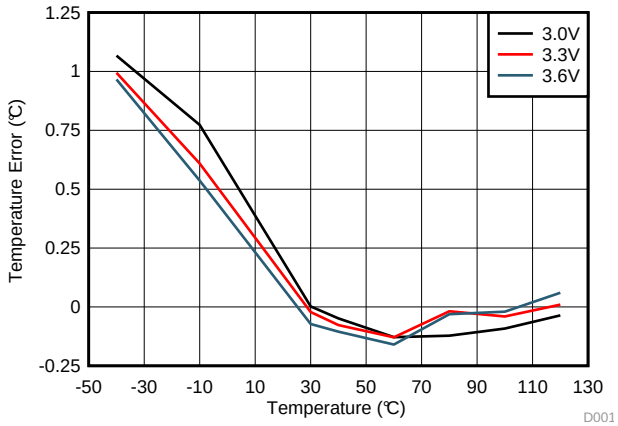


Figure 7. Remote 2 Temperature Error, $T_A = T_D$

Typical Characteristics (continued)

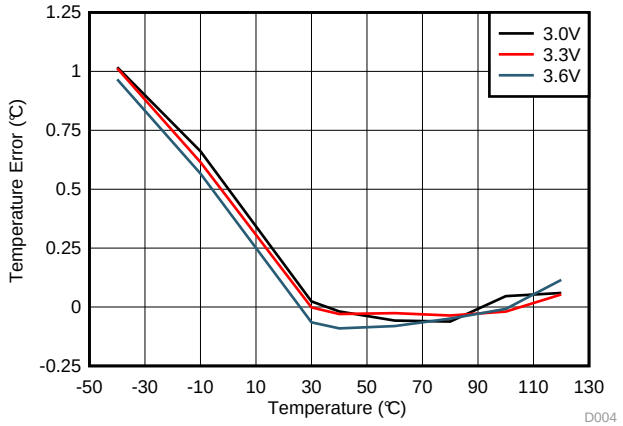


Figure 8. Remote 3 Temperature Error, $T_A = T_D$

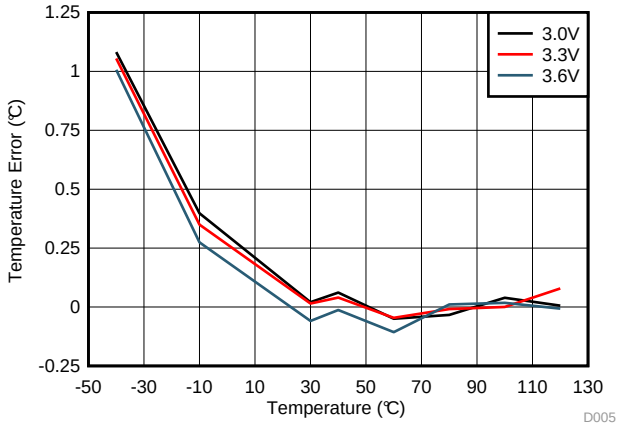


Figure 9. Remote 4 Temperature Error, $T_A = T_D$

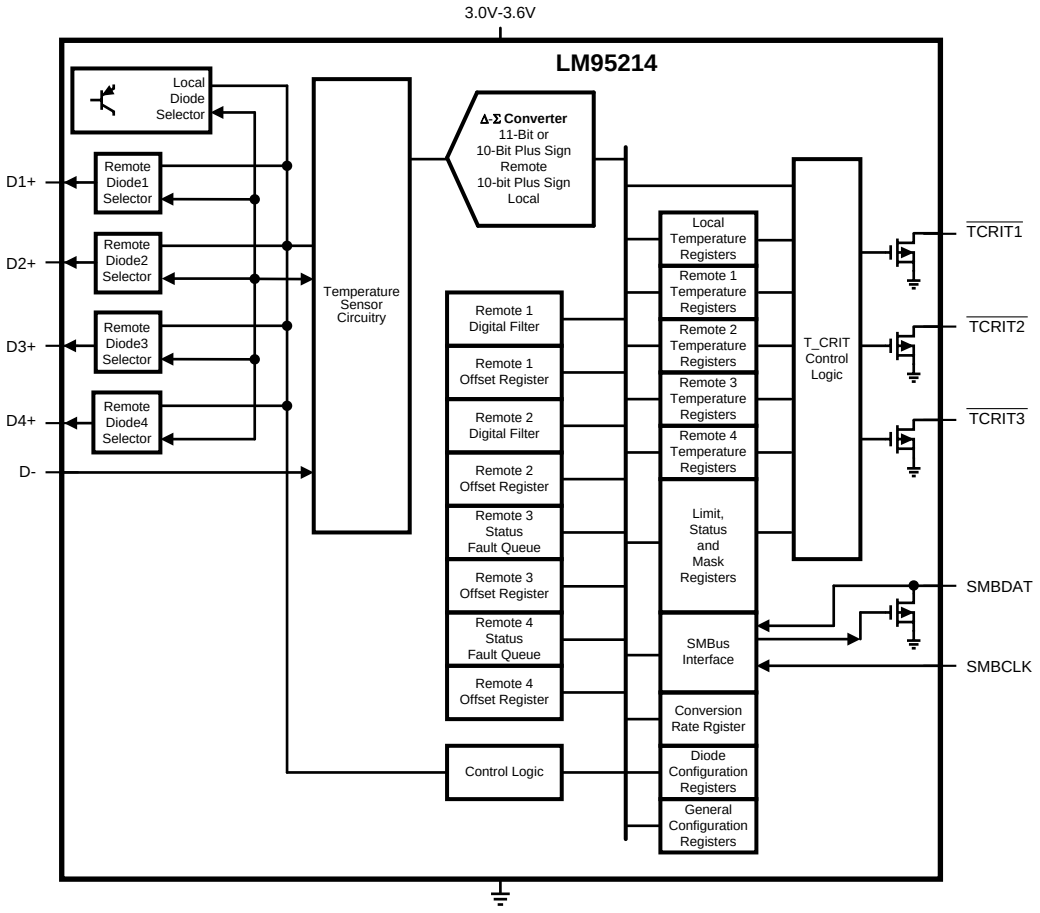
7 Detailed Description

7.1 Overview

The LM95214 is an 11-bit digital temperature sensor with a 2-wire System Management Bus (SMBus) interface that can monitor the temperature of four remote diodes as well as its own temperature. The LM95214 can be used to very accurately monitor the temperature of up to four external devices such as microprocessors, graphics processors or diode-connected 2N3904 transistor. Any device whose thermal diode can be modeled by an MMBT3904 transistor will work well with the LM95214.

The LM95214 reports temperature in two different formats for +127.875°C/–128°C range and 0°C/255°C range. The LM95214 has a Sigma-Delta ADC (Analog-to-Digital Converter) core which provides the first level of noise immunity. For improved performance in a noisy environment the LM95214 includes programmable digital filters for Remote Diode 1 and 2 temperature readings. When the digital filters are invoked the resolution for Remote Diode 1 and 2 readings increases to 0.03125°C. For maximum flexibility and best accuracy the LM95214 includes offset registers that allow calibration of other diode types.

7.2 Functional Block Diagram



7.3 Feature Description

The LM95214 $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, and $\overline{\text{TCRIT3}}$ active low outputs are triggered when any unmasked channel exceeds its corresponding programmable limit and can be used to shutdown the system, to turn on the system fans or as a microcontroller interrupt function. The current status of the $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, and $\overline{\text{TCRIT3}}$ pins can be read back from the status registers through the SMBus interface. Two of the remote channels have two separate limits each that control the $\overline{\text{TCRIT1}}$ and $\overline{\text{TCRIT2}}$ pins. The remaining two channels and the local channel each have one limit to control both the $\overline{\text{TCRIT1}}$ and $\overline{\text{TCRIT2}}$ pins. The $\overline{\text{TCRIT3}}$ pin shares the limits of the $\overline{\text{TCRIT2}}$ pin but allows for different masking options. All limits have a shared programmable hysteresis register.

Diode fault detection circuitry in the LM95214 can detect the absence or fault state of a remote diode: whether D+ is shorted to V_{DD}, D– or ground, or whether D+ is floating.

Remote Diode 1 and 2 temperature channels have programmable digital filters while the other two remote temperature channels utilize a fault-queue to avoid false triggering the $\overline{\text{TCRIT}}$ pins.

The LM95214 has a three-level address pin to connect up to 3 devices to the same SMBus master. LM95214 also has programmable conversion rate register as well as a shutdown mode for power savings. One round of conversions can be triggered in shutdown mode by writing to the one-shot register through the SMBus interface. LM95214 can be programmed to turn off unused channels for more power savings.

The LM95214 register set has an 8-bit data structure and includes:

1. Temperature Value Registers with signed format
   - Most-Significant-Byte (MSB) and Least-Significant-Byte (LSB) Local Temperature
   - MSB and LSB Remote Temperature 1
   - MSB and LSB Remote Temperature 2
   - MSB and LSB Remote Temperature 3
   - MSB and LSB Remote Temperature 4
2. Temperature Value Registers with unsigned format
   - MSB and LSB Remote Temperature 1
   - MSB and LSB Remote Temperature 2
   - MSB and LSB Remote Temperature 3
   - MSB and LSB Remote Temperature 4
3. Diode Configuration Registers
   - Diode Model Select
   - Remote 1 Offset
   - Remote 2 Offset
   - Remote 3 Offset
   - Remote 4 Offset
4. General Configuration Registers
   - Configuration (Standby, Fault Queue enable for Remote 3 and 4; Conversion Rate)
   - Channel Conversion Enable
   - Filter Setting for Remote 1 and 2
   - 1-Shot
5. Status Registers
   - Main Status Register (Busy bit, Not Ready, Status Register 1 to 4 Flags)
   - Status 1 (diode fault)
   - Status 2 (TCRIT1)
   - Status 3 (TCRIT2)
   - Status 4 (TCRIT3)
6. Mask Registers
   - TCRIT1 Mask
   - TCRIT2 Mask

Feature Description (continued)

- TCRIT3 Mask

7. Limit Registers
   - Local Tcrit Limit
   - Remote 1 Tcrit-1 Limit
   - Remote 2 Tcrit-1 Limit
   - Remote 3 Tcrit Limit
   - Remote 4 Tcrit Limit
   - Remote 1 Tcrit-2 and Tcrit-3 Limit
   - Remote 2 Tcrit-2 and Tcrit-3 Limit
   - Common Tcrit Hysteresis
8. Manufacturer ID Register
9. Revision ID Register

7.3.1 Conversion Sequence

The LM95214 takes approximately 190 ms to convert the Local Temperature, Remote Temperatures 1 through 4, and to update all of its registers. These conversions for each thermal diode are addressed in a round robin sequence. Only during the conversion process the busy bit (D7) in Status register (02h) is high. The conversion rate may be modified by the Conversion Rate bits found in the Configuration Register (03h). When the conversion rate is modified a delay is inserted between each round of conversions, the actual time for each round remains at 190 ms (typical all channels enabled). The time a round takes depends on the number of channels that are on. Different conversion rates will cause the LM95214 to draw different amounts of average supply current as shown in Figure 10. This curve assumes all the channels are on. If channels are turned off the average current will drop because the round robin time will decrease and the shutdown time will increase during each conversion interval.

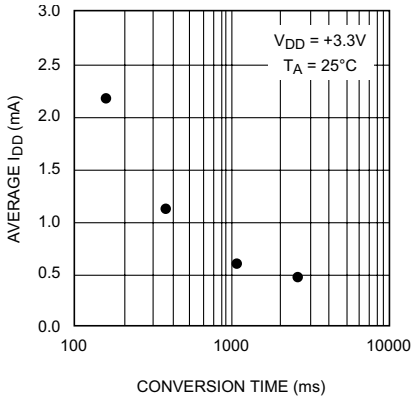


Figure 10. Conversion Rate Effect on Power Supply Current

7.3.2 Power-On-Default States

The LM95214 always powers up to these known default states. The LM95214 remains in these states until after the first conversion.

1. All Temperature readings set to 0°C until the end of the first conversion
2. Remote offset for all channels 0°C
3. Configuration: Active converting, Fault Queue enabled for Remote 3 and 4
4. Continuous conversion with all channels enabled, time = 1 s
5. Enhanced digital filter enabled for Remote 1 and 2
6. Status Registers depends on state of thermal diode inputs
7. Local and Remote Temperature Limits for $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ outputs:

Feature Description (continued)

Table 2. Temperature Channel limits

OUTPUT PIN	TEMPERATURE CHANNEL LIMIT				
	REMOTE 4 (°C)	REMOTE 3 (°C)	REMOTE 2 (°C)	REMOTE 1 (°C)	LOCAL (°C)
$\overline{\text{TCRIT1}}$	Masked, 85	Masked, 85	110	110	Masked, 85
$\overline{\text{TCRIT2}}$	85	85	85	85	85
$\overline{\text{TCRIT3}}$	85	85	Masked, 85	Masked, 85	Masked, 85

8. Manufacturers ID set to 01h
9. Revision ID set to 79h

7.3.3 SMBus Interface

The LM95214 operates as a slave on the SMBus, so the SMBCLK line is an input and the SMBDAT line is bidirectional. The LM95214 never drives the SMBCLK line and it does not support clock stretching. According to SMBus specifications, the LM95214 has a 7-bit slave address. Three SMBus device address can be selected by connecting A0 (pin 6) to either Low, Mid-Supply, or High voltages. The LM95214 has the following SMBus slave address:

Table 3. SMBus Slave Addresses

A0 PIN STATE	SMBus DEVICE ADDRESS A[6:0]	
	HEX	BINARY
Low	18h	001 1000
Mid-Supply	4Dh	100 1101
High	4Eh	100 1110

7.3.4 Temperature Conversion Sequence

Each of the 5 temperature channels of LM95214 can be turned OFF independent from each other through the Channel Enable Register. Turning off unused channels will increase the conversion speed in the fastest conversion speed mode. If the slower conversion speed settings are used, disabling unused channels will reduce the average power consumption of LM95214.

7.3.4.1 Digital Filter

To suppress erroneous remote temperature readings due to noise as well as increase the resolution of the temperature, the LM95214 incorporates a digital filter for Remote 1 and 2 Temperature Channels. When a filter is enabled the filtered readings are used for the TCRIT comparisons. There are two possible digital filter settings that are enabled through the Filter Setting Register at register address 0Fh. The filter for each channel can be set according to the following table:

Table 4. Digital Filter Settings

R1F[1:0] OR R2F[1:0]		FILTER SETTING
0	0	No Filter
0	1	Filter (equivalent to Level 2 filter of the LM86/LM89)
1	0	Reserved
1	1	Enhanced Filter (Filter with transient noise clipping)

Figure 11, Figure 12, and Figure 13 describe the filter output in response to a step input and an impulse input.

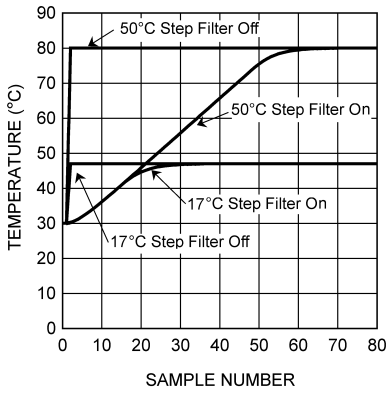


Figure 11. Seventeen and Fifty Degree Step Response

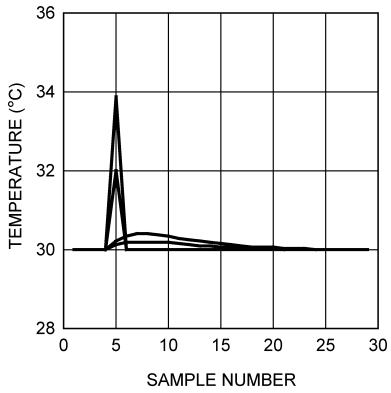


Figure 12. Impulse Response With Input Transients Less Than 4°C

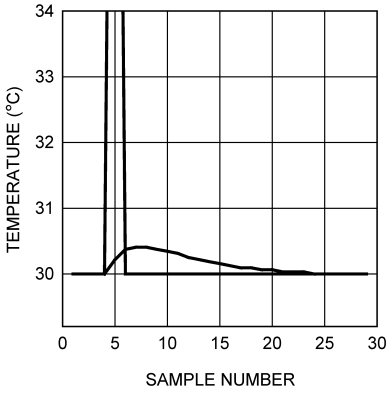


Figure 13. Impulse Response With Input Transients Greater Than 4°C

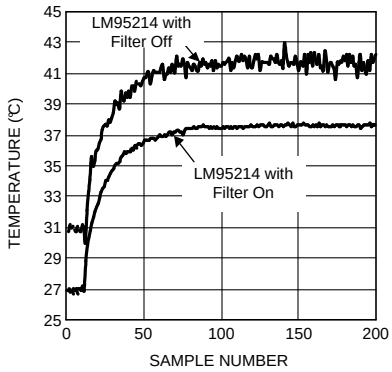


Figure 14. Digital Filter Response in a Typical Intel Processor on a 65 nm or 90 nm Process. The Filter Curves Were Purposely Offset for Clarity.

Figure 14 shows the filter in use in a typical system. Note that the two curves have been purposely offset for clarity. Inserting the filter does not induce an offset as shown.

7.3.5 Fault Queue

To suppress erroneous $\overline{\text{TCRIT1}}$,$\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ triggering the LM95214 incorporates a Fault Queue for the unfiltered remote channels 3 and 4. The Fault Queue acts to ensure the remote temperature measurement of these channels is genuinely beyond the corresponding Tcrit limit by not triggering until three consecutive out of limit measurements have been made, see Figure 15 for an example. The Fault Queue defaults on upon power-up. The fault queue for channels 3 and 4 can be turned ON or OFF through bits 0 and 1 of the Configuration Register. When the fault queue is enabled, the $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ pins will be triggered if the temperature is above the Tcrit limit for 3 consecutive conversions and the corresponding mask bit is 0 in the TCRIT Mask registers. Similarly the temperature needs to be below the Tcrit limit minus the hysteresis value for three consecutive conversions for the $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ pins to deactivate.

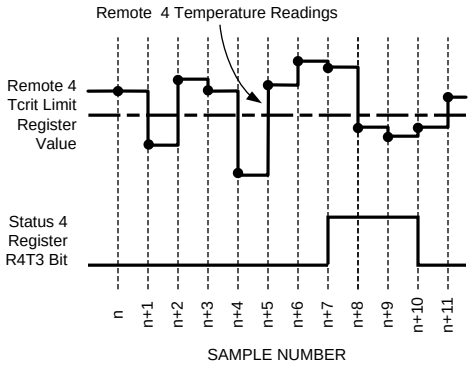


Figure 15. Fault Queue Response Diagram (With 0°C Hysteresis)

7.3.6 Temperature Data Format

Temperature data can only be read from the Local and Remote Temperature value registers. The data format for all temperature values is left justified 16-bit word available in two 8-bit registers. Unused bits will always report 0. All temperature data is clamped and will not roll over when a temperature exceeds full-scale value.

Remote temperature data for all channels can be represented by an 11-bit, two's complement word or unsigned binary word with an LSb (Least Significant Bit) equal to 0.125°C.

Table 5. 11-Bit, 2's Complement (10-Bit Plus Sign)

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.125°C	0000 0000 0010 0000	0020h
0°C	0000 0000 0000 0000	0000h
−0.125°C	1111 1111 1110 0000	FFE0h
−1°C	1111 1111 0000 0000	FF00h
−25°C	1110 0111 0000 0000	E700h
−55°C	1100 1001 0000 0000	C900h

Table 6. 11-Bit Unsigned Binary

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
+255.875°C	1111 1111 1110 0000	FFE0h
+255°C	1111 1111 0000 0000	FF00h
+201°C	1100 1001 0000 0000	C900h
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.125°C	0000 0000 0010 0000	0020h
0°C	0000 0000 0000 0000	0000h

When the digital filter is enabled on Remote 1 and 2 channels temperature data is represented by a 13-bit unsigned binary or 12-bit plus sign (two's complement) word with an LSb equal to 0.03125°C.

Table 7. 13-Bit, 2's Complement (12-Bit Plus Sign)

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.03125°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h
−0.03125°C	1111 1111 1111 1000	FFF8h
−1°C	1111 1111 0000 0000	FF00h
−25°C	1110 0111 0000 0000	E700h
−55°C	1100 1001 0000 0000	C900h

Table 8. 13-Bit, Unsigned Binary

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
+255.875°C	1111 1111 1110 0000	FFE0h
+255°C	1111 1111 0000 0000	FF00h
+201°C	1100 1001 0000 0000	C900h
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.03125°C	0000 0000 0000 1000	0008h
0°C	0000 0000 0000 0000	0000h

Local Temperature data is only represented by an 11-bit, two's complement, word with an LSb equal to 0.125°C.

Table 9. 11-Bit, 2's Complement (10-Bit Plus Sign)

TEMPERATURE	DIGITAL OUTPUT	
	BINARY	HEX
+125°C	0111 1101 0000 0000	7D00h
+25°C	0001 1001 0000 0000	1900h
+1°C	0000 0001 0000 0000	0100h
+0.125°C	0000 0000 0010 0000	0020h
0°C	0000 0000 0000 0000	0000h
−0.125°C	1111 1111 1110 0000	FFE0h
−1°C	1111 1111 0000 0000	FF00h
−25°C	1110 0111 0000 0000	E700h
−55°C	1100 1001 0000 0000	C900h

7.3.7 SMBDAT Open-Drain Output

The SMBDAT output is an open-drain output and does not have internal pullups. A *high* level will not be observed on this pin until pullup current is provided by some external source, typically a pullup resistor. Choice of resistor value depends on many system factors but, in general, the pullup resistor must be as large as possible without effecting the SMBus desired data rate. This will minimize any internal temperature reading errors due to internal heating of the LM95214. The maximum resistance of the pullup to provide a 2.1-V high level, based on LM95214 specification for High Level Output Current with the supply voltage at 3 V, is 82 kΩ (5%) or 88.7 kΩ (1%).

7.3.8 $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, and $\overline{\text{TCRIT3}}$ Outputs

The LM95214's $\overline{\text{TCRIT}}$ pins are active-low open-drain outputs and do not include internal pullup resistors. A *high* level will not be observed on these pins until pullup current is provided by some external source, typically a pullup resistor. Choice of resistor value depends on many system factors but, in general, the pullup resistor must be as large as possible without effecting the performance of the device receiving the signal. This will minimize any internal temperature reading errors due to internal heating of the LM95214. The maximum resistance of the pullup to provide a 2.1-V high level, based on LM95214 specification for High Level Output Current with the supply voltage at 3 V, is 82 kΩ (5%) or 88.7 kΩ (1%). The three $\overline{\text{TCRIT}}$ pins can each sink 6 mA of current and still ensured a *Logic Low* output voltage of 0.4 V. If all three pins are set at maximum current this will cause a power dissipation of 7.2 mW. This power dissipation combined with a thermal resistance of 77.8°C/W will cause the LM95214's junction temperature to rise approximately 0.6°C and thus cause the Local temperature reading to shift. This can only be cancelled out if the environment that the LM95214 is enclosed in has stable and controlled air flow over the LM95214, as airflow can cause the thermal resistance to change dramatically.

7.3.9 TCRIT Limits and $\overline{\text{TCRIT}}$ Outputs

Figure 16 describes a simplified diagram of the temperature comparison and status register logic. Figure 17, Figure 18, and Figure 19 describe simplified logic diagrams of the circuitry associated with the status registers, mask registers, and the $\overline{\text{TCRIT}}$ output pins.

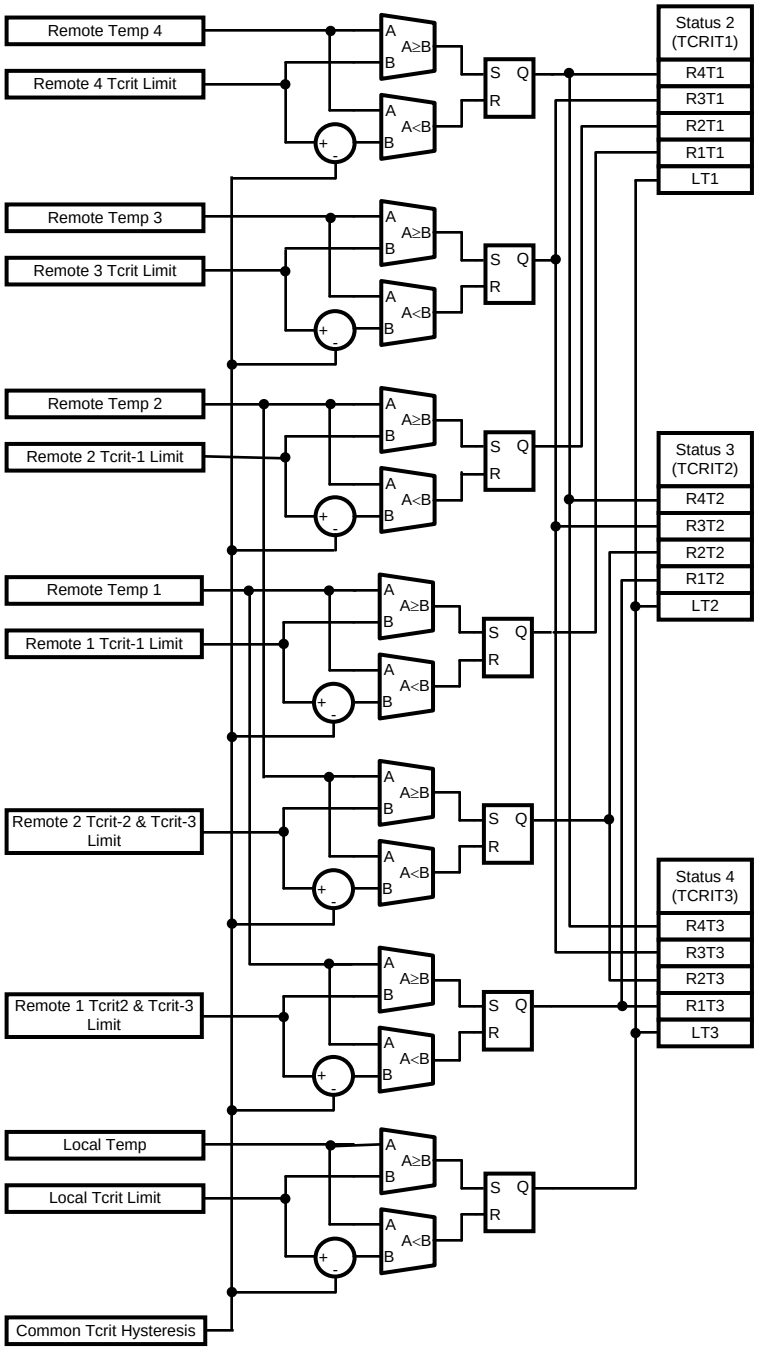


Figure 16. Temperature Comparison Logic and Status Register Simplified Diagram

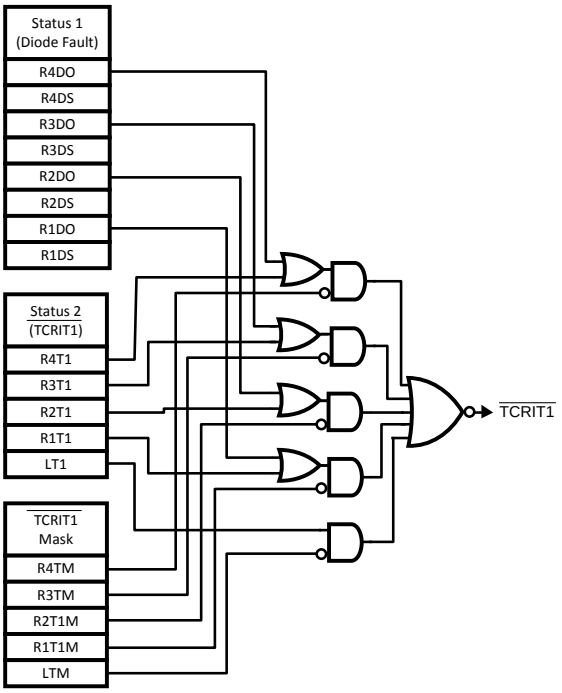


Figure 17. $\overline{\text{TCRIT1}}$ Mask Register, Status Register 1 and 2, and $\overline{\text{TCRIT1}}$ Output Logic Diagram

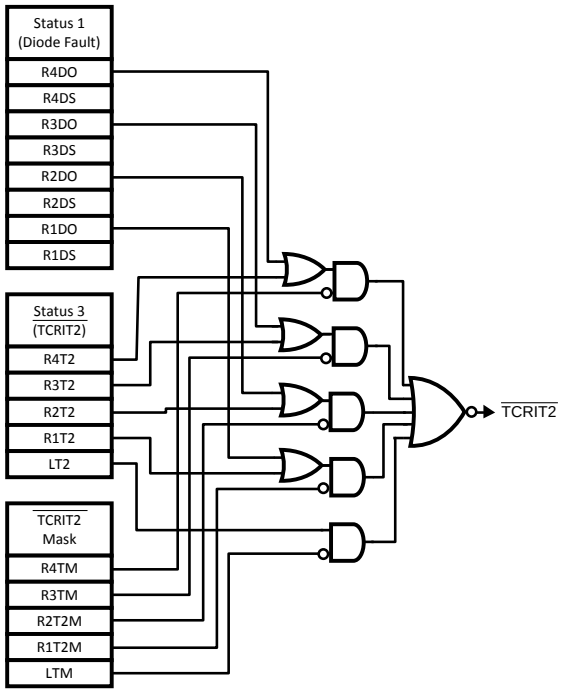


Figure 18. $\overline{\text{TCRIT2}}$ Mask Register, Status Register 1 and 3, and $\overline{\text{TCRIT2}}$ Output Logic Diagram

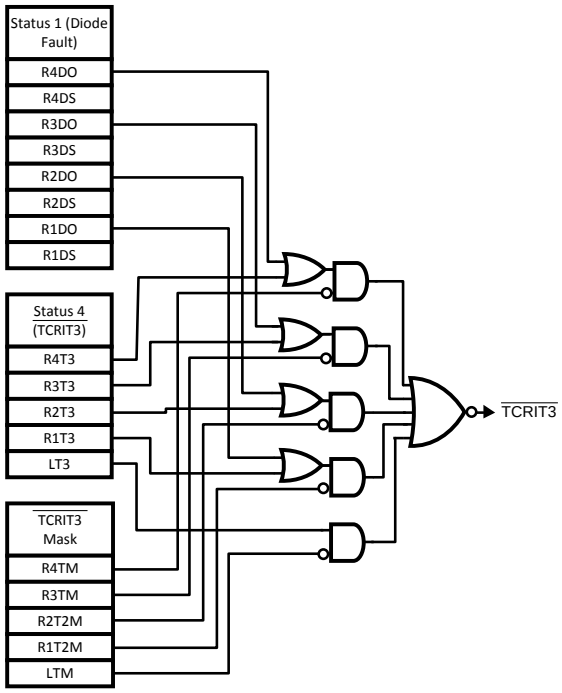


Figure 19. $\overline{\text{TCRIT3}}$ Mask Register, Status Register 1 and 4, and $\overline{\text{TCRIT3}}$ Output Logic Diagram

If enabled, local temperature is compared to the user programmable Local Tcrit Limit Register (Default Value = 85°C). The result of this comparison is stored in Status Register 2, Status Register 3 and Status Register 4 (see Figure 16). The comparison result can trigger $\overline{\text{TCRIT1}}$ pin, $\overline{\text{TCRIT2}}$ pin or $\overline{\text{TCRIT3}}$ pin depending on the settings in the TCRIT1 Mask, TCRIT2 Mask and TCRIT3 Mask Registers (see Figure 17, Figure 18, and Figure 19). The comparison result can also be read back from the Status Register 2, Status Register 3 and Status Register 4.

If enabled, remote temperature 1 is compared to the user programmable Remote 1 Tcrit-1 Limit Register (Default Value 110°C) and Remote 1 Tcrit-2 Limit Register (Default Value = 85°C). The result of this comparison is stored in Status Register 2, Status Register 3 and Status Register 4 (see Figure 16). The comparison result can trigger $\overline{\text{TCRIT1}}$ pin, $\overline{\text{TCRIT2}}$ pin or $\overline{\text{TCRIT3}}$ pin depending on the settings in the $\overline{\text{TCRIT1}}$ Mask, $\overline{\text{TCRIT2}}$ Mask and $\overline{\text{TCRIT3}}$ Mask Registers (see Figure 17, Figure 18, and Figure 19). The comparison result can also be read back from the Status Register 2, Status Register 3 and Status Register 4. The remote temperature 2 operates in a similar manner to remote temperature 1 using its associated user programmable limit registers: Remote 2 Tcrit-1 Limit Register (Default Value 110°C) and Remote 2 Tcrit-2 Limit Register (Default Value = 85°C). When enabled, the remote temperature 3 is compared to the user programmable Remote 3 Tcrit Limit Register (Default Value 85°C). The comparison result can trigger $\overline{\text{TCRIT1}}$ pin, $\overline{\text{TCRIT2}}$ pin or $\overline{\text{TCRIT3}}$ pin depending on the settings in the $\overline{\text{TCRIT1}}$ Mask, $\overline{\text{TCRIT2}}$ Mask and $\overline{\text{TCRIT3}}$ Mask Registers. The comparison result can also be read back from the Status Register 2, Status Register 3 and Status Register 4. The remote temperature 4 operates in a similar manner to remote temperature 3 using its associated user programmable limit register: Remote 4 Tcrit Limit Register (Default Value 85°C).

Table 10. Limit Assignments for Each $\overline{\text{TCRIT}}$ Output Pin:

	$\overline{\text{TCRIT1}}$	$\overline{\text{TCRIT2}}$	$\overline{\text{TCRIT3}}$
Remote 4	Remote 4 Tcrit Limit	Remote 4 Tcrit Limit	Remote 4 Tcrit Limit
Remote 3	Remote 3 Tcrit Limit	Remote 3 Tcrit Limit	Remote 3 Tcrit Limit
Remote 2	Remote 2 Tcrit-1 Limit	Remote 2 Tcrit-2 Limit	Remote 2 Tcrit-2 Limit
Remote 1	Remote 1 Tcrit-1 Limit	Remote 1 Tcrit-2 Limit	Remote 1 Tcrit-2 Limit
Local	Local Tcrit Limit	Local Tcrit Limit	Local Tcrit Limit

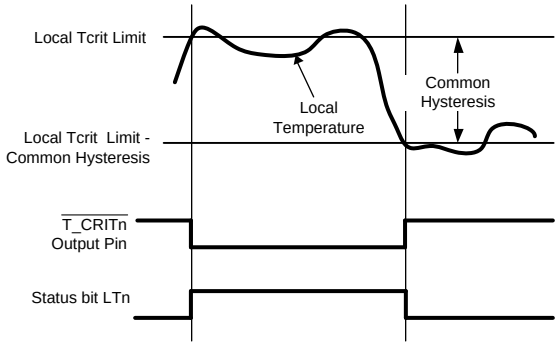


Figure 20. TCRIT Response Diagram (Masking Options Not Included)

The TCRIT response diagram of Figure 20 shows the local temperature interaction with the Tcrit limit and hysteresis value. As can be seen in the diagram when the local temperature exceeds the Tcrit limit register value the LTn Status bit is set and the $\overline{\text{T\_CRITn}}$ output(s) is/are activated. The Status bit(s) and outputs are not deactivated until the temperature goes below the value calculated by subtracting the Common Hysteresis value programmed from the limit. This diagram mainly shows an example function of the hysteresis and is not meant to show complete function of the possible settings and options of all the TCRIT outputs and limit values.

7.4 Device Functional Modes

7.4.1 Diode Fault Detection

The LM95214 is equipped with operational circuitry designed to detect fault conditions concerning the remote diodes. In the event that the D+ pin is detected as shorted to GND, D−, V_{DD} or D+ is floating, the Remote Temperature reading is –128.000°C if signed format is selected and 0°C if unsigned format is selected. In addition, the appropriate status register bits RD1M or RD2M (D1 or D0) are set.

Device Functional Modes (continued)

7.4.2 Communicating With the LM95214

The data registers in the LM95214 are selected by the Command Register. At power-up the Command Register is set to 00, the location for the Read Local Temperature Register. The Command Register latches the last location it was set to. Each data register in the LM95214 falls into one of three types of user accessibility:

1. Read only
2. Write only
3. Write/Read same address

A **Write** to the LM95214 will always include the address byte and the command byte. A write to any register requires one data byte.

Reading the LM95214 can take place either of two ways:

1. If the location latched in the Command Register is correct (most of the time it is expected that the Command Register will point to one of the Read Temperature Registers because that will be the data most frequently read from the LM95214), then the read can simply consist of an address byte, followed by retrieving the data byte.
2. If the Command Register needs to be set, then an address byte, command byte, repeat start, and another address byte will accomplish a read.

The data byte has the most significant bit first. At the end of a read, the LM95214 can accept either acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). It takes the LM95214 190 ms (typical, all channels enabled) to measure the temperature of the remote diodes and internal diode. When retrieving all 11 bits from a previous remote diode temperature measurement, the master must insure that all 11 bits are from the same temperature conversion. This may be achieved by reading the MSB register first. The LSB will be locked after the MSB is read. The LSB will be unlocked after being read. If the user reads MSBs consecutively, each time the MSB is read, the LSB associated with that temperature will be locked in and override the previous LSB value locked-in.

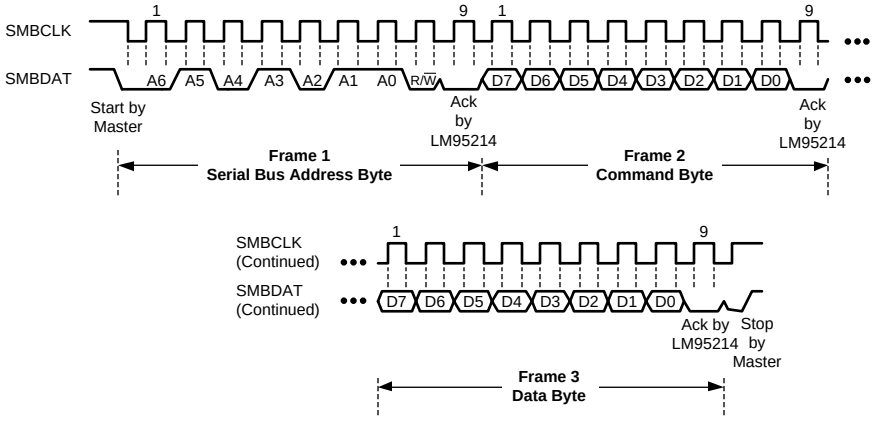


Figure 21. Serial Bus Write to the Internal Command Register Followed by a the Data Byte

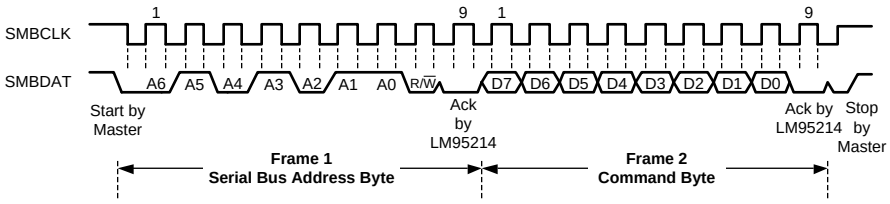


Figure 22. Serial Bus Write to the Internal Command Register

Device Functional Modes (continued)

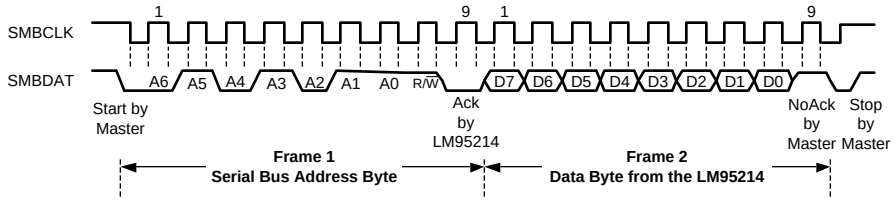


Figure 23. Serial Bus Read From a Register With the Internal Command Register Preset to Desired Value

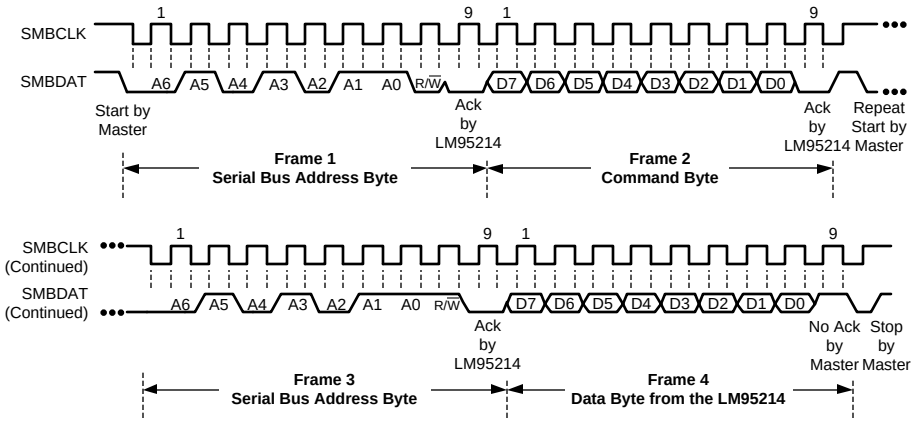


Figure 24. Serial Bus Write Followed by a Repeat Start and Immediate Read

7.4.3 Serial Interface Reset

In the event that the SMBus Master is RESET while the LM95214 is transmitting on the SMBDAT line, the LM95214 must be returned to a known state in the communication protocol. This may be done in one of two ways:

1. When SMBDAT is LOW, the LM95214 SMBus state machine resets to the SMBus idle state if either SMBDAT or SMBCLK are held low for more than 35ms ($t_{TIMEOUT}$). Note that according to SMBus specification 2.0 all devices are to timeout when either the SMBCLK or SMBDAT lines are held low for 25 to 35 ms. Therefore, to insure a timeout of all devices on the bus the SMBCLK or SMBDAT lines must be held low for at least 35 ms.
2. When SMBDAT is HIGH, have the master initiate an SMBus start. The LM95214 will respond properly to an SMBus start condition at any point during the communication. After the start the LM95214 will expect an SMBus Address byte.

7.4.4 One-Shot Conversion

The One-Shot register is used to initiate a round of conversions and comparisons when the device is in standby mode, after which the device returns to standby. This is not a data register and it is the write operation that causes the one-shot conversion. The data written to this address is irrelevant and is not stored. A zero will always be read from this register. All the channels that are enabled in the Channel Enable Register will be converted once and the $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, and $\overline{\text{TCRIT3}}$ pins will reflect the comparison results based on this round of conversion results of the channels that are not masked.

7.5 Register Maps

7.5.1 LM95214 Registers

Command register selects which registers will be read from or written to. Data for this register must be transmitted during the Command Byte of the SMBus write communication.

P7	P6	P5	P4	P3	P2	P1	P0
Command Byte							

P0-P7: Command

Table 11. Register Summary

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Local Temp MSB	0x10	RO	SIGN	64	32	16	8	4	2	1	–
Local Temp LSB	0x20	RO	1/2	1/4	1/8	0	0	0	0	0	–
Remote Temp 1 MSB – Signed	0x11	RO	SIGN	64	32	16	8	4	2	1	–
Remote Temp 1 LSB – Signed, Digital Filter Off	0x21	RO	1/2	1/4	1/8	0	0	0	0	0	–
Remote Temp 1 LSB – Signed, Digital Filter On						1/16	1/32				
Remote Temp 2 MSB – Signed	0x12	RO	SIGN	64	32	16	8	4	2	1	–
Remote Temp 2 LSB – Signed, Digital Filter Off	0x22	RO	1/2	1/4	1/8	0	0	0	0	0	–
Remote Temp 2 LSB – Signed, Digital Filter On						1/16	1/32				
Remote Temp 3 MSB – Signed	0x13	RO	SIGN	64	32	16	8	4	2	1	–
Remote Temp 3 LSB – Signed	0x23	RO	1/2	1/4	1/8	0	0	0	0	0	–
Remote Temp 4 MSB – Signed	0x14	RO	SIGN	64	32	16	8	4	2	0	–
Remote Temp 4 LSB – Signed	0x24	RO	1/2	1/4	1/8	0	0	0	0	0	–
Remote Temp 1 MSB – Unsigned	0x19	RO	128	64	32	16	8	4	2	1	–
Remote Temp 1 LSB – Unsigned, Digital Filter Off	0x29	RO	1/2	1/4	1/8	0	0	0	0	0	–
Remote Temp 1 LSB – Unsigned, Digital Filter On						1/16	1/32				
Remote Temp 2 MSB – Unsigned	0x1A	RO	128	64	32	16	8	4	2	1	–
Remote Temp 2 LSB – Unsigned, Digital Filter Off	0x2A	RO	1/2	1/4	1/8	0	0	0	0	0	–
Remote Temp 2 LSB – Unsigned, Digital Filter On						1/16	1/32				
Remote Temp 3 MSB – Unsigned	0x1B	RO	128	64	32	16	8	4	2	1	–
Remote Temp 3 LSB – Unsigned	0x2B	RO	1/2	1/4	1/8	0	0	0	0	0	–
Remote Temp 4 MSB – Unsigned	0x1C	RO	128	64	32	16	8	4	2	1	–
Remote Temp 4 LSB – Unsigned	0x2C	RO	1/2	1/4	1/8	0	0	0	0	0	–
Remote 1 Offset	0x31	R/W	SIGN	32	16	8	4	2	1	1/2	0x00
Remote 2 Offset	0x32	R/W	SIGN	32	16	8	4	2	1	1/2	0x00
Remote 3 Offset	0x33	R/W	SIGN	32	16	8	4	2	1	1/2	0x00
Remote 4 Offset	0x34	R/W	SIGN	32	16	8	4	2	1	1/2	0x00
Configuration	0x03	R/W	–	STBY	–	–	–	–	R4QE	R3QE	0x03
Conversion Rate	0x04	R/W	–	–	–	–	–	–	CR1	CR0	0x02
Channel Conversion Enable	0x05	R/W	–	–	–	R4CE	R3CE	R2CE	R1CE	LCE	0x1F
Filter Setting	0x06	R/W	–	–	–	–	R2F1	R2F0	R1F1	R1F0	0x0F
1-shot	0x0F	WO	–	–	–	–	–	–	–	–	–

Table 11. Register Summary (continued)

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Common Status Register	0x02	RO	BUSY	NR	–	–	SR4F	SR3F	SR2F	SR1F	0x00
Status 1 (Diode Fault)	0x07	RO	R4DO	R4DS	R3DO	R3DS	R2DO	R2DS	R1DO	R1DS	–
Status 2 ($\overline{\text{TCRIT1}}$)	0x08	RO	–	–	–	R4T1	R3T1	R2T1	R1T1	LT1	–
Status 3 ($\overline{\text{TCRIT2}}$)	0x09	RO	–	–	–	R4T2	R3T2	R2T2	R1T2	LT2	–
Status 4 ($\overline{\text{TCRIT3}}$)	0x0A	RO	–	–	–	R4T3	R3T3	R2T3	R1T3	LT3	–
TCRIT1 Mask	0x0C	R/W	–	–	–	R4TM	R3TM	R2T1M	R1T1M	LTM	0x19
TCRIT2 Mask	0x0D	R/W	–	–	–	R4TM	R3TM	R2T2M	R1T2M	LTM	0x00
TCRIT3 Mask	0x0E	R/W	–	–	–	R4TM	R3TM	R2T2M	R1T2M	LTM	0x07
Local Tcrit Limit	0x40	R/W	0	64	32	16	8	4	2	1	0x55
Remote 1 Tcrit-1 Limit	0x41	R/W	128	64	32	16	8	4	2	1	0x6E
Remote 2 Tcrit-1 Limit	0x42	R/W	128	64	32	16	8	4	2	1	0x6E
Remote 3 Tcrit Limit	0x43	R/W	128	64	32	16	8	4	2	1	0x55
Remote 4 Tcrit Limit	0x44	R/W	128	64	32	16	8	4	2	1	0x55
Remote 1 Tcrit-2 and Tcrit-3 Limit	0x49	R/W	128	64	32	16	8	4	2	1	0x55
Remote 2 Tcrit-2 and Tcrit-3 Limit	0x4A	R/W	128	64	32	16	8	4	2	1	0x55
Common Tcrit Hysteresis	0x5A	R/W	0	0	0	16	8	4	2	1	0x0A
Manufacturer ID	0xFE	RO	0	0	0	0	0	0	0	1	0x01
Revision ID	0xFF	RO	0	1	1	1	1	0	0	1	0x79

7.5.1.1 Value Registers

For data synchronization purposes, the MSB register must be read first if the user wants to read both MSB and LSB registers. The LSB will be locked after the MSB is read. The LSB will be unlocked after being read. If the user reads MSBs consecutively, each time the MSB is read, the LSB associated with that temperature will be locked in and override the previous LSB value locked-in

7.5.1.1.1 Local Value Registers

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Local Temp MSB	0x10	RO	SIGN	64	32	16	8	4	2	1	–
Local Temp LSB	0x20	RO	1/2	1/4	1/8	0	0	0	0	0	–

Bit(s)	Bit Name	Read/Write	Description	
7	SIGN	RO	Sign bit	The Local temperature MSB value register range is +127°C to −128°C. The value programmed in this register is used to determine a local temperature error event.
6	64	RO	bit weight 64°C	
5	32	RO	bit weight 32°C	
4	16	RO	bit weight 16°C	
3	8	RO	bit weight 8°C	
2	4	RO	bit weight 4°C	
1	2	RO	bit weight 2°C	
0	1	RO	bit weight 1°C	

Bit(s)	Bit Name	Read/Write	Description	
7	1/2	RO	bit weight 1/2°C (0.5°C)	The Local Limit register range is 0°C to 127°C. The value programmed in this register is used to determine a local temperature error event.
6	1/4	RO	bit weight 1/4°C (0.25°C)	
5	1/8	RO	bit weight 1/8°C (0.125°C)	
4-0	0	RO	Reserved – will report 0 when read.	

7.5.1.1.2 Remote Temperature Value Registers With Signed Format

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Remote Temp 1 MSB – Signed	0x11	RO	SIGN	64	32	16	8	4	2	1	–
Remote Temp 1 LSB – Signed, Digital Filter Off	0x21	RO	1/2	1/8	0	0	0	0	0	0	–
Remote Temp 1 LSB – Signed, Digital Filter On					1/16	1/32					
Remote Temp 2 MSB – Signed	0x12	RO	SIGN	64	32	16	8	4	2	1	–
Remote Temp 2 LSB – Signed, Digital Filter Off	0x22	RO	1/2	1/8	0	0	0	0	0	0	–
Remote Temp 2 LSB – Signed, Digital Filter On					1/16	1/32					
Remote Temp 3 MSB – Signed	0x13	RO	SIGN	64	32	16	8	4	2	1	–
Remote Temp 3 LSB – Signed	0x23	RO	1/2	1/8	0	0	0	0	0	0	–
Remote Temp 4 MSB – Signed	0x14	RO	SIGN	64	32	16	8	4	2	0	–
Remote Temp 4 LSB – Signed	0x24	RO	1/2	1/8	0	0	0	0	0	0	–

The Local temperature MSB value register range is +127°C to −128°C. The value programmed in this register is used to determine a local temperature error event.

Bit(s)	Bit Name	Read/Write	Description
7	SIGN	RO	Sign bit
6	64	RO	bit weight 64°C
5	32	RO	bit weight 32°C
4	16	RO	bit weight 16°C
3	8	RO	bit weight 8°C
2	4	RO	bit weight 4°C
1	2	RO	bit weight 2°C
0	1	RO	bit weight 1°C

Bit(s)	Bit Name	Read/Write	Description
7	1/2	RO	bit weight 1/2°C (0.5°C)
6	1/4	RO	bit weight 1/4°C (0.25°C)
5	1/8	RO	bit weight 1/8°C (0.125°C)
4	0 or 1/16	RO	When the digital filter is disabled this bit will always read 0. When the digital filter is enabled this bit will report 1/16°C (0.0625°C) bit state.
3	0 or 1/32	RO	When the digital filter is disabled this bit will always read 0. When the digital filter is enabled this bit will report 1/32°C (0.03125°C) bit state.
2-0	0	RO	Reserved – will report 0 when read.

7.5.1.1.3 Remote Temperature Value Registers With Unsigned Format

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Remote Temp 1 MSB – Unsigned	0x19	RO	128	64	32	16	8	4	2	1	–
Remote Temp 1 LSB – Unsigned, Digital Filter Off	0x29	RO	1/2	1/8	0	0	0	0	0	0	–
Remote Temp 1 LSB – Unsigned, Digital Filter On					1/16	1/32					
Remote Temp 2 MSB – Unsigned	0x1A	RO	128	64	32	16	8	4	2	1	–
Remote Temp 2 LSB – Unsigned, Digital Filter Off	0x2A	RO	1/2	1/8	0	0	0	0	0	0	–
Remote Temp 2 LSB – Unsigned, Digital Filter On					1/16	1/32					
Remote Temp 3 MSB – Unsigned	0x1B	RO	128	64	32	16	8	4	2	1	–
Remote Temp 3 LSB – Unsigned	0x2B	RO	1/2	1/8	0	0	0	0	0	0	–
Remote Temp 4 MSB – Unsigned	0x1C	RO	128	64	32	16	8	4	2	1	–
Remote Temp 4 LSB – Unsigned	0x2C	RO	1/2	1/8	0	0	0	0	0	0	–

Bit(s)	Bit Name	Read/Write	Description
7	SIGN	RO	bit weight 128°C
6	64	RO	bit weight 64°C
5	32	RO	bit weight 32°C
4	16	RO	bit weight 16°C
3	8	RO	bit weight 8°C
2	4	RO	bit weight 4°C
1	2	RO	bit weight 2°C
0	1	RO	bit weight 1°C

Bit(s)	Bit Name	Read/Write	Description
7	1/2	RO	bit weight 1/2°C (0.5°C)
6	1/4	RO	bit weight 1/4°C (0.25°C)
5	1/8	RO	bit weight 1/8°C (0.125°C)
4	0 or 1/16	RO	When the digital filter is disabled this bit will always read 0. When the digital filter is enabled this bit will report 1/16°C (0.0625°C) bit state.
3	0 or 1/32	RO	When the digital filter is disabled this bit will always read 0. When the digital filter is enabled this bit will report 1/32°C (0.03125°C) bit state.
2-0	0	RO	Reserved – will report 0 when read.

7.5.1.2 Diode Configuration Register

7.5.1.2.1 Remote 1-4 Offset

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Remote 1 Offset	0x31	R/W	SIGN	32	16	8	4	2	1	1/2	0x00
Remote 2 Offset	0x32	R/W	SIGN	32	16	8	4	2	1	1/2	0x00
Remote 3 Offset	0x33	R/W	SIGN	32	16	8	4	2	1	1/2	0x00
Remote 4 Offset	0x34	R/W	SIGN	32	16	8	4	2	1	1/2	0x00

Bit(s)	Bit Name	Read/Write	Description	
7	SIGN	R/W	Sign bit	All registers have 2's complement format. The offset range for each remote is +63.5°C/−64°C. The value programmed in this register is directly added to the actual reading of the ADC and the modified number is reported in the remote value registers.
6	32	R/W	bit weight 32°C	
5	16	R/W	bit weight 16°C	
4	8	R/W	bit weight 8°C	
3	4	R/W	bit weight 4°C	
2	2	R/W	bit weight 2°C	
1	1	R/W	bit weight 1°C	
0	1/2	R/W	bit weight 1/2°C (0.5°C)	

7.5.1.3 Configuration Registers

7.5.1.3.1 Main Configuration Register

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Configuration	0×03	R/W	–	STBY	–	–	–	–	R4QE	R3QE	0×03

Bit(s)	Bit Name	Read/Write	Description
7	–	RO	Reserved will report 0 when read.
6	STBY	R/W	Software Standby 1 – standby (when in this mode one conversion sequence can be initiated by writing to the one-shot register) 0 – active/converting
5–2	–	RO	Reserved – will report 0 when read.
1	R4QE	R/W	Fault queue enable for Remote 4 1– Fault queue enabled 0– Fault queue disabled
0	R3QE	R/W	Fault queue enable for Remote 3 1– Fault queue enabled 0– Fault queue disabled

7.5.1.3.2 Conversion Rate Register

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Conversion Rate	0×04	R/W	–	–	–	–	–	–	CR1	CR0	0×02

Bit(s)	Bit Name	Read/Write	Description	
7-2	–	RO	Reserved – will report 0 when read.	
1-0	CR[1:0]	R/W	Conversion rate control bits modify the time interval for conversion of the channels enabled. The channels enabled are converted sequentially then standby mode enabled for the remainder of the time interval.	
			CR[1:0]	**Conversion Rate**
			00	continuous (30 ms to 143 ms)
			01	0.364 s
			10	1s
			11	2.5 s

7.5.1.3.3 Channel Conversion Enable

When a conversion is disabled for a particular channel it is skipped. The continuous conversion rate is effected all other conversion rates are not effected as extra standby time is inserted to compensate. See *Conversion Rate Register* description.

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Channel Conversion Enable	0×05	R/W	–	–	–	R4CE	R3CE	R2CE	R1CE	LCE	0×1F

Bit(s)	Bit Name	Read/Write	Description
7–5	–	RO	Reserved – will report 0 when read.
4	R4CE	R/W	Remote 4 Temperature Conversion Enable 1– Remote 4 temp conversion enabled 0– Remote 4 temp conversion disabled
3	R3CE	R/W	Remote 3 Temperature Conversion Enable 1– Remote 3 temp conversion enabled 0– Remote 3 temp conversion disabled
2	R2CE	R/W	Remote 2 Temperature Conversion Enable 1– Remote 2 temp conversion enabled 0– Remote 2 temp conversion disabled
1	R1CE	R/W	Remote 1 Temperature Conversion Enable 1– Remote 1 temp conversion enabled 0– Remote 1 temp conversion disabled
0	LCE	R/W	Local Temperature Conversion Enable 1– Local temp conversion enabled 0– Local temp conversion disabled

7.5.1.3.4 Filter Setting

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Filter Setting	0x06	R/W	–	–	–	–	R2F1	R2F0	R1F1	R1F0	0x0F

Bit(s)	Bit Name	Read/Write	Description	
7–4	–	RO	Reserved – will report 0 when read.	
3–2	R2F[1:0]	R/W	Remote Channel 2 Filter Enable Bits	
			R2F[1:0]	**Digital Filter State**
			00	disable all digital filtering
			01	enable basic filter
			10	reserved (do not use)
			11	enable enhanced filter
1–0	R1F[1:0]	R/W	Remote Channel 1 Filter Enable	
			R1F[1:0]	**Filter State**
			00	disable all digital filtering
			01	enable basic filter
			10	reserved (do not use)
			11	enable enhanced filter

7.5.1.3.5 1-Shot

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
1-Shot	0×0F	WO	–	–	–	–	–	–	–	–	–

Bit(s)	Bit Name	Read/Write	Description
7–0	-	WO	Writing to this register activates one conversion for all the enabled channels if the chip is in standby mode (that is,. standby bit = 1). The actual data written does not matter and is not stored.

7.5.1.4 Status Registers

7.5.1.4.1 Common Status Register

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Common Status Register	0×02	RO	BUSY	NR	–	–	SR4F	SR3F	SR2F	SR1F	0×00

Bit(s)	Bit Name	Read/Write	Description
7	BUSY	RO	Busy bit (device converting)
6	NR	RO	Not Ready bit (30 ms), indicates power up initialization sequence is in progress
5–4	–	RO	Reserved – will report 0 when read.
3	SR4F	RO	Status Register 4 Flag: 1 – indicates that Status Register 4 has at least one bit set 0 – indicates that all of Status Register 4 bits are cleared
2	SR3F	RO	Status Register 3 Flag: 1 – indicates that Status Register 3 has at least one bit set 0 – indicates that all of Status Register 3 bits are cleared
1	SR2F	RO	Status Register 2 Flag: 1 – indicates that Status Register 2 has at least one bit set 0 – indicates that all of Status Register 2 bits are cleared
0	SR1F	RO	Status Register 1 Flag: 1 – indicates that Status Register 1 has at least one bit set 0 – indicates that all of Status Register 1 bits are cleared

7.5.1.4.2 Status 1 Register (Diode Fault)

Status fault bits for open or shorted diode (that is,. Short Fault: D+ shorted to Ground or D-; Open Fault: D+ shorted to V_{DD}, or floating). During fault conditions the temperature reading is 0 °C if unsigned value registers are read or –128.000 °C if signed value registers are read.

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Status 1 (Diode Fault)	0×07	RO	R4DO	R4DS	R3DO	R3DS	R2DO	R2DS	R1DO	R1DS	–

Bit(s)	Bit Name	Read/Write	Description
7	R4DO	RO	Remote 4 diode open fault status: 1 – indicates that remote 4 diode has an "open" fault 0 – indicates that remote 4 diode does not have an "open" fault
6	R4DS	RO	Remote 4 diode short fault status: 1 – indicates that remote 4 diode has a "short" fault 0 – indicates that remote 4 diode does not have a "short" fault
5	R3DO	RO	Remote 3 diode open fault status: 1 – indicates that remote 3 diode has an "open" fault 0 – indicates that remote 3 diode does not have an "open" fault
4	R3DS	RO	Remote 3 diode short fault status: 1 – indicates that remote 3 diode has a "short" fault 0 – indicates that remote 3 diode does not have a "short" fault
3	R2DO	RO	Remote 2 diode open fault status: 1 – indicates that remote 2 diode has an "open" fault 0 – indicates that remote 2 diode does not have an "open" fault
2	R2DS	RO	Remote 2 diode short fault status: 1 – indicates that remote 2 diode has a "short" fault 0 – indicates that remote 2 diode does not have a "short" fault
1	R1DO	RO	Remote 1 diode open fault status: 1 – indicates that remote 1 diode has an "open" fault 0 – indicates that remote 1 diode does not have an "open" fault

Bit(s)	Bit Name	Read/Write	Description
0	R1DS	RO	Remote 1 diode short fault status: 1 – indicates that remote 1 diode has a "short" fault 0 – indicates that remote 1 diode does not have a "short" fault

7.5.1.4.3 Status 2 ($\overline{\text{TCRIT1}}$)

Status bits for $\overline{\text{TCRIT1}}$. When one or more of these bits are set and if not masked the $\overline{\text{TCRIT1}}$ output will activate. $\overline{\text{TCRIT1}}$ will deactivate when all these bits are cleared.

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Status 2 ($\overline{\text{TCRIT1}}$)	0×08	RO	–	–	–	R4T1	R3T1	R2T1	R1T1	LT1	–

Bit(s)	Bit Name	Read/Write	Description
7–5	-	RO	Reserved – will report 0 when read.
4	R4T1	RO	Remote 4 Tcrit Status: 1 – indicates that remote 4 reading is greater than or equal to the value set in Remote 4 Tcrit Limit register 0 – indicates that that remote 4 reading is less than the value set in Remote 4 Tcrit Limit register minus the Common Hysteresis value
3	R3T1	RO	Remote 3 Tcrit Status: 1 – indicates that remote 3 reading is greater than or equal to the value set in Remote 3 Tcrit Limit register 0 – indicates that that remote 3 reading is less than the value set in Remote 3 Tcrit Limit register minus the Common Hysteresis value
2	R2T1	RO	Remote 2 Tcrit-1 Status: 1 – indicates that remote 2 reading is greater than or equal to the value set in Remote 2 Tcrit-1 Limit register 0 – indicates that that remote 2 reading is less than the value set in Remote 2 Tcrit-1 Limit register minus the Common Hysteresis value
1	R1T1	RO	Remote 1 Tcrit-1 Status: 1 – indicates that remote 1 reading is greater than or equal to the value set in Remote 1 Tcrit-1 Limit register 0 – indicates that that remote 1 reading is less than the value set in Remote 1 Tcrit-1 Limit register minus the Common Hysteresis value
0	LT1	RO	Local Tcrit Status: 1 – indicates that local reading is greater than or equal to the value set in Local Tcrit Limit register 0 – indicates that local reading is less than the value set in Local Tcrit Limit register minus the Common Hysteresis value

7.5.1.4.4 Status 3 ($\overline{\text{TCRIT2}}$)

Status bits for $\overline{\text{TCRIT2}}$. When one or more of these bits are set and if not masked the $\overline{\text{TCRIT2}}$ output will activate. $\overline{\text{TCRIT2}}$ will deactivate when all these bits are cleared.

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Status 3 ($\overline{\text{TCRIT2}}$)	0×09	RO	–	–	–	R4T2	R3T2	R2T2	R1T2	LT2	–

Bit(s)	Bit Name	Read/Write	Description
7–5	-	RO	Reserved – will report 0 when read.
4	R4T2	RO	Remote 4 Tcrit Status: 1 – indicates that remote 4 reading is greater than or equal to the value set in Remote 4 Tcrit Limit register 0 – indicates that that remote 4 reading is less than the value set in Remote 4 Tcrit Limit register minus the Common Hysteresis value
3	R3T2	RO	Remote 3 Tcrit Status: 1 – indicates that remote 3 reading is greater than or equal to the value set in Remote 3 Tcrit Limit register 0 – indicates that that remote 3 reading is less than the value set in Remote 3 Tcrit Limit register minus the Common Hysteresis value
2	R2T2	RO	Remote 2 Tcrit-2 Status: 1 – indicates that remote 2 reading is greater than or equal to the value set in Remote 2 Tcrit-2 Limit register 0 – indicates that that remote 2 reading is less than the value set in Remote 2 Tcrit-2 Limit register minus the Common Hysteresis value
1	R1T2	RO	Remote 1 Tcrit-2 Status: 1 – indicates that remote 1 reading is greater than or equal to the value set in Remote 1 Tcrit-2 Limit register 0 – indicates that that remote 1 reading is less than the value set in Remote 1 Tcrit-2 Limit register minus the Common Hysteresis value
0	LT2	RO	Local Tcrit Status: 1 – indicates that local reading is greater than or equal to the value set in Local Tcrit Limit register 0 – indicates that local reading is less than the value set in Local Tcrit Limit register minus the Common Hysteresis value

7.5.1.4.5 Status 4 ($\overline{\text{TCRIT3}}$)

Status bits for $\overline{\text{TCRIT3}}$. When one or more of these bits are set and if not masked the $\overline{\text{TCRIT3}}$ output will activate. $\overline{\text{TCRIT3}}$ will deactivate when all these bits are cleared.

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Status 4 ($\overline{\text{TCRIT3}}$)	0×0A	RO	–	–	–	R4T3	R3T3	R2T3	R1T3	LT3	–

Bit(s)	Bit Name	Read/Write	Description
7–5	-	RO	Reserved – will report 0 when read.
4	R4T3	RO	Remote 4 Tcrit Status: 1 – indicates that remote 4 reading is greater than or equal to the value set in Remote 4 Tcrit Limit register 0 – indicates that that remote 4 reading is less than the value set in Remote 4 Tcrit Limit register minus the Common Hysteresis value
3	R3T3	RO	Remote 3 Tcrit Status: 1 – indicates that remote 3 reading is greater than or equal to the value set in Remote 3 Tcrit Limit register 0 – indicates that that remote 3 reading is less than the value set in Remote 3 Tcrit Limit register minus the Common Hysteresis value
2	R2T3	RO	Remote 2 Tcrit-2 Status: 1 – indicates that remote 2 reading is greater than or equal to the value set in Remote 2 Tcrit-2 Limit register 0 – indicates that that remote 2 reading is less than the value set in Remote 2 Tcrit-2 Limit register minus the Common Hysteresis value
1	R1T3	RO	Remote 1 Tcrit-2 Status: 1 – indicates that remote 1 reading is greater than or equal to the value set in Remote 1 Tcrit-2 Limit register 0 – indicates that that remote 1 reading is less than the value set in Remote 1 Tcrit-2 Limit register minus the Common Hysteresis value
0	LT3	RO	Local Tcrit Status: 1 – indicates that local reading is greater than or equal to the value set in Local Tcrit Limit register 0 – indicates that local reading is less than the value set in Local Tcrit Limit register minus the Common Hysteresis value

7.5.1.5 Mask Registers

7.5.1.5.1 TCRIT1 Mask Register

The mask bits in this register allow control over which error events propagate to the $\overline{\text{TCRIT1}}$ pin.

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
$\overline{\text{TCRIT1}}$ Mask	0×0C	R/W	–	–	–	R4TM	R3TM	R2T1M	R1T1M	LTM	0×19

Bit(s)	Bit Name	Read/Write	Description
7-5	–	RO	Reserved – will report 0 when read.
4	R4TM	R/W	Remote 4 Tcrit Mask: 1 – prevents the remote 4 temperature error event from propagating to the $\overline{\text{TCRIT1}}$ pin 0 – allows the remote 4 temperature error event to propagate to the $\overline{\text{TCRIT1}}$ pin
3	R3TM	R/W	Remote 3 Tcrit Mask: 1 – prevents the remote 3 temperature error event from propagating to the $\overline{\text{TCRIT1}}$ pin 0 – allows the remote 3 temperature error event to propagate to the $\overline{\text{TCRIT1}}$ pin
2	R2T1M	R/W	Remote 2 Tcrit-1 Mask: 1 – prevents the remote 2 temperature error event from propagating to the $\overline{\text{TCRIT1}}$ pin 0 – allows the remote 2 temperature error event to propagate to the $\overline{\text{TCRIT1}}$ pin
1	R1T1M	R/W	Remote 1 Tcrit-1 Mask: 1 – prevents the remote 1 temperature error event from propagating to the $\overline{\text{TCRIT1}}$ pin 0 – allows the remote 1 temperature error event to propagate to the $\overline{\text{TCRIT1}}$ pin
0	LTM	R/W	Local Tcrit Mask: 1 – prevents the local temperature error event from propagating to the $\overline{\text{TCRIT1}}$ pin 0 – allows the local temperature error event to propagate to the $\overline{\text{TCRIT1}}$ pin

7.5.1.5.2 $\overline{\text{TCRIT2}}$ Mask Registers

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
$\overline{\text{TCRIT2}}$ Mask	0×0D	R/W	–	–	–	R4TM	R3TM	R2T2M	R1T2M	LTM	0×00

Bit(s)	Bit Name	Read/Write	Description
7-5	–	RO	Reserved – will report 0 when read.
4	R4TM	R/W	Remote 4 Tcrit Mask: 1 – prevents the remote 4 temperature error event from propagating to the $\overline{\text{TCRIT2}}$ pin 0 – allows the remote 4 temperature error event to propagate to the $\overline{\text{TCRIT2}}$ pin
3	R3TM	R/W	Remote 3 Tcrit Mask: 1 – prevents the remote 3 temperature error event from propagating to the $\overline{\text{TCRIT2}}$ pin 0 – allows the remote 3 temperature error event to propagate to the $\overline{\text{TCRIT2}}$ pin
2	R2T2M	R/W	Remote 2 Tcrit-2 Mask: 1 – prevents the remote 2 temperature error event from propagating to the $\overline{\text{TCRIT2}}$ pin 0 – allows the remote 2 temperature error event to propagate to the $\overline{\text{TCRIT2}}$ pin
1	R1T2M	R/W	Remote 1 Tcrit-2 Mask: 1 – prevents the remote 1 temperature error event from propagating to the $\overline{\text{TCRIT2}}$ pin 0 – allows the remote 1 temperature error event to propagate to the $\overline{\text{TCRIT2}}$ pin
0	LTM	R/W	Local Tcrit Mask: 1 – prevents the local temperature error event from propagating to the $\overline{\text{TCRIT2}}$ pin 0 – allows the local temperature error event to propagate to the $\overline{\text{TCRIT2}}$ pin

7.5.1.5.3 $\overline{\text{TCRIT3}}$ Mask Register

The mask bits in this register allow control over which error events propagate to the $\overline{\text{TCRIT3}}$ pin.

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
$\overline{\text{TCRIT3}}$ Mask	0×0E	R/W	–	–	–	R4TM	R3TM	R2T2M	R1T2M	LTM	0×07

Bit(s)	Bit Name	Read/Write	Description
7-5	–	RO	Reserved – will report 0 when read.
4	R4TM	R/W	Remote 4 Tcrit Mask: 1 – prevents the remote 4 temperature error event from propagating to the $\overline{\text{TCRIT3}}$ pin 0 – allows the remote 4 temperature error event to propagate to the $\overline{\text{TCRIT3}}$ pin
3	R3TM	R/W	Remote 3 Tcrit Mask: 1 – prevents the remote 3 temperature error event from propagating to the $\overline{\text{TCRIT3}}$ pin 0 – allows the remote 3 temperature error event to propagate to the $\overline{\text{TCRIT3}}$ pin
2	R2T2M	R/W	Remote 2 Tcrit-2 Mask: 1 – prevents the remote 2 temperature error event from propagating to the $\overline{\text{TCRIT3}}$ pin 0 – allows the remote 2 temperature error event to propagate to the $\overline{\text{TCRIT3}}$ pin
1	R1T2M	R/W	Remote 1 Tcrit-2 Mask: 1 – prevents the remote 1 temperature error event from propagating to the $\overline{\text{TCRIT3}}$ pin 0 – allows the remote 1 temperature error event to propagate to the $\overline{\text{TCRIT3}}$ pin
0	LTM	R/W	Local Tcrit Mask: 1 – prevents the local temperature error event from propagating to the $\overline{\text{TCRIT3}}$ pin 0 – allows the local temperature error event to propagate to the $\overline{\text{TCRIT3}}$ pin

7.5.1.6 Limit Registers

7.5.1.6.1 Local Limit Register

The Local Limit register range is 0°C to 127°C. The value programmed in this register is used to determine a local temperature error event.

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Local Tcrit Limit	0×40	R/W	0	64	32	16	8	4	2	1	0×55

Bit(s)	Bit Name	Read/Write	Description
7	0	R0	Read only bit will always report 0.
6	64	R/W	bit weight 64°C
5	32	R/W	bit weight 32°C
4	16	R/W	bit weight 16°C
3	8	R/W	bit weight 8°C
2	4	R/W	bit weight 4°C
1	2	R/W	bit weight 2°C
0	1	R/W	bit weight 1°C

7.5.1.6.2 Remote Limit Registers

The range for these registers is 0°C to 255°C.

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Remote 1 Tcrit-1 Limit (used by $\overline{\text{TCRIT1}}$ error events)	0x41	R/W	128	64	32	16	8	4	2	1	0x6E
Remote 2 Tcrit-1 Limit (used by $\overline{\text{TCRIT1}}$ error events)	0x42	R/W	128	64	32	16	8	4	2	1	0x6E
Remote 3 Tcrit Limit (used by $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ error events)	0x43	R/W	128	64	32	16	8	4	2	1	0x55
Remote 4 Tcrit Limit (used by $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ error events)	0x44	R/W	128	64	32	16	8	4	2	1	0x55
Remote 1 Tcrit-2 and Tcrit3 Limit (used by $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ error events)	0x49	R/W	128	64	32	16	8	4	2	1	0x55
Remote 2 Tcrit-2 and Tcrit3 Limit (used by $\overline{\text{TCRIT2}}$ and $\overline{\text{TCRIT3}}$ error events)	0x4A	R/W	128	64	32	16	8	4	2	1	0x55

Bit(s)	Bit Name	Read/Write	Description
7	128	R/W	bit weight 128°C
6	64	R/W	bit weight 64°C
5	32	R/W	bit weight 32°C
4	16	R/W	bit weight 16°C
3	8	R/W	bit weight 8°C
2	4	R/W	bit weight 4°C
1	2	R/W	bit weight 2°C
0	1	R/W	bit weight 1°C

Limit assignments for each $\overline{\text{TCRIT}}$ output pin:

OUTPUT PIN	REMOTE 4	REMOTE 3	REMOTE 2	REMOTE 1	LOCAL
$\overline{\text{TCRIT1}}$	Remote 4 Tcrit Limit	Remote 3 Tcrit Limit	Remote 2 Tcrit-1 Limit	Remote 1 Tcrit-1 Limit	Local Tcrit Limit
$\overline{\text{TCRIT2}}$	Remote 4 Tcrit Limit	Remote 3 Tcrit Limit	Remote 2 Tcrit-2 Limit	Remote 1 Tcrit-2 Limit	Local Tcrit Limit
$\overline{\text{TCRIT3}}$	Remote 4 Tcrit Limit	Remote 3 Tcrit Limit	Remote 2 Tcrit-2 Limit	Remote 1 Tcrit-2 Limit	Local Tcrit Limit

7.5.1.6.3 Common Tcrit Hysteresis Register

The hysteresis register range is 0°C to 32°C. The value programmed in this register is used to modify all the limit values for decreasing temperature.

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Common Tcrit Hysteresis	0×5A	R/W	0	0	0	16	8	4	2	1	0×0A

Bit(s)	Bit Name	Read/Write	Description
7	0	RO	Read only bit will always report 0.
6	0	RO	Read only bit will always report 0.
5	0	RO	Read only bit will always report 0.
4	16	R/W	bit weight 16°C
3	8	R/W	bit weight 8°C
2	4	R/W	bit weight 4°C
1	2	R/W	bit weight 2°C
0	1	R/W	bit weight 1°C

7.5.1.7 Identification Registers

Register Name	Command Byte (Hex)	Read/ Write	D7	D6	D5	D4	D3	D2	D1	D0	POR Default (Hex)
Manufacturer ID	0×FE	RO	0	0	0	0	0	0	0	1	0×01
Revision ID	0×FF	RO	0	1	1	1	1	0	0	1	0×79

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM95214 can be applied easily in the same way as other integrated-circuit temperature sensors, and its remote diode sensing capability allows it to be used in new ways as well. It can be soldered to a printed-circuit board, and because the path of best thermal conductivity is between the die and the pins, its temperature will effectively be that of the printed-circuit board lands and traces soldered to the LM95214's pins. This presumes that the ambient air temperature is almost the same as the surface temperature of the printed-circuit board; if the air temperature is much higher or lower than the surface temperature, the actual temperature of the LM95214 die will be at an intermediate temperature between the surface and air temperatures. Again, the primary thermal conduction path is through the leads, so the circuit board temperature will contribute to the die temperature much more strongly than will the air temperature.

8.2 Typical Application

To measure temperature external to the LM95214's die, incorporates remote diode sensing technology. This diode can be located on the die of a target IC, allowing measurement of the IC's temperature, independent of the LM95214's temperature. A discrete diode can also be used to sense the temperature of external objects or ambient air. Remember that a discrete diode's temperature will be affected, and often dominated, by the temperature of its leads. Most silicon diodes do not lend themselves well to this application. TI recommends that an MMBT3904 transistor base emitter junction be used with the collector tied to the base.

The LM95214 can measure a diode-connected transistor such as the MMBT3904 or the thermal diode found in an AMD processor. The LM95214 has been optimized to measure the MMBT3904 remote thermal diode the offset register can be used to calibrate for other thermal diodes easily. The LM95214 does not include TruTherm™ technology that allows sensing of sub-micron geometry process thermal diodes. For this application the LM95234 would be better suited.

The LM95234 has been specifically optimized to measure the remote thermal diode integrated in a typical Intel processor on 65 nm or 90 nm process or an MMBT3904 transistor. Using the Remote Diode Model Select register found in the LM95234 any of the four remote inputs can be optimized for a typical Intel processor on 65 nm or 90 nm process or an MMBT3904.

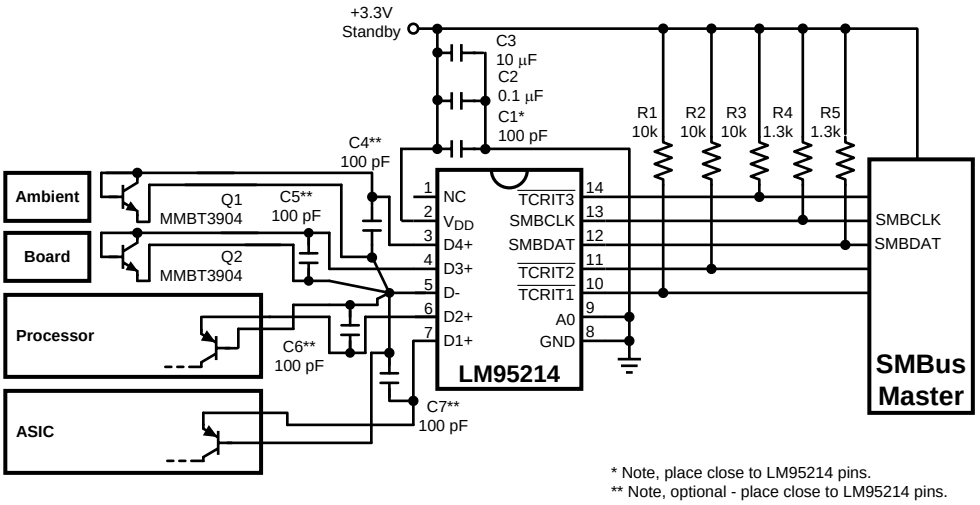


Figure 25. Typical Application

Typical Application (continued)

8.2.1 Design Requirements

The LM95214 operates only as a slave device and communicates with the host through the SMBus serial interface essentially compatible with I^2C. SMBCLK is the clock input pin, SMBDATA is a bidirectional data pin, and $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, $\overline{\text{TCRIT3}}$ are the output pins. The LM95214 requires a pullup resistor on the SMBCLK, SMBDATA, and $\overline{\text{TCRIT1}}$, $\overline{\text{TCRIT2}}$, $\overline{\text{TCRIT3}}$ pins due to an open-drain output. It is very important to consider the pullup resistor for the I^2C systems. The recommended value for the pullup resistors is in Figure 25. Use a ceramic capacitor type with a temperature rating from –40°C to +125°C, placed as close as possible to the V_{DD} pin of the LM95214. The decoupling capacitor reduces any noise induced by the system. A0 (pin 6) can be connected to either Low, Mid-Supply or High voltages for address selection for configuring three possible unique slave ID addresses; *SMBus Interface* explains the addressing scheme.

8.3 Diode Non-Ideality

8.3.1 Diode Non-Ideality Factor Effect on Accuracy

When a transistor is connected as a diode, the following relationship holds for variables V_{BE}, T and I_F:

$$I_F = I_S \times \left[e^{\left(\frac{V_{BE}}{\eta \times V_t}\right)} - 1 \right]$$

where

- $V_t = \frac{kT}{q}$
- q = 1.6×10^{-19} Coulombs (the electron charge)
- T = Absolute Temperature in Kelvin
- k = 1.38×10^{-23} joules/K (Boltzmann's constant)
- η is the non-ideality factor of the process the diode is manufactured on
- I_S = Saturation Current and is process dependent
- I_f = Forward Current through the base-emitter junction
- V_{BE} = Base-Emitter Voltage drop (1)

In the active region, the –1 term is negligible and may be eliminated, yielding Equation 2

$$I_F = I_S \times \left[e^{\left(\frac{V_{BE}}{\eta \times V_t}\right)} \right] \quad (2)$$

In Equation 2, η and I_S are dependant upon the process that was used in the fabrication of the particular diode. By forcing two currents with a very controlled ratio(I_{F2} / I_{F1}) and measuring the resulting voltage difference, it is possible to eliminate the I_S term. Solving for the forward voltage difference yields the relationship:

$$\Delta V_{BE} = \eta \times \left(\frac{kT}{q}\right) \times \ln\left(\frac{I_{F2}}{I_{F1}}\right) \quad (3)$$

Solving Equation 3 for temperature yields:

$$T = \frac{q \times \Delta V_{BE}}{\eta \times k \times \ln\left(\frac{I_{F2}}{I_{F1}}\right)} \quad (4)$$

Equation 4 holds true when a diode connected transistor such as the MMBT3904 is used. When this *diode* equation is applied to an integrated diode such as a processor transistor with its collector tied to GND as shown in Figure 26 it will yield a wide non-ideality spread. This wide non-ideality spread is not due to true process variation but due to the fact that Equation 4 is an approximation.

Diode Non-Ideality (continued)

Texas Instruments invented TruTherm beta cancellation technology that uses the transistor equation, Equation 5, which is a more accurate representation of the topology of the thermal diode found in some sub-micron FPGAs or processors.

$$T = \frac{q \times \Delta V_{BE}}{\eta \times k \times \ln\left(\frac{I_{C2}}{I_{C1}}\right)} \quad (5)$$

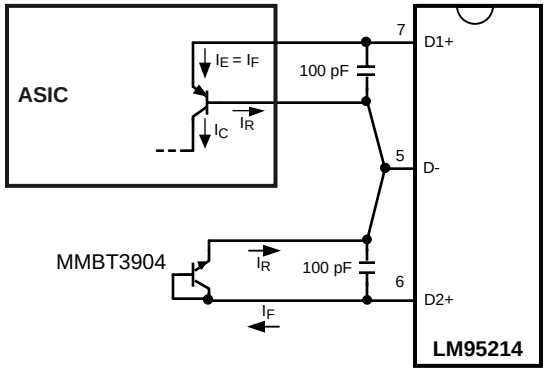


Figure 26. Thermal Diode Current Paths

TruTherm technology can be found in the LM95234 four channel remote diode sensor that is pin and register compatible with the LM95214. The LM95214 does not support this technology.

8.3.2 Calculating Total System Accuracy

The voltage seen by the LM95214 also includes the $I_F R_S$ voltage drop of the series resistance. The non-ideality factor, η, is the only other parameter not accounted for and depends on the diode that is used for measurement. Because ΔV_{BE} is proportional to both η and T, the variations in η cannot be distinguished from variations in temperature. Because the non-ideality factor is not controlled by the temperature sensor, it will directly add to the inaccuracy of the sensor. For the for Intel processor on 65 nm process, Intel specifies a +4.06%/−0.897% variation in η from part to part when the processor diode is measured by a circuit that assumes diode equation, Equation 4, as true. As an example, assume a temperature sensor has an accuracy specification of ±1.0°C at a temperature of 80°C (353 Kelvin) and the processor diode has a non-ideality variation of +1.19%/−0.27%. The resulting system accuracy of the processor temperature being sensed will be:

T_{ACC} = + 1.0°C + (+4.06% of 353 K) = +15.3°C

and

T_{ACC} = –1.0°C + (−0.89% of 353 K) = –4.1°C

The next error term to be discussed is that due to the series resistance of the thermal diode and printed-circuit board traces. The thermal diode series resistance is specified on most processor data sheets. For the MMBT3904 transistor, this is specified at 0 Ω typical. The LM95214 accommodates the typical series resistance of a circuit with the offset register compensation. The error that is not accounted for is the spread of the thermal diodes series resistance. If a circuit has a series resistance spread that is 2.79 Ω to 6.24 Ω or 4.515 Ω ±1.73 Ω, the 4.515 Ω can be cancelled out with the offset register setting. The ±1.73 Ω spread cannot be cancelled out. The equation to calculate the temperature error due to series resistance (T_{ER}) for the LM95214 is simply:

$$T_{ER} = \left(0.62 \frac{^{\circ}C}{\Omega}\right) \times R_{PCB} \quad (6)$$

Solving Equation 6 for R_{PCB} equal to ±1.73 Ω results in the additional error due to the spread in the series resistance of ±1.07°C. The bulk of the error caused by the 4.515 Ω will cause a positive offset in the temperature reading of 2.79°C, which can be cancelled out by setting the offset register to –2.75°C. The spread in error cannot be canceled out, as it would require measuring each individual thermal diode device. This is quite difficult and impractical in a large volume production environment.

Diode Non-Ideality (continued)

Equation 6 can also be used to calculate the additional error caused by series resistance on the printed circuit board. Because the variation of the PCB series resistance is minimal, the bulk of the error term is always positive and can simply be cancelled out by subtracting it from the output readings of the LM95214.

PROCESSOR FAMILY	DIODE EQUATION η_D, non-ideality			SERIES R,Ω
	MIN	TYP	MAX	
Pentium III CPUID 67h	1	1.0065	1.0125	
Pentium III CPUID 68h/PGA370Socket/ Celeron	1.0057	1.008	1.0125	
Pentium 4, 423 pin	0.9933	1.0045	1.0368	
Pentium 4, 478 pin	0.9933	1.0045	1.0368	
Pentium 4 on 0.13 micron process, 2 - 3.06 GHz	1.0011	1.0021	1.0030	3.64
Pentium 4 on 90 nm process	1.0083	1.011	1.023	3.33
Intel Processor on 65 nm process	1.000	1.009	1.050	4.52
Pentium M (Centrino)	1.00151	1.00220	1.00289	3.06
MMBT3904		1.003		
AMD Athlon MP model 6	1.002	1.008	1.016	
AMD Athlon 64	1.008	1.008	1.096	
AMD Opteron	1.008	1.008	1.096	
AMD Sempron		1.00261		0.93

8.3.3 Compensating for Different Non-Ideality

To compensate for the errors introduced by non-ideality, the temperature sensor is calibrated for a particular processor. Texas Instruments temperature sensors are always calibrated to the typical non-ideality and series resistance of a given transistor type. The LM95214 is calibrated for the non-ideality factor and series resistance values of the MMBT3904 transistor without the requirement for additional trims. When a temperature sensor calibrated for a particular thermal diode type is used with a different thermal diode type, additional errors are introduced.

Temperature errors associated with non-ideality of different processor types may be reduced in a specific temperature range of concern through use of software calibration. Typical Non-ideality specification differences cause a gain variation of the transfer function, therefore the center of the temperature range of interest must be the target temperature for calibration purposes. The Equation 7 can be used to calculate the temperature correction factor (T_{CF}) required to compensate for a target non-ideality differing from that supported by the LM95214.

$$T_{CF} = \left(\frac{\eta_S - \eta_{PROCESSOR}}{\eta_S} \right) x \, (T_{CR} + 273K) \tag{7}$$

where

- η_S = LM95214 non-ideality for accuracy specification
- $\eta_{PROCESSOR}$ = Processor thermal diode typical non-ideality
- T_{CR} = center of the temperature range of interest in °C

The correction factor must be directly added to the temperature reading produced by the LM95214. For example when using the LM95214, with the 3904 mode selected, to measure a AMD Athlon processor, with a typical non-ideality of 1.008, for a temperature range of 60°C to 100°C the correction factor would calculate to:

$$T_{CF} = \left(\frac{1.003 - 1.008}{1.003} \right) \cdot (80 + 273) = -1.75^{\circ}C \tag{8}$$

Therefore, 1.75°C must be subtracted from the temperature readings of the LM95214 to compensate for the differing typical non-ideality target.

9 Power Supply Recommendations

The LM95214 operates on a power-supply range from 3.0 V to 3.6 V. A power-supply bypass capacitor is required, which much be placed as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 100 nF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

In a noisy environment, such as a processor mother board, layout considerations are very critical. Noise induced on traces running between the remote temperature diode sensor and the LM95214 can cause temperature conversion errors. Keep in mind that the signal level the LM95214 is trying to measure is in microvolts. The following guidelines must be followed:

1. V_{DD} must be bypassed with a 0.1-µF capacitor in parallel with 100 pF. The 100-pF capacitor must be placed as close as possible to the power supply pin. A bulk capacitance of approximately 10 µF must be in the near vicinity of the LM95214.
2. Ti recommends the use of a 100-pF diode bypass capacitor to filter high-frequency noise, but it may not be necessary. Make sure the traces to the 100-pF capacitor are matched. Place the filter capacitors close to the LM95214 pins.
3. Ideally, the LM95214 must be placed within 10 cm of the Processor diode pins with the traces being as straight, short and identical as possible. Trace resistance of 1 Ω can cause as much as 0.62°C of error. This error can be compensated by using simple software offset compensation.
4. Diode traces must be surrounded by a GND guard ring to either side, above and below if possible. This GND guard must not be between the D+ and D− lines. In the event that noise does couple to the diode lines it would be ideal if it is coupled common mode. That is equally to the D+ and D− lines.
5. Avoid routing diode traces in close proximity to power supply switching or filtering inductors.
6. Avoid running diode traces close to or parallel to high-speed digital and bus lines. Diode traces must be kept at least 2 cm apart from the high-speed digital traces.
7. If it is necessary to cross high-speed digital traces, the diode traces and the high-speed digital traces must cross at a 90 degree angle.
8. The ideal place to connect the LM95214's GND pin is as close as possible to the Processors GND associated with the sense diode.
9. Leakage current between D+ and GND and between D+ and D− must be kept to a minimum. Thirteen nano-amperes of leakage can cause as much as 0.2°C of error in the diode temperature reading. Keeping the printed-circuit board as clean as possible will minimize leakage current.

Noise coupling into the digital lines greater than 400 mVp-p (typical hysteresis) and undershoot less than 500 mV below GND, may prevent successful SMBus communication with the LM95214. SMBus no acknowledge is the most common symptom, causing unnecessary traffic on the bus. Although the SMBus maximum frequency of communication is rather low (100 kHz maximum), care still needs to be taken to ensure proper termination within a system with multiple parts on the bus and long printed-circuit board traces. An RC lowpass filter with a 3-dB corner frequency of about 40 MHz is included on the LM95214's SMBCLK input. Additional resistance can be added in series with the SMBDAT and SMBCLK lines to further help filter noise and ringing. Minimize noise coupling by keeping digital traces out of switching power supply areas as well as ensuring that digital lines containing high-speed data communications cross at right angles to the SMBDAT and SMBCLK lines.

10.2 Layout Example

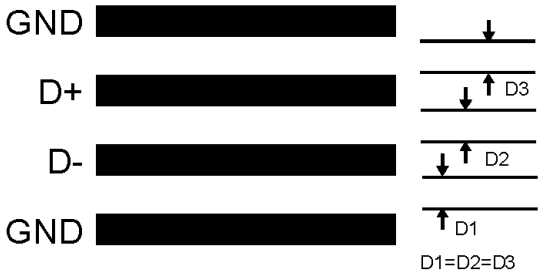


Figure 27. Ideal Diode Trace Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM95214CISD/NOPB	ACTIVE	WSON	NHL	14	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 140	95214CI	Samples
LM95214CISDX/NOPB	ACTIVE	WSON	NHL	14	4500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 140	95214CI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

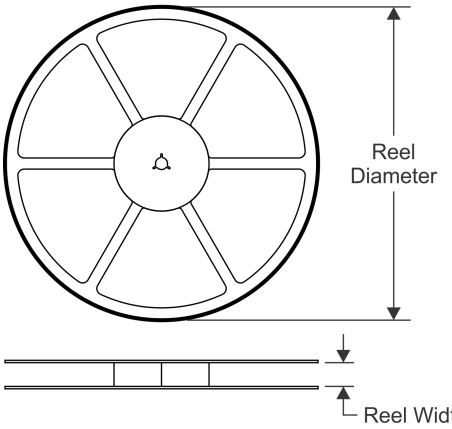
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

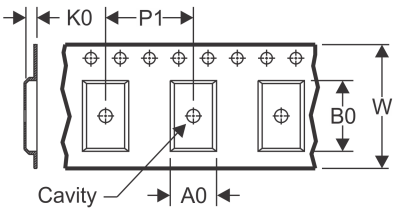
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

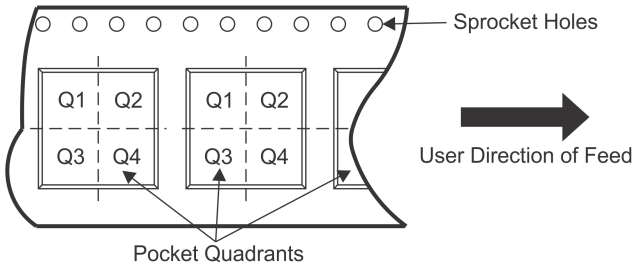


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

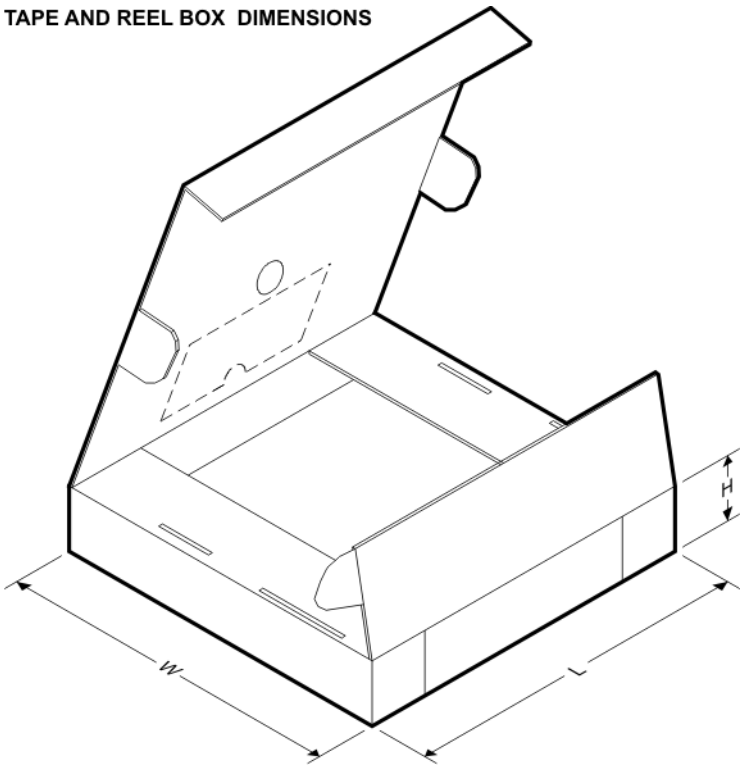
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM95214CISD/NOPB	WSON	NHL	14	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM95214CISDX/NOPB	WSON	NHL	14	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

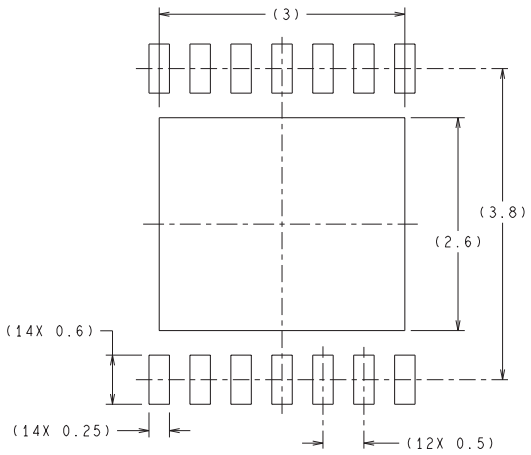
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

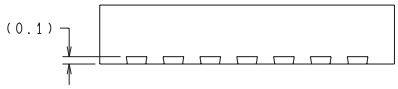
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM95214CISD/NOPB	WSON	NHL	14	1000	210.0	185.0	35.0
LM95214CISDX/NOPB	WSON	NHL	14	4500	367.0	367.0	35.0

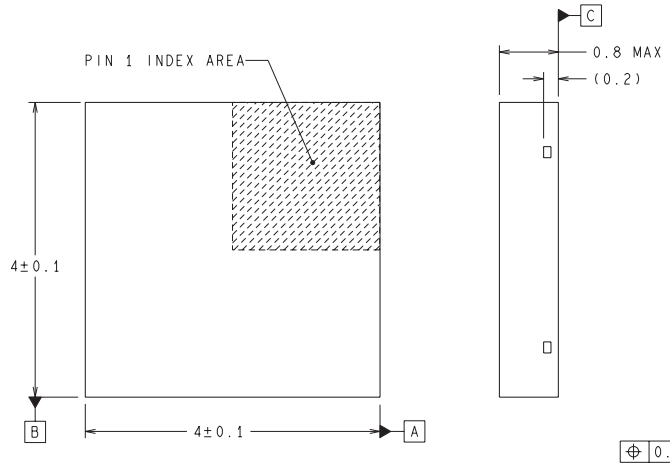
NHL0014B

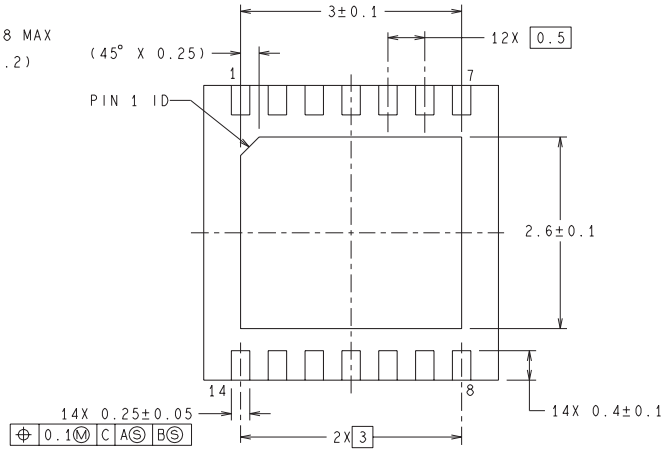


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







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