TEXAS INSTRUMENTS

User's Guide

SLUU379–November 2009

Using the TPS51727EVM, a Dual-Phase, Eco-mode™ Step-Down Power Management IC for 40-A+ Application

The TPS51727EVM evaluation module (EVM) is a dual-phase, ECO-mode™synchronous buck converter providing a fixed 1.5-V or 4-bit VID with 0.875-V to 1.25-V output range at up to 40 A from a 12-V input bus. The EVM uses the TPS51727 synchronous buck controller with selectable 200/300/400/500 kHz.

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1 Description

The TPS51727EVM is designed to use a regulated 12-V (8-V to 14-V) bus to produce a high-current, regulated 1.5 V or 4-bit digital-to-analog converter (DAC) with a 0.875-V to 1.25-V output range at up to 40 A of the load current. The TPS51727EVM is designed to demonstrate the TPS51727 in a typical, low-voltage application while providing a number of test points to evaluate the performance of the TPS51727.

1.1 2.1 Typical Applications

- High-current, low-voltage application for adapter and battery
- Distributed power supplies
- General dc-dc converters

1.2 Features

The TPS51727EVM features:

- Fixed 1.5 V or 4-bit VID with 0.875-V to 1.25-V output range
- 40-Adc steady-state current
- Auto-phase control to optimize efficiency depending on the load requirement
- Selectable 200/300/400/500-kHz switching frequency
- Selectable current limit
- Selectable output overshoot reduction (OSR™)
- J11 for enable function
- Convenient test points for probing critical waveforms
- Six-layer printed-circuit board with 2-oz copper on the outside layers

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2 Electrical Performance Specifications

Table 1. TPS51727EVM Electrical Performance Specifications

Parameter	Test Conditions	Min	Typ	Max	Units
Input Characteristics					
Voltage range	VIN	8	12	14	V
Maximum input current	VIN = 8 V, Io = 40 A			8.5	A
No load input current	Vin = 14 V, Io = 0 A			20	mA
Output Characteristics					
Output voltage VOUT	1.5 V or 0.875–1.250 V		1.25		V
Output voltage regulation	Line regulation			0.1%	
	Load regulation (Load line Rout = –1.8 mΩ)		–3.0% +6.7%		
Output voltage ripple	Vin = 12 V, Io = 20 A			30	mVpp
Output load current		0		40	A
Output over current			50		A
System Characteristics					
Switching frequency	Selectable	200	300	500	kHz
Peak efficiency	Vin = 12 V, 1.25 V/15 A		91.66%		
Full load efficiency	Vin = 12 V, 1.25 V/40 A		88.79%		
Operating temperature			25		°C

3 Schematic

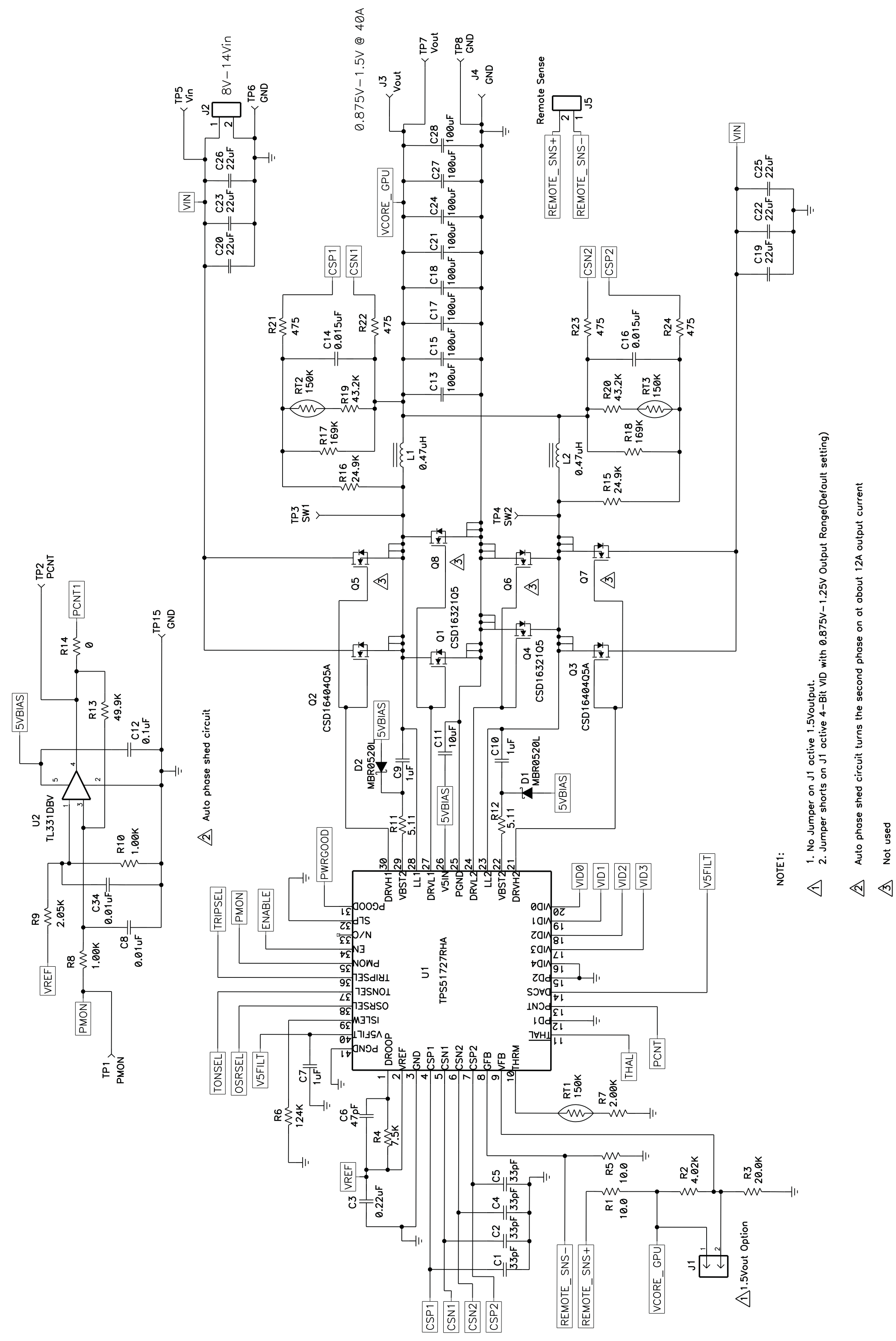

Figure 1. TPS51727EVM Schematic, Sheet 1

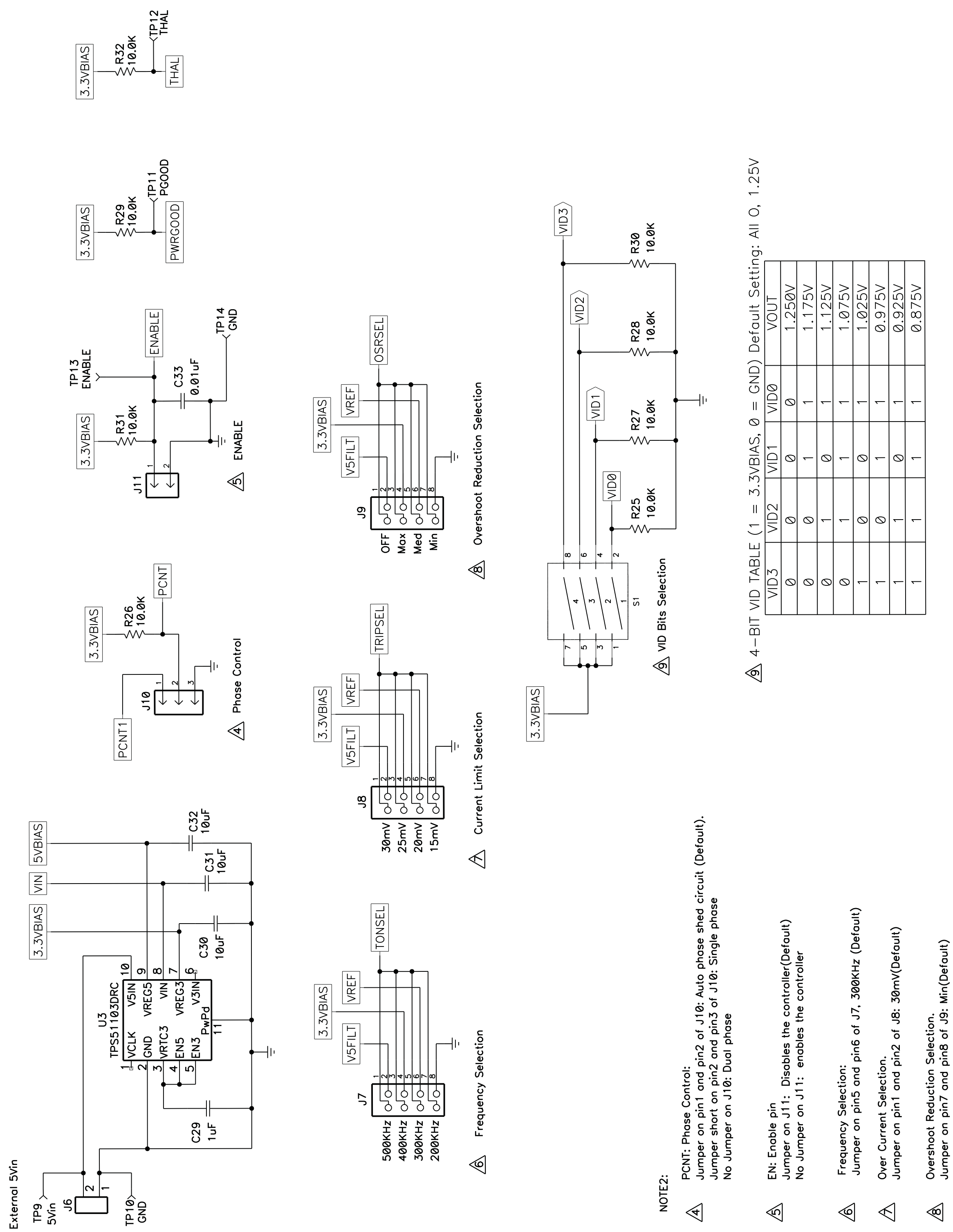

Figure 2. TPS51727EVM Schematic, Sheet 2

4 Test Setup

4.1 Test Equipment

Voltage Source: The input voltage source Vin must be a 0-V to 14-V variable dc source capable of supplying 20 Adc. Connect Vin to J2 as shown in Figure 4.

Multimeters: A 0-V to 14-V voltmeter must be used to measure Vin at TP5 (Vin) and TP6 (GND). A 0-V to 5-V voltmeter must be used for Vout measurement at TP7(Vout) and TP8(GND). A 0-A to 20-A current meter (A1) as shown in Figure 4 is used for input current measurements.

Output Load: The output load must be an electronic constant resistance mode load capable of 0 A to 50 Adc at 1.5 V.

Oscilloscope: A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope must be set for 1-MΩ impedance, 20-MHz bandwidth, ac coupling, 1-µs/division horizontal resolution, 20-mV/division vertical resolution. Test points TP7 and TP8 can be used to measure the output ripple voltage by placing the oscilloscope probe tip through TP7 and holding the ground barrel TP8 as shown in Figure 3. Using a leaded ground connection may induce additional noise due to the large ground loop.

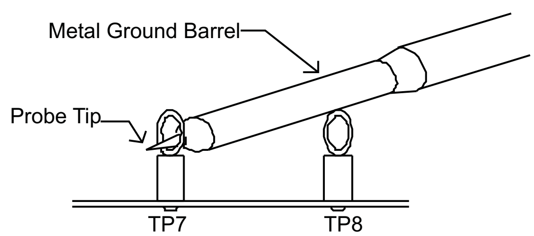

Figure 3. Tip and Barrel Measurement for Vout Ripple

Fan: Some of the components in this EVM may get hot and approach temperatures of 60ºC during operation. A small fan capable of 200-400 LFM is recommended to reduce component temperatures while the EVM is operating. The EVM must not be probed while the fan is not running.

Recommended Wire Gauge: For VIN to J2(12-V input) the recommended wire size is 2x AWG 14 per input connection, with the total length of wire less than 4 feet (2-foot input, 2-foot return). For J3, J4 to LOAD, the minimum recommended wire size is 4x AWG 14, with the total length of wire less than 4 feet (2-foot output, 2-foot return).

4.2 Recommended Test Setup

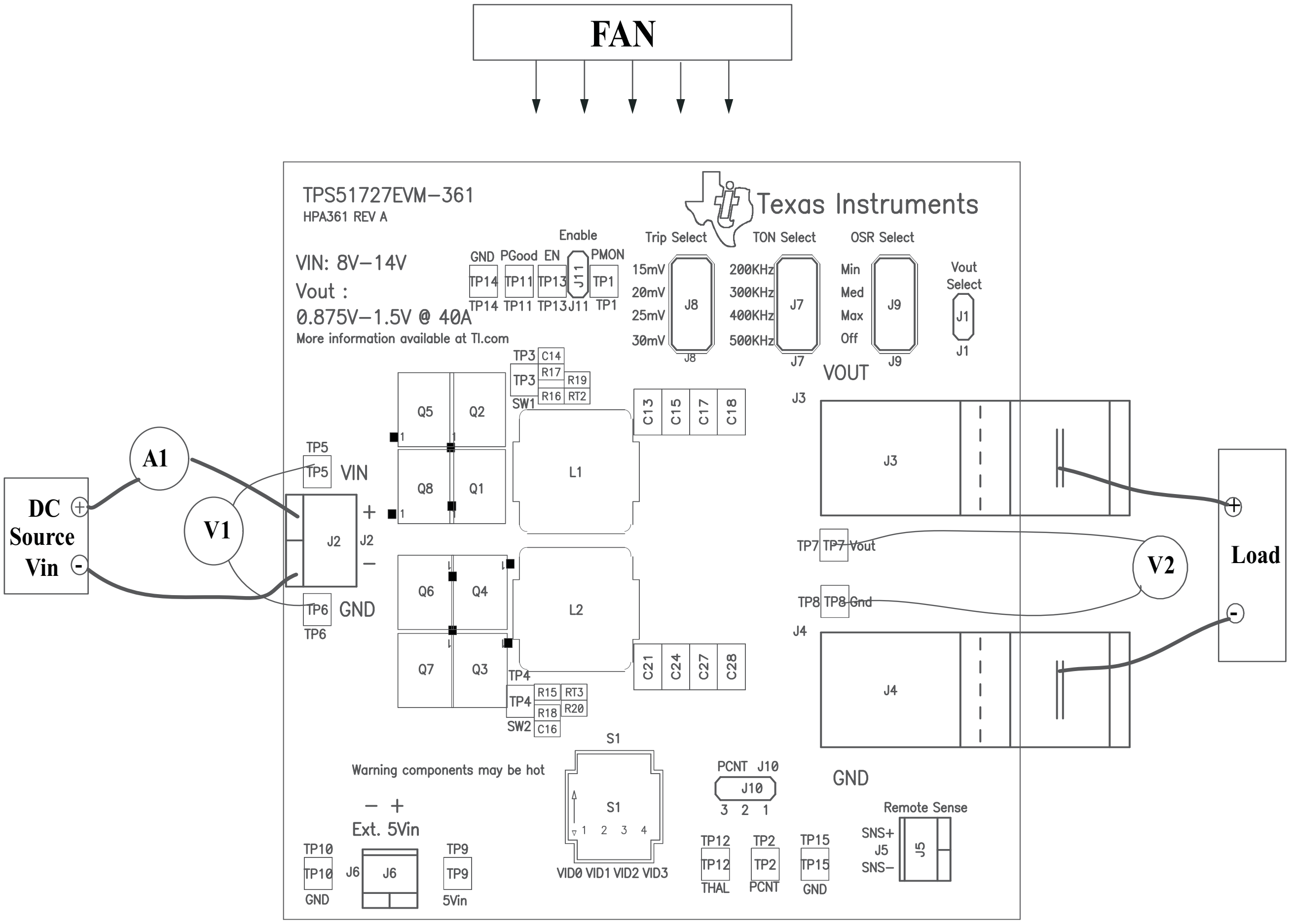

Figure 4. TPS51727EVM Recommended Test Setup

Figure 4 is the recommended test setup to evaluate the TPS51727EVM. Working at an ESD workstation, ensure that any wrist straps, bootstraps, or mats are connected, referencing the user to earth ground before power is applied to the EVM.

Input Connections:

1. Prior to connecting the dc input source Vin, it is advisable to limit the source current from Vin to 15 A maximum. Ensure that Vin is initially set to 0 V and connected as shown in Figure 4.
2. Connect a voltmeter V1 at TP5 (Vin) and TP6 (GND) to measure the input voltage.

Output Connections:

1. Connect Load to J3 and J4, and set Load to constant resistance mode to sink 0 Adc before Vin is applied.
2. Connect a voltmeter V2 at TP7(Vout) and TP8 (GND) to measure the output voltage.

Other Connections:

Place a fan as shown in Figure 4 and turn it on, ensuring that air is flowing across the EVM.

5 Configuration

The user can configure this EVM per the following configurations

5.1 Current Limit Trip Selection (J8: Trip Select)

The overcurrent protection (OCP) can be set by J8 Trip Select.

Default setting is 30 mV.

Table 2. Current Limit Trip Selection

Jumper Set To	Trip Select	OCP Limit per Phase (Typical)
Top (7-8 pin shorted)	GND (15 mV)	15.1 A
Second (5-6 pin shorted)	VREF (20 mV)	18.4 A
Third (3-4 pin shorted)	3.3VBIAS (25 mV)	22.3 A
Bottom (1-2 pin shorted)	**V5FILT(30 mV)**	**27.9 A**

5.2 Frequency Selection (J7: TON Select)

The operating frequency can be set by J7 TON Select.

Default setting is 300 kHz.

Table 3. Frequency Selection

Jumper Set To	TON Select	Frequency (kHz)
Top (7-8 pin shorted)	GND	200
Second (5-6 pin shorted)	**VREF**	**300**
Third (3-4 pin shorted)	3.3VBIAS	400
Bottom (1-2 pin shorted)	V5FILT	500

5.3 Overshoot Reduction Selection (J9: OSR™ Select)

The overshoot reduction can be set by J9 OSR™ Select.

Default setting is Minimum.

Table 4. Overshoot Reduction Selection

Jumper Set To	OSR	Overshoot Voltage
Top (7-8 pin shorted)	**GND (Minimum)**	**Minimum**
Second (5-6 pin shorted)	VREF (Medium)	Medium
Third (3-4 pin shorted)	3.3VBIAS (Maximum)	Maximum
Bottom (1-2 pin shorted)	V5FILT (Off)	OSR Off

5.4 VID Bits Selection (S1)

The output voltage can be set by Switch S1(VID Bits).

Default setting is 0000.

Table 5. VID Bits Selection(1)

VID3	VID2	VID1	VID0	Vout(V)
0	**0**	**0**	**0**	1.250
0	0	1	1	1.175
0	1	0	1	1.125
0	1	1	1	1.075
1	0	0	1	1.025
1	0	1	1	0.975

(1) 4-Bit VID Table (1=3.3VBIAS=on, 0=GND=off)

Table 5. VID Bits Selection[(1)] (continued)

VID3	VID2	VID1	VID0	Vout(V)
1	1	0	1	0.925
1	1	1	1	0.875

5.5 Phase Control Selection (PCNT)

The phase control can be set by J10 (PCNT).

Default setting is jumper on pin1 and pin 2 of J10 for Auto phase control.

Table 6. Phase Control Selection

JUMPER SET TO	PHASE CONTROL
1-2 pin shorted	**Auto phase control (around 12-A change to dual phase)**
2-3 pin shorted	Single phase
No Jumper	Dual phase

5.6 1.5-V Output Voltage Selection (J1: 1.5-Vout Selection)

The 1.5-V output can be set by J1 (Vout Select).

Default setting: Jumper shorts on J1 to set 1.25-V output.

Table 7. 1.5-V Output Option Selection

JUMPER SET TO	OUTPUT RANGE
No Jumper	1.5-V output
Jumper shorted	**4-bits VID with 0.875 V – 1.25 V**

6 Test Procedure

6.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Ensure that Load is set to constant resistance mode and to sink 0 Adc.
2. Ensure that the jumper provided in the EVM is set to short on J11 before Vin is applied.
3. Increase Vin from 0 V to 12 V. Using V1 to measure input voltage.
4. Remove the jumper on J11 to enable the controller.
5. Vary Load from 0 Adc to 40 Adc; Vout must remain in load regulation.
6. Vary Vin from 8 V to 14 V; Vout must remain in line regulation.
7. Put the jumper on J11 to disable the controller.
8. Decrease Load to 0 A
9. Decrease Vin to 0 V.

6.2 List of Test Points

Table 8. Functions of Each Test Points

Test Points	Name	Description
TP1	PMON	Power Monitor Output, SeeFigure 8.
TP2	PCNT	Phase Control Input
TP3	SW1	Phase 1 Switching Node
TP4	SW2	Phase 2 Switching Node

Table 8. Functions of Each Test Points (continued)

Test Points	Name	Description
TP5	Vin	12 Vin
TP6	GND	12 Vin GND
TP7	Vout	Vout
TP8	GND	Vout GND
TP9	5Vin	External 5 Vin(optional)
TP10	GND	External 5 Vin GND
TP11	PGOOD	Power Good, Active High
TP12	THAL	Thermal Alarm, Active Low
TP13	ENABLE	Enable, Active High
TP14	GND	PGOOD GND
TP15	GND	PCNT GND

6.3 Equipment Shutdown

1. Shut down Load.
2. Shut down Vin.
3. Shut down fan.

7 Performance Data and Typical Characteristic Curves

Figure 5 through Figure 14 present typical performance curves for TPS51727EVM.

7.1 Efficiency

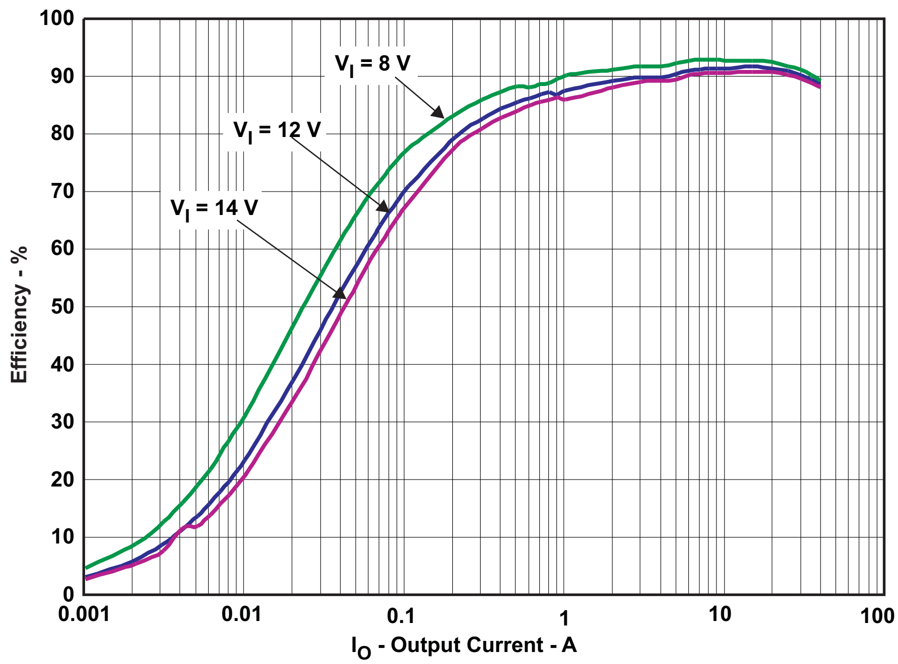

Figure 5. TPS51727EVM Efficiency

7.2 Load Regulation

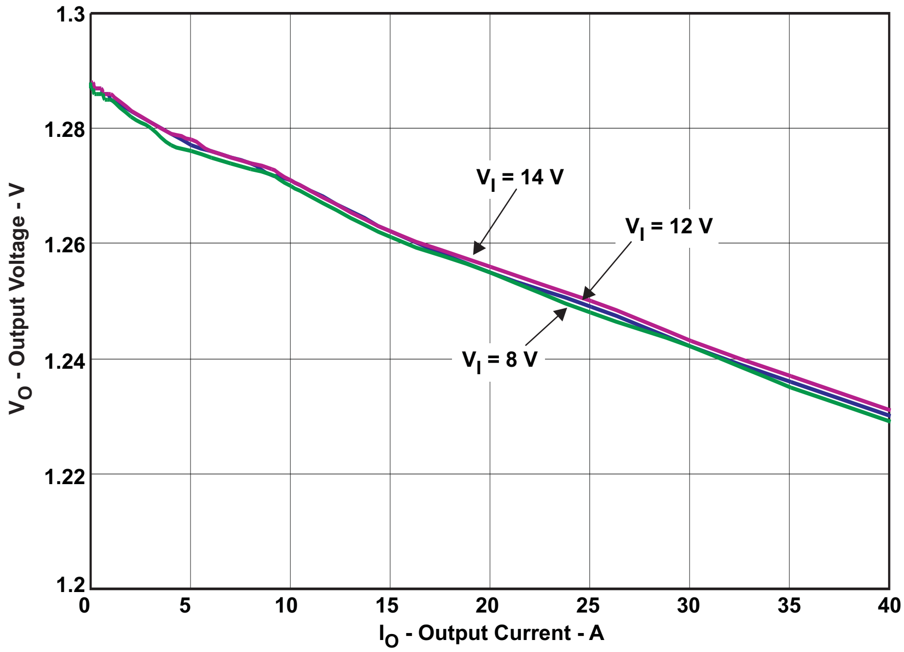

Figure 6. TPS51727 Load Regulation

7.3 Line Regulation

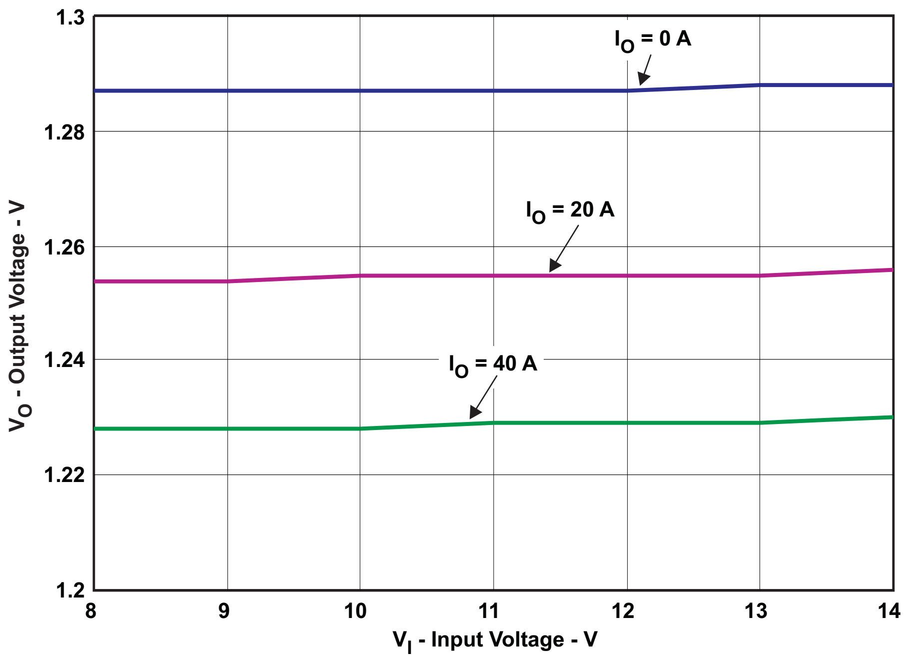

Figure 7. TPS51727 Line Regulation

7.4 Power Monitor Voltage Curve

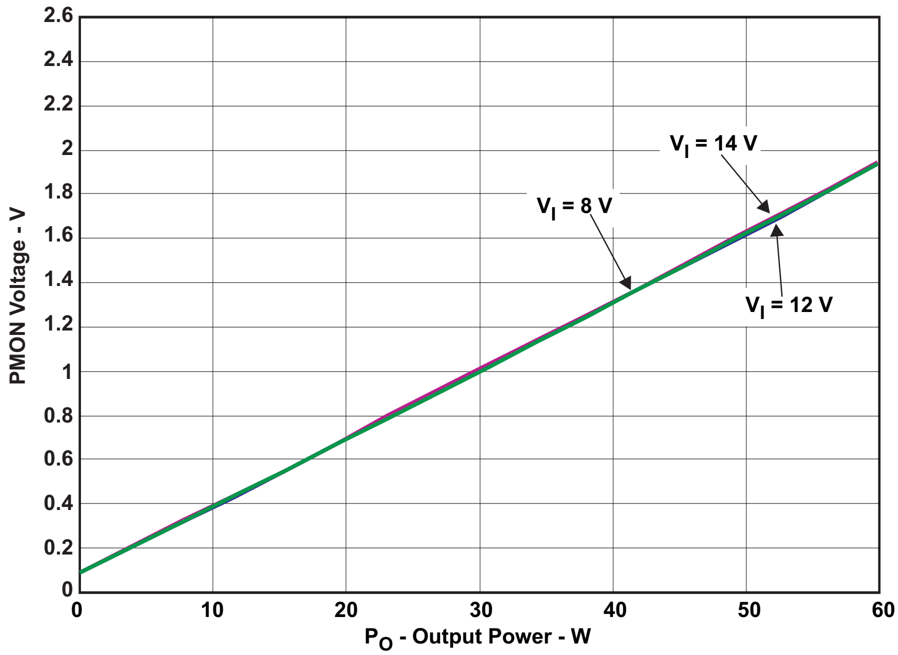

Figure 8. TPS51727EVM PMON Curve

7.5 Phase 1 and Phase 2 Current Share

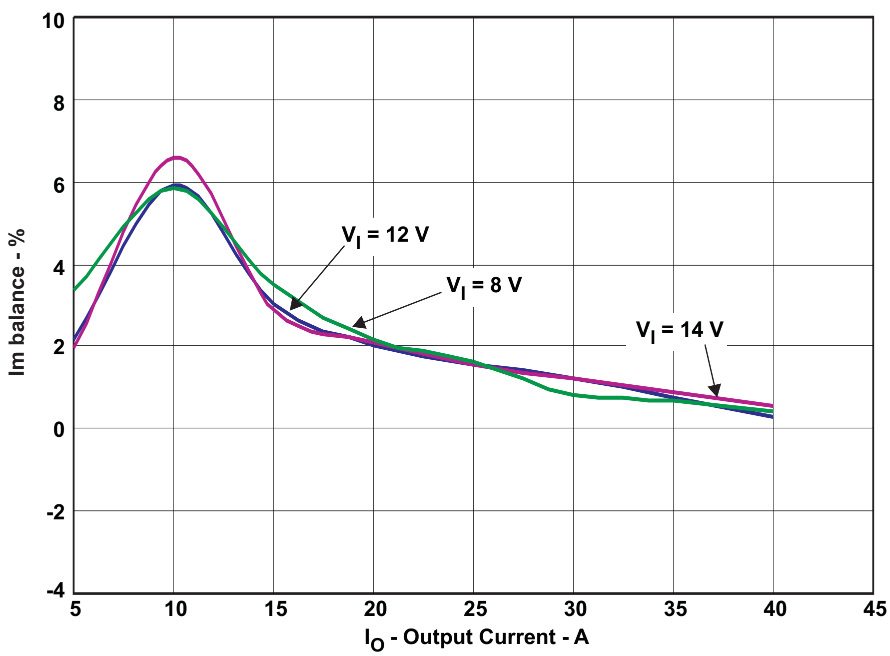

Figure 9. TPS51727EVM Phase 1 and Phase 2 Current Share

7.6 Output Ripple

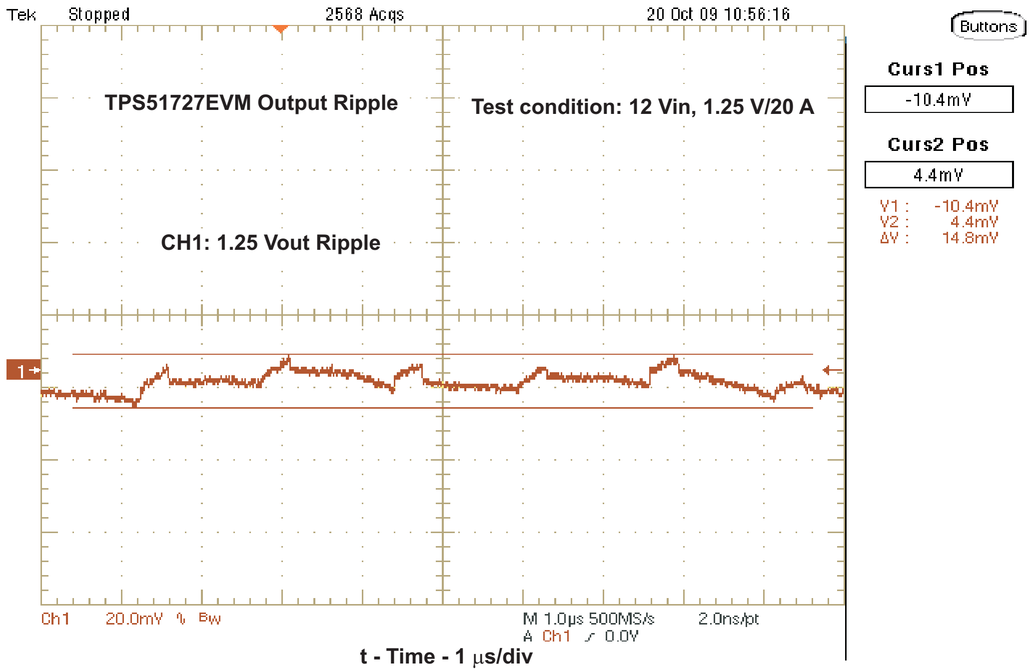

Figure 10. TPS51727EVM Output Ripple

7.7 Switching Node

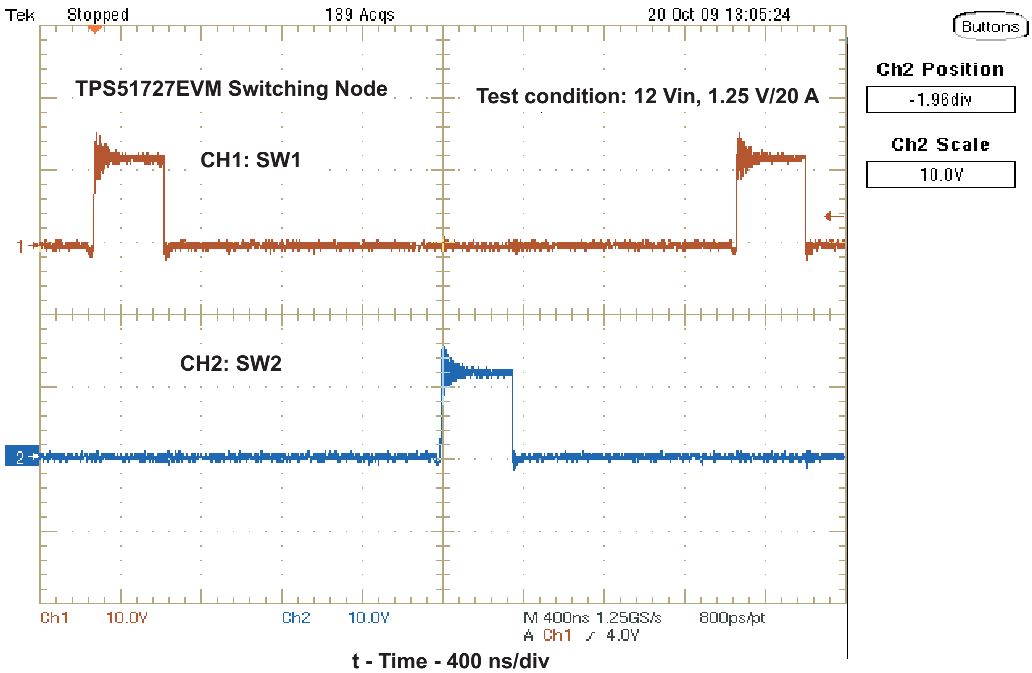

Figure 11. Switching Node

7.8 Output Transient

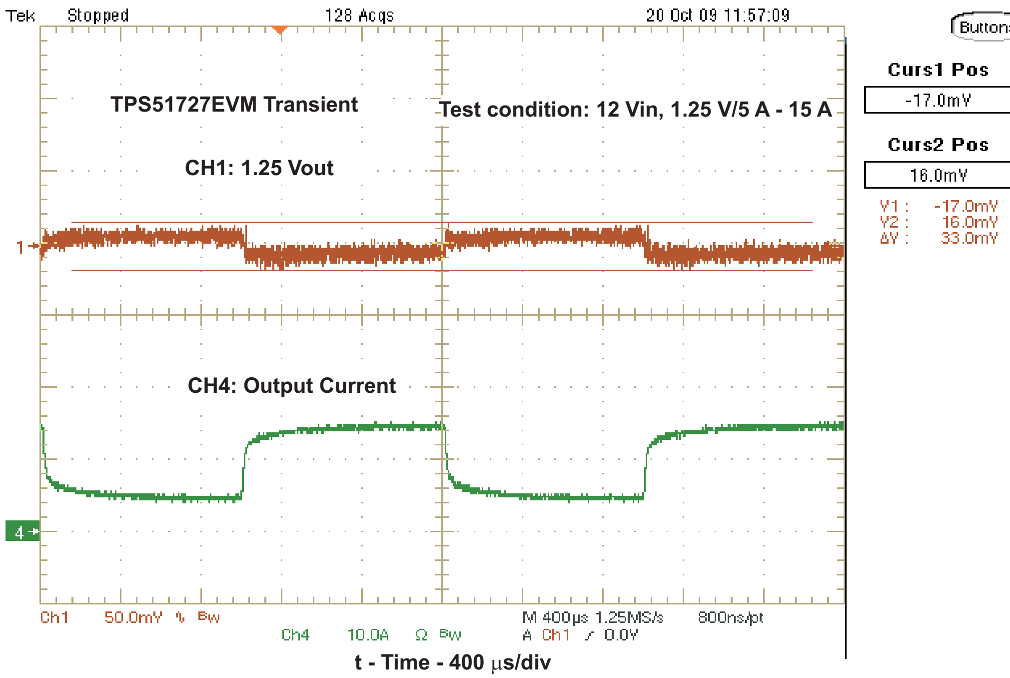

Figure 12. Output Transient

7.9 Turnon Waveform

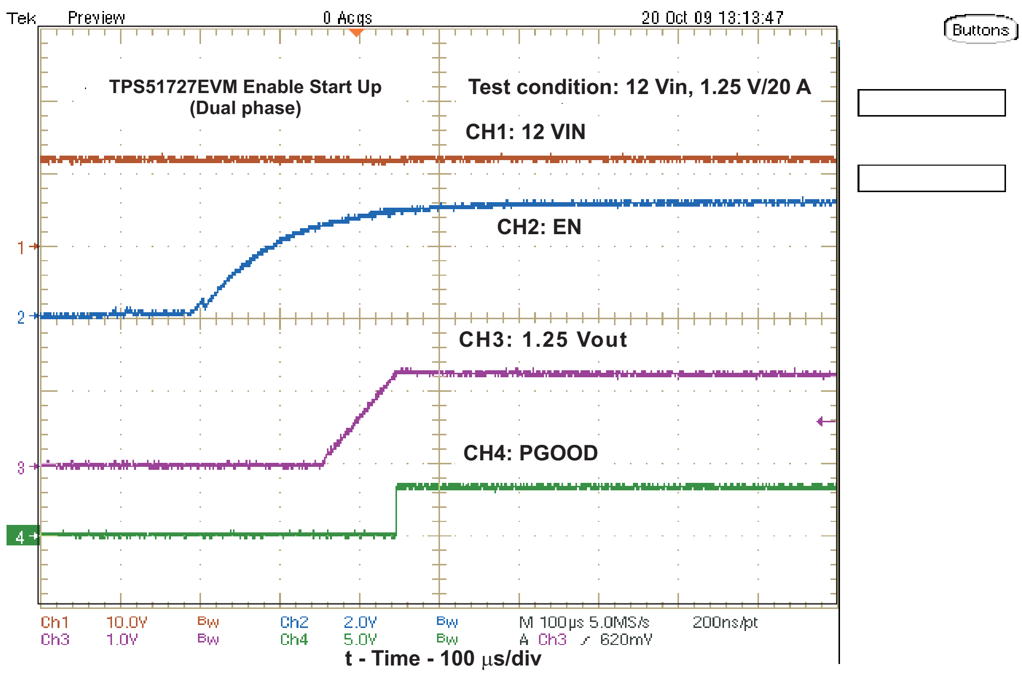

Figure 13. Enable Turnon Waveform

7.10 Turnoff Waveform

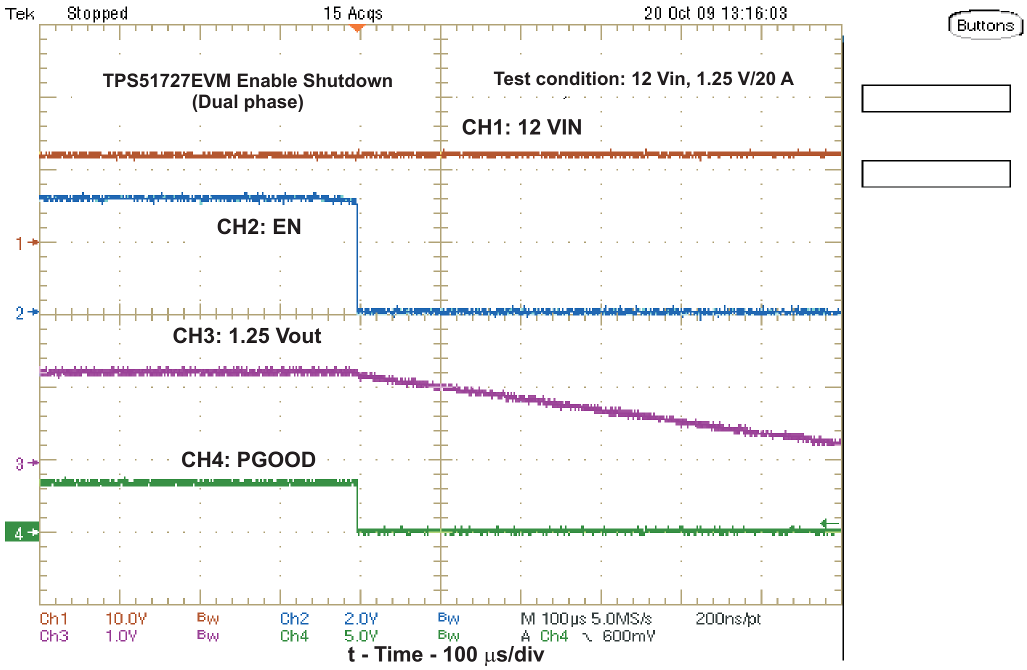

Figure 14. Enable Turnoff Waveform

8 EVM Assembly Drawing and PCB Layout

Figure 15 through Figure 22 show the design of the TPS51727EVM printed-circuit board. The EVM has been designed using a six-layer circuit board with 2-oz copper on outside layers.

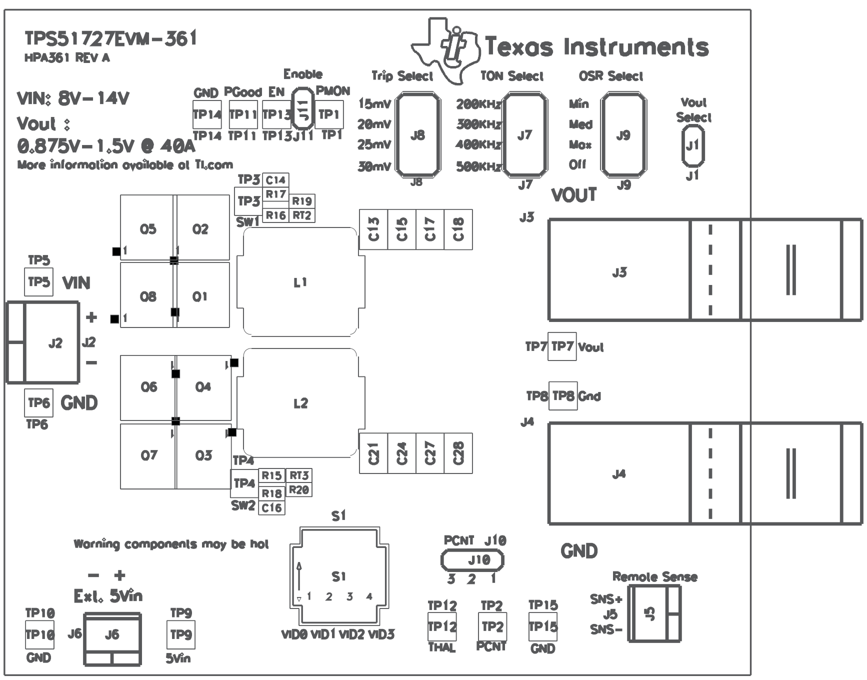

Figure 15. TPS51727EVM Top Layer Assembly Drawing, Top View

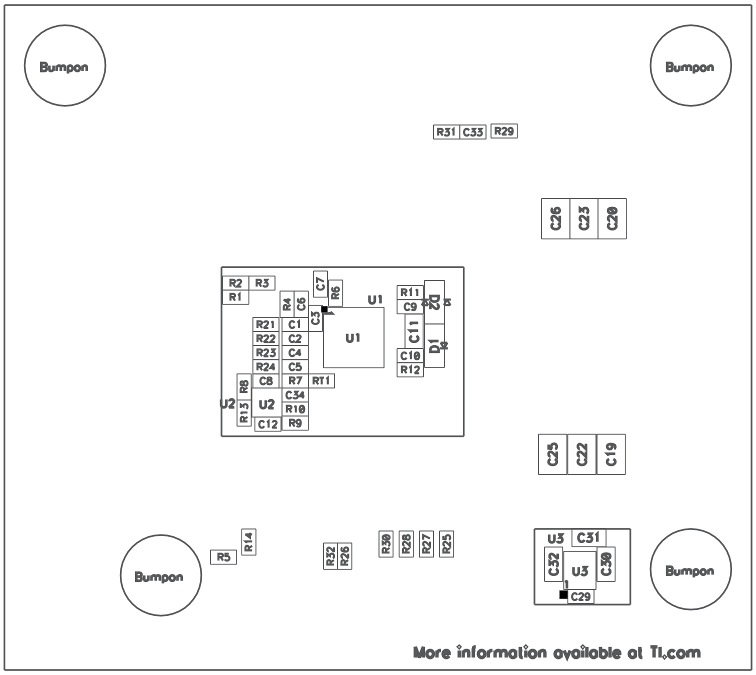

Figure 16. TPS51727EVM Bottom Assembly Drawing, Bottom View

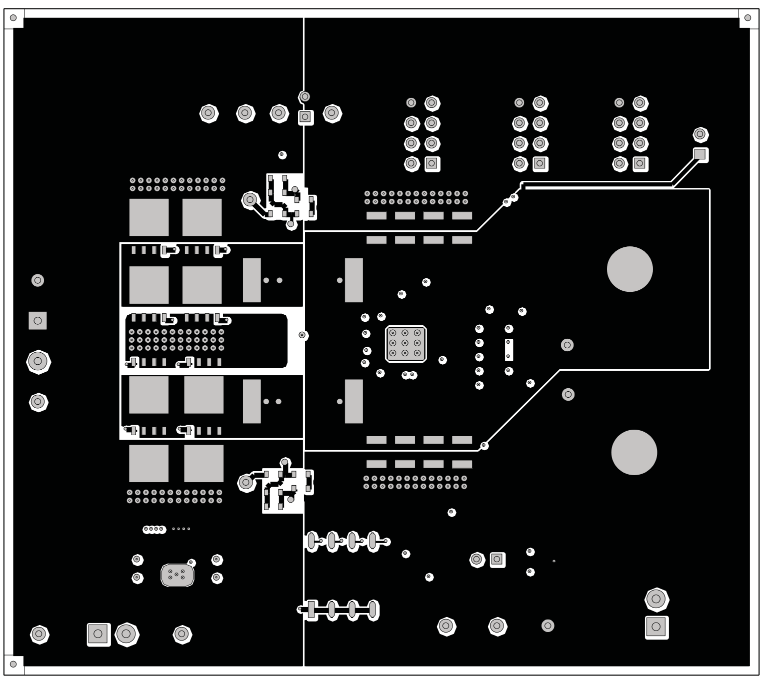

Figure 17. TPS51727EVM Top Copper, Top View

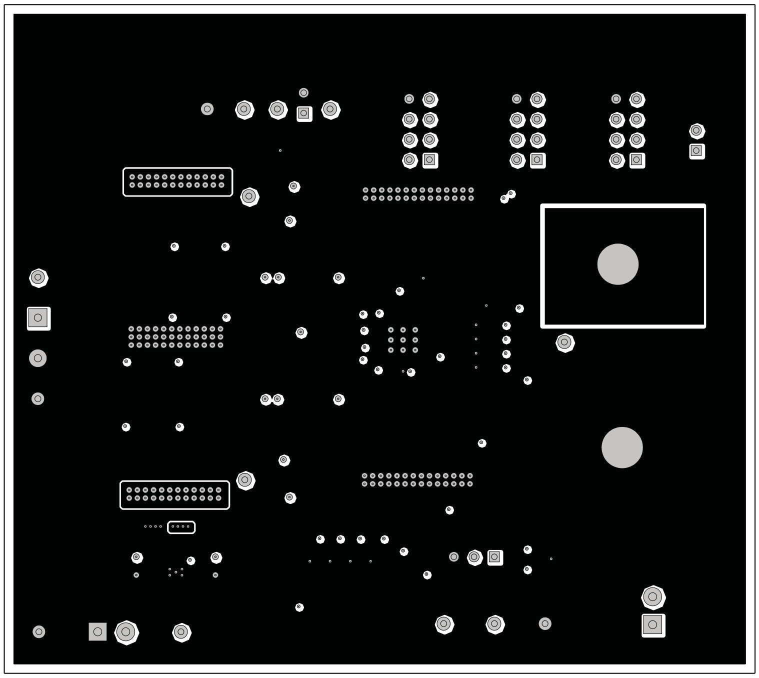

Figure 18. TPS51727EVM Internal Layer 2, Top View

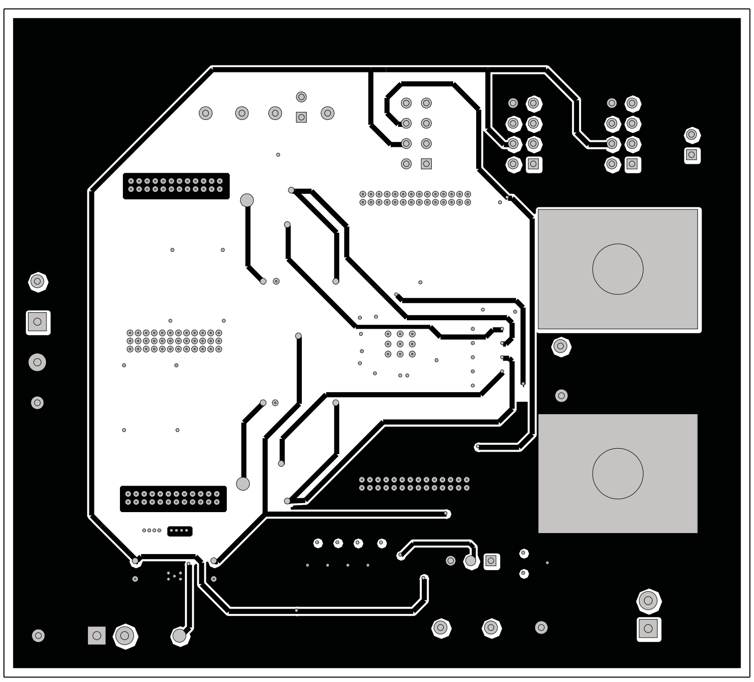

Figure 19. TPS51727EVM Internal Layer 3, Top View

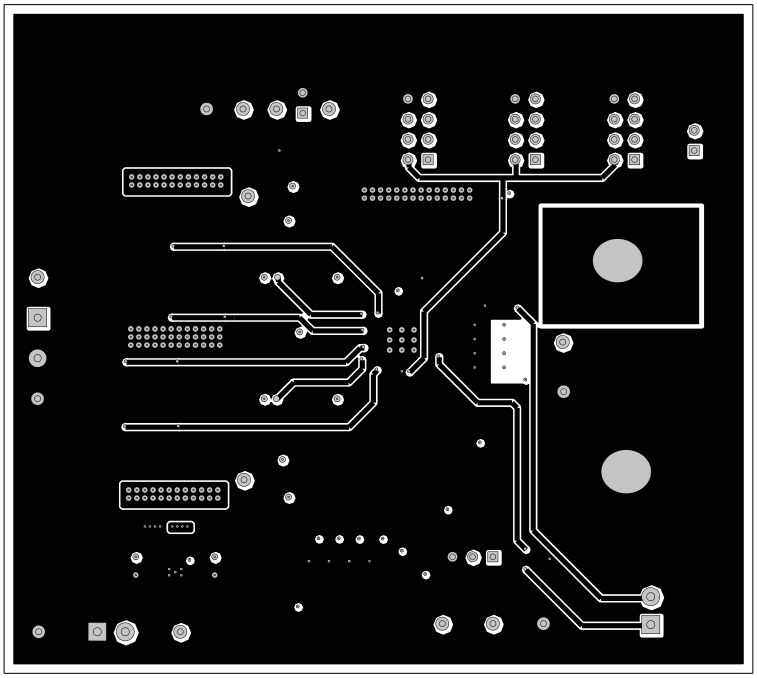

Figure 20. TPS51727EVM Internal Layer 4, Top View

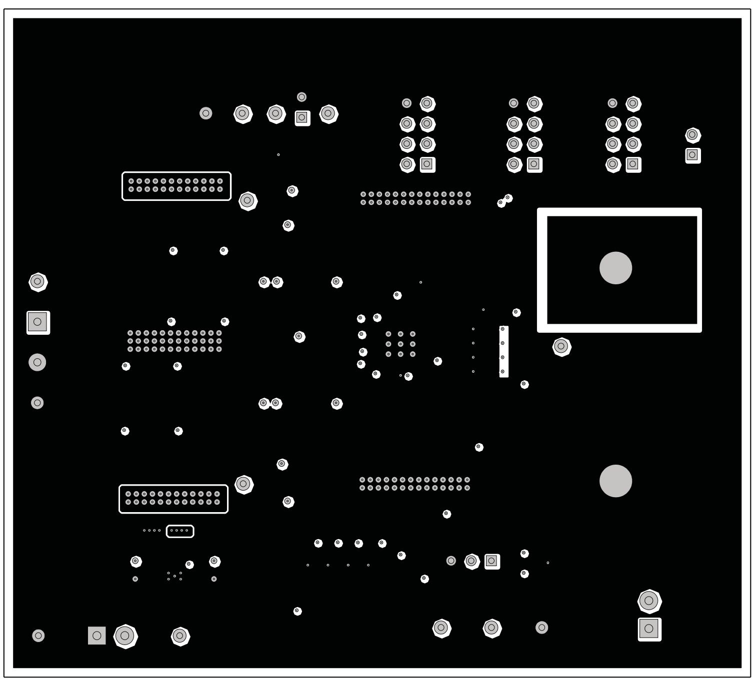

Figure 21. TPS51727EVM Internal Layer 5, Top View

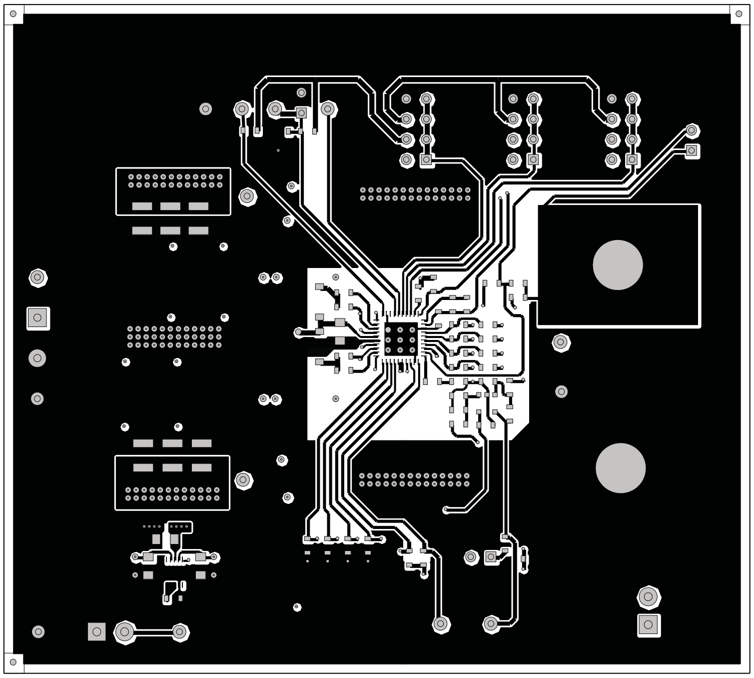

Figure 22. TPS51727EVM Bottom Copper, Top View

9 Bill of Materials

Table 9 presents the EVM bill of materials according to the schematic shown in Figure 1 and Figure 2.

Table 9. EVM Bill of Materials

QTY	REFDES	DESCRIPTION	MFR	PART NUMBER
6	C19, C20, C22, C23, C25, C26	Capacitor, Ceramic, 22 µF, 16V, X5R, 10%, 1210	MuRata	GRM32ER61C226KE20L
1	C6	Capacitor, Ceramic, 47 pF, 25V, COG or NPO, 10%, 0603	STD	STD
4	C1, C2, C4, C5	Capacitor, Ceramic, 33 pF, 25V, COG or NPO, 10%, 0603	STD	STD
1	C12	Capacitor, Ceramic, 0.1 µF, 10V, X7R, 10%, 0603	STD	STD
2	C14, C16	Capacitor, Ceramic, 0.015 µF, 25V, X7R, 10%, 0603	STD	STD
1	C3	Capacitor, Ceramic, 0.22 µF, 6.3V, X7R, 10%, 0603	STD	STD
4	C11, C30, C31, C32	Capacitor, Ceramic, 10 µF, 16V, X5R, 10%, 0805	STD	STD
4	C7, C9, C10, C29	Capacitor, Ceramic, 1 µF, 10V, X7R, 10%, 0603	STD	STD
8	C13, C15, C17, C18, C21, C24, C27, C28	Capacitor, Ceramic, 100 µF, 6.3V, X5R, 20%, 1210	Murata	GRM32ER60J107ME20L
3	C8, C33, C34	Capacitor, Ceramic, 0.01 µF, 10V, X7R, 10%, 0603	STD	STD
2	D1, D2	Diode, Schottky, 0.5A, 20V	Fairchild	MBR0520L
2	L1, L2	Inductor, SMT, 0.47 µH, 41A, 0.001Ω	Vishay	IHLP5050FDERR47M01
2	R1, R5	Resistor, Chip, 10.0, 1/16W, 1%, 0603	STD	STD
2	R11, R12	Resistor, Chip, 5.11, 1/16W, 1%, 0603	STD	STD
1	R13	Resistor, Chip, 49.9K, 1/16W, 1%, 0603	STD	STD
1	R14	Resistor, Chip, 0, 1/16W, 1%, 0603	STD	STD
2	R15, R16	Resistor, Chip, 24.9K, 1/16W, 1%, 0603	STD	STD
2	R17, R18	Resistor, Chip, 169K, 1/16W, 1%, 0603	STD	STD
2	R19, R20	Resistor, Chip, 43.2K, 1/16W, 1%, 0603	STD	STD
1	R2	Resistor, Chip, 4.02K, 1/16W, 1%, 0603	STD	STD

Table 9. EVM Bill of Materials (continued)

QTY	REFDES	DESCRIPTION	MFR	PART NUMBER
1	R3	Resistor, Chip, 20.0K, 1/16W, 1%, 0603	STD	STD
1	R4	Resistor, Chip, 7.5K, 1/16W, 1%, 0603	STD	STD
1	R6	Resistor, Chip, 124K, 1/16W, 1%, 0603	STD	STD
1	R7	Resistor, Chip, 2.00K, 1/16W, 1%, 0603	STD	STD
2	R8, R10	Resistor, Chip, 1.00K, 1/16W, 1%, 0603	STD	STD
1	R9	Resistor, Chip, 2.05K, 1/16W, 1%, 0603	STD	STD
3	RT1,RT2,RT3	NTC, Chip, Thermistor, 150K, 5%, 0603	Panasonic-ECG	ERT-J1VV154J
4	R21, R22, R23, R24	Resistor, Chip, 475, 1/16W, 1%, 0603	STD	STD
8	R25, R26, R27, R28, R29, R30, R31, R32	Resistor, Chip, 10.0K, 1/16W, 1%, 0603	STD	STD
2	Q2, Q3	MOSFET, Nch, 25V, 21A, 5.7 mΩ, TDSON-8	Ciclon	CSD16404Q5A
2	Q1, Q4	MOSFET, Nch, 25V, 31A, 2.1 mΩ, TDSON-8	Ciclon	CSD16321Q5
1	U1	IC, Dual-phase, ECO-mode, Step-down Synchronous Buck Controller, QFN40	TI	TPS51727RHA
1	U2	IC, Comparator, Differential, single, SOT_23_5(DBV)	TI	TL331IDBV
1	U3	IC, Integrated LDO with switch-over circuit, DGS10	TI	TPS51103DRC

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 8 V to 14 V and the output voltage range of 0.875 V to 1.5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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