CMOS Static RAM 256K (32K x 8-Bit)

71256SA

Features

- **32K x 8 advanced high-speed CMOS static RAM**
- **Commercial (0° to 70°C) and Industrial (-40° to 85°C) temperature options**
- **Equal access and cycle times**
  - *Commercial: 12ns*
  - *Commercial and Industrial: 15/20/25ns*
- **One Chip Select plus one Output Enable pin**
- **Bidirectional data inputs and outputs directly TTL-compatible**
- **Low power consumption via chip deselect**
- **Commercial product available in 28-pin 300-mil Plastic DIP, 300 mil Plastic SOJ and TSOP packages**
- **Industrial product available in 28-pin 300 mil Plastic SOJ and TSOP packages**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

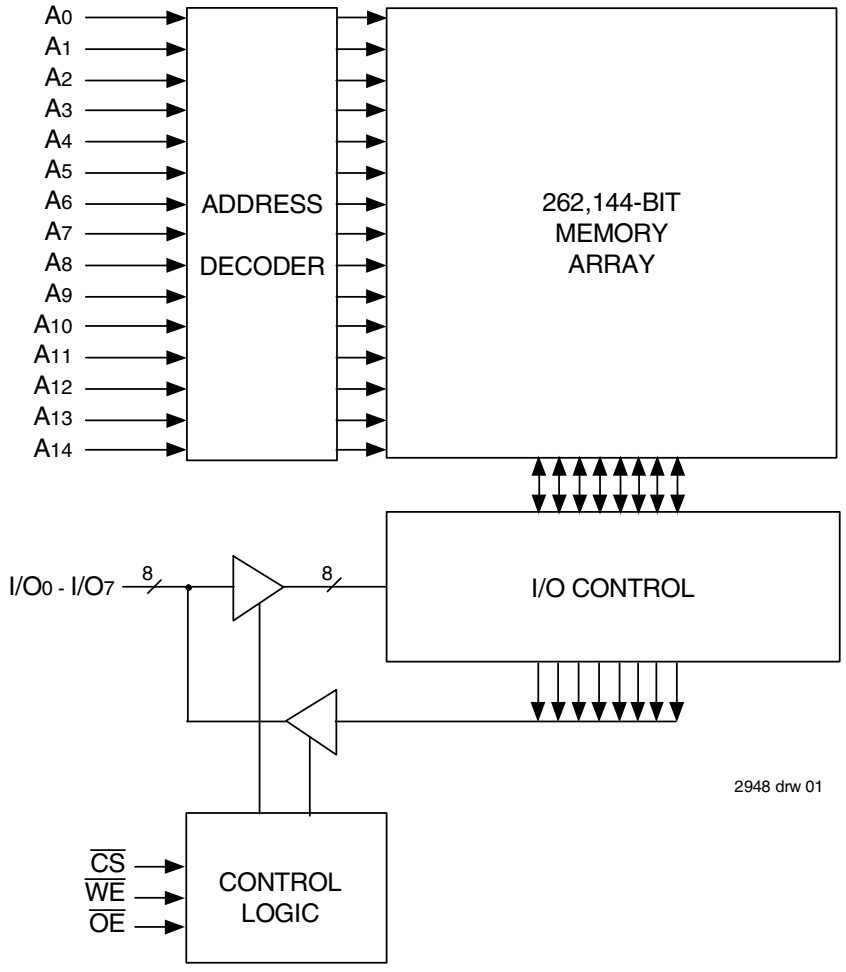
Description

The IDT71256SA is a 262,144-bit high-speed Static RAM organized as 32K x 8. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

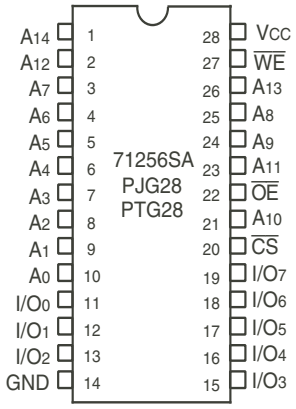
The IDT71256SA has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns. All bidirectional inputs and outputs of the IDT71256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71256SA is packaged in 28-pin 300-mil Plastic DIP, 28-pin 300 mil Plastic SOJ and TSOP.

Functional Block Diagram

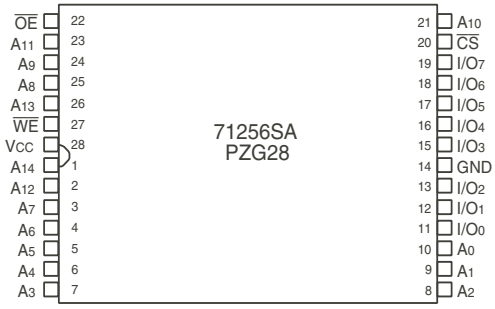


Pin Configurations[1]



2948 drw 02

DIP/SOJ
Top View



2948 drw 02a

TSOP
Top View

NOTE:
1. This text does not indicate orientation of actual part-marking.

Absolute Maximum Ratings[1]

Symbol	Rating	Value	Unit
V_{CC}	Supply Voltage Relative to GND	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage Relative to GND	-0.5 to V_{CC}+0.5	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

2948 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth Table[1,2]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	$DATA_{OUT}$	Read Data
L	X	L	$DATA_{IN}$	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V_{HC}[3]	X	X	High-Z	Deselected - Standby (I_{SB1})

2948 tbl 03

NOTES:
1. H = V_{IH}, L = V_{IL}, x = Don't care.
2. V_{LC} = 0.2V, V_{HC} = V_{CC} –0.2V.
3. Other inputs ≥V_{HC} or ≤V_{LC}.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	4.5V ± 5.5V
Industrial	-40°C to +85°C	0V	4.5V ± 5.5V

2948 tbl 01

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} +0.5	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

2948 tbl 04

NOTE:
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC Electrical Characteristics

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT71256SA		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	V

2948 tbl 05

DC Electrical Characteristics(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC}–0.2V)

Symbol	Parameter	71256SA12	71256SA15	71256SA20	71256SA25	Unit
I_{CC}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	160	150	145	145	mA
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	50	40	40	40	mA
I_{SB1}	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, V_{CC} = Max., f = 0(2), $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	15	15	15	15	mA

2948 tbl 06

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC} (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2948 tbl 07

Capacitance

(T_A = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

2948 tbl 08

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

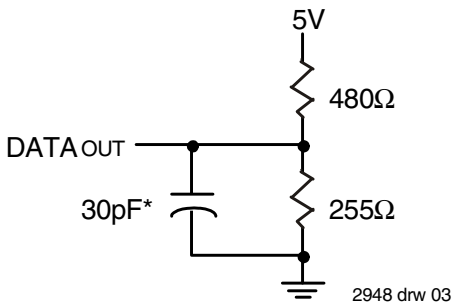


Figure 1. AC Test Load

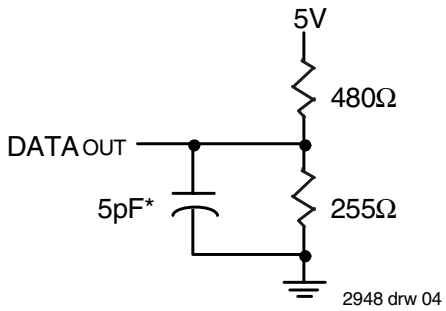


Figure 2. AC Test Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Including jig and scope capacitance.

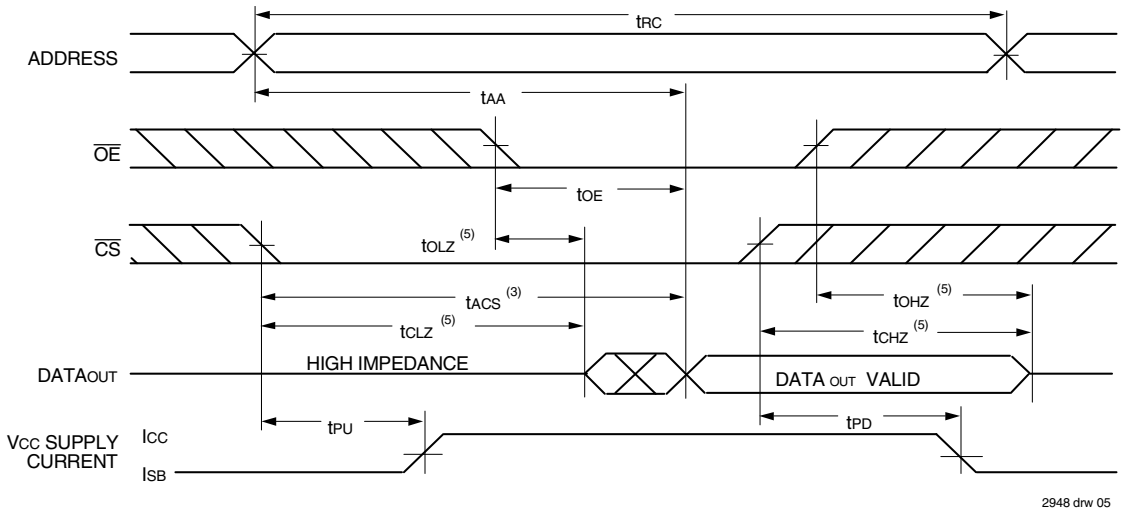
AC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71256SA12		71256SA15		71256SA20		71256SA25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	—	25	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	4	—	4	—	4	—	4	—	ns
t_{CHZ}[1]	Chip Select to Output in High-Z	0	6	0	7	0	10	0	11	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	10	—	11	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	0	6	0	6	0	8	0	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Down Time	—	12	—	15	—	20	—	25	ns
Write Cycle										
t_{WC}	Write Cycle Time	12	—	15	—	20	—	25	—	ns
t_{AW}	Address Valid to End-of-Write	9	—	10	—	15	—	20	—	ns
t_{CW}	Chip Select to End-of-Write	9	—	10	—	15	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	10	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	6	—	7	—	11	—	13	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{OW}[1]	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	0	6	0	6	0	10	0	11	ns

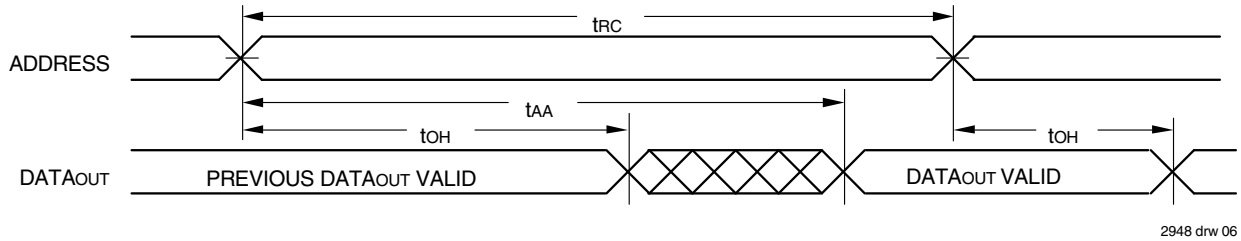
2948 tbl 09

NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

Timing Waveform of Read Cycle No. 1(1)

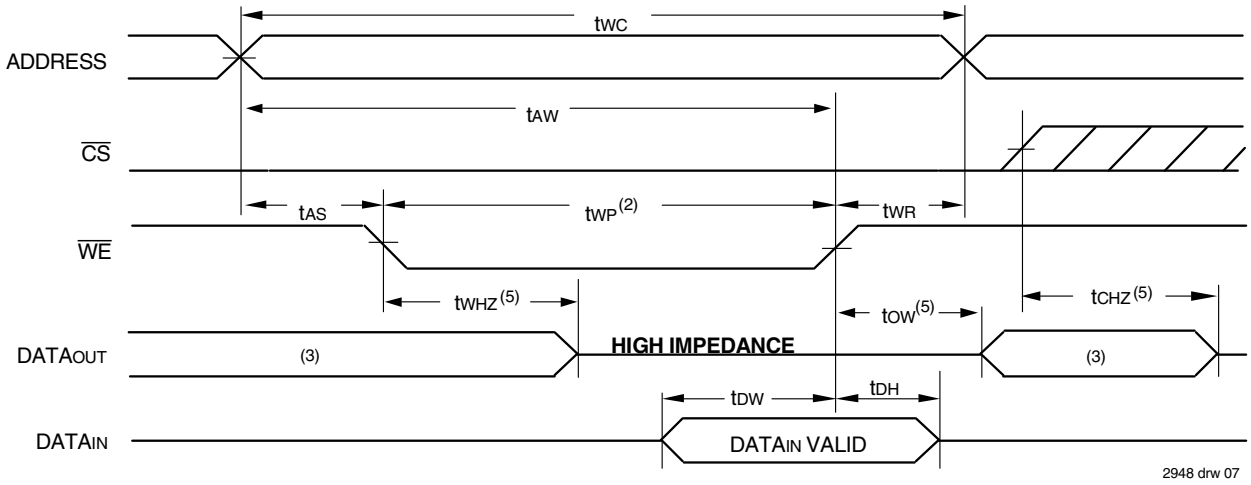


Timing Waveform of Read Cycle No. 2(1,2,4)

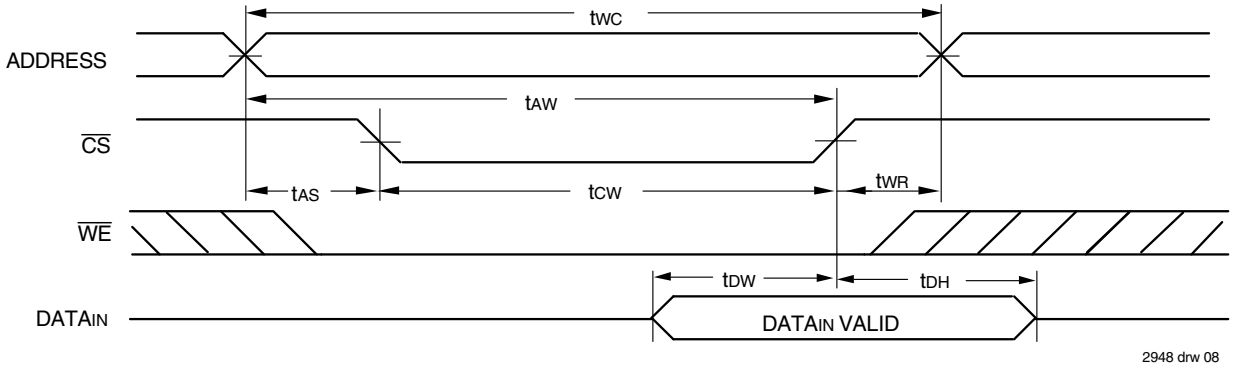


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled Timing)(1,2,4)



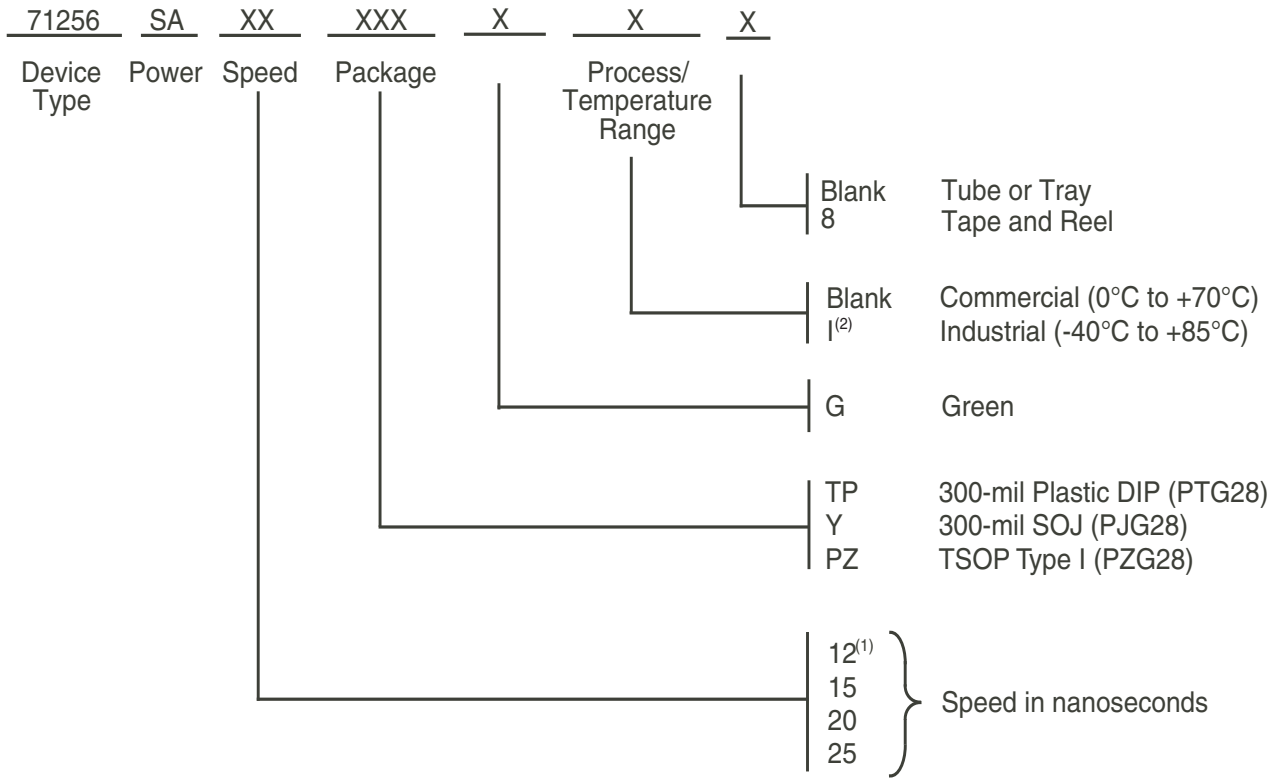
Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled Timing)(1,4)



NOTES:

1. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
2. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
5. Transition is measured ±200mV from steady state.

Ordering Information



2948 drw 09

NOTES:
1. Available in commercial temperature range only.
2. Contact your local sales office for Industrial temp range for other speeds, packages and powers.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
12	71256SA12PZG	PZG28	TSOP	C
	71256SA12PZG8	PZG28	TSOP	C
	71256SA12TPG	PTG28	PDIP	C
	71256SA12YG	PJG28	SOJ	C
	71256SA12YG8	PJG28	SOJ	C
15	71256SA15PZG	PZG28	TSOP	C
	71256SA15PZG8	PZG28	TSOP	C
	71256SA15PZGI	PZG28	TSOP	I
	71256SA15PZGI8	PZG28	TSOP	I
	71256SA15TPG	PTG28	PDIP	C
	71256SA15TPGI	PTG28	PDIP	I
	71256SA15YG	PJG28	SOJ	C
	71256SA15YG8	PJG28	SOJ	C
	71256SA15YGI	PJG28	SOJ	I
	71256SA15YGI8	PJG28	SOJ	I

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
20	71256SA20PZG	PZG28	TSOP	C
	71256SA20PZG8	PZG28	TSOP	C
	71256SA20PZGI	PZG28	TSOP	I
	71256SA20PZGI8	PZG28	TSOP	I
	71256SA20TPG	PTG28	PDIP	C
	71256SA20TPGI	PTG28	PDIP	I
	71256SA20YG	PJG28	SOJ	C
	71256SA20YG8	PJG28	SOJ	C
	71256SA20YGI	PJG28	SOJ	I
	71256SA20YGI8	PJG28	SOJ	I
25	71256SA25PZG	PZG28	TSOP	C
	71256SA25PZG8	PZG28	TSOP	C
	71256SA25PZGI	PZG28	TSOP	I
	71256SA25PZGI8	PZG28	TSOP	I
	71256SA25TPG	PTG28	PDIP	C
	71256SA25TPGI	PTG28	PDIP	I
	71256SA25YG	PJG28	SOJ	C
	71256SA25YG8	PJG28	SOJ	C

Datasheet Document History

1/7/00		Updated to new format
	Pg. 1, 3, 4, 7	Revised Industrial Temperature range offerings
	Pg. 6	Removed Note No. 1 for Write Cycle diagrams, renumbered footnotes and notes
	Pg. 8	Added Datasheet Document History
08/09/00		Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"
09/30/04	Pg. 7	Added "Restricted hazardous substance device" to ordering informations.
02/20/07	Pg. 7	Added TT generation die step to data sheet ordering information.
04/28/11	Pg. 1, 2, 7	Obsoleted 28-pin 600 mil and removed TT generation die step from Ordering information. Added Tape and Reel to Ordering information and updated description of Restricted hazardous substance device to Green
11/03/14	Pg. 1 & 8	Removed 12ns I-temp offering in Features. Added note regarding 12ns commercial only on the Ordering information page. Removed IDT as a reference for fabrication in Description.
	Pg. 2 & 8	Removed package extensions from pinouts and from Ordering information.
06/29/20	Pg. 1 - 9	Rebranded as Renesas datasheet
	Pg. 1 & 7	Updated Industrial temp range and green availability
	Pg. 2 & 7	Updated package codes
	Pg. 7	Added Orderable Part Information tables

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