Using the UCC2891 Active-Clamp Current-Mode PWM Controller

User's Guide

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48-V to 3.3-V Forward Converter With Active-Clamp Reset Using the UCC2891 Active-Clamp Current-Mode PWM Controller

1 Introduction

The UCC2891EVM-520 evaluation module (EVM) is a forward converter providing a 3.3-V regulated output at 30 A of load current, operating from a 48-V input. The EVM operates over the full 36-V to 75-V telecom-input range, and is able to fully regulate down to zero-load current. The module uses the UCC2891 current-mode active-clamp PWM controller for effectively demonstrating the active-clamp transformer-reset technique.

Benefits of the active clamp include a control-driven transformer-reset scheme allowing zero-voltage switching (ZVS) to increase overall efficiency, lower drain-to-source voltage stress, extended duty cycle beyond 50%, and reduced electromagnetic radiated emissions. Combined with synchronous rectification, this EVM is configured to operate at 300 kHz and exhibits a peak efficiency of just over 92%, with a full load efficiency of 90%. The EVM displays many features that might be typical of a more complex design, yet the compact board layout and low component count make it elegantly simple.

This EVM features active-current limiting on the output. Because the unit continues to operate into a short circuit or overload condition the operator must shut the unit off before the thermal limitations of the components are exceeded.

2 Description

The UCC2891 controller family provides advanced active-clamp control features such as programmable maximum duty-cycle clamp, programmable dead time between the two primary switches and the ability to drive either a P-channel, or N-channel MOSFET in either a high-side or low-side active-clamp configuration. The UCC2891 also allows the ability to start-up directly from the 48-V telecom-bus voltage, eliminating the need for external start-up circuitry. The EVM includes programmable soft start, internal slope compensation for peak current-mode control, internal low-line voltage sensing, internal syncronizable-clock input, cycle-by-cycle current limiting, and a robust 2-A sink/source TrueDrive™ internal gate-drive circuit. The result is a highly efficient design loaded with features, requiring very few external components.

The TrueDrive™ hybrid output architecture used in the UCC2891 uses TI's unique TrueDrive Bipolar-CMOS output. To the user, TrueDrive simply means ultra-fast rise and fall times by providing the highest possible drive current where it is needed most, at the MOSFET Miller plateau region.

The UCC2891/2/3/4 is available in either a 16-pin SOIC or 16-pin TSSOP package for applications where absolute minimal board space is required.

The UCC2891EVM-520 highlights the many benefits of using the UCC2891 active-clamp current-mode PWM controller. This user's guide provides the schematic, component list, assembly drawing, artwork, and test setup necessary to evaluate the UCC2891 in a typical telecom application. More detailed design information is listed in the Section 10 section.

2.1 Applications

The UCC2891 is suited for use in isolated telecom 48-V input systems requiring high-efficiency and high-power density for very low-output voltage, high-current converter applications, including:

- Server Systems
- Datacom
- Telecom
- DSP's, ASIC's, FPGA's

2.2 Features

The UCC2891EVM-520 features include:

- ZVS transformer reset using active-clamp technique in forward converter
- All surface mount components, double-sided half-brick (2.2 × 2.28 × 0.5) inches
- Complementary auxiliary drive for active clamp with programmable dead time for ZVS
- Current-mode control with synchronization function
- Internal PWM-slope compensation
- Start up directly from telecom input voltage
- Synchronous rectifier-output stage allows high-efficiency operation
- Programmable soft-start
- Up to 30-A dc-output current
- Regulation to zero-load current
- Non-latching output-current limiting
- Non-latching input-undervoltage protection
- 1500-V isolation primary to secondary

3 UCC2891EVM-520 Electrical Performance Specifications

The UCC2891EVM-520 electrical performance specifications are listed in Table 1.

Table 1. UCC2891EVM-520 Performance Summary

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Input voltage range		36	48	75	V
No load input current	V_{IN} = 36 V, I_{OUT} = 0 A		75	100	mA
Maximum input current	V_{IN} = 36 V, I_{OUT} = 30 A		3.00	3.25	A
Input voltage ripple	V_{IN} = 75 V, I_{OUT} = 30 A		1.50	1.75	V_{P-P}
Input voltage ripple					
Output voltage	36 V ≤ V_{IN} ≤ 75 V, 0 A ≤ I_{OUT} ≤ 30 A	3.25	3.30	3.35	V
Output voltage regulation	Line regulation (36 V ≤ V_{IN} ≤ 75 V, I_{OUT} = 0 A)		±0.30%		
	Load regulation (0 A ≤ I_{OUT} ≤ 30 A, V_{IN} = 48 V)		0.050%		
Output voltage ripple	V_{IN} = 48 V, I_{OUT} = 30 A		30	40	mV_{P-P}
Output load current	V_{IN} = 48 V, I_{OUT} = 30 A	0		30	A
Output current limit	36 V ≤ V_{IN} ≤ 72 V	32		<40	
Output current limit					
Switching frequency		275		325	kHz
Control loop bandwidth	36 V ≤ V_{IN} ≤ 75 V, I_{OUT} = 10 A	5		8	
Control loop bandwidth	36 V ≤ V_{IN} ≤ 75 V, 2 A ≤ I_{OUT} ≤ 30 A	30		50	°C
Peak efficiency			92%		
Full load efficiency	V_{IN} = 48 V, I_{OUT} = 30 A		90%		

4 Schematic

A schematic of the UCC2891EVM-520 is shown in Figure 1. Terminal block J1 is the 48-V input voltage-source connector and J8 is the output and return for the 3.3-V output voltage.

On the primary side, U1 is the UCC2891 shown with the necessary discrete circuitry for configuring the controller to operate at 300 kHz with the maximum duty clamp set for 0.65. The EVM is programmed to start at VIN = 36 V, as determined by R11 and R12. To minimize power dissipation in the current sense, a current-sense transformer, T1 is used, as opposed to simply using a sense resistor between the source of Q2 and power ground. Q2 is the primary switching MOSFET and is selected based upon VDS and low $R_{DS(on)}$. Q1 is the AUX (active reset) MOSFET and is selected based upon preferred package only, with only minor consideration given for $R_{DS(on)}$ and Qg. Since the active clamp used in this design is low-side referenced, Q1 must be a P-channel type MOSFET. The reason for this is further explained in application note SLUA299 (see Section 10). C9 is the clamp capacitor used to maintain a constant dc voltage. The input voltage is subtracted from the clamp voltage to allow transformer reset during the active-clamp period.

High efficiency is achieved using self-driven synchronous rectification on the secondary side. Q3 and Q4 are placed in parallel and make up the forward synchronous rectifier (SR), while the reverse SR is made up of the parallel combination of Q5, Q7, and Q8. If the duty cycle were limited to 50% then the reverse SR reduces to only two parallel MOSFETs, but because these devices are operating near 60% duty cycle during the freewheel-mode, they carry a higher average current than seen by Q3 and Q4. The output inductor L1 has a coupled secondary, referenced to the primary side, used to provide bootstrapping voltage to U1. A stable bias for the optocoupler, U2, is provided by the series-pass regulator made up of D6, Q6 and some associated filtering.

Scope jacks J2 and J3 allow the user to measure the gate-to-source and drain-to-source signals for Q2, the primary MOSFET. J4 and J5 allow convenient access to the gate-drive signals of each SR on the secondary side. J6 and J7 are available allowing the option of using a network analyzer to non-invasively measure the control to output loop-gain and phase.

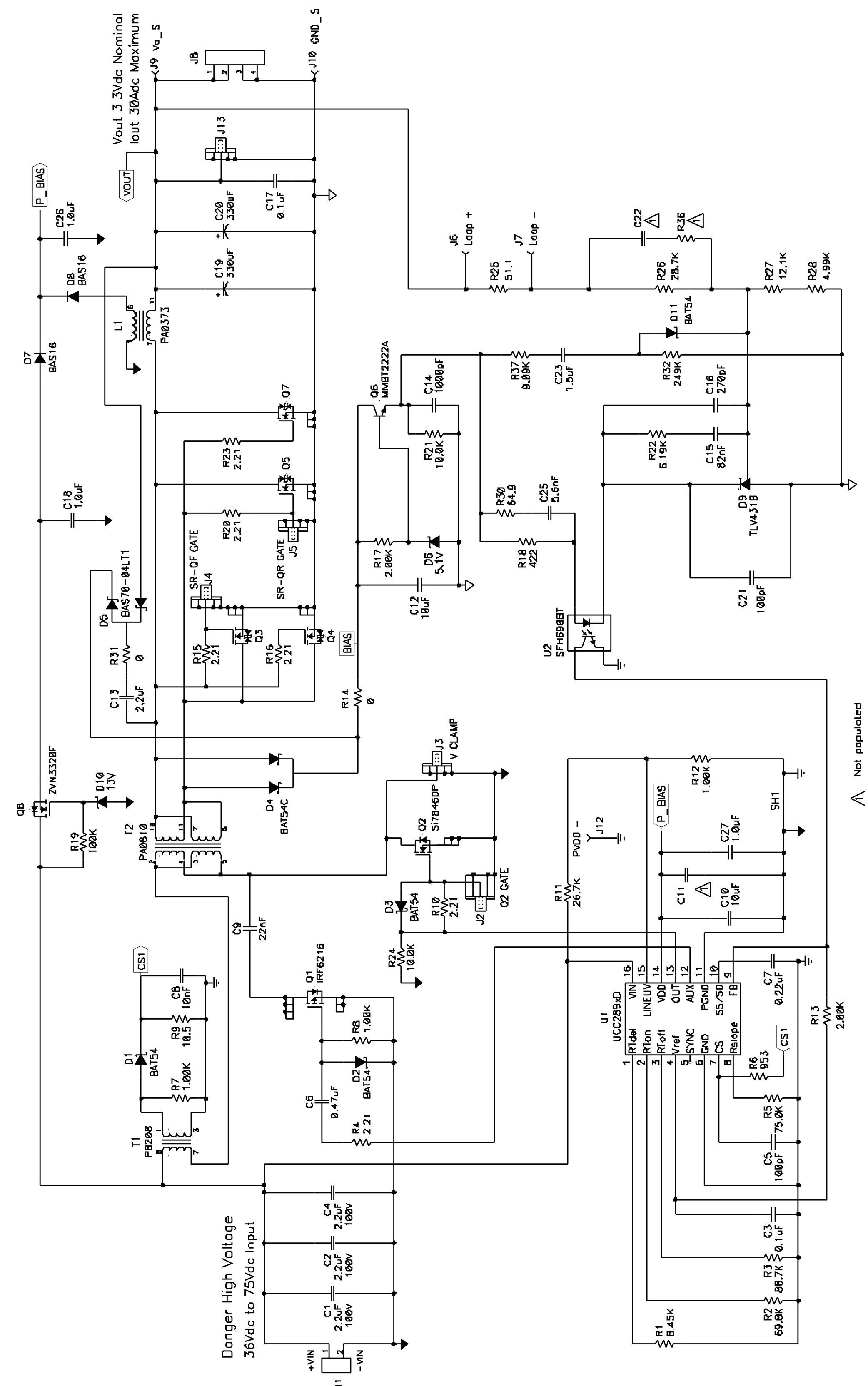


Figure 1. UCC2891EVM-520 Schematic

5 EVM Test Setup

Figure 2 shows the basic test setup recommended to evaluate the UCC2891EVM-520.

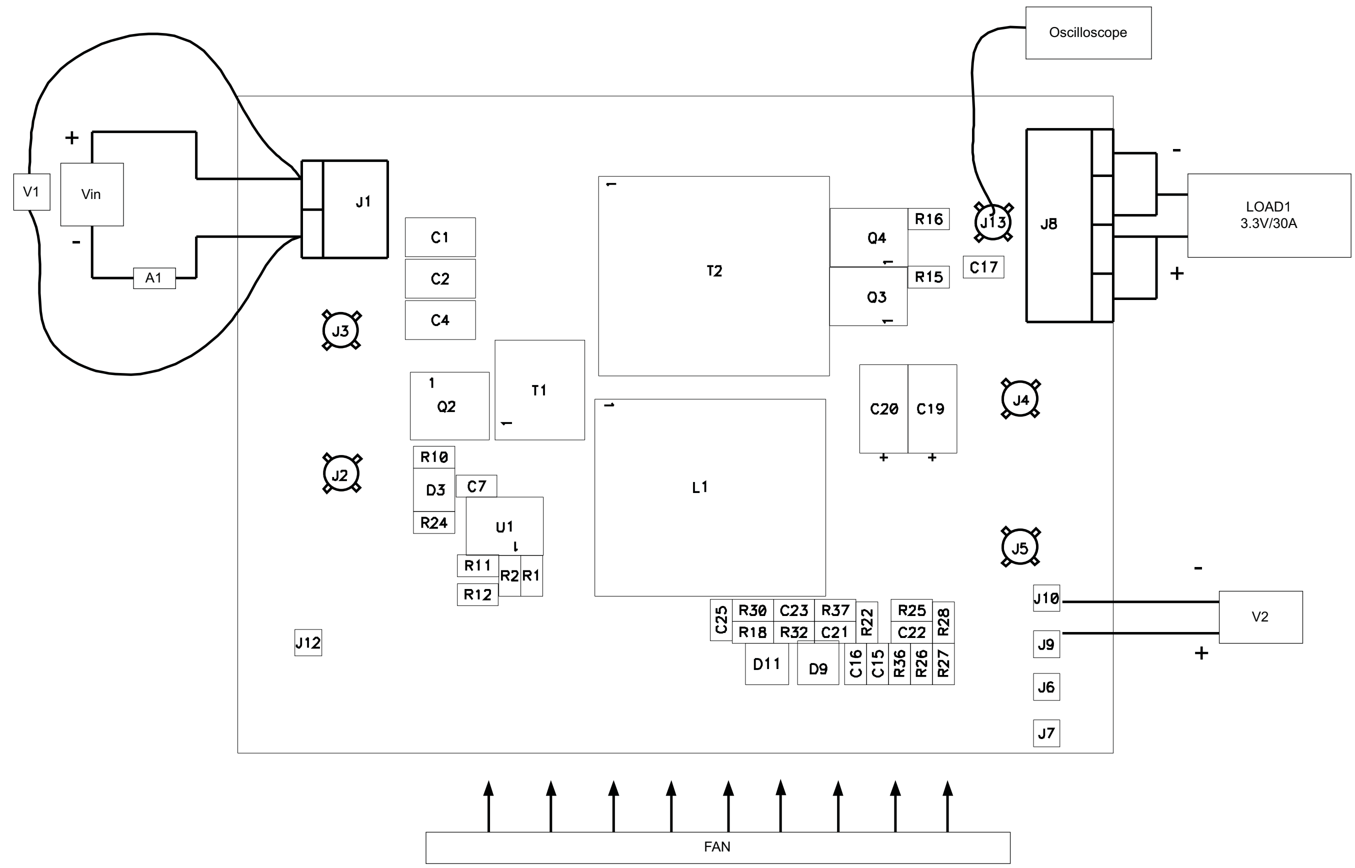


Figure 2. Recommended EVM Test Configuration

5.1 Output Load (LOAD1)

For the output load to VOUT, a programmable electronic load set to constant-current mode and capable of sinking between 0A_{DC} and 30A_{DC}, is used. Using a dc voltmeter, V2, making all output voltage measurements directly at J9 and J10 pins is advised. Unless the load has remote-sense capability, measuring VOUT at LOAD1 results in some voltage measurement error, especially at higher load current, due to finite voltage drops across the wires between J8 and the electronic load.

5.2 DC Input Source (VIN)

The input voltage is a variable DC source capable of supplying between 0 V_{DC} and 72 V_{DC} at no less than 3.5 A_{DC}, and connected to J1 and A1 as shown in Figure 2. For fault protection to the EVM, limiting the source current to no more than 4 A_{DC} for a 36 V input is a good common practice. A dc ammeter, A1 is also inserted between VIN and J1 as shown in Figure 2.

5.3 Network Analyzer

A network analyzer connects directly to J6 and J7. The UCC2891EVM-520 provides a 51.1-Ω resistor (R25) between the output and the voltage feedback to allow easy non-invasive measurement of the control-to-output loop response.

5.4 Output Ripple Measurement

An oscilloscope probe is connected using scope jack J13 to measure output ripple as shown in Figure 2. Set the scope to be AC coupled, 50 mV/div. amplitude resolution, 2-µs/div. time resolution and 20-MHz bandwidth limited.

5.5 Recommended Wire Gauge

The connection between the source voltage, VIN and J1 of the EVM carry as much as 3.25A_{DC}. The minimum recommended wire size is AWG #20 with the total length of wire less than 8 feet (4-feet input, 4-feet return). The connection between J8 of the EVM and LOAD1 carries as much as 30A_{DC}. The minimum recommended wire size is AWG #16, with the total length of wire less than 8 feet (4-feet output, 4-feet return).

5.6 Fan

Most power converters include components that are hot to the touch when approaching temperatures of 605°C. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 LFM is recommended to reduce component temperatures when operating at or above 50% maximum rated load current.

6 Power Up and Power Down Test Procedures

The following test procedure is recommended primarily for power up and shut down of the EVM. Whenever the EVM is running above an output load of 15 A_{DC}, the fan must be turned on. Also, never walk away from a powered EVM for extended periods of time.

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected to reference the user to earth-ground before power is applied to the EVM. Electrostatic smock and safety glasses must also be worn.
2. Limiting the source current from VIN to 3.5-A maximum prior to connecting the DC-input source, VIN, is advisable. Make sure VIN is initially set to 0 V and connected to J1 as shown in Figure 2.
3. Connect the ammeter A1 (0A to10A range) between VIN and J1 as shown in Figure 2.
4. Connect voltmeter (can optionally use voltmeter from VIN source if available), V1 across VIN as shown in Figure 2.
5. Connect LOAD1 to J8 as shown in Figure 2. Set LOAD1 to constant-current mode to sink 0 A_{DC} before VIN is applied.
6. Connect voltmeter, V2 across J9 and J10 as shown in Figure 2.
7. Connect an Oscilloscope to J13 as shown in Figure 2.
8. Increase VIN from 0 V to 36 V_{DC}.
9. Observe that VOUT is regulating when VIN is at 36 V.
10. Increase VIN to 48 V.
11. Increase LOAD1 from 0 A to 15 A_{DC}.
12. Turn on fan making sure to blow air directly on the EVM.
13. Increase LOAD1 from 15 A_{DC} to 30 A_{DC}.
14. Decrease LOAD1 to 0 A.
15. Decrease VIN from 48 V_{DC} to 0 V.
16. Shut down VIN.

7 Power Up/Down Test Procedures

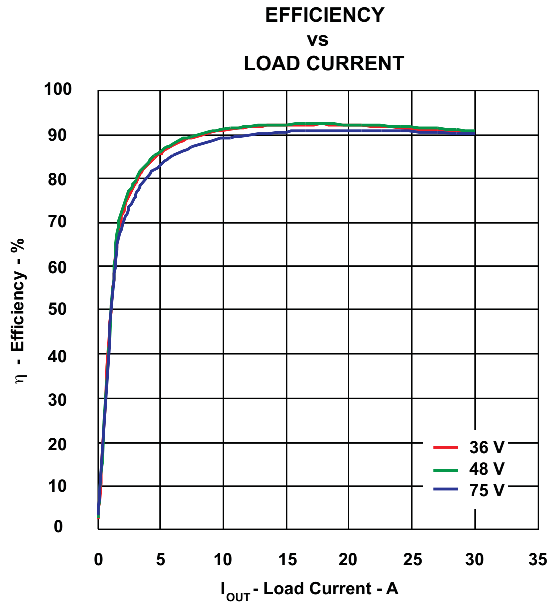


Figure 3.

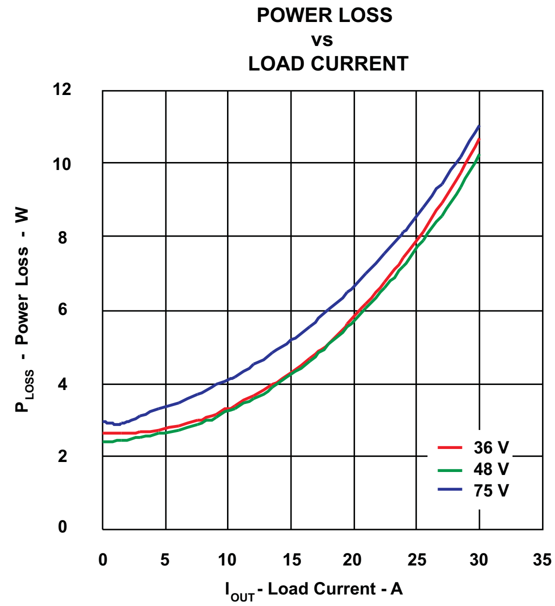


Figure 4.

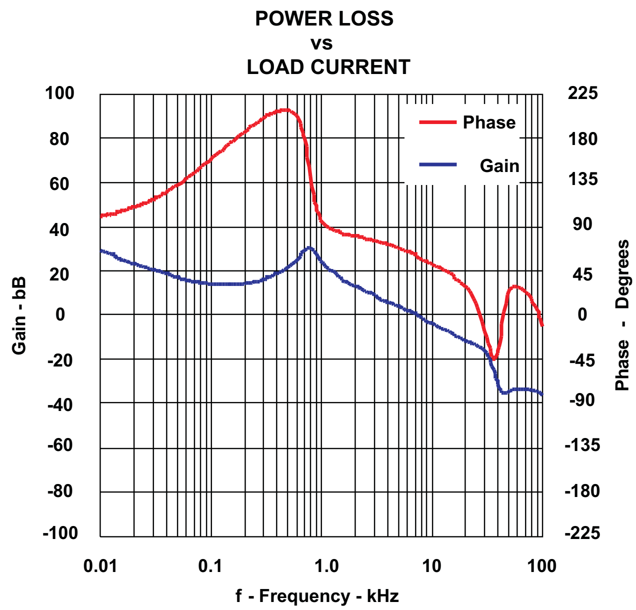


Figure 5.

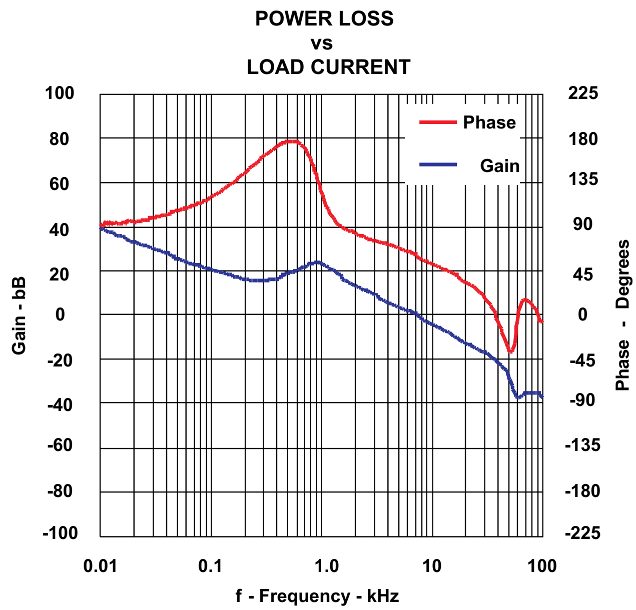


Figure 6.

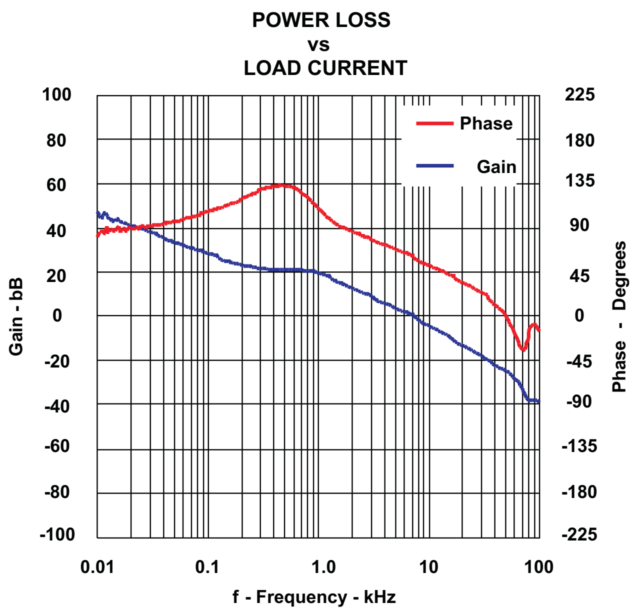


Figure 7.

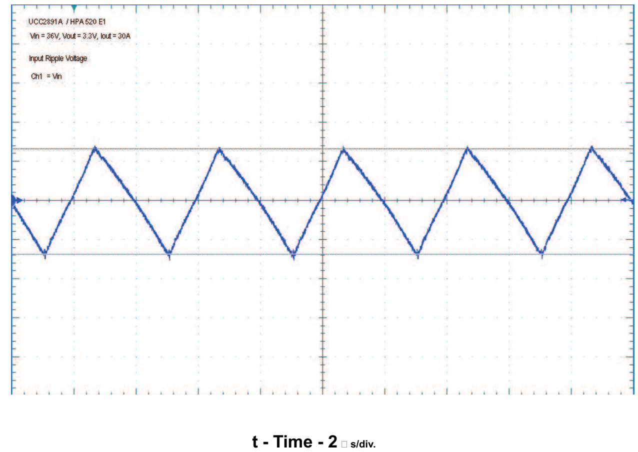


Figure 8. 500 mV/div., 1.3 V Peak-to-Peak

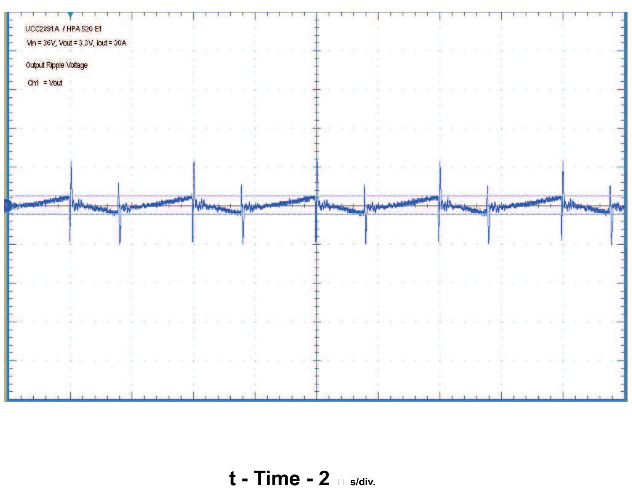


Figure 9. 50 mV/div., 38.8 V Peak-to-Peak

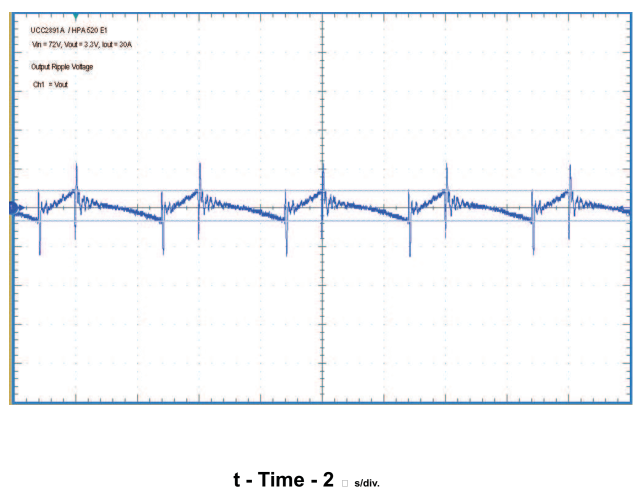
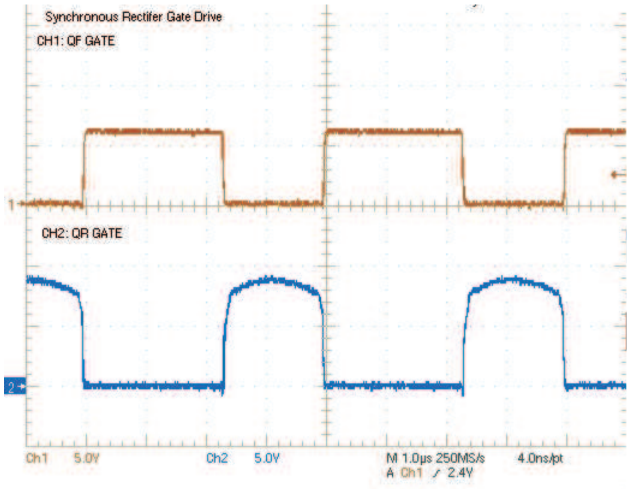
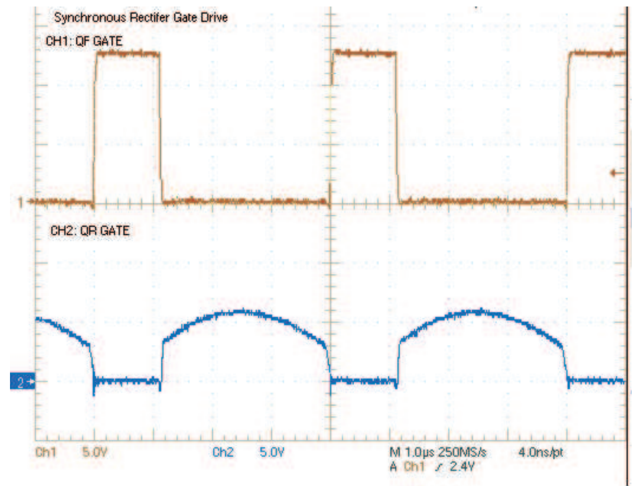


Figure 10. 50 mV/div., 23 mV Peak-to-Peak



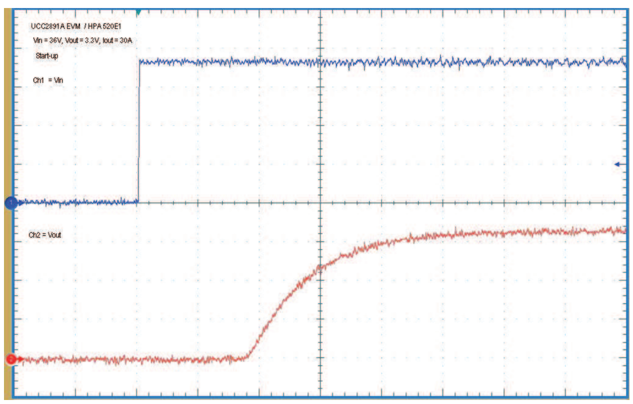
t - Time - 1 µs/div.

Figure 11. V_{IN} = 36 V



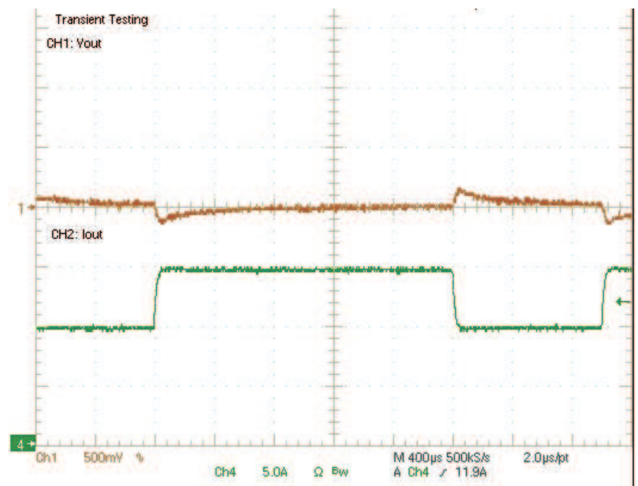
t - Time - 1 µs/div.

Figure 12. V_{IN} = 75 V



t - Time - 1 □ s/div.

Figure 13. Startup at V_{IN} = 36 V, I_{OUT} = 30 A



t - Time - 400 µs/div.

Figure 14. Transient Testing at V_{IN} = 48 V, I_{OUT} = 10 A - 15 A - 10 A

8 EVM Assembly Drawing and Layout

Figure 15 through Figure 21 show the top-side and bottom-side component placement for the EVM, as well as device pin numbers where necessary. A four-layer PCB was designed using the top and bottom layers for signal traces and component placement along with an internal ground plane. The PCB dimensions are 3.6 in × 2.7 in with a design goal of fitting all components within the industry standard half-brick format, as outlined by the box dimensions 2.28 in × 2.20 in shown in Figure 16. All components are standard OTS surface-mount components placed on the both sides of the PCB. The copper-etch for each layer is also shown.

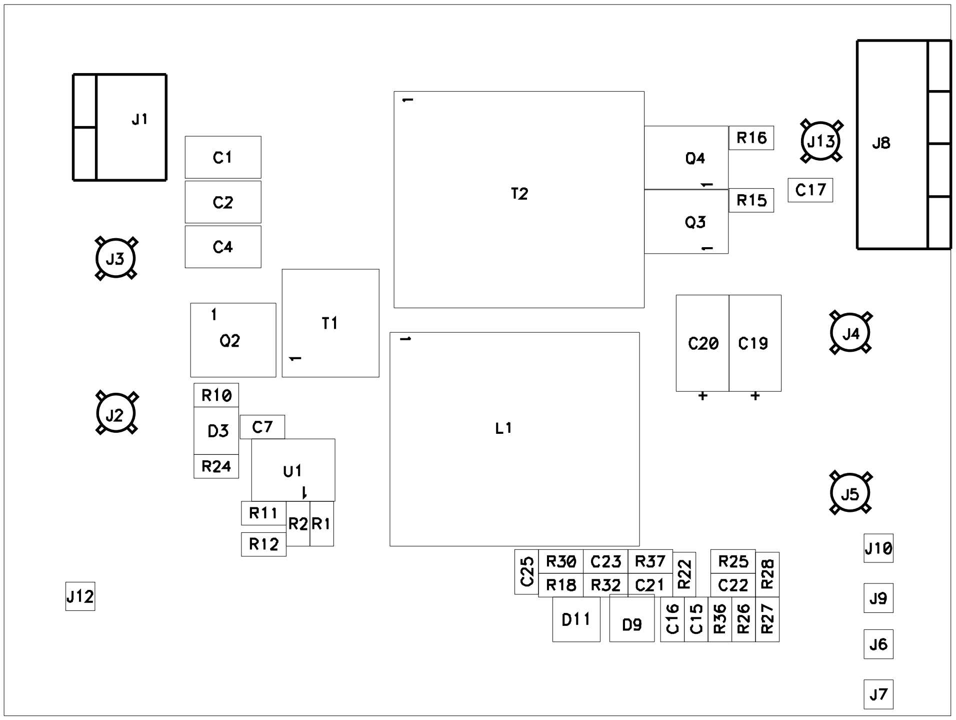


Figure 15. Top-Side Component Assembly

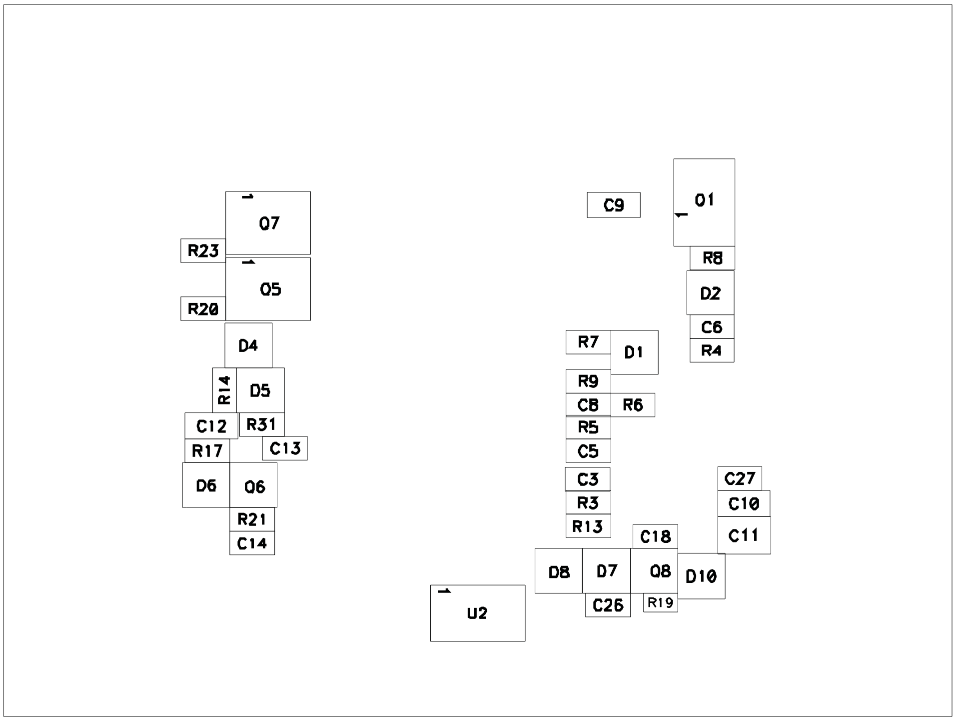


Figure 16. Top-Side Silk Screen

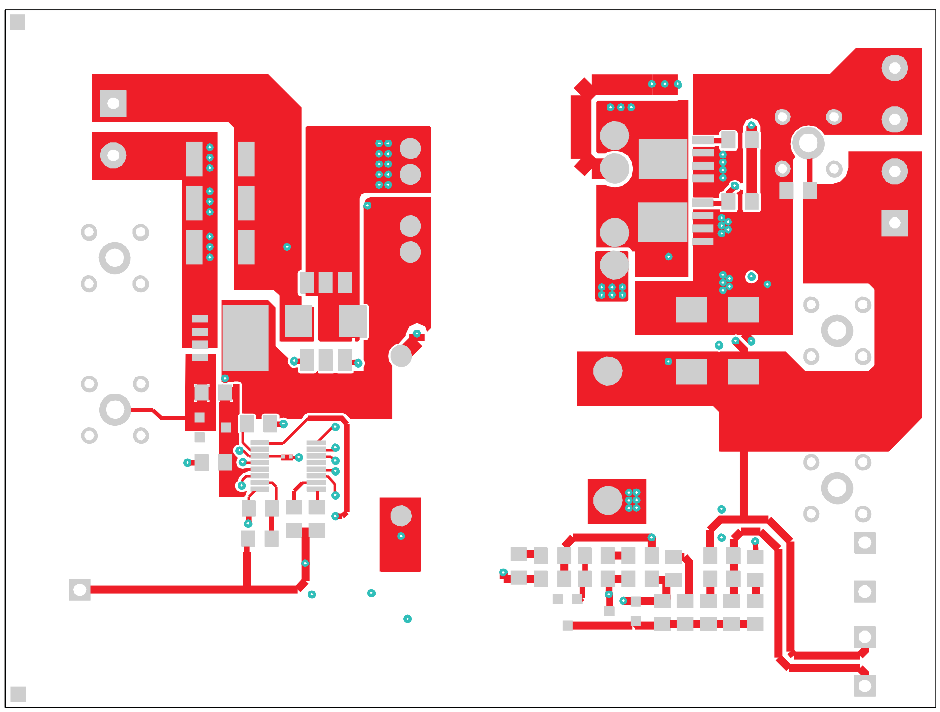


Figure 17. Top Signal Trace Layer

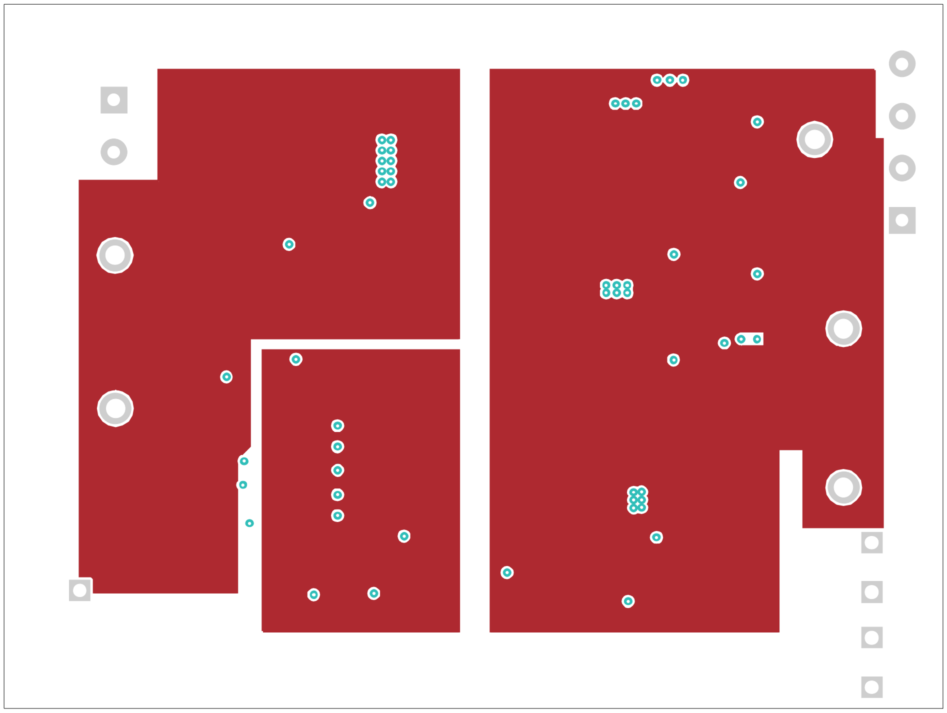


Figure 18. Internal Split Ground Plane

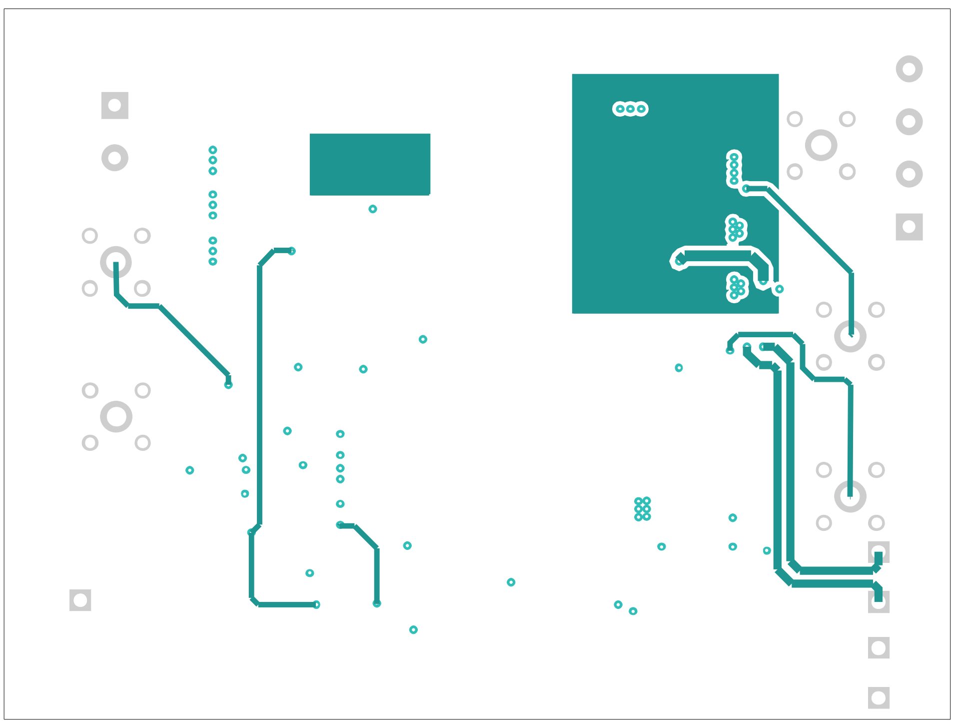


Figure 19. Internal Signal Trace Layer

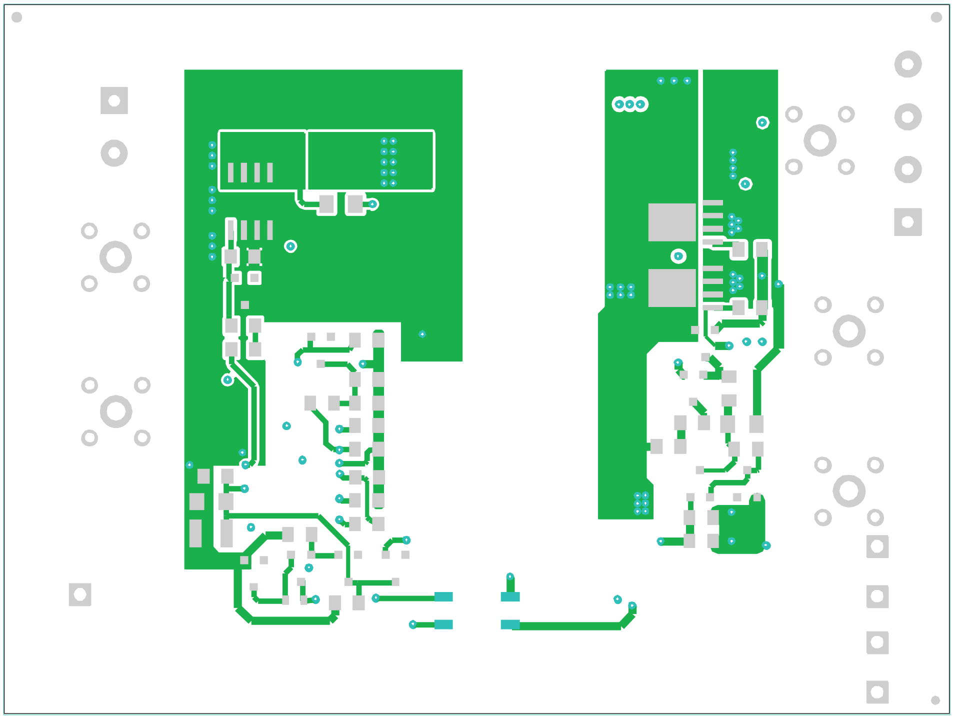


Figure 20. Bottom Signal Trace Layer

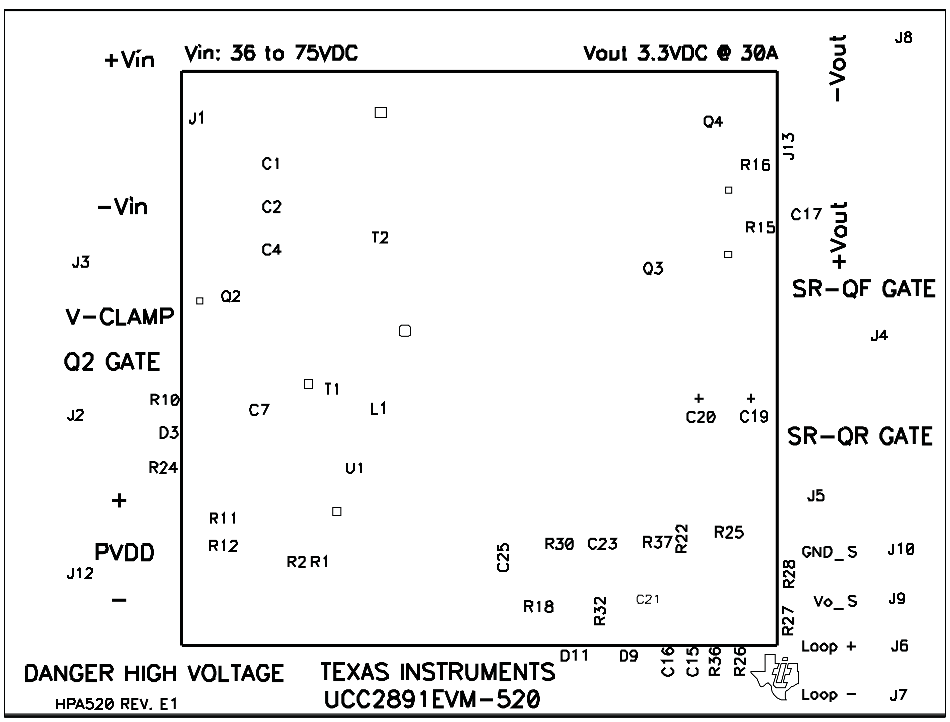


Figure 21. Top-Side Silk Screen

9 List of Materials

The following table lists the UCC2891EVM-520 components corresponding to the schematic shown in Figure 1.

Table 2. List of Materials (1) (2) (3) (4)

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
3	C1, C2, C4	Capacitor, ceramic, 2.2 µF, 100 V, X7R, 20%, 2.2uF, 1812	GRM43ER72A225MA01L	MURATA
2	C10, C12	Capacitor, ceramic, 16 V, X5R, 20%, 10 µF, 1206	C3216X5R1C106K	TDK
1	C11	Capacitor, ceramic, vv V, [temp], [tol], open, 1210	Std	Vishay
1	C13	Capacitor, ceramic, 50 V, X7R, 10%, 2.2 µF, 0805	C2012Y5V1H225Z	TDK
1	C14	Capacitor, ceramic, 50 V, X7R, 20%, 1000 pF, 0805	C0805C102K5RACTU	Kemet
1	C15	Capacitor, ceramic, 50 V, X7R, 10%, 82 nF, 0805	08055C823KAT2A	AVX
1	C16	Capacitor, ceramic, 50 V, X7R, 10%, 270 pF, 0805	08055C271KAT2A	AVX
3	C18, C26, C27	Capacitor, ceramic, 25 V, X7R, 10%, 1.0 µF, 0805	GCM21BR7YA105KA55L	MURATA
2	C19, C20	Capacitor, POSCAP, 9.0 mΩ, 6.3 V, 20%, 330 µF, 7343 (D)	6TPF330M9L	Sanyo
1	C22	Capacitor, ceramic, 50 V, X7R, 10%, open, 0805	std	std
1	C23	Capacitor, ceramic, 16 V, X7R, 10%, 1.5 µF, 0805	C0805C155K4RACTU	Kemet
1	C25	Capacitor, ceramic, 50 V, X7R, 10%, 5.6 nF, 0805	08055C562KAT2A	AVX
2	C3, C17	Capacitor, ceramic, 50 V, X7R, 20%, 0.1 µF, 0805	C0805C104K5RACTU	Kemet
2	C5, C21	Capacitor, ceramic, 50 V, NPO, 10%, 100 pF, 0805	501R15N101KV4T	Johnson dialetric
1	C6	Capacitor, ceramic, 50 V, X7R, 20%, 0.47 µF, 0805	GRM21BR71H474KA88L	MURATA
1	C7	Capacitor, ceramic, 50 V, X7R, 20%, 0.22 µF, 0805	UMK212B7224KG-T	Taiyo Yuden
1	C8	Capacitor, ceramic, 50 V, X7R, 20%, 10 nF, 0805	C0805C103K5RACTU	Kemet
1	C9	Capacitor, ceramic, 250 V, X7R, 10%, 22 nF, 1206	CC1206KRX7R9BB223	Yageo
4	D1, D2, D3, D11	Diode, Schottky, 200 mA, 30 V, SOT23	BAT54	Fairchild
1	D10	Diode, Zener, 13 V,150 mW, 13 V, SOT23	BZX84C13-7-F	Diodes
1	D4	Diode, Dual Schottky, 200 mA, 30 V, SOT23	BAT54C	Fairchild
1	D5	Diode, Dual series Schottky, 70 V, SOT23	BAS70-04LT1	On Semi
1	D6	Diode, Zener, 5.1 V, 350 mW, 5.1 V, SOT23	BZX84C5V1-7-F	Fairchild
2	D7, D8	Diode, switching, 200 mA, 85 V, 350 mW, SOT23	BAS16	Fairchild
1	D9	Adjustable precision shunt regulator, 0.5%, SOT23	TLV431BQDBZT	TI
1	J1	Terminal block, 2 pin, 15 A, 5.1 mm, V_{IN}, 0.40 x 0.35	ED500/2DS	OST
5	J2, J3, J4, J5, J13	Adaptor, 3.5-mm probe clip, 3.5 mm	131-4353-00 or 131-5031-00	Tektronix
5	J6, J7, J9, J10, J12	Printed circuit pin, 0.043 hole, 0.3 length, test pin, 0.043	3103-1-00-15-00-00-08-0	Mill-Max
1	J8	Terminal block, 4 pin, 15 A, 5.1 mm, V_O, 0.80 x 0.35	ED500/4DS	OST

(1) These assemblies are ESD sensitive, ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

Table 2. List of Materials[(1)(2)(3)(4)] (continued)

COUNT	REF DES	DESCRIPTION	PART NUMBER	MFR
1	L1	Inductor, 2 µH, 1 primary, 1 secondary, 0.920 X 0.780	PA0373	Pulse
1	Q1	MOSFET, P-channel, 150 V, 2.2 A, 240 mΩ, SO8	IRF6216	IR
1	Q2	MOSFET, N-channel, 150 V, 6.7 A, 50 mΩ, PowerPak S08	Si7846DP	Vishay
4	Q3, Q4, Q5, Q7	MOSFET, N-channel, 30 V, 60 A, 1.6 mΩ, LFPAK	RJK0328DPB	Renesas
1	Q6	Bipolar, NPN, 40 V, 600 mA, 225 mW, SOT23	MMBT2222A	Vishay
1	Q8	MOSFET, N-channel, 200 V, 60 mA, 25 Ω, SOT23	ZVN3320F	Zetex
1	R1	Resistor, chip, 1/8 W, 1%, 8.45 kΩ, 0805	MCR10EZPF8451	std
1	R11	Resistor, chip, 1/8 W, 1%, 26.7 kΩ, 0805	MCR10EZHF2672	std
2	R13, R17	Resistor, chip, 1/8 W, 1%, 2.00 kΩ, 0805	MCR10EZHF2001	std
2	R14, R31	Resistor, chip, 1/8 W, 1%, 0 Ω, 0805	MCR10EZHJ000	Std
1	R18	Resistor, chip, 1/8 W, 1%, 442 Ω, 0805	MCR10EZHF6490	std
1	R19	Resistor, chip, 1/10 W, 1%, 100 kΩ, 0603	MCR03EZPFX1003	std
1	R2	Resistor, chip, 1/8 W, 1%, 69.8 kΩ, 0805	MCR10EZHF6982	std
1	R21	Resistor, chip, 1/8 W, 1%, 10.0 kΩ, 0805	MCR10EZHF1003	std
1	R22	Resistor, chip, 1/8 W, 1%, 6.19 kΩ, 0805	MCR10EZHF5111	Std
1	R24	Resistor, chip, 1/8 W, 1%, 10.0 kΩ, 0805	MCR10EZHF1002	std
1	R25	Resistor, chip, 1/8 W, 1%, 51.1 Ω, 0805	MCR10EZHF51R1	std
1	R26	Resistor, chip, 1/8 W, 1%, 28.7 kΩ, 0805	MCR10EZPF2872	std
1	R27	Resistor, chip, 1/8 W, 1%, 12.1 kΩ, 0805	MCR10EZHF1212	std
1	R28	Resistor, chip, 1/8 W, 1%, 4.99 kΩ, 0805	MCR10EZPF4991	std
1	R3	Resistor, chip, 1/8 W, 1%, 88.7 kΩ, 0805	MCR10EZPF8872	std
1	R30	Resistor, chip, 1/8 W, 1%, 64.9 Ω, 0805	MCR10EZPF64R9	std
1	R32	Resistor, chip, 1/8 W, 1%, 249 kΩ, 0805	MCR10EZHF2493	std
1	R36	Resistor, chip, 1/8 W, 1%, open, 0805	std	std
1	R37	Resistor, chip, 1/8 W, 1%, 9.09 kΩ, 0805	MCR10EZHF9091	std
6	R4, R10, R15, R16, R20, R23	Resistor, chip, 1/8 W, 1%, 2.21 Ω, 0805	RC0805FR-072R21L	Yageo
1	R5	Resistor, chip, 1/8 W, 1%, 75.0 kΩ, 0805	MCR10EZPF1691	std
1	R6	Resistor, chip, 1/8 W, 1%, 953 Ω, 0805	MCR10EZPF9530	std
3	R7, R8, R12	Resistor, chip, 1/8 W, 1%, 1.00 kΩ, 0805	MCR10EZHF1001	std
1	R9	Resistor, chip, 1/8 W, 1%, 10.5 Ω, 0805	MCR10EZHF10R0	std
1	SH1	Short jumper, length 30 mil	std	std
1	T1	Transformer, Current Sense, 10 A, 1:100, SMD	P8208NL	Pulse
1	T2	Transformer, High Frequency Planar	PA0810	Pulse
1	U1	Current Mode Active Clamp PWM Controller, DPW16	UCC289xPW	TI
1	U2	Phototransistor, CTR 100%-300%, SOP4	SFH690BT	Vishay

10 References

1. *UCC2891 Current-Mode Active-Clamp PWM Controller*, Datasheet, (SLUS542)
2. *Designing for High Efficiency with the UCC2891 Active-Clamp PWM Controller*, by Steve Mappus, Application Note (SLUA299)

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 36 V to 75 V and the output voltage range of 3.3 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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